Control and modulation strategies for MMC - based HVDC

Master Thesis

PED3-942

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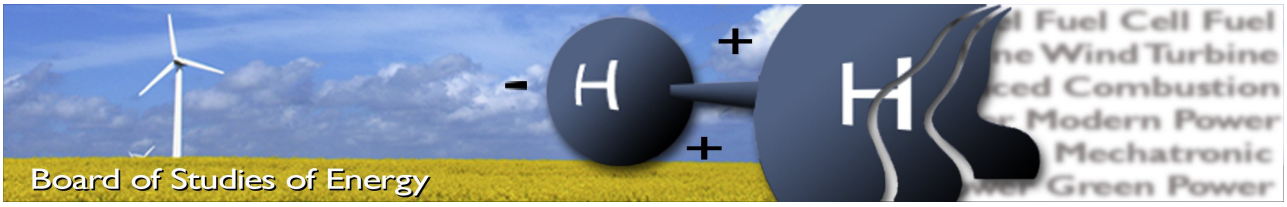

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SYNOPSIS:

MMC is a new topology that has revolutionized the VSC-HVDC for electrical transmission over long distances and interconnecting asynchronous AC grids. Being a very complex and distributed plant, the modulation become more challenging. The purpose of this thesis is to analyse the existing modulation techniques and propose improved solutions that are able to: improve the capacitor voltage balancing, reduce the switching frequency and uniformly distribute the losses among power switches. A comparison of different modulation techniques has been carried out for several converter power ratings, a small scale prototype and a HVDC system, in order to compare their performance. Finally a small scale prototype has been designed and built in order to validate the simulation results.

Copies:	3
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By signing this document, each member of the group confirms that all participated in the project work and thereby all members are collectively liable for the content of the report.

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Preface

The Control and Modulation strategies for MMC based HVDC Master Thesis is conducted at The Department of Energy Technology as part of M.Sc. Energy Engineering, Power Electronics and Drives. It is written by group PED3-942 during the period from the 1st of September of 2014 to the 27 of May 2015 and corresponds to 50 ECTS.

The report is written in LATEX, simulations are performed in PLECS Standalone. All units are written between brackets, as [V].

The references can be found at the Bibliography, they are made according to the Institute of Electrical and Electronics Engineers (IEEE) citation style. References are shown in square brackets as [X]. Figures, Tables, Sections are enumerated in each chapter, e.g. Fig. Y.Z. refers to Y chapter Z figure. Equations are under the same notation, but in round brackets as (X.Y).

The author would firstly like to thank the Master thesis supervisors Professor Remus Teodorescu and Associate Professor Laszlo Mathe, both at Aalborg University for all their guidance and support during this time. The author would like thank also to Heverton Pereira, Paul Dan Burlacu and Ariya Sangwongwanich for their help, advice and discussions before and during the realization of this thesis. Additionally the author would like to thank the colleagues, Professors, PHDs and personal of the department that have collaborated at any time during this time. In addition the author would like to thank his girlfriend for her help and patience. Last but least the author would like to express her most sincere gratitude to his family, especially to his parents, for their support and encouragement.

Aalborg University, May 27, 2015

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Summary

Nowadays there is an increasing demand for electric power at load centres, while the generation can be located far away, for example in offshore windfarms. HVDC systems are one of the solutions for electrical energy transmission over long distances. The appearance in the market of IGBT devices that are fully controllable made possible the use of Voltage Source Converters (VSC-HVDC). Modular Multilevel Converter (MMC) was proposed by Marquardt in 2003. Among other multilevel converter topologies the MMC has gained popularity due to its modularity and scalability. A MMC consists of 3 legs, one per phase, each leg has two arms called upper and lower. In total there are 6 arms and each arm has N cells.

The basic terms and equations of the MMC have been presented along control loops. The effect of the sampling frequency on the performance of the MMC has been studied as well as the relation between the sampling frequency, the THD and the number of output voltage levels. It has been seen that for larger systems (high N) a higher sampling frequency is needed. Furthermore the size of the cell capacitor depends on the parameters of the converter in order to achieve the desired voltage ripple. A simplified arm converter is used in order to accelerate the simulation time without losing accuracy in the calculations.

Several modulation methods have been studied, they can be divided into two groups multicarrier based and carrier less methods. Additionally these modulation methods are compared in order to analyze their performance. Important parameters such as capacitor voltage balancing, circulating current ripple, switching frequency and THD at the output voltage are considered. These comparisons are performed for different converter ratings.

In MMC with low number of SM per arm the PWM plays an important role in the performance of the converter. In converters with high number of cells, the sampling frequency has to be considered in order generate the desired output voltage levels. It has been seen that the highest harmonic content when using PWM, e.g. PSPWM or NLC+PWM, is located the sampling frequency and its sidebands. While for methods without PWM the highest harmonic content is located at low frequencies below the switching frequency of each SM. In addition the NLC + Advanced CRC method

allows the converter to operate with low switching frequency while maintaining the capacitor voltage ripple within limits.

In order to validate the simulation results small scale three phase MMC prototype has been designed and built with a power rating of 2 KVA.

Nomenclature

Abbreviations

HVDC	High Voltage Direct Current
AC	Alternating Current
DC	Direct Current
MMC	Modular Multilevel Converter
SM	Submodule
NLC	Nearest Level Control
PWM	Pulse Width Modulation
THD	Total Harmonic Distorsion
IPM	Intelligent Power Module
IGBT	Insulated Gate Bipolar Transistor
THD	Total Harmonic Distorsion
VSC	Voltage Source Converter
NPC	Neutral Point Clamped
LCC	Line Commutated Converter

List of Symbols

N	Number of submodules per phase per arm
$V_{cu,l}$	Inserted arm voltage
V_{cap}	SM capacitor voltage
f_s	Sampling frequency
N_{sm}	Number of SM inserted
f_{sw}	Switching frequency

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Chapter 1

Introduction

This chapter contains an introduction to the HVDC and the MMC. A literature review, project formulations, objectives and limitations.

1.1 High Voltage Direct Current - HVDC

Nowadays there is an increasing demand for electric power at load centres, while the generation can be located far away, for example in offshore windfarms. HVDC systems are one of the solutions for electrical energy transmission over long distances. Furthermore HVDC systems can also be used to interconnect asynchronous AC grids [1] [2], for example the Nordic to the European grid.
The initial cost of a HVDC system is higher than a HVAC system. However due to its lower losses, HVDC becomes a more economic solution than HVAC over a certain distance called "break-even" as can be seen in Fig. 1.1. The break-even distance is between 500-800 Km for overhead lines and around to 50 Km for submarines cables [1] [2].

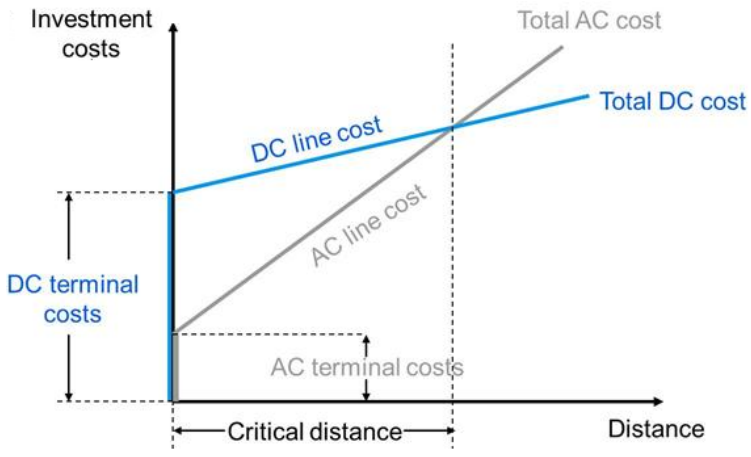

Figure 1.1: Cost in function of the distance for HVAC and HVDC [1].

1.1.1 Converter station

HVDC has been traditionally based on Line Commutated Converters(LCC) using thyristors. In Fig. 1.2, an example of two LCC converter topologies can be seen. The appearance in the market of IGBT devices that are fully controllable, for both turn-on and turn-off, made possible the use of Voltage Source Converters (VSC-HVDC). In 1997, the first HVDC based on VSC started operating in central Sweden, between Hellsjön and Grängesberg [3].

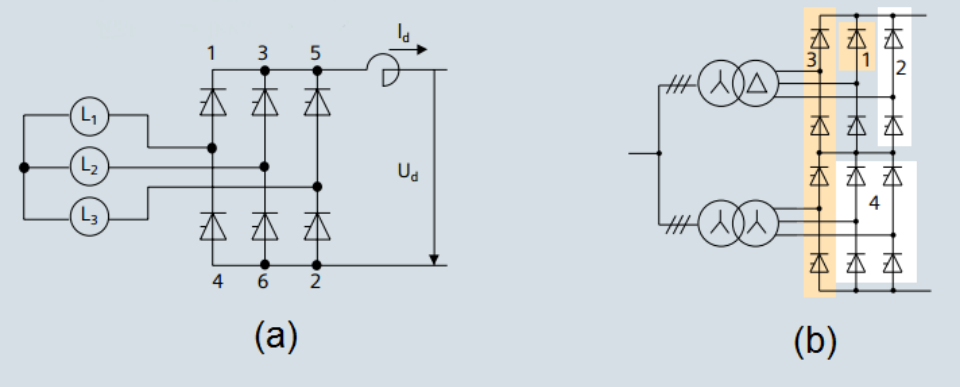

Figure 1.2: Siemens LCC- HVDC: (a) 6 pulse converter bridge. (b) 12 pulse converter bridge [2].

Later, a three level Neutral Point Clamped converter (NPC) was developed in order to improve the performance of the two level converters. Nevertheless the complexity of the circuit topology prevented the development of the NPC [4]. The concept of the Modular Multilevel Converter (MMC) was proposed by Marquardt in 2003 [5]. Among other multilevel converter topologies the MMC has gained popularity due to its modularity scalability, high efficiency and lower harmonic content in the output voltage due to the high number of discrete voltage levels that it is able to generate at its output [6] [7].

1.1.2 The first HVDC based on MMC: Trans Bay Cable

The first HVDC VSC based on MMC is the Trans Bay Cable commissioned in November 2010 in the USA. The solution used is the HVDC PLUS developed by SIEMENS. It connects Pittsburg to Potrero, located in the centre of San Francisco. The link consists of 85 Km underwater cable across the San Francisco Bay as can be seen in Fig. 1.3. The active power capability is 400 MW, while the reactive power capability is 170 MVAr at Potrero station and 145 MVAr at Pittsburg station. The DC link voltage is ±200 kV. The converter consists of 3 legs with 2 arms per leg. Each arm contains 216 (16 extra) cells consisting of an IGBT half bridge and a capacitor. A parallel connection of IGBTs is used in order to increase the current capability of the submodule, as an industrial IGBT module of 4.5 kV can not handle the total current [8]. The use of MMC allows to reduce the switching losses as the switching

frequency is in the 100-200 Hz range which is relatevely low compared to the switching frequency in the two or three level converters. Due to the high number of cells, the output voltage is quasi sinusoidal, reducing the size of the output filters [9].

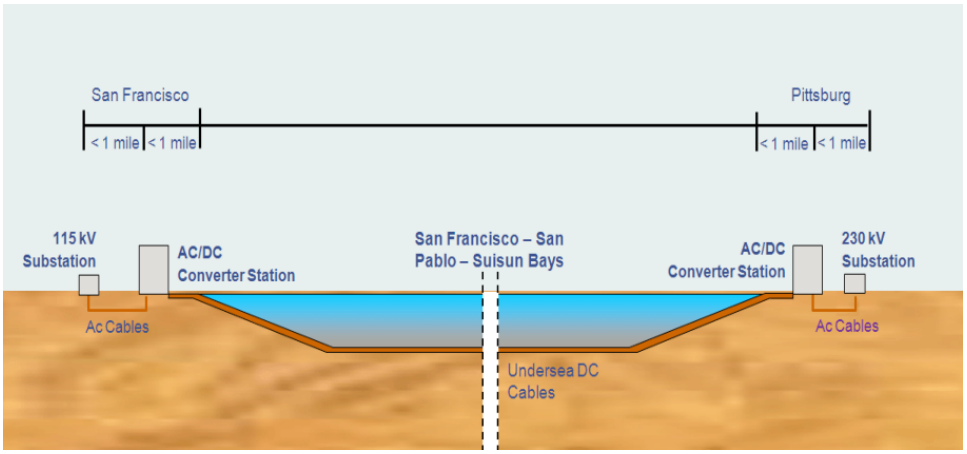

Figure 1.3: Trans Bay Cable HVDC link scheme [8].

1.1.3 Commercial HVDC based MMC

Nowadays several manufacturers offer HVDC solutions based on MMC, such as ABB with its HVDC light [1], Siemens with its HVDC Plus [2], Alstom with its HVDC MaxSine [10]. These solutions are already in use in several commissioned projects around the world.

Figure 1.4: Skagerrak 4 converter station [11].

Recently the Skagerrak HVDC connection between Norway and Denmark in-

creased its capacity with the commission of the Skagerrak 4. The fourth pole of the HVDC connection uses the HVDC Light developed by ABB which is based on MMC. The new link increases the transmission capacity by 700 MW to a total of 1700 MW. The link spans of 240 km, which 140 km are underwater. The Skagerrak 4 has an operating DC voltage of 500 kV and works in bipole mode with Skagerrak 3 which uses LCC technology [11].A diagram of the Skagerrak HDVC connection is shown in Fig. 1.5.

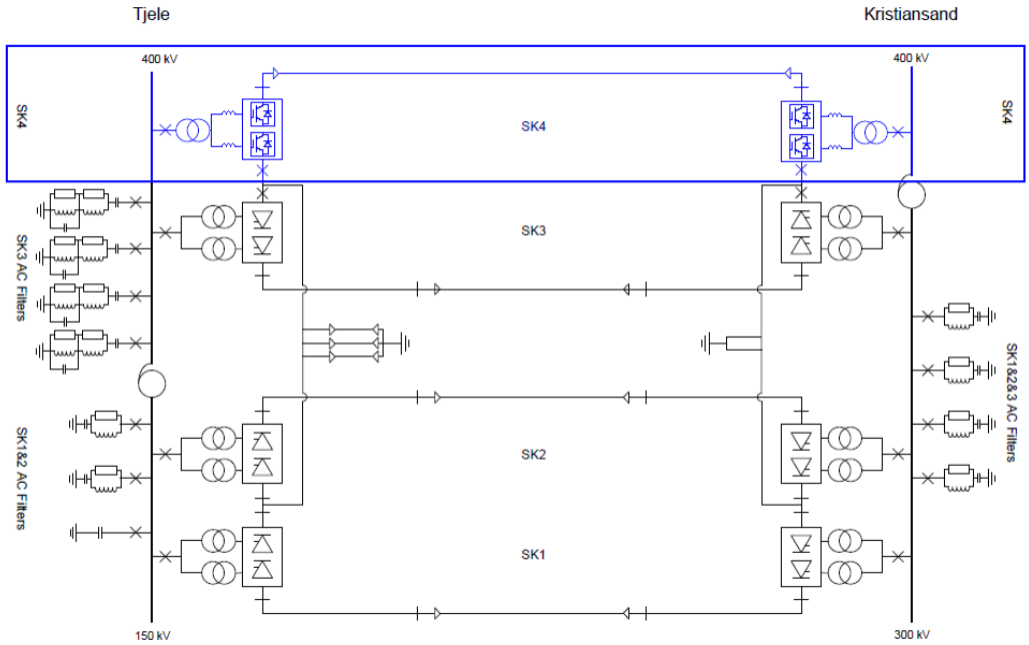

Figure 1.5: Skagerrak HVDC connection [11].

1.2 MMC Overview

In Fig. 1.6 (a) the circuit diagram of a MMC is presented. It consists of 3 legs, one per phase, each leg has two arms called upper and lower. In total there are 6 arms, each arm has N cells. Additionaly each arm has an arm inductance which must be connected in order to limit the current due to voltage differences in the arms [6].

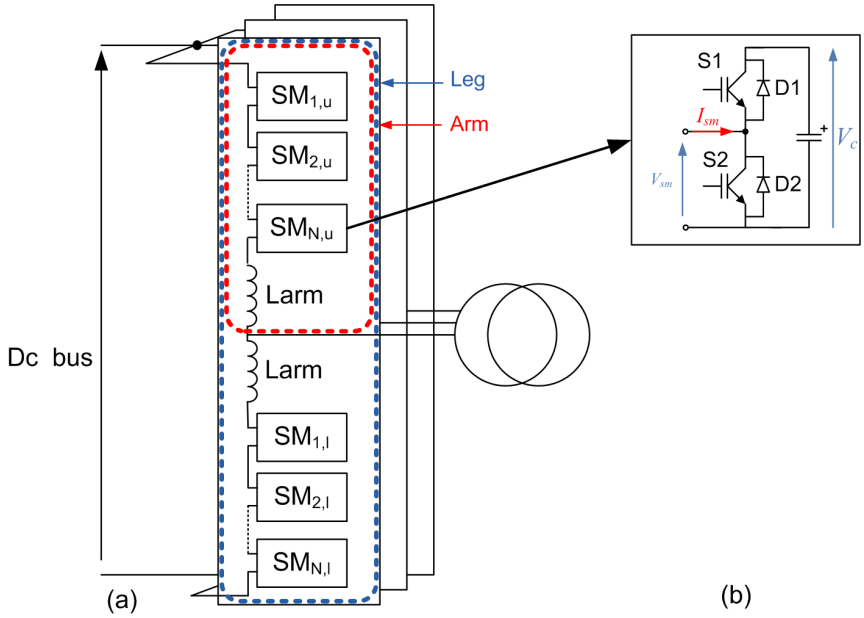

Figure 1.6: (a) Three phase MMC circuit diagram. (b) Generic cell schematic circuit.

The arm output voltage is the sum of the voltages of the cells inserted in the circuit. A MMC with a high number of cell can deliver a quasi sinusoidal output voltage due to the high number of voltage levels that the converter can generate [12]. In Fig. 1.6 (b) the simplest half bridge topology of the submodule is shown. Depending on the sign of the cell current and the on-off state of the two switches (S1 and S2) from the SM, eight different states can be identified as can be seen in Table 1.1. Therefore the modulation methods make use of these states in order to generate the gate pulse signals depending on the reference signals. Two control loops are present in a MMC, an outer loop that controls the voltages or currents at the terminals of the converter, and an inner loop in order to control the capacitor voltages, switching losses of each cell [6].

Table 1.1: SubModule States.

I_{sm}	S1	S2	Capacitor State	Conducting device
$I_{sm} > 0$	0	0	Charging	D1
	1	0	Charging	D1
	0	1	Bypassed	S2
	1	1	ShortCircuit	Not Valid
$I_{sm} < 0$	0	0	Bypassed	D2
	1	0	Discharging	S1
	0	1	Bypassed	D2
	1	1	ShortCircuit	Not Valid

1.3 State of art study

A review of the related literature can be found in this section.

1.3.1 Topologies

Several cell topologies for MMC have been investigated as can been seen in Fig. 1.7. The most commonly used topologies are the half-bridge and full bridge, Fig. 1.7 (a) and (b). One drawback of the half bridge cells is that it can only generate positive and zero voltages while the full-bridge can generate positive, negative and zero voltages. One drawback of the full bridge is the higher number of electronic components needed. In order to reduce the number of components a unidirectional cell has been proposed. However its functionality is limited by the current direction [13]. The standard cells can be replaced by more complex topologies such as Multilevel NPC Fig. 1.7 (d) and Multilevel flying capacitor Fig. 1.7 (e). The sizing of the

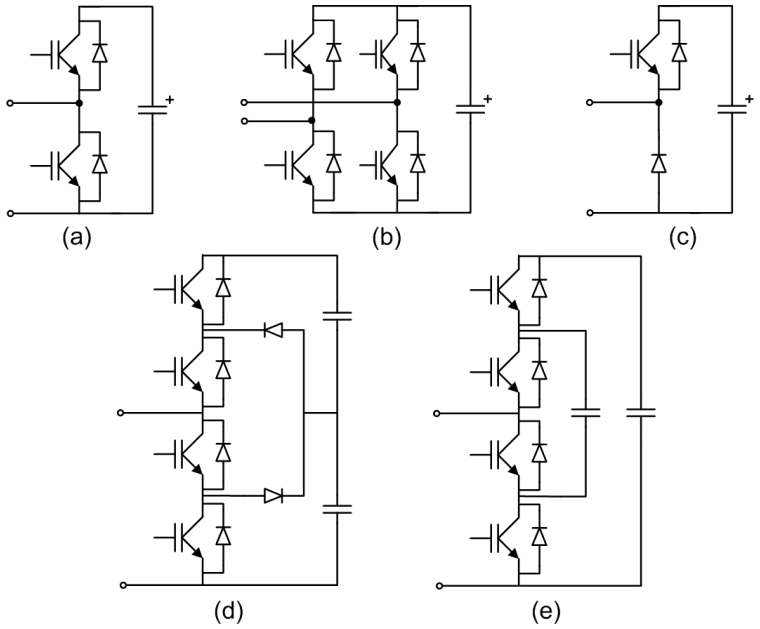

Figure 1.7: Cell topologies: (a) Half bridge. (b) Full bridge. (c) Unidirectional. (d) Multilevel NPC. (e) Multilevel flying capacitor. [6].

cell capacitors is studied in [14] where the authors present a method to obtain the minimum size of the capacitors while keeping the ripple under predefined limits. By using this method the volume on the cells and hence the volume of the converter can be reduced. A method to calculate the size of the arm current is presented in [15].

1.3.2 Control and Modulation

The voltage generated by the MMC should be as close as possible to the output reference voltage, while the converter ensures high efficiency. Furthermore, the series connected SM capacitor voltages should be controlled in order to remain balanced. Other challenges can be controlling the circulating currents, evenly distributing the switching stress and reducing and spreading the losses among the different SM [6]. There are several modulation/control techniques for the MMC. They can be divided into two groups PWM multicarrier based and sort and select methods.

Multicarrier PWM methods

For these techniques N carrier waveforms are generated per arm, displaced with respect to the zero axis such as phased disposition (PD), phase opposition disposition (POD), alternate phase opposition disposition (APOD). These techniques have drawbacks such as unequal distribution of the ripple in the capacitor voltage and large circulating currents [6].

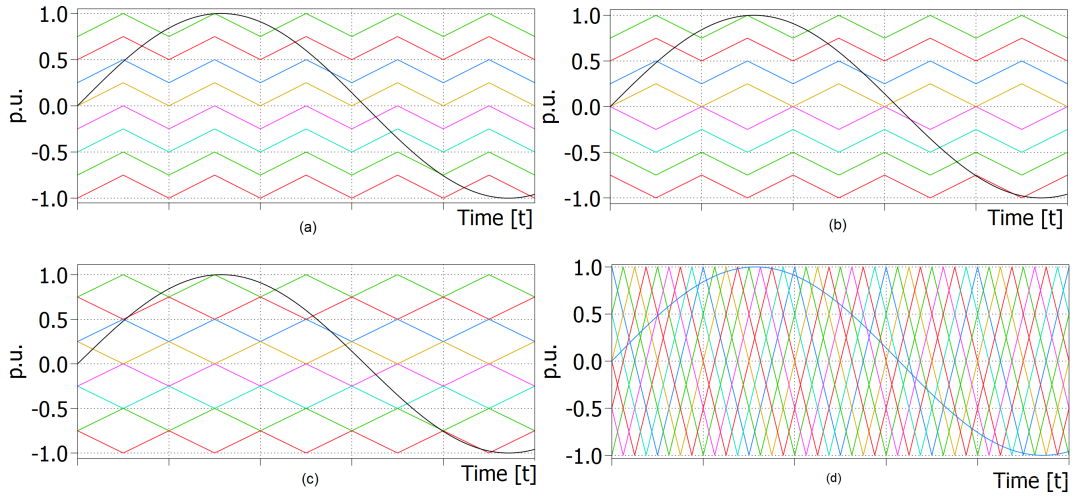

Figure 1.8: (a) Phase disposition PD. (b) Phase opposition disposition POD. (c) Alternate phase opposition disposition APOD. (d) Phase shifted PWM. [7].

Due to these mayor drawbacks these techniques are not widely used, except for the phase shifted PWM (PS-PWM) where N carriers are compared to the reference signal. An additional control algorithm that includes averaging and balancing control to modify these reference signals may be used in order to improve the internal capacitor balancing [16]. However, a large number of SM can increase the difficulty in the implementation of the PSPWM method, which is the main drawback of this modulation technique [6]. An analysis of the displacement angle of the triangular carriers between the two arms is done in [17] in order to minimize the output voltage harmonic distortion. A resampled uniform PWM is proposed in [18] in order to

increase the sampling frequency and improve the accuracy of the system.

Sort and Select methods

In these approaches the SMs are sorted periodically depending on their capacitor voltage. The number of SMs that has to be inserted in each arm is obtained by several methods such as Nearest Level Control (NLC), Selective Harmonic Elimination (SHE), or Model Predictive Control (MPC).

A Modified NLC is proposed in [19], where the reference signal can be converted into a staircase instead of sampled. Furthermore, an estimation of the capacitor energy open-loop control is used in order to minimize the circulating current. In [20] an enhanced NLC is developed in order to avoid voltage spikes that are introduced by the SM swapping and therefore reduce the total harmonic distortion at the output voltage of the converter. In [21] a simplified NLC is investigated in order to reduce the computation burden. A tolerance band modulation method is developed in [22] in order to generate the voltage reference for the cell sorting control where a voltage flux variable is derived from the reference voltage and the actual measured voltage. Advanced methods such as a Multilevel selective harmonic elimination pulse-width modulation (MSHE-PWM) is proposed in [23] where the converter switches, based on look up tables, with low frequency while maintaining low harmonic content. A predictive sorting algorithm is proposed in [24] in order to distribute the stored charge among all the SM. The proposed capacitor balancing method can reduce the capacitor unbalance while operating at low switching frequencies.

1.4 Problem formulation and project objectives

In this Master thesis several questions must be answered.

1. *What are the advantages and disadvantages of the existing modulation techniques in terms of total harmonic content, losses and implementation complexity?*
2. *How is the performance of the modulation strategies affected by the number of SM in the MMC?*
3. *Can a new modulation technique that may offer better performance than the existing ones in any of the terms previously mentioned be proposed?*
4. *Is it possible to implement the proposed modulation in a small scale prototype?*

Therefore, several project objectives are set:

- To make a comparison of the existing modulation methods for MMC.
- Propose a new modulation technique in order to reduce the switching losses.
- Build a small scale prototype to verify the theory and simulations.

1.5 Project Limitations

Some limitations are present due to physical resources and some boundaries have to be set in order to limit the extension of the project.

- Prototype rating is limited to the available resources at the department.
- The number of SM per arm is limited to 4 due to complexity and cost.
- Only the inverter mode functionality is considered.

Chapter 2

Design and control of the MMC

In this chapter the basic principles of the MMC and its equations are explained. Several control loops are presented, as well as the effect of the sampling frequency on the performance of the MMC. Furthermore the sizing of the cell capacitor and the concept of a simplified arm converter for speeding up the simulations are presented.

2.1 Basics equations of the MMC

First, the output arm voltage can be defined as the sum of the voltages of the cells that are inserted

$$v_{c_x} = \sum_{N}^{j=1} Sw_j \; v_{cap_j} \tag{2.1}$$

The arm currents are composed by three components: one third of the DC link current, half of the output current and the AC component of the circulating current [25]

$$\begin{cases} i_{u_x} = \frac{i_{DC}}{3} + \frac{is}{2} + i_{circ_{ac}} \\ i_{l_x} = \frac{i_{DC}}{3} - \frac{is}{2} + i_{circ_{ac}} \end{cases} \tag{2.2}$$

The output current can be defined as:

$$i_s = i_u - i_l \tag{2.3}$$

The circulating current term can be defined as the semi sum of the two arm currents. This current does not affect the output current, and it flows internally through the arm converters and the DC link

$$i_c = \frac{i_u + i_l}{2} \tag{2.4}$$

This current should be minimized as it can have a negative impact on the sizing of the components of the converter, efficiency of the converter as well as in the

internal balancing of the capacitor cells [26]. The internal voltage that generates the circulating current can be defined as

$$v_c = \frac{E - (v_{cu} + v_{cl})}{2} \tag{2.5}$$

and the voltage driving i_s can be defined as

$$v_s = \frac{v_{cl} - v_{cu}}{2} \tag{2.6}$$

If the circulating current term i_c is introduced in Eq. 2.3 it can be obtained as

$$i_u = i_c + \frac{i_s}{2} \tag{2.7}$$

and

$$i_l = i_c - \frac{i_s}{2} \tag{2.8}$$

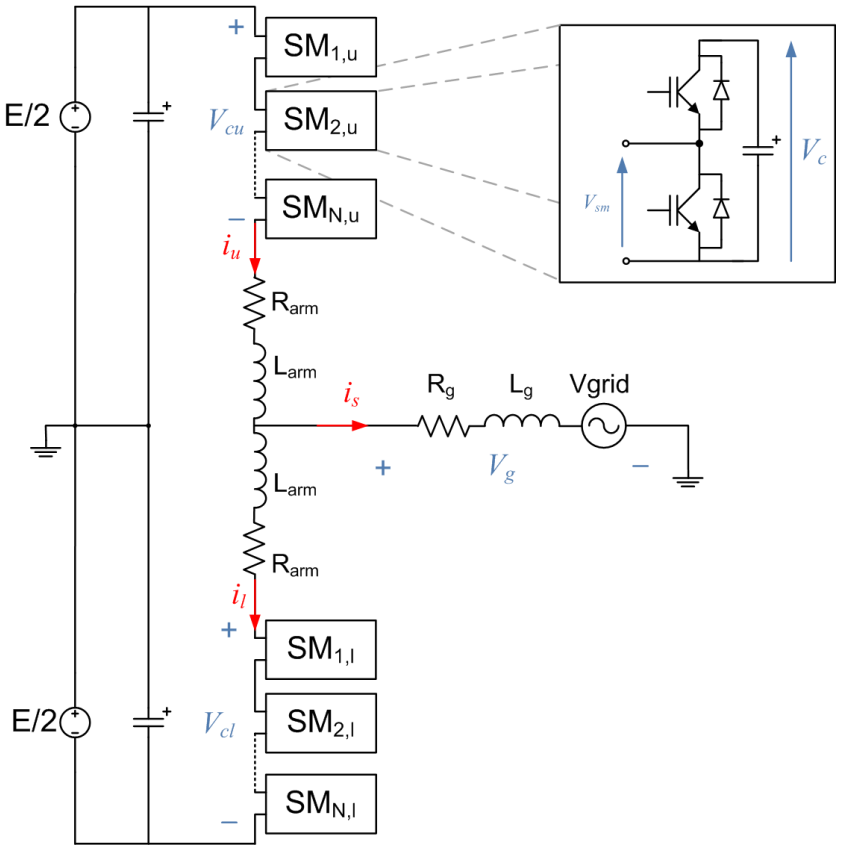

Figure 2.1: MMC circuit diagram and one cell circuit.

By applying Kirchoff's Law in the single phase MMC circuit in Fig. 2.1 and as can be seen in references [26] [27], the equations of the arm voltage can be expressed as

$$v_{cu} = \frac{E}{2} - v_g - R_{arm} i_u - L_{arm} \frac{di_u}{dt} \tag{2.9}$$

$$v_{cl} = \frac{E}{2} + v_g - R_{arm} i_l - L_{arm} \frac{di_l}{dt} \tag{2.10}$$

By subtracting of Eq. 2.9 from Eq. 2.10 the output voltage is calculated:

$$v_g = \frac{v_{cl} - v_{cu}}{2} - \frac{R_{arm}}{2}(i_u - i_l) - \frac{L_{arm}}{2} \frac{d(i_u - i_l)}{dt} \tag{2.11}$$

including the output current term from Eq. 2.3 and the v_s term from Eq. 2.6

$$v_g = v_s - \frac{R_{arm}}{2} i_s - \frac{L_{arm}}{2} \frac{di_s}{dt} \tag{2.12}$$

From Eq. 2.12 it can be noticed that output voltage v_g is not affected by the circulating current. Moreover, if Eq. 2.9 and Eq. 2.10 are added together the following is obtained:

$$v_{cu} + v_{cl} = E - R_{arm}(i_u + i_l) - L_{arm} \frac{d(i_u + i_l)}{dt} \tag{2.13}$$

If the circulating current term and Eq. 2.5 are introduced in Eq. 2.13 the following can be obtained

$$v_c = \frac{E - (v_{cu} + v_{cl})}{2} = \frac{R_{arm} i_c}{2} + \frac{L_{arm}}{2} \frac{di_c}{dt} \tag{2.14}$$

where it can be seen that the circulating current only depends on the difference between the sum of the arm voltages and the dc link voltage [26].

2.2 Control structures

The overall control diagram of the MMC is depicted in Fig. 2.2 and it is composed by:

- An active/reactive power control block.
- A circulating current control block which main objective is to minimize the alternating component of the circulating current. This block may be integrated by several blocks depending on the strategy used.
- Reference generator block. It is used to generate the reference voltage for the different arms.
- Modulator. From the arm reference voltage, it generates the gate signals for the switches of each SM.
- Balancing control. Multi carrier techniques may require additional control in order to balance the capacitor voltages.

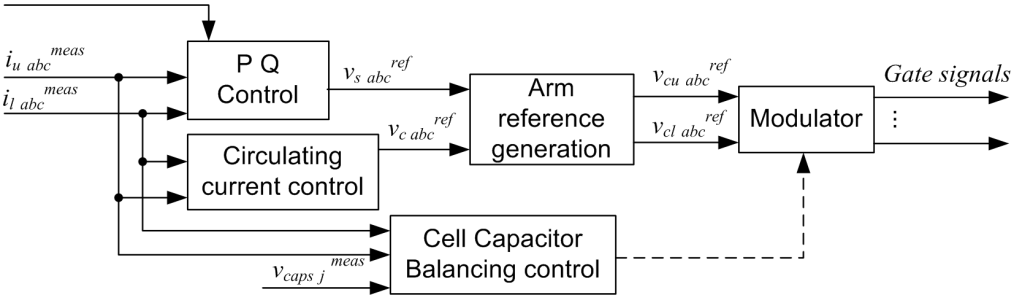

Figure 2.2: MMC control block diagram overview.

2.2.1 Arm reference generation block

From Eq. 2.5 and Eq. 2.6 and the reference voltages is obtained as:

$$v_{cu}^{ref} = \frac{E}{2} - v_s^{ref} - v_c^{ref} \tag{2.15}$$

$$v_{cl}^{ref} = \frac{E}{2} + v_s^{ref} - v_c^{ref} \tag{2.16}$$

that can be used for generating the reference voltages of the arm converters, where $v_{cu,l}$ are the reference voltage for the arm, v_s^{ref} is the output reference voltage generated by the outer control loop, and v_c^{ref} is the reference voltage generated by the circulating current control loop.

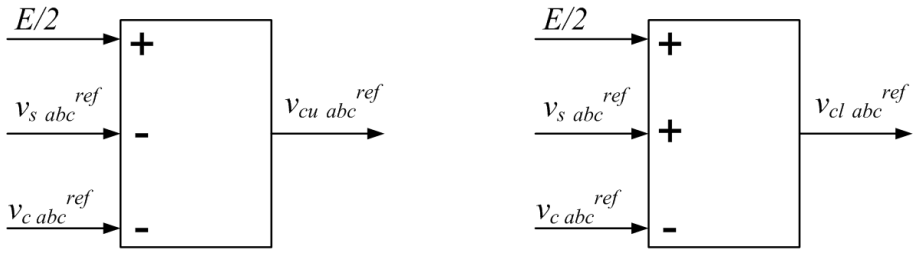

Figure 2.3: Arm reference voltage diagram block.

2.2.2 Outer control loop

The outer control loop of the MMC can be developed analogously to others VSC as an active reactive power control. The output currents are calculated from the measurement of the different arm currents. This control must have a high bandwidth in order to achieve a good dynamic performance, reduction of transients and reduction of current harmonics [27].

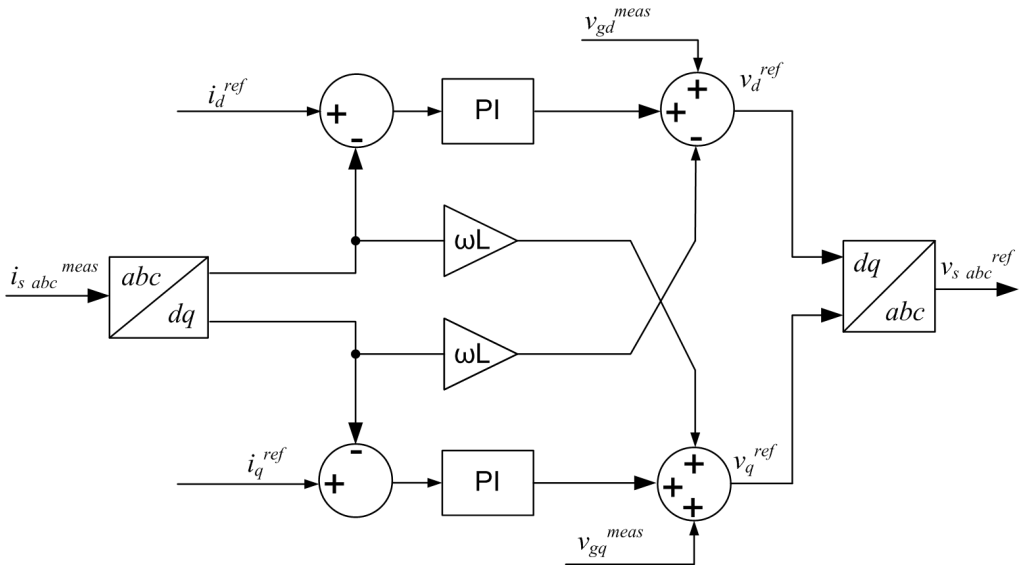

Figure 2.4: Outer control block diagram.

2.2.3 Circulating current control loop

As previously stated the circulating current flows through the 3 phases of the converter and does not affect the output voltage and current. The circulating current has two terms, a DC component with one third of the value of the DC current $I_{DC}/3$, this component is the responsible of the DC/AC power transfer. The other component is an AC component with twice the fundamental frequency and negative sequence that increments the total rms value of the current and affects the balancing of the capacitors [26] [28] . The expression of the circulating current is as follows

$$i_{circ_a} = \frac{I_{DC}}{3} + i_{circ_{peak}} sin(2\omega t + \phi) \tag{2.17}$$

$$i_{circ_b} = \frac{I_{DC}}{3} + i_{circ_{peak}} sin\left[2(\omega t - \frac{2\pi}{3}) + \phi)\right] \tag{2.18}$$

$$i_{circ_c} = \frac{I_{DC}}{3} + i_{circ_{peak}} sin\left[2(\omega t + \frac{2\pi}{3}) + \phi)\right] \tag{2.19}$$

where I_{DC} is the total current delivered by the DC link, $I_{circ_{peak}}$ is the peak value of the AC component and ϕ the phase angle. These three phase currents can be transformed into a rotating reference frame for control purposes. By using Park Transformation

$$T_{abc/dq} = \frac{2}{3}\begin{bmatrix} cos\theta & cos(\theta - \frac{2\pi}{3}) & cos(\theta + \frac{2\pi}{3}) \\ -sin\theta & -sin(\theta - \frac{2\pi}{3} & -sin(\theta + \frac{2\pi}{3}\end{bmatrix} \tag{2.20}$$

if $\theta = 0$, then it can be obtained

$$i_{circ_{dq}} = \begin{bmatrix} i_{circ_d} \\ i_{circ_q} \end{bmatrix} = T_{abc/dq} \begin{bmatrix} i_{circ_a} \\ i_{circ_b} \\ i_{circ_c} \end{bmatrix} = \begin{bmatrix} 0 \\ i_{circ_{peak}} \end{bmatrix} \tag{2.21}$$

Therefore the resulting current in the dq frame only contains DC components that can be controlled by means of PI controllers as depicted in Fig. 2.5 and therefore minimize or suppress the alternating component of the circulating current.

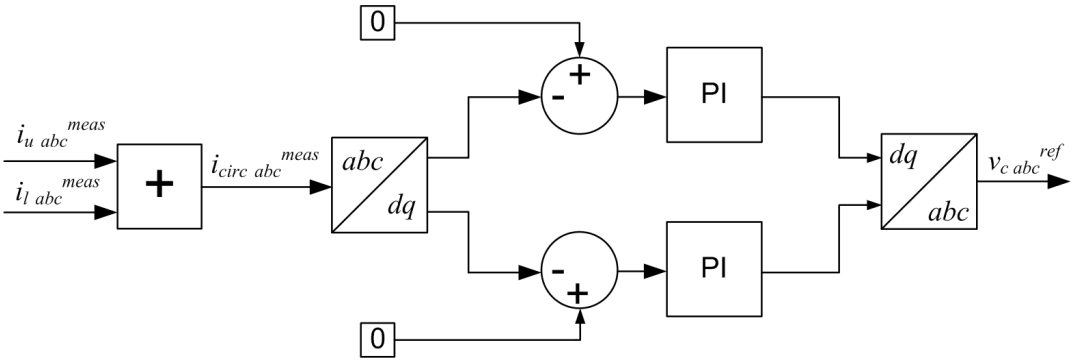

Figure 2.5: Circulating current control block diagram.

2.2.4 Balancing control techniques

A balancing control can be implemented in order to improve the internal balancing of the capacitors. This control is implemented in on each SM reference voltage by forcing its DC voltage to follow its reference value V_{dc}/N [29]. The block diagram is depicted in Fig. 2.6. The measured cell capacitor voltage is subtracted from the nominal cell voltage, multiplied by constant K and by ± 1 depending on the sign of the current.

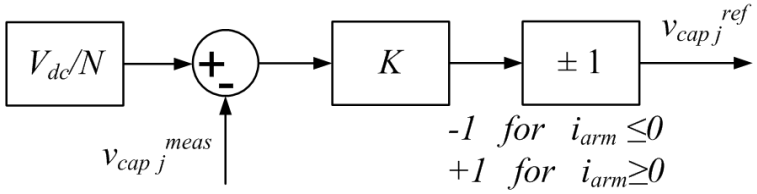

Figure 2.6: Capacitor voltage balancing control block diagram [29].

2.3 Sizing of cell capacitor

The cell capacitor is a key component in the MMC as the output voltage depends on the cell capacitor voltages. Due to the alternating arm current the capacitor

voltage variates through each fundamental cycle. In order to avoid overcharging and underchaging the capacitor over a certain limits, the size should be choosen accordingly [14]. On the other hand an oversize of the cell capacitor will result in bulkier and more expensive converters.
The size of the SM capacitor can be derived from the energy equation

$$E_{arm}(t) = \frac{1}{2} N C_{cell} V_{cell}^2(t) \tag{2.22}$$

where E_{arm} is the total energy of the arm, C_{cell} is the capacitance of the cell and V_{cell} the voltage of the cell. In [14] is derived that

$$E_{arm} = \frac{\Delta E_{arm}}{4\Delta V} \tag{2.23}$$

the energy of the arm E_{arm} is proportional to the energy deviation in the arm ΔE_{arm}, divided by the desired voltage variation in per unit. By combining Eq. 2.22 and Eq. 2.23 the size of the capacitor can be derived as [14]

$$C_{cell} = \frac{\Delta E_{arm}}{2N V_{cell_{nom}}^2 \Delta V} \tag{2.24}$$

Furthermore from [14] it is obtained that the maximum variation of the Energy in the arm is

$$\Delta E_{arm} \approx 2\frac{|S|}{3\omega} \tag{2.25}$$

where S is the apparent power of the converter. Therefore by inserting Eq. 2.25 in Eq. 2.24 it can be obtained

$$C_{SM} \geq \frac{|S|}{3\omega} \frac{1}{V_{DC} V_{cell_{nom}} \Delta V} \tag{2.26}$$

2.4 Simplified equivalent arm circuit

HVDCs are generally consisted of a high number of components. Its simulation can lead to high computation requirements. Solutions as FPGAs or RTDS are widely used in order to accelerate the simulation speed. In Fig. 2.7 a simplified equivalent arm circuit consisting of N cells is used in this thesis in order to speed up the simulations performed in PLECS. From the circuit, it can be seen that the output voltage of the arm can be obtained as the summatory of the inserted capacitor voltages.

$$Varm = \sum_{j=1}^{N} V_{cap}(j) * Sw(j) \tag{2.27}$$

where N is the number of cells, V_{cap} is a vector of N length that contains the capacitor voltages and Sw is a binary vector of N length that contains the gate pulse

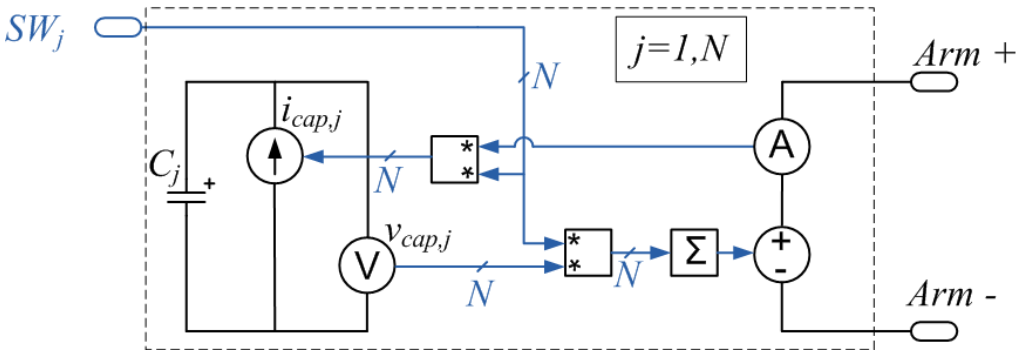

Figure 2.7: Simplified equivalent arm circuit [35].

signals. Therefore the output voltage will contain only the sum of the inserted capacitor voltages. On the other hand the inserted cell capacitors should be charged or discharged depending on the arm current, while the voltage at the bypassed cell capacitors remains unaltered. Therefore by multiplying the measured arm current by the Sw vector, a vector $I_{arm,j}$ containing the arm current only for the inserted capacitors is obtained.

$$I_{arm,j} = i_{arm} * Sw_j \qquad for \;\; j = 1...N \tag{2.28}$$

By using this equivalent circuit the use of semiconductor devices is avoided and the simulation time is accelerated remarkably. Nevertheless some drawbacks arise with the use of the equivalent circuit. For example, a deadtime between the upper and lower switch of the cell can not be implemented. In addition the lack of semiconductors makes it impossible to implement a thermal model and obtain the losses in PLECS.

2.5 Effect of the Sampling frequency on the MMC performance

The sampling frequency is an important factor that has to be taken into account when simulating or designing MMC. For MMCs with low number of SMs per arm it can be assumed that the number of output voltage levels can be calculated as

$$n_{level} = N + 1 \tag{2.29}$$

Nevertheless, for real systems with high number of cells per arm, this assumption is not longer valid as the number of output voltage levels depends on

- Sampling frequency f_s
- Number of submodules N
- Modulation index m

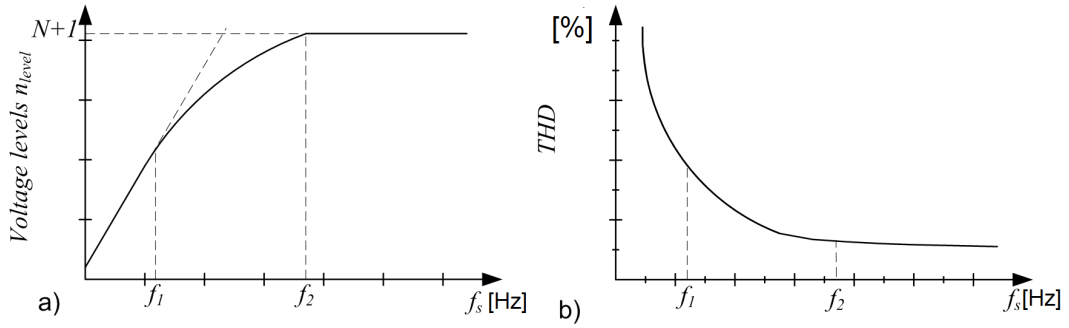

Figure 2.8: a) Number of voltage output levels as a function of the sampling frequency b) Output voltage THD as function of the sampling frequency [30].

In Fig. 2.8 a) the relationship between sampling frequency and the number of the output voltage levels for a generic MMC can be seen. The equation describing such curve is as follows

$$n_{level} = \begin{cases} \frac{f_s}{2f_0} + 1 \quad for \quad (f_s < f_1) \\ N + 1 \quad for \quad (f_s > f_2) \end{cases} \tag{2.30}$$

where f_0 is the fundamental frequency of 50 Hz. In order to calculate the frequencies f_1 and f_2, the Eqs. 2.31 and 2.32 can be used [30]. Furthermore the THD at the output voltage is related to the sampling frequency as it is depicted in Fig. 2.8 a). Table 2.1 shows the values of f_1 and f_2 for different number of cells per arm.

$$f_1 = \pi \; f_0 \; \sqrt{2m \; N} \tag{2.31}$$

$$f_2 = \pi \; f_0 \; m \; N \tag{2.32}$$

Table 2.1: Frequencies f_1 and f_2 for different number of cells per arm converter.

	N				
	4	10	20	40	100
f_1 [Hz]	444	702	993	1405	2221
f_2 [Hz]	628	1571	3142	6283	15707

Summary

Firstly the basic terms and equations of the MMC have been presented along control loops. The effect of the sampling frequency on the performance of the MMC has been studied as well as the relation between the sampling frequency the THD and the number of output voltage levels. It has been seen that for larger systems (high N) a higher sampling frequency is needed. Furthermore the size of the cell capacitor depends on the parameters of the converter in order to achieve the desired voltage ripple. The simplified arm converter allows to accelerate the simulation time without losing accuracy in the calculations.

Chapter 3

Multicarrier PWM methods

In this chapter the multicarrier methods PSPWM and PDPWM are studied along with simulation demonstrations.

3.1 Phase Shift PWM

In a similar way as the PWM generation for the two level converters, in the PSPWM the triangular carriers are compared to the reference signal as depicted in Fig. 3.1. For the MMC a triangular carrier is generated by every SM. These carriers have a phase shift of $\alpha = 2\pi/N$ rad between each signal. Furthermore there is a phase shift between the carriers in the two arms

$$\theta = \begin{cases} 0 & if\ N\ is\ odd \\ \frac{\pi}{N} & if\ N\ is\ even \end{cases} \tag{3.1}$$

In this way a lower harmonic content in the output voltage can be achieved [17] and 2N+1 levels are obtained at the output of the converter [31].

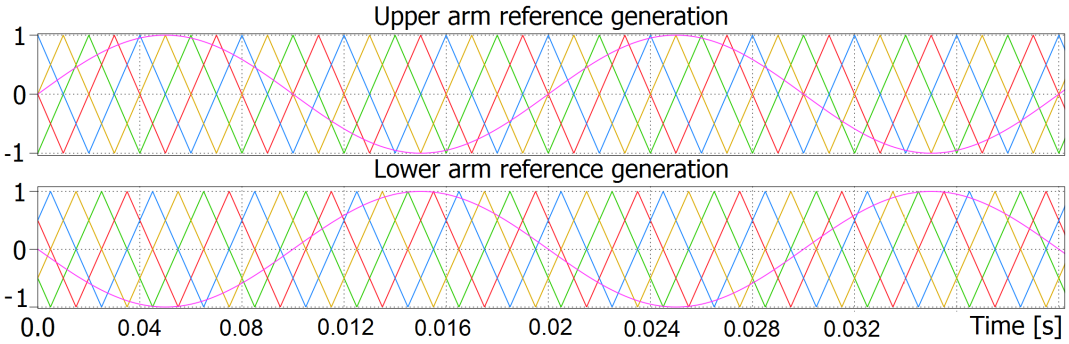

Figure 3.1: PSPWM: Gate signal generation.

In Fig. 3.2(a) the reference and the output voltage can be seen. The output voltage has 2N+1 levels and the output switching frequency is 2N times the carrier

frequency. In this case 8 SM are used and the carrier frequency is 1 kHz. From the harmonic spectrum in Fig. 3.3 it can be noticed that the biggest harmonic content is located at 8 KHz, its sidebands and at multiples of the resultant switching frequency.

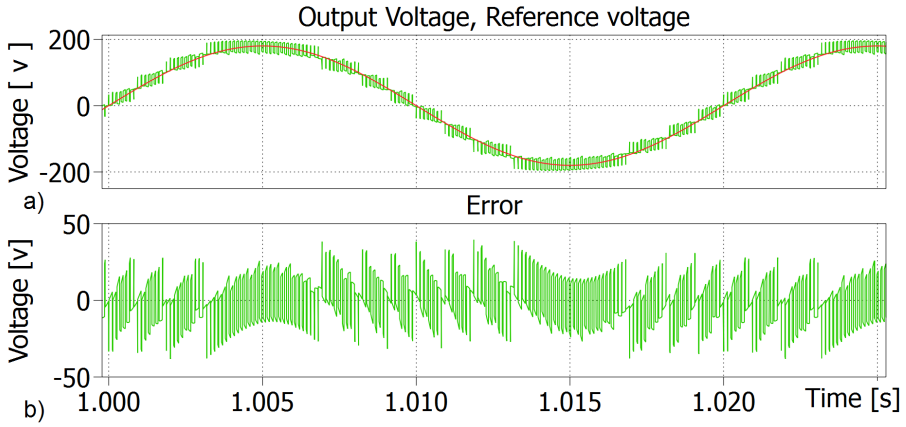

Figure 3.2: PSPWM: (a) Output and reference voltage. (b) Error.

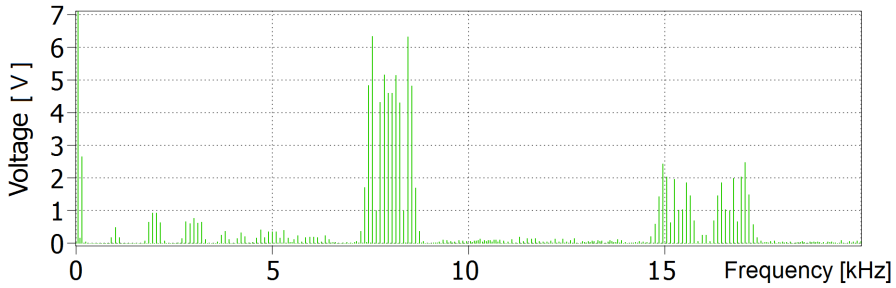

Figure 3.3: PSPWM : Harmonic content

3.1.1 Adding capacitor balancing control

A balancing control can be implemented in order to improve the internal balancing of the capacitors when using PSPWM. In Fig. 3.4 it can be seen that the cell capacitor voltages are diverging from their nominal value until t = 2 s where the balancing control is enabled.

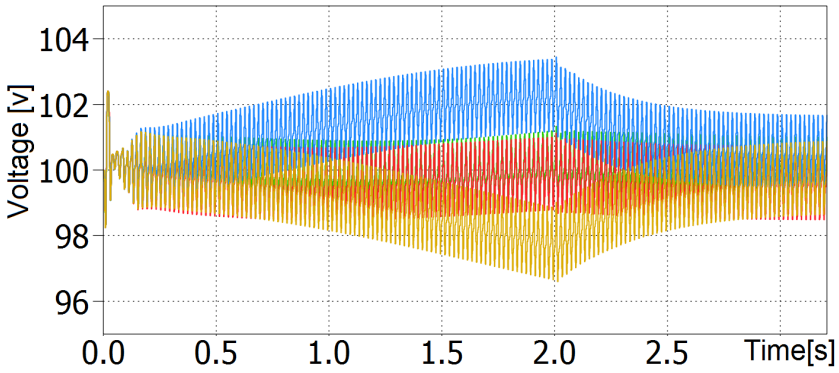

Figure 3.4: Cell capacitor ripple waveform.

3.2 Phase disposition PWM

Another multicarrier technique is the Phase Disposition Pulse Width Modulation (PDPWM) where N triangular carriers displaced with respect to the zero axis are compared to the reference signal as seen in Fig. 3.5. The technique has several disadvantages such as unequal cell capacitor ripple and hence higher harmonic distortion at the output voltage and a higher circulating current. In order to overcome these disadvantages in [32] a strategy is proposed combining PDPWM and a sort and select, where the carriers are not longer tied to each cell. As the sort and select methods are studied in the next chapter the PDPWM technique is not further studied.

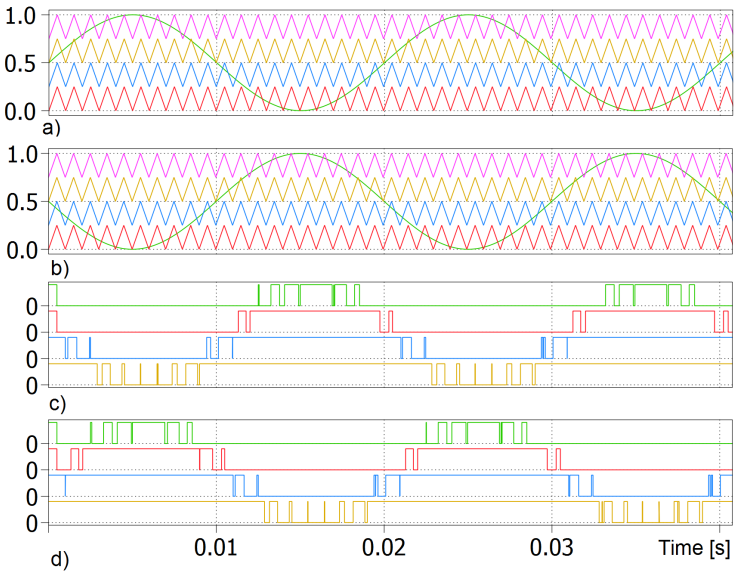

Figure 3.5: Phase Disposition Pulse Width Modulation: a) Upper arm reference generation b) Lower arm reference generation c) Upper arm gate signals d) Lower arm gate signals.

Summary

The operation principle of the PSPWM has been explained. The gate signals are generated by comparing the reference signal to N carriers. The phase displacement between carriers in the same arm, and the phase displacement between the carriers in the upper and lower arm is also presented. In order to improve the internal balancing of the cell capacitor, an balancing control method is implemented in the simulation model. Additionally PDPWM is studied, although is only explained briefly due to the necessity of adding a balancing algorithm.

Chapter 4

Carrierless methods

In this chapter several approaches of sort and select methods are presented along with simulations in order to compare their performance in terms of capacitor voltage balancing, switching frequency, output voltage harmonic content and circulating current ripple

4.1 Theory

4.1.1 Sorting

The sorting algorithm ranks the capacitor voltages from the highest to the lowest. This process has to be done in an efficient way, disregarding methods such as the bubble sorting method. In systems with a high number of cells or systems with a high sampling frequency, this could be an issue due to the computational cost. An appropriate sorting method has to be chosen depending on the hardware limitations such as memory and processor speed [33].

4.1.2 Selection

In the selection stage, the NLC performance is better than other methods in converters with a high number of levels N; on the other hand if N is low, the harmonic distortion increases due to the limited number of output voltage levels [34]. The NLC implementation is simpler than other techniques and switching losses are lower due to the low switching frequency. Nevertheless, in order to suppress or reduce the circulating current ripple a feedback controller has to be used [19]. The basic operation of the NLC is that in every sampling period, the different SM are sorted depending on their capacitor voltage and a number of cells N_{sm} are selected and introduced in the circuit depending on the reference voltage and the arm current. It can be noticed that by using this method only voltage values multiples of the capacitor voltage can be generated.

The NLC method consists of different stages as can be seen in Fig. 4.1. First the

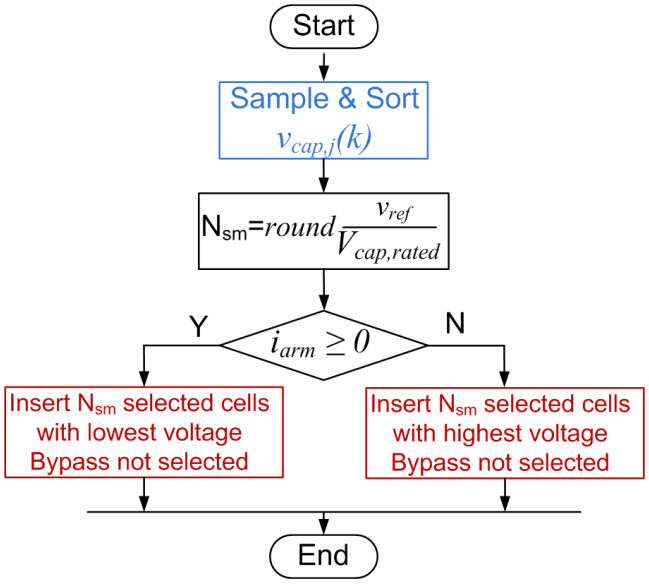

Figure 4.1: Nearest Level Control (NLC) flowchart.

phase arm reference voltage is sampled, after that it is divided by the SM capacitor voltage v_{cap} that is considered to be constant and equal to E/N. The resulting value is rounded to the closest integer, this value N_{sm} represents the number of SMs that have to be inserted in the corresponding phase arm in order to generate the nearest voltage level to the reference voltage [21]. The next stage is the capacitor balancing algorithm that makes use of N_{sm}, the arm current i_{arm} and the sorted capacitor voltages. This algorithm is in charge of maintaining the voltage level at the SM capacitors stable and balanced between the different SMs. This block inserts the N_{sm} with the most or the least charged capacitors depending on i_{arm} sign. If i_{arm} is positive the capacitors of the inserted SMs will get charged, hence the SMs with the lowest voltage level are inserted. On the other hand, if i_{arm} is negative the capacitors of the SMs inserted will get discharged, hence the SMs with the highest voltage level are inserted [20].

4.1.3 Nearest Level Control (NLC)+ Extra SM modulation

The method described in Sec. 4.1.2 has the limitation that it can only generate a finite number $N + 1$ voltage levels and only multiples of v_D/N. These issues limit the performance of MMC with a low N number of SMs. In order to avoid these limitations an additional stage can be implemented. From Fig. 4.3 it can be seen that at the sampling time instants the arm reference voltage is between two voltage levels. In the classic NLC, the nearest level will be generated, therefore the voltage level of the arm during this sampling period will be different than the reference voltage.

In order to overcome this drawback an additional stage inserts an extra SM for a

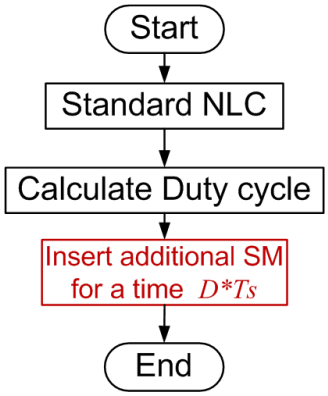

Figure 4.2: NLC+PWM flow chart.

time interval DT_s, therefore the average voltage during the sampling period can be equal to the reference signal.

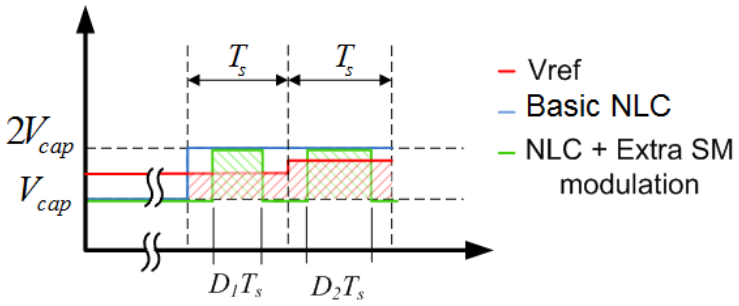

Figure 4.3: NLC + Extra SM modulation.

$$D = \frac{(V_{ref})\ MODULE\ (V_{cap})}{V_{cap}} \tag{4.1}$$

The location of the pulse on which the extra SM in inserted can be changed at the beginning or end of each sample period. This idea is further developed in the simulation in Sec. 4.2.3.

4.2 Simulation

The simulations are performed in PLECS. All the simulations models consist of a single phase MMC connected to an RL load. The parameters of the simulation are shown in Table 4.1. Two C-scripts blocks, one for each arm converter, perform the configured modulation technique. Overall the model remains the same, by changing the parameters in the control block each approach is done. A more detailed explanation about the PLECS simulation model can be found in Appendix A.

Table 4.1: Simulation model parameters.

	Value
DC link voltage	400 v
Arm inductor	1 mH
Arm resistance	10 mΩ
Number of SM per arm	4
SM capacitor	6 mF
Load inductance	1 mH
Load resistance	10 Ω

First the arm current, capacitor voltages and converter reference voltage are sampled. Second the capacitor voltages are sorted depending on their voltage value. As has been stated in Sec. 4.1, an efficient sorting method must be used. In this case the "merge sort" method is used for its better performance than other sorting methods [33]. After this, the number of SMs that have to be introduced is calculated, depending on the method used the the number of the SMs is rounded or truncated. After that the gate driving signals are generated according to the method in use.

4.2.1 Basic NLC

In the first case the basic NLC is done. The closest integer voltage value to the reference voltage is generated by the arm converter. The method is performed with a switching frequency of 5 KHz. As can be seen in Fig. 4.4 the output voltage does not contain visible switching. This is due to the fact that there is no blanking time when one SM is exchanged for another SM. It can also be noticed that the output voltage only contains the $N + 1$ possible levels that the converter can generate.

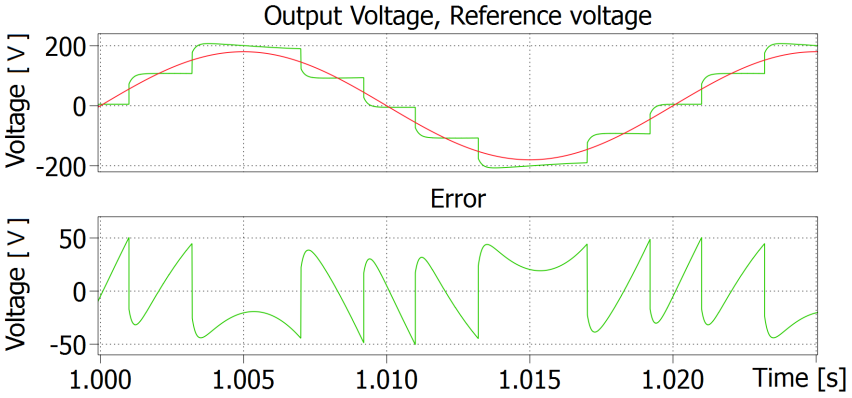

Figure 4.4: Basic NLC fs= 5 kHz, (a) Output and reference voltage. (b) Voltage error.

In Fig. 4.5 the harmonic spectrum of the output voltage can be seen. The

spectrum shows that the harmonic content is located at low frequencies around 450 Hz. There is not a considerable improvement in terms of THD if the sampling

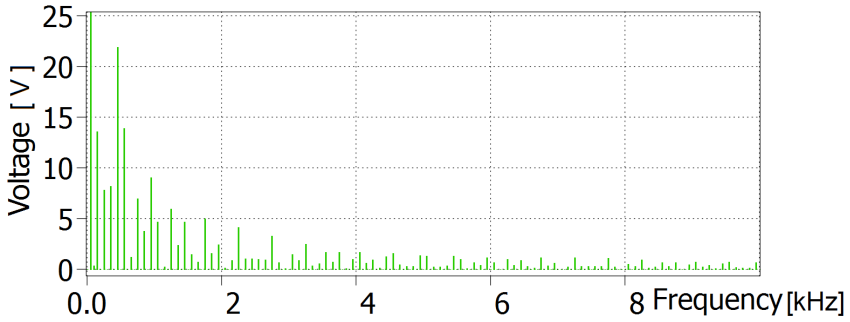

Figure 4.5: Basic NLC, fs = 5 kHz: Harmonic Spectrum.

frequency is increased as can be seen in Table 4.2, due to most of times the control algorithm change one SM by another when the capacitor voltage is not longer the highest or the lowest (depending of the current). Overall the performance of this method is poor due to the low number of SMs.

Table 4.2: THD at the different frequencies using NLC.

Sampling frequency [KHz]	1	2	3	4	5	6	7	8	9	10
THD [%]	25	20	19.5	19.3	18.4	18.6	18.7	20	20	18.7

4.2.2 NLC + PWM in an additional SM

The second method that is simulated is the NLC with Pulse Width Modulation in an additional SM. From this point, this method will be addressed as NLC+PWM. In this case the control block uses the floor function in order to calculate the number of SMs that needs to be inserted, and the PWM is performed in an extra SM. In

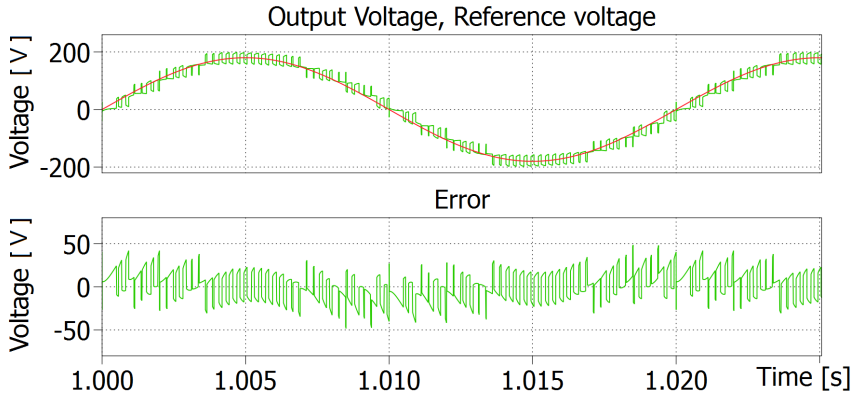

Figure 4.6: NLC+PWM, fs = 2 kHz: (a)Output and reference voltage. (b) Voltage error.

Fig. 4.6 the output and the reference voltages are depicted. In this case $2N + 1$ levels are generated due to the modulation in the extra SM in the lower and upper arm is interleaved. A more detailed view is shown in Fig. 4.7. Due to this aspect the resulting output voltage switching frequency is the sum of the two arm sampling frequencies (4 kHz).

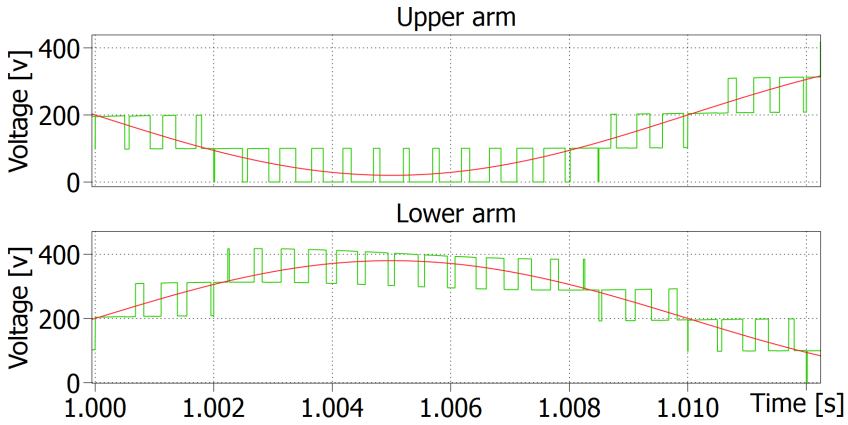

Figure 4.7: NLC+PWM: Detailed view of upper an lower arm output and reference voltages.

Nevertheless, the fact that the two arm converter switch at different time instant has the drawback that the circulating current i_c increases. From Eq. 2.14 it can be seen that in order the keep the i_c constant the sum of the two arm converter has to be constant. One issue is that when switching at the different time instants, the relation V_l and V_u is not constant, therefore a high frequency component is created in the circulating current ripple as can be seen in Fig 4.8.

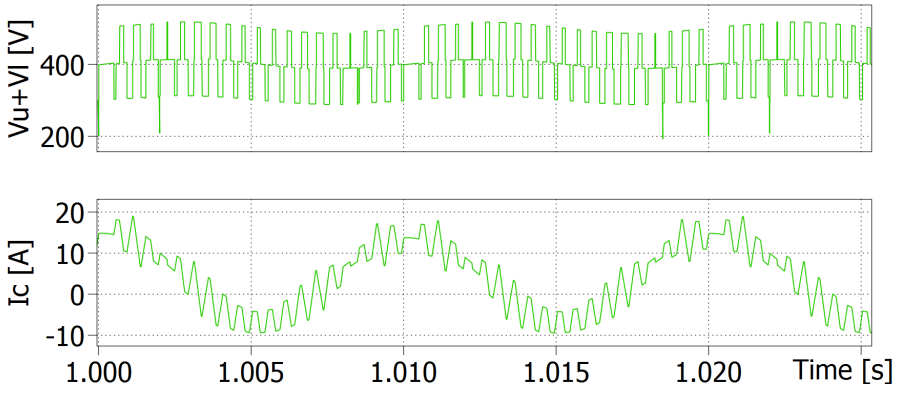

Figure 4.8: NLC+PWM, fs = 2 KHz: Sum of the the two converter arms. Circulating current.

In Fig. 4.9 it can be noticed that at 4 KHz and its side bands it is located the highest harmonic content. Moreover, it can be seen that the harmonic content

is spread along the range, with higher content at multiples of the output sampling frequency such as 8, 12, 16 KHz.

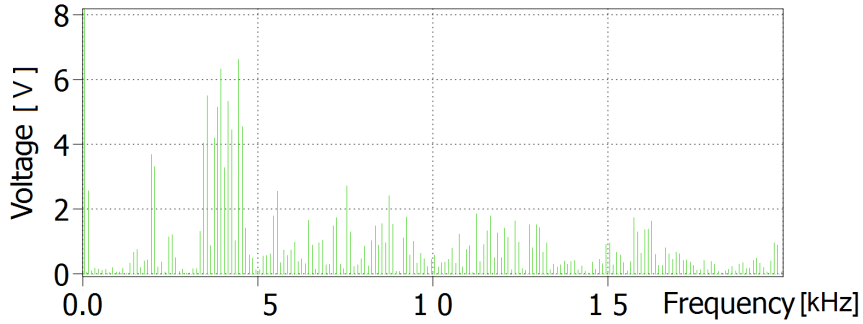

Figure 4.9: NLC+PWM, fs = 2 KHz: Harmonic Spectrum.

4.2.3 NLC with extra SM PWM: Change the location of the pulse

In this third case the difference lies in where PWM is generated within the sampling period. Taking into account if the reference voltage is increasing or decreasing, one may decide to place the pulse at the end or at the beginning of the sampling period in order to reduce the number of switchings. The main idea is that, for example, if the arm converter reference voltage is increasing it is more likely that in the next iteration of the control block, the number of SMs to be inserted is higher than in the actual iteration. Therefore, placing the pulse at the end of the sampling period would avoid two switchings.

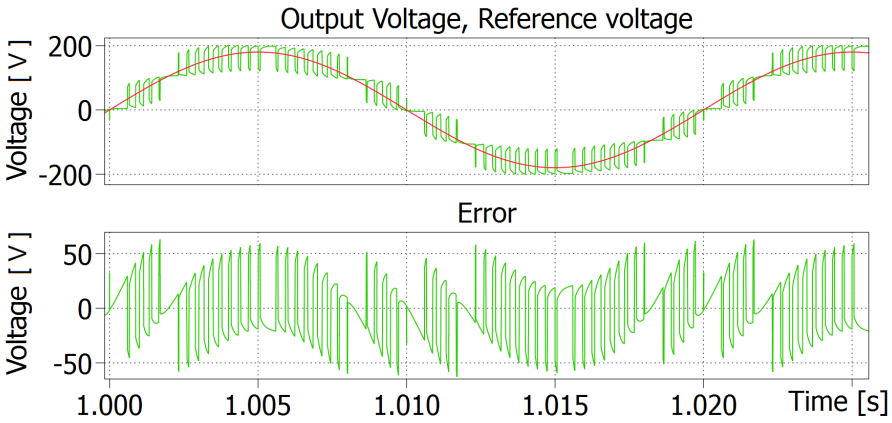

Figure 4.10: NLC+PWM, fs = 2 KHz: Output and reference voltage.

Using this approach, the sampling frequency can be increased from 2 to 3 KHz with the same number of switchings by one semiperiod of the fundamental frequency. One noticeable aspect in Fig. 4.10 is that the output voltage has only 5 levels $N+1$ in opposition to the previous case. Due to the two arm converters are inserting SMs at

the same time instant as can be seen in Fig. 4.11. For this reason the high frequency component in the circulating current is eliminated as can be seen in Fig. 4.12 as opposed to the NLC+PWM technique.

Figure 4.11: NLC+PWM, fs = 3KHz: Upper and Lower arm voltage.

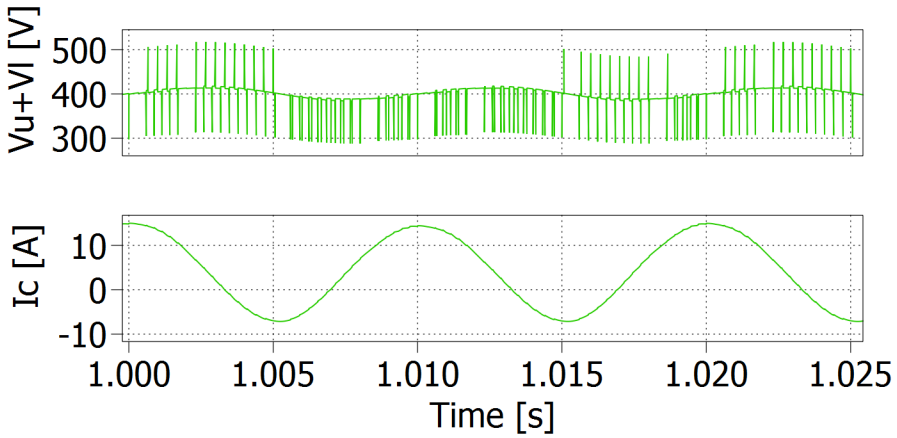

Figure 4.12: NLC+PWM, fs = 3KHz: Sum of the two arm converters. Circulation current.

The harmonic spectrum can be seen in Fig 4.13, the highest content is located at 3 KHz and its sidebands due to the switching frequency.

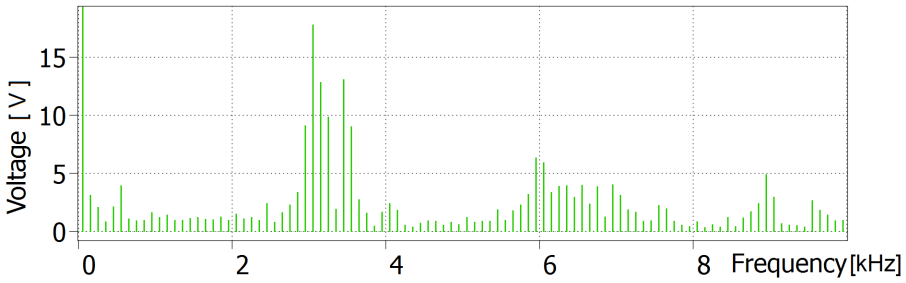

Figure 4.13: NLC+PWM, fs = 3KHz: Harmonic Spectrum.

4.2.4 NLC + Capacitor ripple control

In this section a modification of the NLC is presented. In Fig. 4.14 a zoomed view of the output arm voltage using NLC as in Sec. 4.2.1 shows that during multiple time instants the converter introduce the same number of cells as the previous time instant with the only difference that it exchanges the cell or cells used.

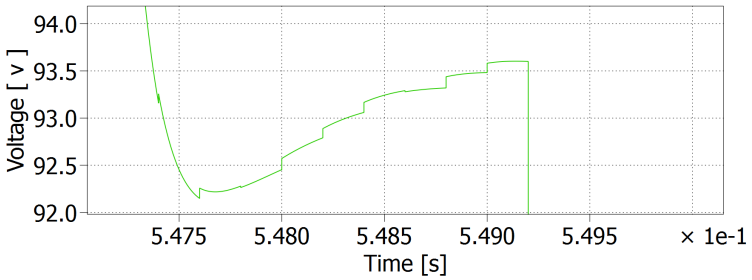

Figure 4.14: Basic NLC: Output Voltage zoomed view.

Using the classical NLC approach the capacitor voltage ripple is minimized, nevertheless the switching frequency gets increased and consequently the switching losses of the converter. The main idea of the method presented in this section is to avoid unnecessary switching while maintaining the capacitor voltages within certain limits. This would create a tolerance band for the capacitor voltage where the switching of the SM is avoided. Generally this band is ±10% of the nominal value. A flowchart of this method is shown in Fig. 4.15.

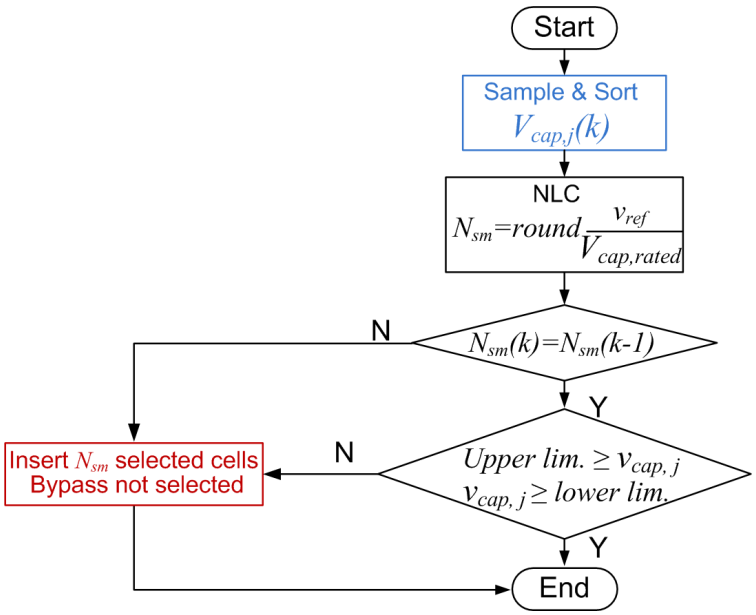

Figure 4.15: NLC + Capacitor ripple control: Flowchart.

The output voltage and the error between the reference and the output voltage can be seen in Fig. 4.16. It can be noticed that there are practically no differences to the classic NLC in Fig. 4.4. A zoomed view is shown in Fig. 4.17. It can be noticed that the switching is eliminated during that time period. Using this approach with a capacitor sampling frequency of 5 KHz and 4 SM per arm, the switching frequency is reduced from approximately 1000 Hz to 80-100 Hz per SM.

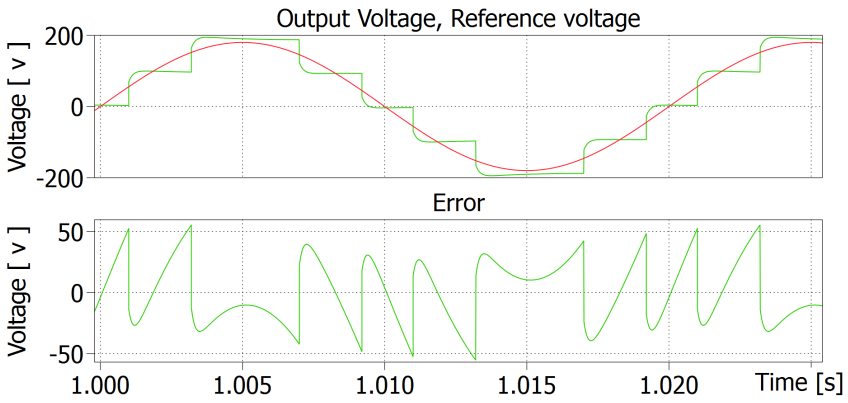

Figure 4.16: NLC+ Capacitor ripple control: (a) Output Voltage. (b) Error.

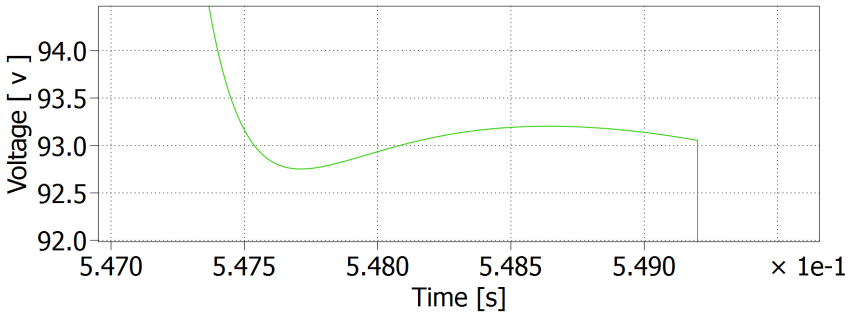

Figure 4.17: NLC Capacitor ripple control: Output voltage zoomed view.

As can be seen in Fig. 4.18 a), during the charging of the capacitor as soon as one capacitor is not longer the least charged, is immediately changed in the next iteration of the control script by the new least charged capacitor. This results in a high number of switchings that cause higher losses in the converter. On the other hand the capacitor ripple is kept to less than 2% of the nominal value. In Fig. 4.18 b) the exchange of SM is avoided unless the capacitor voltage exceeds ±5% of the nominal value. A comparison of the gate signals for both methods is shown in Fig. 4.19. As can be seen for the NLC classic has a higher number of switching as it exchanges the cells multiple times whereas in the other method the switching is reduced to a minimum.

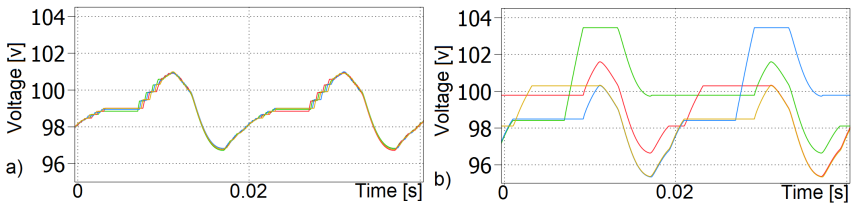

Figure 4.18: Arm capacitor voltages: a) Basic NLC b) NLC with capacitor ripple control.

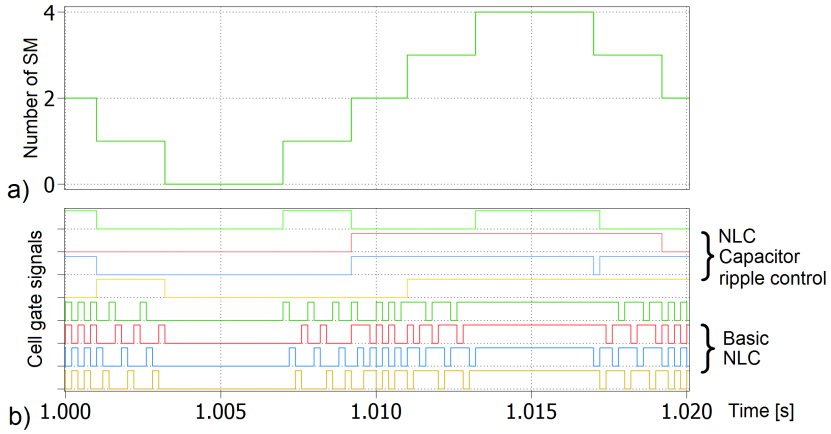

Figure 4.19: a) Arm output voltage levels b) Cell gate signals.

The harmonic spectrum of the output voltage can be seen in Fig. 4.20. The highest harmonic content is located at the resultant switching frequency (550 Hz). Furthermore, there are harmonic components at frequencies multiples of 550 Hz and their sidebands.

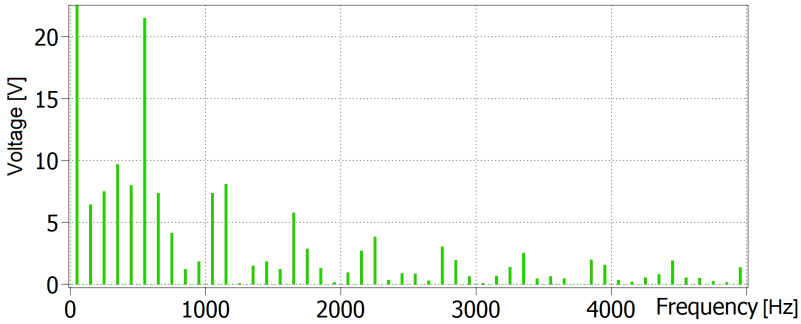

Figure 4.20: Output voltage harmonic spectrum: NLC + Capacitor ripple control.

4.2.5 NLC + advanced capacitor ripple

The control algorithm presented in the previous section is based on the fact that for multiple time instants the number of SM inserted is the same as the previous time

instant. This is valid for MMC with a low number of SM, however for MMC with higher number of SM this approach is not valid as it can be seen in Table 4.3. With the increasing number of SM, there is a increasing number of voltage levels, therefore the control algorithm changes the number of cells inserted more frequently.

Table 4.3: Switching frequency for different number of cells per arm. f_s =5000 Hz.

Number of cells N	4	8	12	20	40	100
NLC Classic [Hz]	850	800	800	850	900	800-900
NLC+Cap.ripple [Hz]	80-100	90-130	120-200	380-440	700-850	700-900

In Table 4.3 it is shown that for MMCs with higher number of SM the switching frequency tends to equalize. In order to improve the performance of modulation algorithm presented in the previous section a more complex method has to be designed. A flowchart of the modulation algorithm is depicted in Fig 4.21. Moreover, several improvements have been introduced in the modulation algorithm as it has to be executed with a high frequency especially in large MMCs, as previously explained in Sec. 2.5. These modifications avoid the sorting of the list containing the cell capacitor voltages for the cases where it is unnecessary like for example when all SM have to be inserted or bypassed.

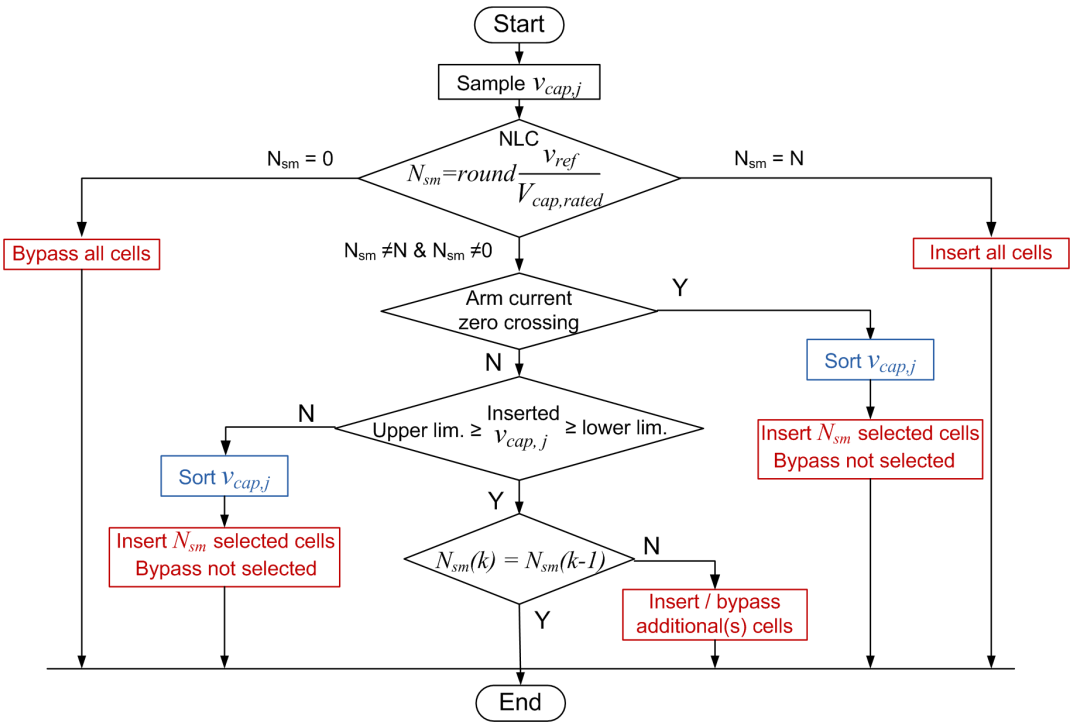

Figure 4.21: NLC+ Advanced Capacitor ripple flowchart.

Simulation results of the MMC with different number of cells are presented in Table 4.4 where the resultant switching frequency and the cell capacitor voltage ripple are shown. As it can be seen the capacitor voltage ripple is kept within limits while ensuring a lower switching frequency than the previously presented methods. From this point of the document only the NLC + advanced capacitor ripple is considered and it is referred as NLC +CRC.

Table 4.4: Switching frequency for different number of cells per arm, f_s =5000 Hz.

Number of cells N	4	8	12	20	40	100
Switching freq. [Hz]	50-85	60-140	50-120	60-190	80-200	200-300
Capacitor voltage ripple [%]	4	10	10	10	10	10

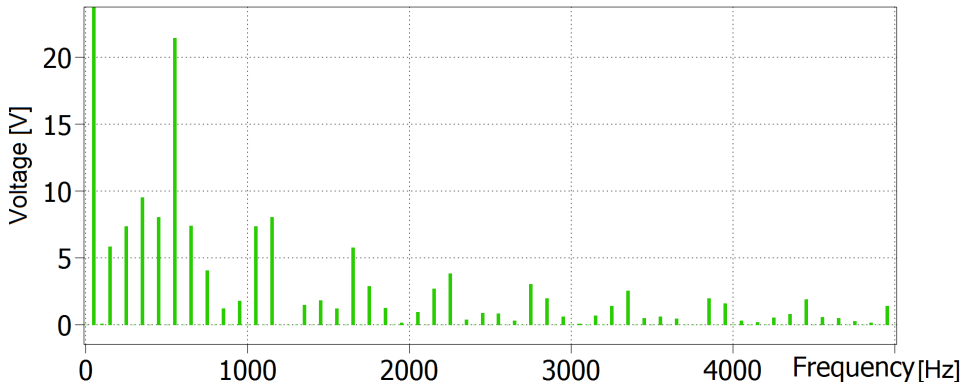

Figure 4.22: Output voltage harmonic spectrum: NLC+ Advanced Capacitor ripple.

Summary

Several NLC methods have been studied and simulated. Their performance in terms of switching frequency, capacitor voltage, circulating current and output voltage THD has been evaluated. It has been seen that the highest harmonic content when using PWM is located the sampling frequency and its sidebands, while for methods without PWM is located at low frequencies below the switching frequency of each SM. For MMCs with a low number of SM a PWM in required for a better performance of the converter. In addition the NLC+ Advanced CRC method allows the converter to operate with low switching frequency while maintaining the capacitor voltage ripple within limits.

Chapter 5

Comparison of modulation methods

A comparison of the different control methods previously explained is performed in this chapter. The simulations are done for different numbers of cells per arm per phase 4, 40, 100. Notice that the case for 4 cells is far from being realistic for an HVDC converter therefore it is performed with the laboratory setup parameters. For the test cases of 40, 100 the simplified model of the arm converter presented in Sec. 2.4 has been used in order to accelerate the simulation speed.

The comparisons are done in the following way:

1. The simulation is performed for the PSPWM case for the selected number of cells.
2. Either the resulting THD content or the resulting switching frequency is considered as fixed.
3. The remaining control methods are simulated in order to obtain similar results as the previously fixed result from the PSPWM case.
4. Results for the three cases are presented and discussed.

5.1 Model description

The simulations model in this chapter makes use of a circulating current control and power control. The NLC and its derived methods are performed by C-script for each arm converter. A more detailed view is depicted in Appendix A.

5.2 Comparison: Laboratory parameters

In this section a comparison of the different modulation methods is performed using the parameters of the small scale prototype listed in Table 5.1.

Table 5.1: Small scale prototype parameters used for the comparison.

Parameters of the small scale prototype		
Power	2 KVA	
DC link voltage	±200 V	
Alternating voltage line to line	240 V	
Number of cells per arm	4	
Arm Resistance	0.1 Ω	
Arm Inductance	5.2 mH	0.082 pu
Grid Resistance	0.144 Ω	0.005 pu
Grid Inductance	1.89 mH	0.03 pu

The common denominator in the results of the comparison is the switching frequency that in this case is 800 Hz as it can be seen in Table 5.2. Nevertheless, with the NLC+CRC the switching can not be increased up to 800 Hz despite increasing the sampling frequency up to 10000 Hz. In Fig. 5.1 the three phase output voltage are shown where the PWM for the two cases PSPWM and NLC+PWM can be noticed. The waveforms of the capacitor voltages for the 4 cases are shown in Fig. 5.4.

Table 5.2: Comparison. Laboratory Prototype parameters. Caps = 4 mF.

Modulation technique	PSPWM	NLC	NLC+PWM	NLC+CRC
Switching freq. [Hz]	800	800-900	800-900	60-120*
Capacitor sampling freq. [Hz]	-	5000	2000	10000
Capacitor voltage ripple [%]	1.5	2	1.5	3.5
Output voltage THD [%]	6.41	7.6	7.15	7.6
Ripple i_c [pu]	0.9	1.5	1.25	1.25

As it can be noticed in Fig. 5.2 the circulating current ripple is high for the 4 cases due to the low number of SM. For the two cases where PWM is performed, PSPWM and NLC+PWM, the amplitude of the current ripple is more constant in opposition to the other two techniques. A more detailed view of the circulating current waveform is shown in Fig. 5.3 where it can seen that circulating current is composed by a DC component and 100 Hz component, additionally in the two cases where the modulation performed there is a high frequency component. The waveforms of the capacitor voltages for the 4 cases are shown in Fig. 5.4 where all the four techniques are able to maintain the voltage ripple under 4%.

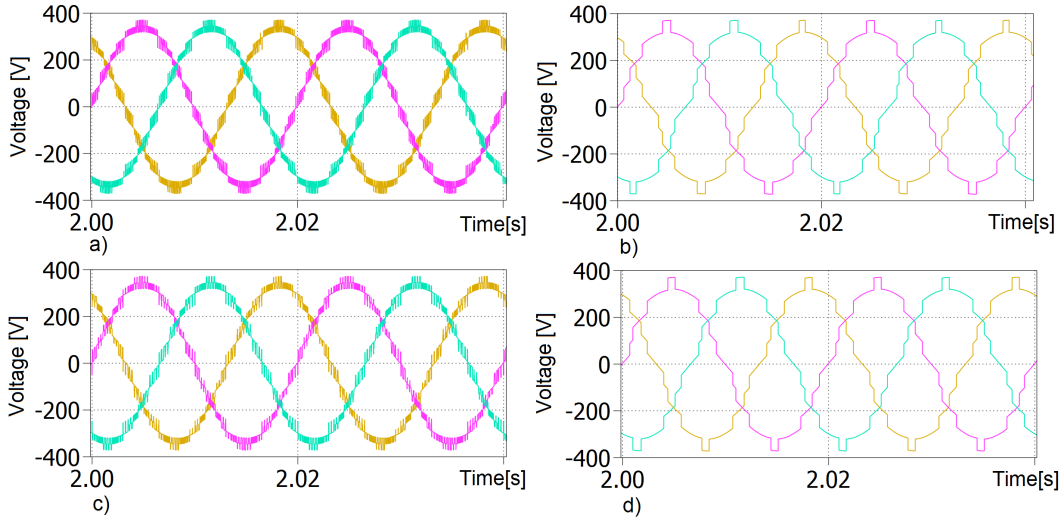

Figure 5.1: Three phase line to line output voltage: a) PSPWM b) NLC c) NLC+PWM d) NLC+CRC.

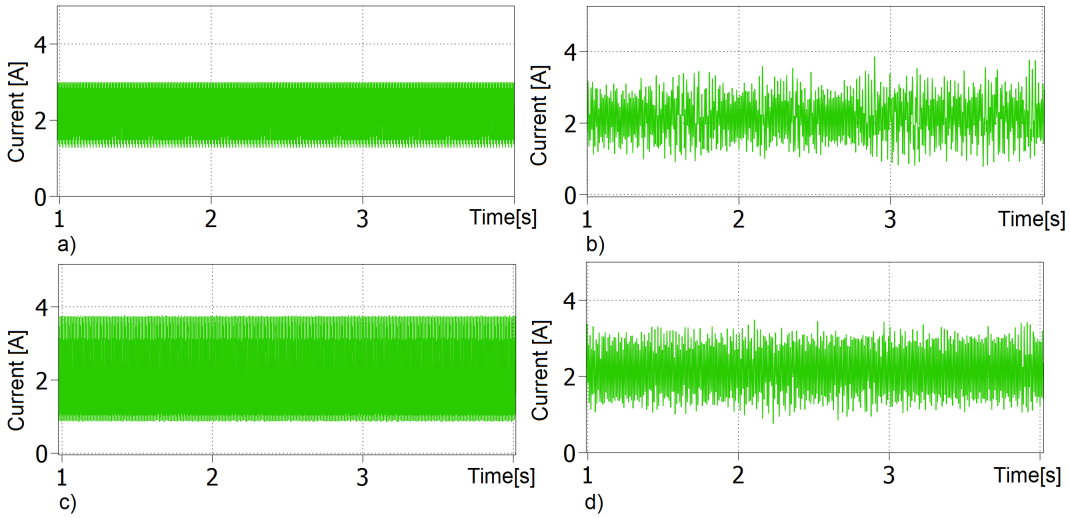

Figure 5.2: Phase A circulating current: a) PSPWM b) NLC c) NLC+PWM d) NLC+CRC.

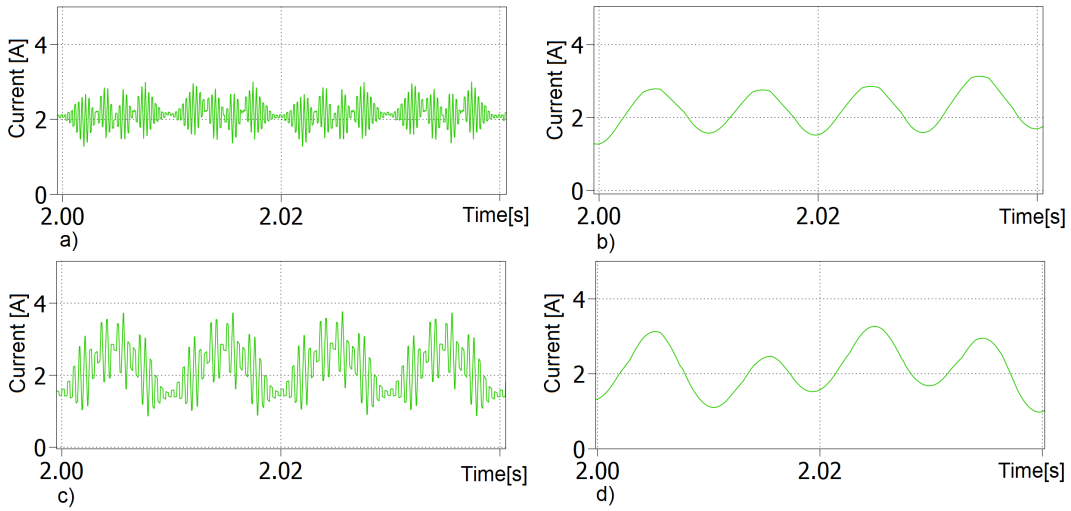

Figure 5.3: Phase A circulating current zoomed view: a) PSPWM b) NLC c) NLC+PWM d) NLC+CRC.

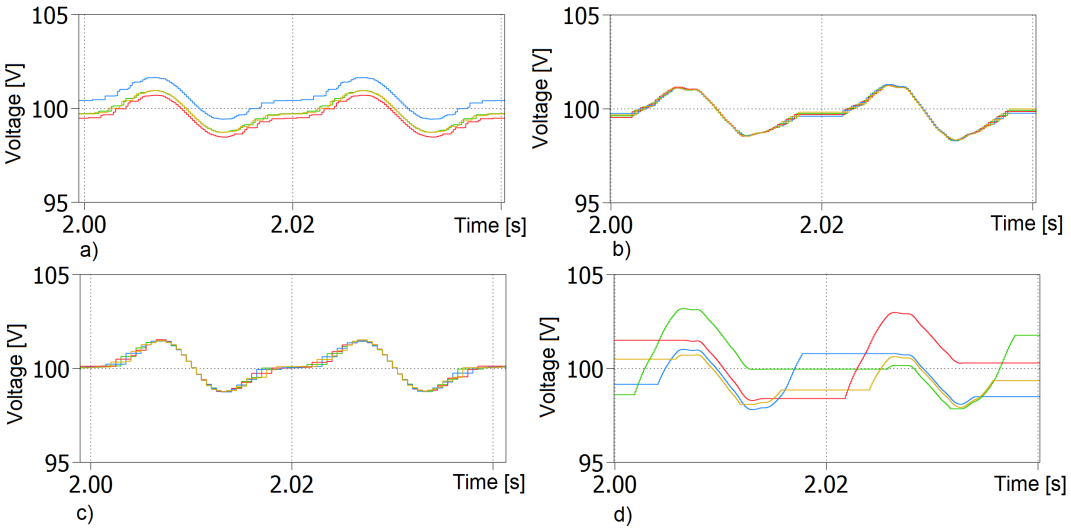

Figure 5.4: Cell capacitor voltage ripple: a) PSPWM b) NLC c) NLC+PWM d) NLC+CRC.

5.3 Comparison: HVDC parameters.

The simulation parameters are chosen based on the parameters of the 1 GW MMC-HVDC system [22] which are depicted in Table 5.3. The size of the capacitor is calculated according to Eq. 2.26. A detailed description of PLECS simulation model is given in Appendix A

Table 5.3: HVDC parameters used for the comparison [22].

Parameters		
Active power	1 GW	-
cos ϕ	0.957	-
Reactive power	300 MVAR	-
DC link voltage	±320 kV	
Alternating voltage Line to line	400 kV	
Arm Resistance	12.26 Ω	0.08 pu
Arm Inductance	48 mH	0.10 pu
Grid Resistance	0.76 Ω	0.005 pu
Grid Inductance	24 mH	0.05 pu

5.3.1 40 SM: Similar switching frequency

For this first comparison 40 SM per arm are used. In this case the PSPWM case is simulated with a switching frequency of 222 Hz per SM as it can be seen in Table 5.4. Frequencies that are integer multiples of the fundamental frequency should not be used in order to avoid imbalances at the capacitor voltage [31]. For the NLC and NLC+PWM cases the sampling frequency of the system had to be decreased in order to obtain a similar switching frequency as the PSPWM case. This leads to a higher harmonic distortion at the output voltage, 2.4% and 3.0% for NLC and NLC+PWM respectively. As the output voltage does not contain N+1 levels as it can be seen in Fig. 5.5. On the other hand for NLC+CRC the sampling frequency has been increased in order to try to obtain a similar switching frequency to the other cases. Due to the high sampling frequency the THD for this case is the lowest (0.7%).

Table 5.4: Comparison N=40. Same switching frequency. Caps=1.1 mF

Modulation technique	PSPWM	NLC	NLC+PWM	NLC+CRC
Switching freq. [Hz]	222	180-280	160-260	80-180
Capacitor sampling freq. [Hz]	-	2000	1600	10000
Capacitor voltage ripple [%]	14	10	9	10
Output voltage THD [%]	1.2	2.4	3.0	0.7
Ripple i_c [pu]	0.14	0.34	0.10	0.16

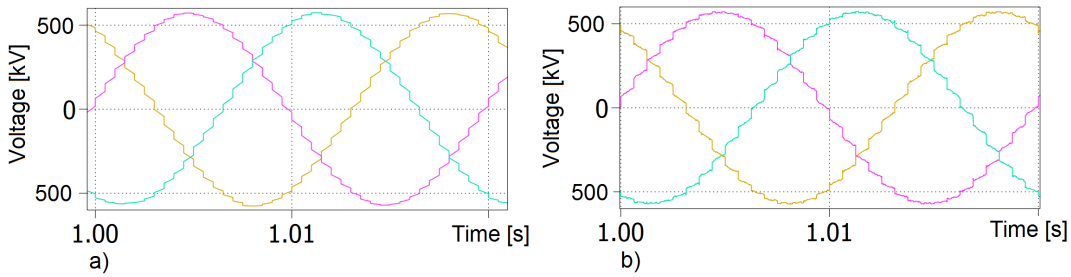

Figure 5.5: Three phase output voltage: a) NLC. b) NLC+PWM.

5.3.2 40 SM: Similar THD content

For the second comparison the converter consists of 40 SM per phase per arm. The fixed result is the THD at the output voltage. It can be noticed from Table 5.5 that in order to obtain similar THD at the output voltage the NLC and NLC+PWM modulation techniques have to switch three times faster with the PSPWM. This leads to higher switching losses and lower efficiency of the converter. On the other hand, the NLC+CRC is able to switch with the lowest frequency among the 4 cases and therefore keep the switching losses to a minimum. The cell capacitor voltage ripple in the PSPWM is the highest 14%, due to the lack of an additional capacitor voltage control as proposed in [16].

Table 5.5: Comparison N=40. Same THD. Caps=1.1 mF

Modulation technique	PSPWM	NLC	NLC+PWM	NLC+CRC
Output voltage THD [%]	1.2	1.2	1.25	1.26
Switching freq. [Hz]	222	500-650	600-750	60-160
Capacitor sampling freq. [Hz]	-	4800	4500	4500
Capacitor voltage ripple [%]	14	9	8	11
Ripple i_c [pu]	0.14	0.21	0.04	0.16

It can be seen in Fig. 5.6 that for the four cases the highest harmonic contents are located at the sampling frequencies and their multiples. In Fig. 5.6 a) it can be noticed that there are low frequency harmonics located at the switching frequency (222 Hz) while in Fig. 5.6 b) c) and d) the harmonics are spread along the different switching frequencies. In Fig. 5.6 c) the harmonics are located at 4500 hz and its sidebands due to the PWM done in the additional SM. Moreover, there are harmonics at double of this frequency originated by the sum of the switching frequencies of the upper and lower arm.

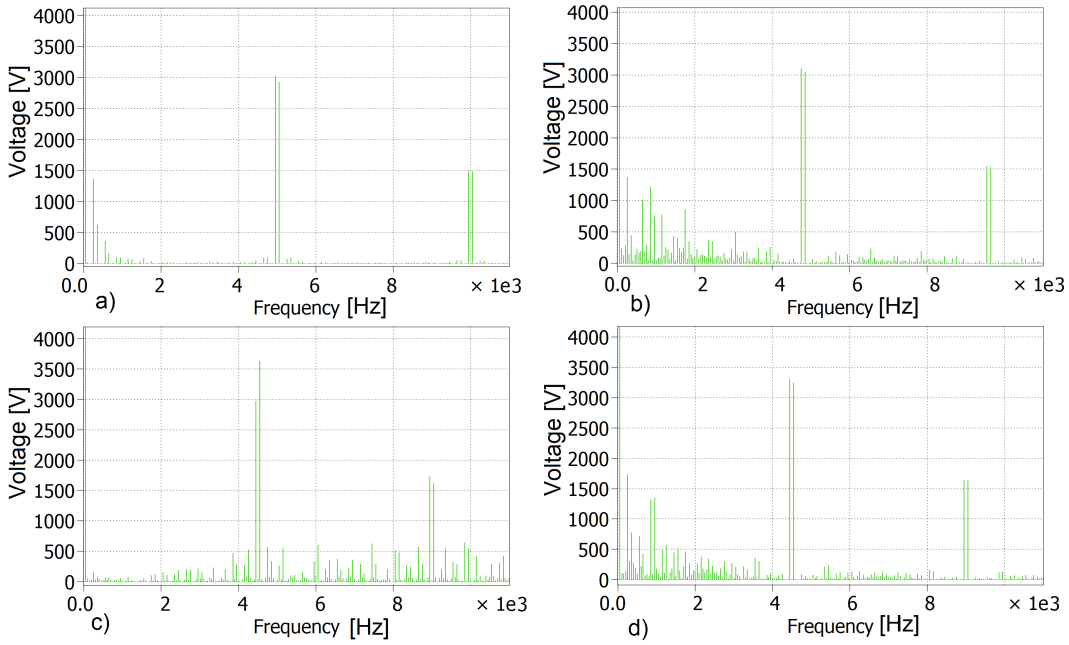

Figure 5.6: Output voltage Harmonic Spectrum, N=40. Phase A : a) PSPWM b) NLC c) NLC+PWM d) NLC+CRC.

5.3.3 100 SM: Similar Switching frequency

In this comparison the MMC has 100 cell per arm.

Table 5.6: Comparison N=100. Same Switching frequency. Caps=2.7 mF

Modulation technique	PSPWM	NLC	NLC+PWM	NLC+CRC
Switching freq. [Hz]	168	140-220	150-250	60-200
Output voltage THD [%]	1.07	3.0	3.0	1.2
Capacitor sampling freq. [Hz]	-	1600	1600	4000
Capacitor voltage ripple [%]	19	9	8	11
Ripple i_c [pu]	0.15	0.23	0.10	0.18

In Table 5.6 it can be appreciated that for similar switching frequencies the NLC and NLC+PWM methods present higher THD than the other control methods. This is due to the fact that the sampling frequencies have been reduced in order to obtain a similar switching frequency as in the PSPWM. These frequencies are below the frequency f_1 that is 2221 Hz as it has been previously calculated in Sec. 2.5. Therefore the converter is not able to generate N+1 levels and its output. In addition, it can be noticed that a converter with 40 and 100 cells per arm with equal sampling frequency present similar THD at the output voltage due to the low sampling frequency. Fig. 5.8 shows that both converters can only generate 17 different voltage output levels despite having 40 and 100 cells in each case.

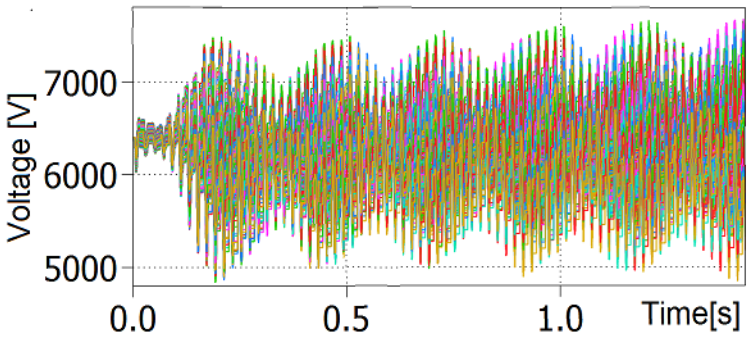

Figure 5.7: Cell Capacitor voltages: PSPWM N=100.

In Table 5.6 it is shown that the capacitor voltage ripple for PSPWM case is 19% while with other methods it is not higher than 11%. Fig. 5.7 shows the cell capacitor voltages time evolution for the PSPWM case.

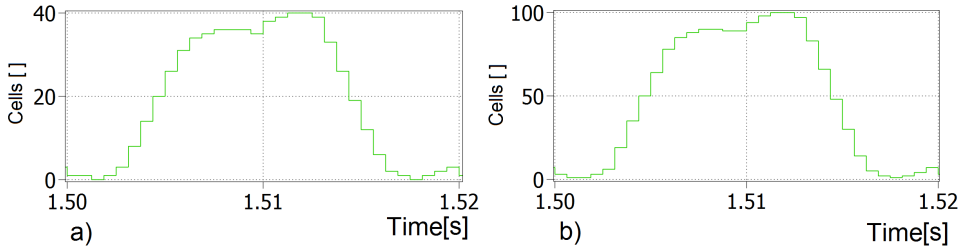

Figure 5.8: Levels at the upper arm converter : a) N=40 b) N=100.

5.3.4 100 SM: Similar THD content

Table 5.7: Comparison N=100. Same THD. Caps=2.7 mF

Modulation technique	PSPWM	NLC	NLC+PWM	NLC+CRC
Output voltage THD [%]	1.07	0.87	1.07	1.08
Switching freq. [Hz]	168	500-660	500-700	60-200
Capacitor sampling freq. [Hz]	-	5000	4500	4500
Capacitor voltage ripple [%]	19	8	8	11
Ripple i_c [pu]	0.15	0.07	0.04	0.15

The four methods present similar harmonic content as it can be noticed in Table 5.7, nevertheless, the NLC and NLC+PWM methods switch with higher frequency and therefore the converter have higher losses. On the other hand, with these two methods the circulating current ripple is reduced unlike the other methods.

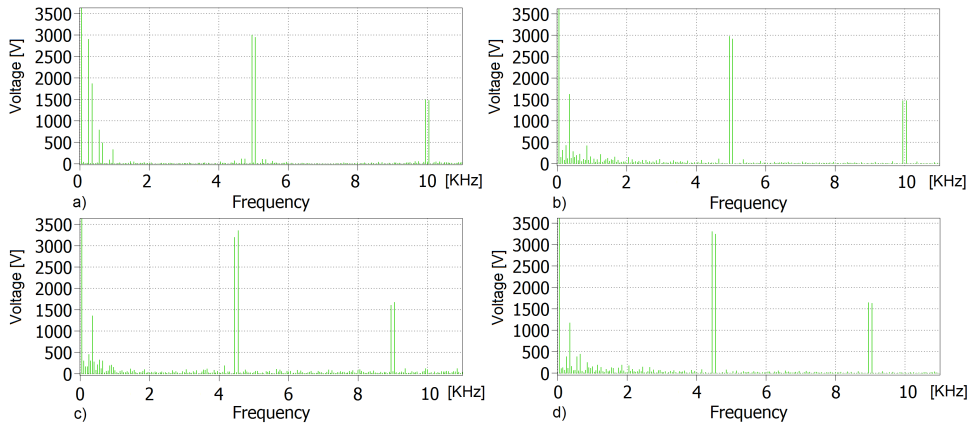

Figure 5.9: Output voltage Harmonic Spectrum: a) PSPWM b) NLC Classic c) NLC+PWM d) NLC+CRC.

In Fig. 5.9 the output voltage harmonic for the four cases is shown. It can be noticed harmonic content at low frequencies (<1 KHz). While the highest harmonic content is located at the sampling frequency and its multiples.

5.4 Summary

A comparison of the different modulation techniques is performed in this chapter for different converter types. The first comparison uses the parameters of the small scale prototype. The performance of the different methods is limited by the low number of cells per arm (4), especially in terms of THD at the output voltage and circulating current ripple. On the other hand the modulation methods are able to maintain balanced the cell capacitor voltages. The second and third comparison make use of an HVDC system parameters. The PSPWM technique offers a good performance in terms of switching frequency and THD at the output voltage. Nevertheless in order to limit the capacitor voltage ripple a balancing control is needed. NLC+PWM offers the best in terms of reducing the circulating current ripple. However, the method has the highest switching frequency among the compared methods. Finally the NLC+CRC ensures a low switching frequency while ensuring the balancing in the capacitor voltages.

Chapter 6

Experimental Setup

In this chapter it is explained the hardware developed and used for this thesis. As some of the SM hardware design was previously developed, a more detailed explanation is given only for the work done during this project although the whole system is described.

6.1 SubModule description

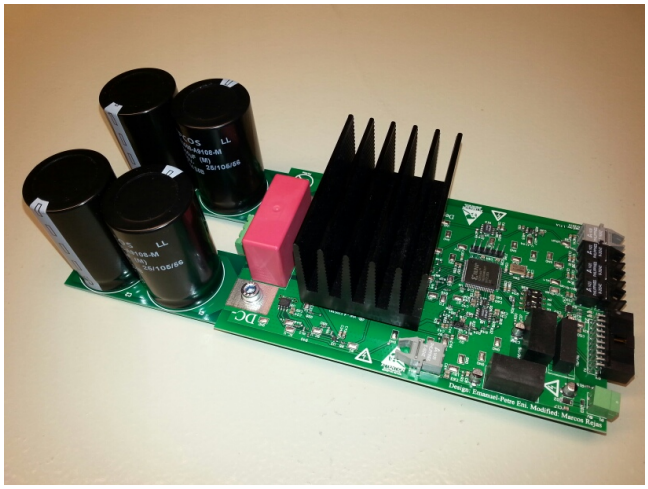

Figure 6.1: Submodule board with the Capacitor board.

The main features of the SM board are the following:

- Power modules of 600V / 15A 3 phase IGBT.
- Overcurrent, Overtemperature and overvoltage protection.
- Capacitor voltage measurement.

- Intelligent Power Module temperature measurement.
- Communication with the dSPACE system.
- Dead time generation.
- 4 mF total cell capacitance.

6.1.1 Complex Programmable Logic Device (CPLD)

On each SM a CPLD is placed, a Xilinx XC95144XL-10TQG100I. The tasks of the CPLD are:

- Receive the PWM signals from dSPACE system.
- Receive the enable signal from the dSPACE system.
- Generate the PWM signals for the IPM module with an appropriate dead time.
- Receive the fault signals and stop the generation of the PWM signals in case a fault has been triggered.

Run-Stop behaviour

One of the optic fiber receivers is used for the Run-Stop signal of each board. The main idea is that when there is a low voltage level at the Run input, the board remains in stop mode. During the transition from low to high a reset signal is generated to clear the fault flags. When there is a high voltage level on the Run input during more than 3 ms, the board goes to run or normal operation mode. In order to implement this behaviour a Finite State Machine(FSM) has been designed as it can be seen in Fig. 6.2. The VHDL code for the FSM can be found in the Appendix C.2.

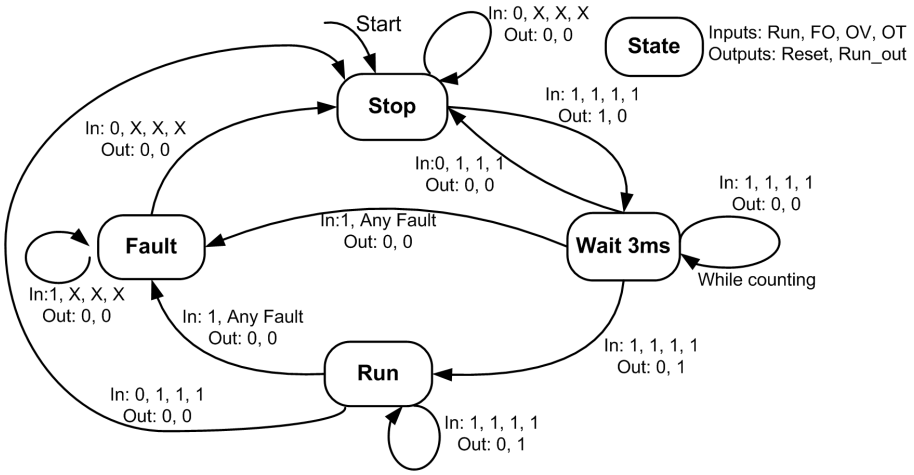

Figure 6.2: Run-Stop State Machine.

6.2 MMC prototype description

A diagram of the laboratory setup build for this Master Thesis is depicted in Fig. 6.3. The prototype is a 3 phase MMC with four cells per arm. Each cell has been modified in order to create a half bridge cell. The hardware setup consist on:

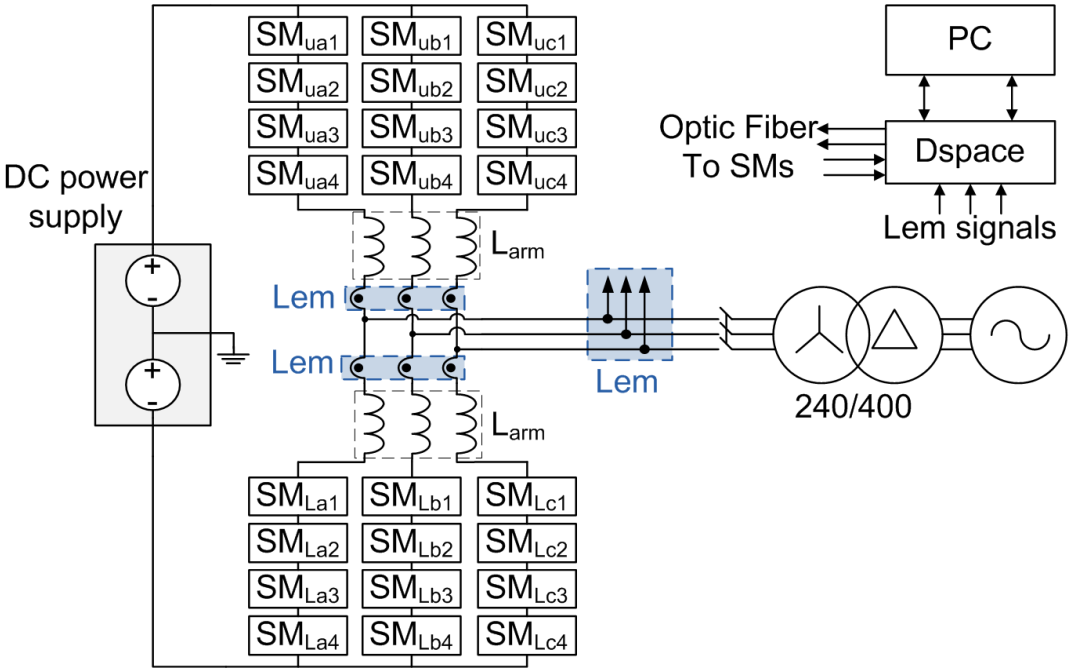

Figure 6.3: Laboratory setup diagram.

- Constant DC power supply 400 V / 8A acting as the DC-link.
- Lem box measurement in order to measure arm currents and output voltage.
- Three phase arm inductor of 5.2 mH.
- Star-Delta transformer.
- AC power supply acting as grid.
- PC equipped with dSPACE for a centralized control connected by means of optic fiber to every SM.

In Fig.6.4, a picture of the small scale prototype is shown with the different components that integrate the setup.

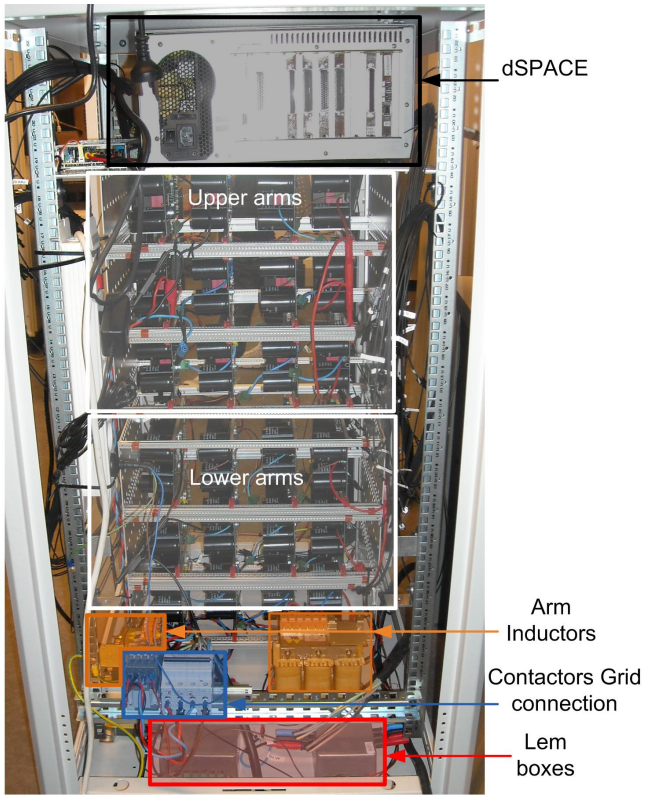

Figure 6.4: Back view: Small scale prototype setup.

6.3 Experiments and results

Experimental implementation of the studied methods has been performed yet. Nevertheless several test has been done in order to verify the correct performance of the SMs. They are shown in Appendix B

Chapter 7

Conclusion and future work

7.1 Conclusion

Several modulation methods have been studied and simulated. They have been compared in order to study their performance for different converter ratings and some conclusions can drawn:

- There is not best modulation, every analysed method have advantages and disadvantages.
- For low number of SMs, a PWM is needed in order to offer a better performance.
- It has been shown that some modulation methods performances depend on the number of cells of the converter.
- In addition for MMC with high number of cells the modulation algorithm complexity gets increased. Furthermore the sorting /balancing algorithm must perform in a efficient way as sampling frequency must increase with the increment of the number of cells.
- PSPWM offers a good performance, with the advantage that there is no required to measured the capacitor voltages. Nevertheless, in order to improve the capacitor voltage balance an additional balancing control is needed. Therefore the advantage of not requiring the measure the capacitor voltage is eliminated.

Some of the contributions of this Master Thesis are the developed tools:

- MMC PLECS model: A totally configurable MMC model for any power rating, number of cells, arm inductance. Furthermore any thermal description may be included.
- Switching counter: In order to calculate the switching frequency when no carrier are used, a switching frequency calculation block has been developed.
- Small scale prototype: It has been designed and assembled.

7.2 Future work

The first task that should be solved is to finish the verification of the laboratory setup and implement the simulation models that have been studied. Reduction of switching losses, reduction of the ripple in the cell capacitor voltage or improve the balancing of the capacitors are aspects that can be validated in the low scale prototype. In addition the control and modulation for N equal to 4, has to be improved. Another future task could be to improve the NLC+CRC in order to obtain switching frequencies close to the fundamental (50 Hz). An study of the time that the different methods require to recover from an unbalanced situation on the capacitor voltages can be performed. Other multi carriers methods can be object of study in the future. Moreover, advanced modulations techniques such as the ones mentioned in the state of art are worth to study and therefore improve the comparison between the different modulation methods.

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Appendix A

PLECS modelling

A.1 Thermal model

In order to design the converter, ensure a safe operation and measure the losses in each cell a thermal model of the switching device has been designed in PLECS as it is depicted in Fig.A.1. The switching devices are enclosed within a heatsink that has a thermal resistance represented by R_{th}. These devices and the heatsink are at the same temperature that variates depending on the losses of the components that are covered by the heatsink. In order to account the losses of the switching devices

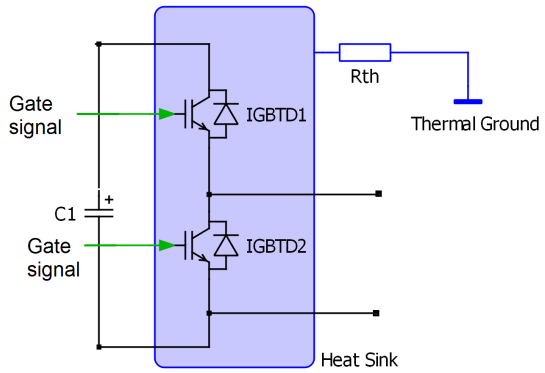

Figure A.1: Plecs cell schematic including thermal components.

a thermal description is modelled according to the documentation provided by the manufacturer. In Figs A.3 and A.2 the thermal description of the Intelligent Power Module (IPM) is shown.

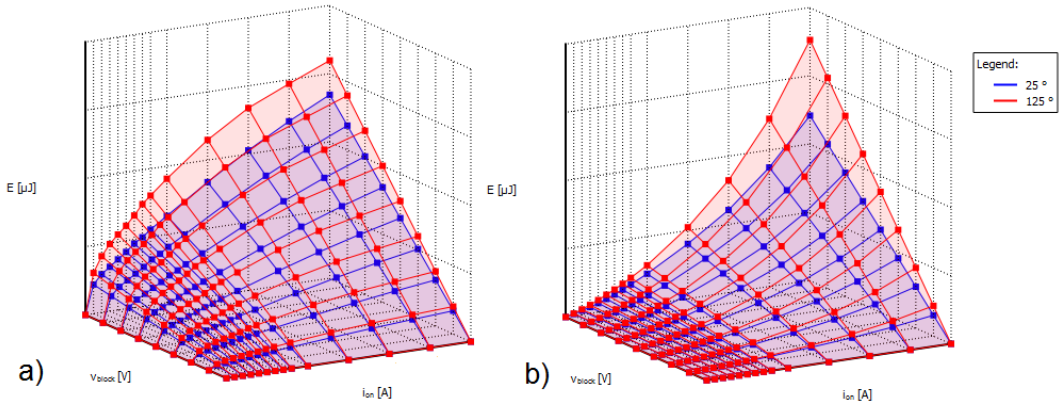

Figure A.2: IGBT Switching losses: a) Turn off b) Turn on.

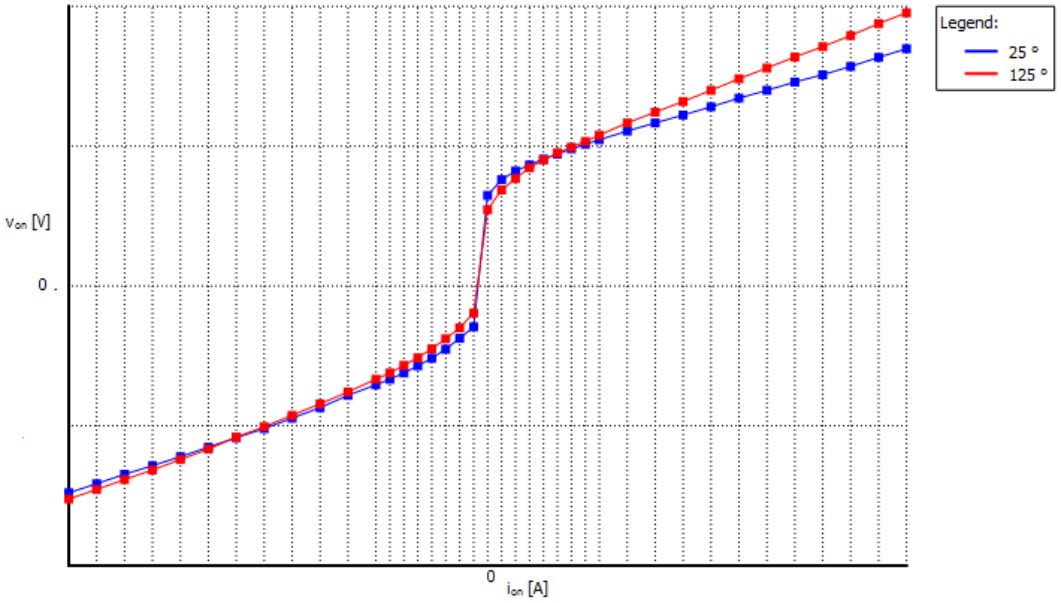

Figure A.3: IGBT Conduction losses.

A.2 Arm Converter

The arm converter is a N cell series connected subcircuit. It has two configurations, the switched configuration as shown in Fig. A.4 that also includes the thermal modelling of the IGBTs. The second configuration is depicted in Fig. A.5 which functionality has been previously explained in Sec. 2.4.

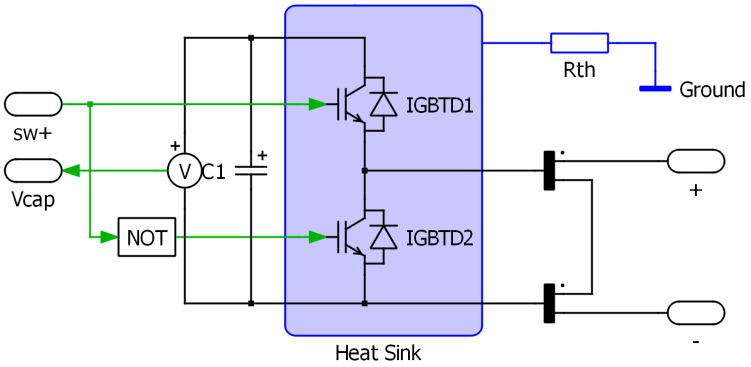

Figure A.4: Arm converter PLECS circuit [35].

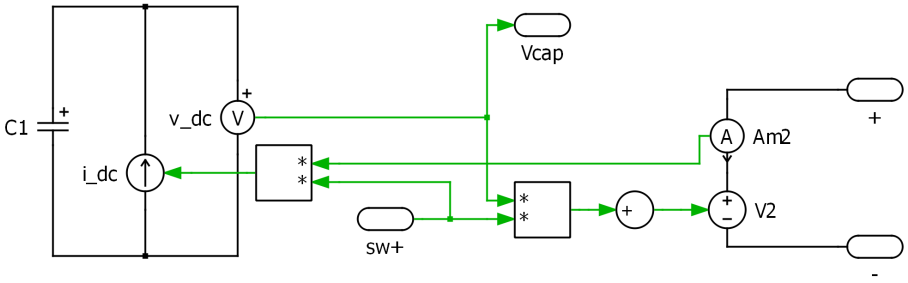

Figure A.5: Simplified arm converter PLECS circuit [35].

For chapters 3 and 4 the MMC consists on only one phase, while in the rest of the chapters, the simulation model has been extended to three phases. The MMC has 6 arm converters as is shown in Fig.A.6. The MMC is connected to the DC link in one terminal, and the output terminals are connected to AC 3 phase source acting as a grid.

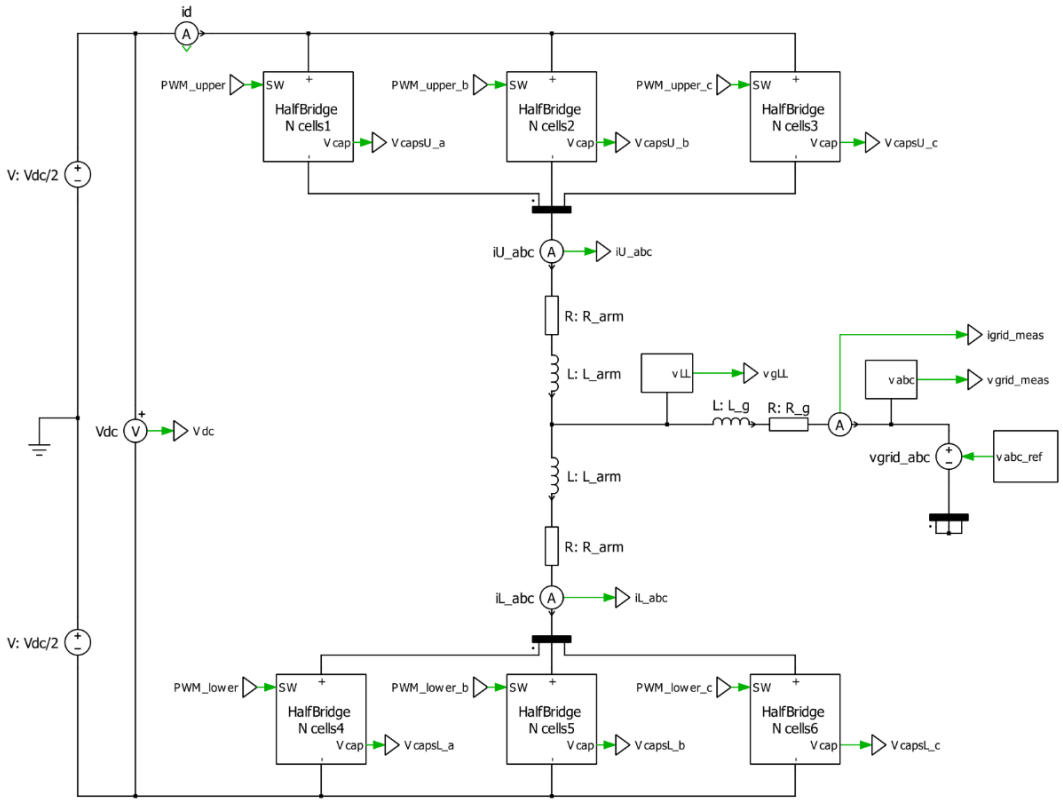

Figure A.6: MMC Plecs circuit.

A.3 Controllers

In this Section the different controllers that has been implemented in the simulation model are shown.

A.3.1 Circulating current

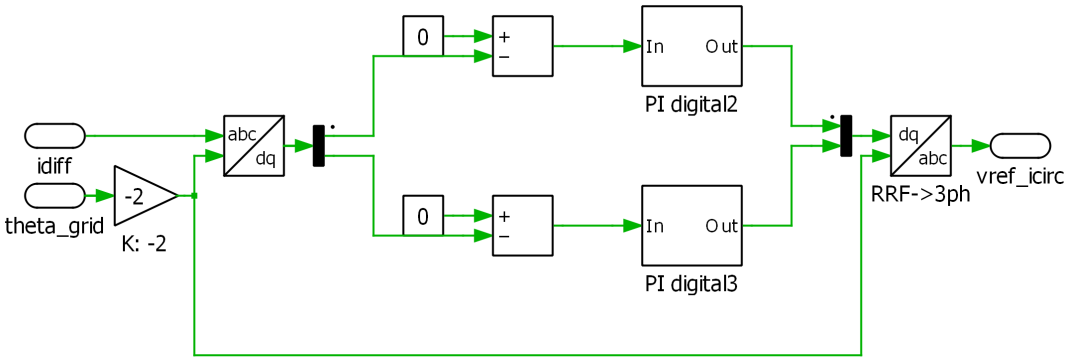

Figure A.7: Circulating current control PLECS circuit.

A.3.2 PQ control

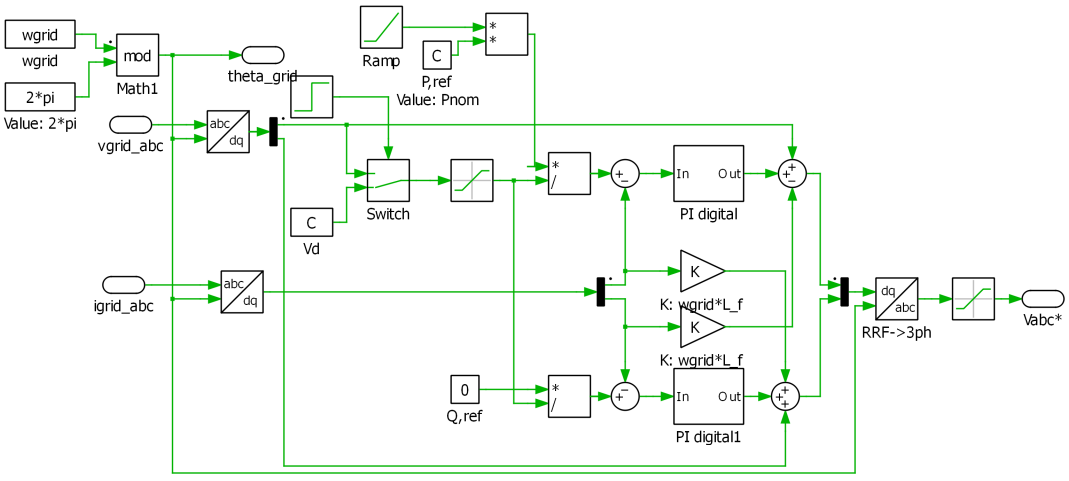

Figure A.8: PQ control PLECS circuit.

A.3.3 Balancing control

As is shown in Fig. A.9, the arm capacitor voltage errors are calculated for all the capacitors in the converter then are multiplied by a constant K and by the sign of the arm current. Additionally a enable signal was added in order activate or deactivate the control.

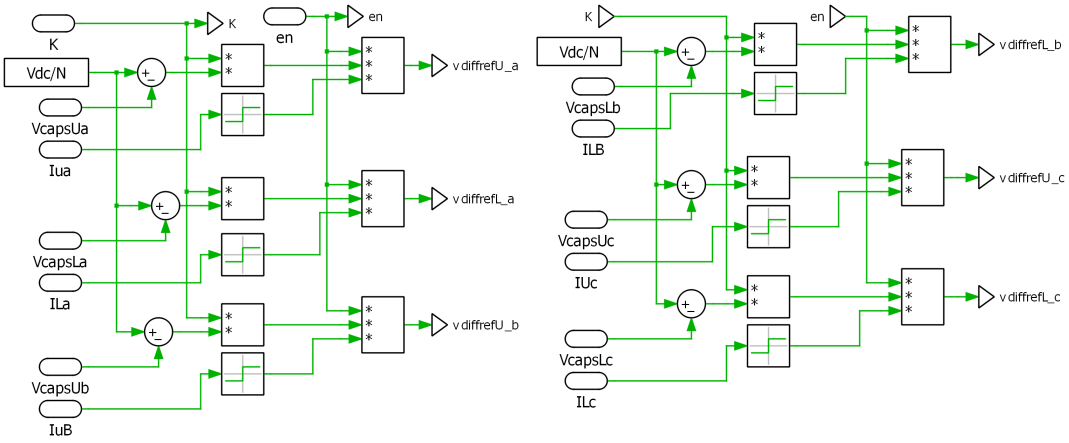

Figure A.9: Balancing control PLECS circuit.

A.4 Modulators

A.4.1 PSPWM

The PSPWM block diagram for three phases is shown in Fig. A.10. By means of the $vdiffref$ signal can be connected to the balancing control

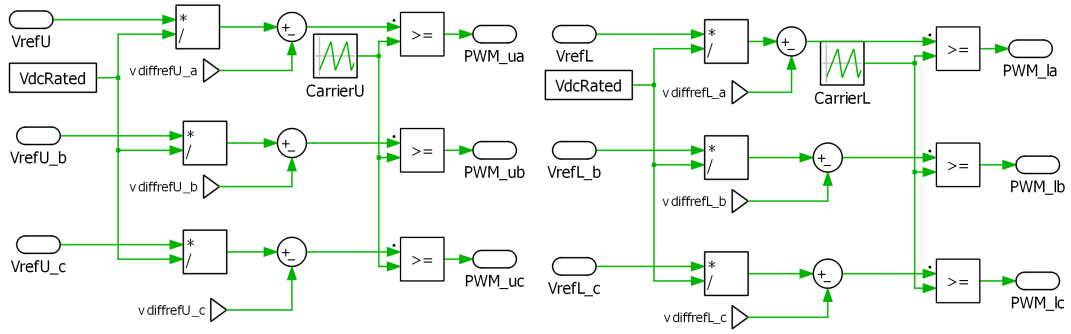

Figure A.10: PSPWM circuit

A.4.2 NLC

In Fig. A.11 is depicted the block diagram of the NLC techniques for one arm. There are two C-scripts blocks, one for each arm converter. These C-scripts are are able to work for any number of cells per arm without any extra configuration.

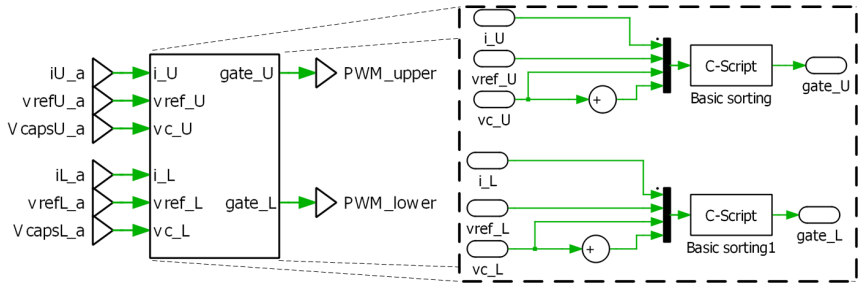

Figure A.11: One phase Sorting and Select block diagram.

Appendix B

Cell testing procedure

The voltage measurement of the SM has to be tested in order to check its performance and its linearity over the whole range of voltages. The SM measures the voltage in three different stages: first the voltage is scaled down by using a voltage divider. This voltage is feed into an operational amplifier acting as a voltage follower. And the output of the operational amplified is feed into a Voltage Controlled Oscillator (VCO). The measurements are shown in Fig. B.1 where can be noticed that there is a linear relation between the cell voltage and the measured parameters. Additionally to these measurements the over voltage test is performed.

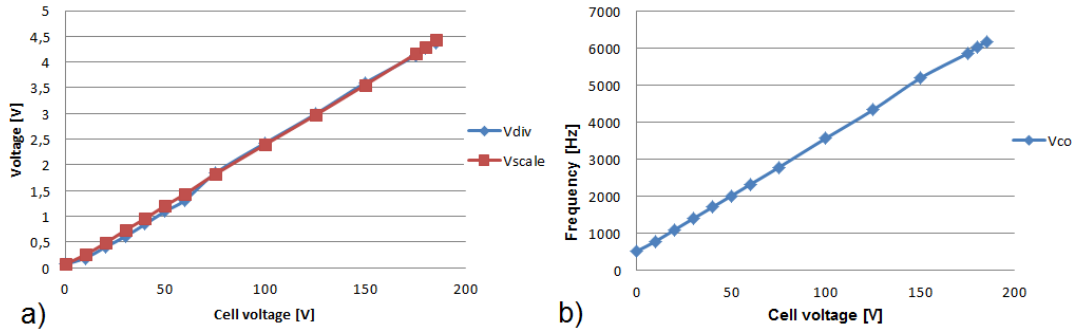

Figure B.1: a) Voltage divider and Op.Amp output as function of the cell voltage. b) VCO output frequency as function of the cell voltage.

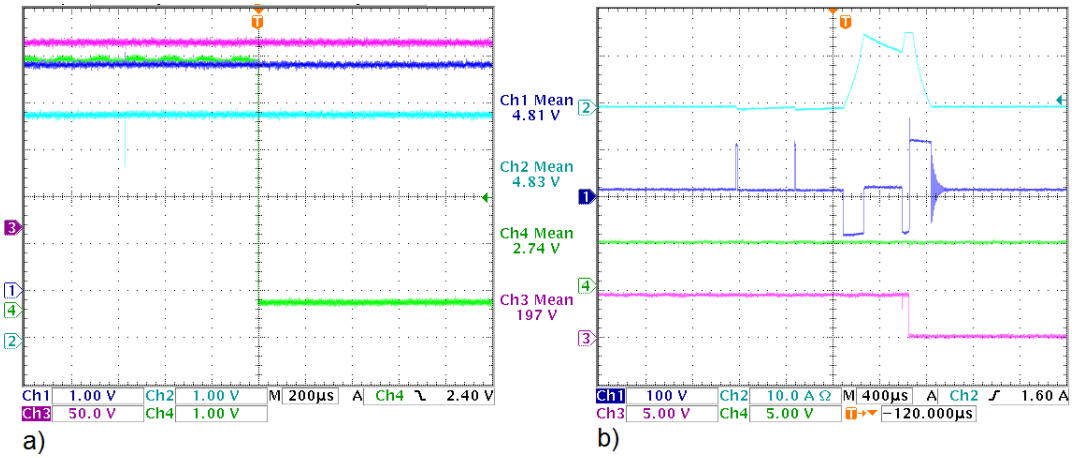

Figure B.2: a) Cell overvoltage test. Trigger=197 V. b) Cell overcurrent test Tigger=25 A.

In Fig. B.2b) the overcurrent test is shown in order the test the protection which is triggered when the current is higher than 25 A. Once the voltage measurement is checked, we can start a normal switching in the SM connected to a passive load as shown in Fig. B.3.

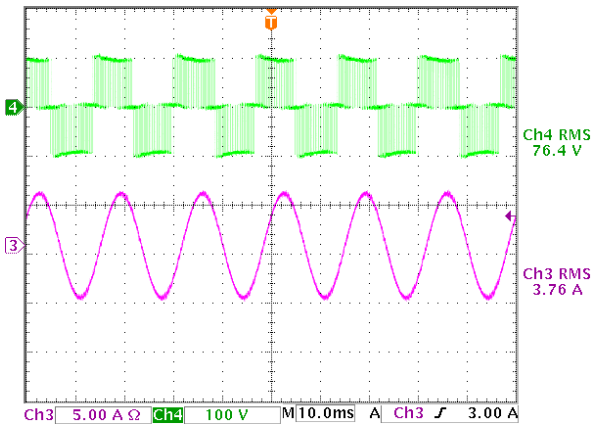

Figure B.3: Cell switching test. With load, $f_s w = 1kHz$.

Appendix C

Programming Code

C.1 NLC PLECS C-code

Listing C.1: Plecs C-Script: Code declarations.

```
#include <float.h>
#include <stdio.h>
#include <stdlib.h>

#define current Input(0)
#define Vref Input(1)
#define Vdcmeas Input(N+2)

#define NEVER DBL_MAX
#define N ParamRealData(0,0)
#define Vdc ParamRealData(1,0)
#define fs ParamRealData(2,0)
#define pwm_en ParamRealData(3,0)
#define limit ParamRealData(4,0)
#define State DiscState(0)

typedef struct
{
  float volt;
  char state;
  char position;
}inputdata;

char *outputpointer;
static float outemp=0, Ts, T1, T2, duty, vsubglobal, vlimu,
   vliml, vsubnom;
```

```
static int Next_state, n2insert, index_pwm, nprevious=0,
   previous_curr, act_curr;
inputdata *inputpointer, *datatempp;

void mergesort(inputdata *a, int low, int mid, int high)//
   order array
{
    //inputdata datatemp[N+1];
    int i = low, j = mid + 1, k = 0;

    while (i <= mid && j <= high) {
        if (a[i].volt <= a[j].volt)
            datatempp[k++] = a[i++];
        else
            datatempp[k++] = a[j++];
    }
    while (i <= mid)
        datatempp[k++] = a[i++];

    while (j <= high)
        datatempp[k++] = a[j++];

    k--;
    while (k >= 0) {
        a[low + k] = datatempp[k];
        k--;
    }
}
void dividesort (inputdata *datafun, int low, int high)//
   divide array
{
  int med;
  if(low<high)
  {
        med=(low+high)/2;
        dividesort(datafun,low, med);
        //printf("checkpoint 1\n");
        dividesort(datafun, med+1, high);
        //printf("chheckpoint 2\n");
        mergesort(datafun, low, med, high);
   }
   else
   {
```

```
    }
}

void balancing (inputdata *datafun, char *outputdata, float
    nsm, float curr)
{
  int i;
  //printf("Balancing Vref=%.02F Vnom-SM=%.02f n2insert=%d \n
      ",vref, vsub, n2insert);
  if (curr >= 0)//charging
  {//take the smallest SMs that can make the desired ref
    for (i=0; i<(n2insert); i++)
    {
      datafun[i].state = 2;
      outputdata[(datafun[i].position)-1]= 1;
    }
    for (i=n2insert; i< nsm; i++)
    {
      datafun[i].state = 1;
      outputdata[(datafun[i].position)-1]= 0;
    }
  }
  else //discharging
  {//take the biggest SMs that can make the desired ref
    for (i=0; i<(nsm-n2insert); i++)
    {
      datafun[i].state = 1;
      outputdata[(datafun[i].position)-1]= 0;
    }
    for (i=(nsm-n2insert); i< nsm; i++)
    {
      datafun[i].state = 2;
      outputdata[(datafun[i].position)-1]= 1;
    }
  }
  nprevious = n2insert;
}
void pwm (float vref, float curr, int Nsm)//generate the pwm
    with one SM
{
  //printf("inside pwm\n");
  if (n2insert == Nsm)//all inserted
  {
```

```
    Next_state =0;
    return;
  }
  else if (vref <=0)//not possible
  {
    Next_state =0;
    return;
  }
  //duty = (((int)vref % (int)(vdc/Nsm))/(vdc/Nsm));//duty
     cycle between 0 and 1
  duty = (((int)vref % (int)(vsubglobal))/(vsubglobal));//
     duty cycle between 0 and 1
  //printf("vref=%0.2f, vdc=%.2f, duty=%f\n", vref, vdc, duty
     );
  if (duty <= 0)//safety
  {
    Next_state=0;
    return;
  }
  T1= ((1-duty)*Ts)/2;//time when the SM is off
  T2= duty*Ts;//time when the SM is on
  if (curr >= 0)//look for the choosen SM
    index_pwm = n2insert;
  else
    index_pwm= (Nsm-n2insert)-1;
  //printf("Extra index_pwm=%d\n", index_pwm);
  Next_state=1;
}
```

Listing C.2: Plecs C-Script: Start function code.

```
printf("Start function\n");
int i;
Ts= 1/fs;
NextSampleHit = CurrentTime + Ts;
vsubglobal = Vdc/N;//nominal voltage per SM
vlimu = vsubglobal*(1 + limit);
vliml = vsubglobal*(1 - limit);
printf(" Limits are %f %f \n", vlimu ,vliml);
State=0;
inputpointer = (inputdata *) malloc(sizeof(inputdata)*N);
outputpointer = (char *) malloc(sizeof(char)*N);
datatempp = (inputdata *) malloc(sizeof(inputdata)*(N+1));
```

```
if (current >= 0)
  previous_curr = 1;
else
  previous_curr = 0;

for(i=0; i<N; i++)
{
    inputpointer[i].volt= Input(i+2);
    inputpointer[i].position = (i+1);
    if (Output(i) > 0)
      inputpointer[i].state=2;
    else if (Output(i) <= 0)
      inputpointer[i].state=1;
    else
      printf("Never here\n");
}

for (i=0; i< N; i++)//initializations
{
  Output(i)= 1;//upper
}
```

Listing C.3: Plecs C-Script: Output function code.

```
int i, j=0, stop=0;;
//printf("Update: %f\n", CurrentTime);
switch((char) State)
{
case 0:
/*for(i=0; i<N; i++)
{
  inputpointer[i].volt= Input(i+2);
  inputpointer[i].position = (i+1);
  if (Output(i) > 0)
    inputpointer[i].state=2;
  else if (Output(i) <= 0)
    inputpointer[i].state=1;
  else
    printf("Never here\n");
}*/
if (current >= 0)
  act_curr=1;
else
  act_curr=0;
```

```
/*printf("Inputs before shorting\n");
for(i=0; i<N; i++)
  printf("position = %d volt= %f state=%d \n",inputarray[i].
     position, inputarray[i].volt, inputarray[i].state);*/
//vsubglobal = Vdcmeas /N;
n2insert = ((Vref + (vsubglobal/2)) / vsubglobal);  //
   rounding
//printf("currenttime = %f I=%d ", CurrentTime, act_curr);
if (n2insert >= N)
{
  //printf("N2insert >= N. No sorting.\n");
  n2insert = N;
  balancing(inputpointer, outputpointer, N, current);
  for (i=0; i<(N); i++)//update outputs
    Output(i)=outputpointer[i];
}
else if ((n2insert == 0) && (pwm_en ==0))
{
  //printf("Nothing to insert.\n");
  for(i=0; i<N; i++)
  {
    inputpointer[i].volt= Input(i+2);
    inputpointer[i].position = (i+1);
    if (Output(i) > 0)
      inputpointer[i].state=2;
    else if (Output(i) <= 0)
      inputpointer[i].state=1;
    else
      printf("Never here\n");
  }
  dividesort(inputpointer, 0, N-1);//Sort the array
  balancing(inputpointer, outputpointer, N, current);
  for (i=0; i<(N); i++)//update outputs
    Output(i)=outputpointer[i];
}
else
{
  //printf("check1 nprevios= %d and n2insert= %d \n",
     nprevious, n2insert);
  if (act_curr == previous_curr)
  {
    if (nprevious == n2insert)
    {
```

```
j=0;
for (i=0; i<N; i++)
{
  if (inputpointer[i].state == 2)
  {
    inputpointer[i].volt = Input(inputpointer[i].
       position+2-1);
    //printf("Cap %d volt=%f \n",inputpointer[i].
       position, inputpointer[i].volt);
    if(!((inputpointer[i].volt > vliml) && (
       inputpointer[i].volt < vlimu)))
    {
      //printf("Cap %d volt=%f overlimits ",
         inputpointer[i].position, inputpointer[i].volt
         );
      break;
    }
    else
      j=j+1;
  }
}
if (j >= n2insert)
{
//printf("N= N(t-1)=%d, caps within limits\n", n2insert
   );
}
else
{
  //printf("N= N(t-1) overlimits j=%d n2insert=%d \n",
     j, n2insert);
  for(i=0; i<N; i++)
  {
    inputpointer[i].volt= Input(i+2);
    inputpointer[i].position = (i+1);
    if (Output(i) > 0)
      inputpointer[i].state=2;
    else if (Output(i) <= 0)
      inputpointer[i].state=1;
    else
      printf("Never here\n");
  }
  dividesort(inputpointer, 0, N-1);//Sort the array
  balancing(inputpointer, outputpointer, N, current);
```

```
      for (i=0; i<(N); i++)//update outputs
        Output(i)=outputpointer[i];
    }
  }
  else//N!= N(t-1)
  {
    j=0;
    stop=0;
    for (i=0; i<N; i++)
    {
      if (inputpointer[i].state == 2)
      {
        inputpointer[i].volt = Input(inputpointer[i].
            position+2-1);
        if(!((inputpointer[i].volt > vliml) && (
            inputpointer[i].volt < vlimu)))
        {
          //printf("Cap %d volt=%f overlimits ",(i+1),
              inputpointer[i].volt);
          stop=1;
          break;
        }
        else
          j=j+1;
      }
    }
    if (stop == 0)//(j >= n2insert)
    {
      //printf("n=%d Caps within limits no sort, prev.List\
          n", n2insert);
      //Nothing?
      balancing(inputpointer, outputpointer, N, current);
      for (i=0; i<(N); i++)//update outputs
        Output(i)=outputpointer[i];
    }
    else
    {
      //printf("usual nlc sort j=%d n2insert=%d \n", j,
          n2insert);
      for(i=0; i<N; i++)
      {
        inputpointer[i].volt= Input(i+2);
        inputpointer[i].position = (i+1);
```

```
          if (Output(i) > 0)
            inputpointer[i].state=2;
          else if (Output(i) <= 0)
            inputpointer[i].state=1;
          else
            printf("Never here\n");
        }
        dividesort(inputpointer, 0, N-1);//Sort the array
        balancing(inputpointer, outputpointer, N, current);
        for (i=0; i<(N); i++)//update outputs
          Output(i)=outputpointer[i];
      }
    }
  }
  else
  {
    //printf("ZC current: Sort\n");
    for(i=0; i<N; i++)
    {
      inputpointer[i].volt= Input(i+2);
      inputpointer[i].position = (i+1);
      if (Output(i) > 0)
        inputpointer[i].state=2;
      else if (Output(i) <= 0)
        inputpointer[i].state=1;
      else
        printf("Never here\n");
    }
    dividesort(inputpointer, 0, N-1);//Sort the array
    /*for(i=0; i<N; i++)
      printf("position = %d volt= %f state=%d \n",
         inputpointer[i].position, inputpointer[i].volt,
         inputpointer[i].state);*/
    balancing(inputpointer, outputpointer, N, current);
    for (i=0; i<(N); i++)//update outputs
      Output(i)=outputpointer[i];
  }



}
previous_curr = act_curr;
```

```
//Output(4)=outemp;
if (pwm_en == 1)
  pwm(Vref, current, N);//see if we need to do pwm and where
else
  Next_state = 0;
if (Next_state == 0)
  NextSampleHit = CurrentTime + Ts;
else
  NextSampleHit = CurrentTime + T1;
break;
//------------------------------
case 1:
//sm_pwm on
//printf("case1\n");
Output((inputpointer[index_pwm].position)-1)=1;
//Output(4)=Output(4)+Input(2+(index_pwm-1));
NextSampleHit = CurrentTime + T2;
Next_state=2;
break;
//------------------------------
case 2:
//sm_pwm off
//printf("case2\n");
Output((inputpointer[index_pwm].position)-1)=0;
//Output(4)=Output(4)-Input(2+(index_pwm-1));
NextSampleHit = CurrentTime + T1;
Next_state=0;//and back to shorting and balancing
break;

}
```

Listing C.4: Plecs C-Script: Update function code.

```
State = Next_state;
```

Listing C.5: Plecs C-Script: Update function code.

```
free(inputpointer);
free(outputpointer);
free(datatempp);
```

C.2 CPLD VHDL Code: Start/Stop

Listing C.6: CPLD VHDL code: Run-Stop State Machine

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use IEEE.STD_LOGIC_ARITH.ALL;
use IEEE.numeric_std.ALL;
use IEEE.STD_LOGIC_UNSIGNED.ALL;

-- Uncomment the following library declaration if using
-- arithmetic functions with Signed or Unsigned values
--use IEEE.NUMERIC_STD.ALL;

-- Uncomment the following library declaration if
   instantiating
-- any Xilinx primitives in this code.
--library UNISIM;
--use UNISIM.VComponents.all;

entity run_stop_StateMach is
    Port ( clk : in  STD_LOGIC;
           run : in  STD_LOGIC;
    FO : in  STD_LOGIC;
    OV : in  STD_LOGIC;
    OT : in  STD_LOGIC;
           rst : out  STD_LOGIC;
           run_out : out  STD_LOGIC);
end run_stop_StateMach;

architecture Behavioral of run_stop_StateMach is
--signal counter : STD_LOGIC_VECTOR(3 DOWNTO 0):= "0000";
signal changestate: STD_LOGIC:='0';
signal state: STD_LOGIC_VECTOR(1 DOWNTO 0):= "00";
signal next_state: STD_LOGIC_VECTOR(1 DOWNTO 0):= "00";

begin

process(clk, run)
variable cnt: STD_LOGIC_VECTOR (3 DOWNTO 0);
begin
  if (run = '0')  then--we should be in state stop
    state <= "00";
    cnt:= "0000";
    changestate <='0';
  elsif (clk'event and clk = '1') then
```

```
    state <= next_state;
    if (state = "01") then
      if (cnt < "1101") then
        cnt := cnt+1;
        changestate <= '0';
      else
        cnt:= "0000";
        changestate <= '1';
      end if;
    else
      changestate <= '0';
    end if;
  end if;
  --counter <= cnt;
end process;

process(FO, OV, OT, run, state, changestate)--process
begin
  case state is
    when "00" =>--stop
      run_out<='0';
      if FO = '1' and OV = '1' and OT = '1' then
        if (run = '1') then
          next_state <= "01";
          rst<= '1';
        else
          next_state <= "00";
          rst<= '0';
        end if;
      else
        next_state <="00";
        rst<= '0';
      end if;
    when "01" =>--counting state
      rst <='0';
      if (run = '1' ) then
        if FO = '1' and OV = '1' and OT = '1' then
          if (changestate = '1') then--counter reach limit
            next_state <= "10";
            run_out <='1';
          else
            next_state <= "01";
            run_out <='0';
```

```
          end if;
        else--any fault
          next_state <= "11";
          run_out <='0';
        end if;
      else
        next_state <= "00";
        run_out <='0';
      end if;
    when "10" =>--run state
      rst <='0';
      if (run = '1') then
        if FO = '1' and OV = '1' and OT = '1' then
          next_state <= "10";
          run_out <='1';
        else--any fault
          next_state <= "11";
          run_out <='0';
        end if;
      else-- go to stop
        next_state <= "00";
        run_out <='0';
      end if;
    when "11" =>--fault state
      run_out <='0';
      rst<='0';
      if (run ='0') then
        next_state <= "00";
      else
        next_state <= "11";
      end if;
    when others =>
      next_state <= "00";
      run_out <='0';
      rst<='0';
  end case;
end process;


end Behavioral;
```

Appendix D

CD content

- Report in PDF format.
- Plecs models.