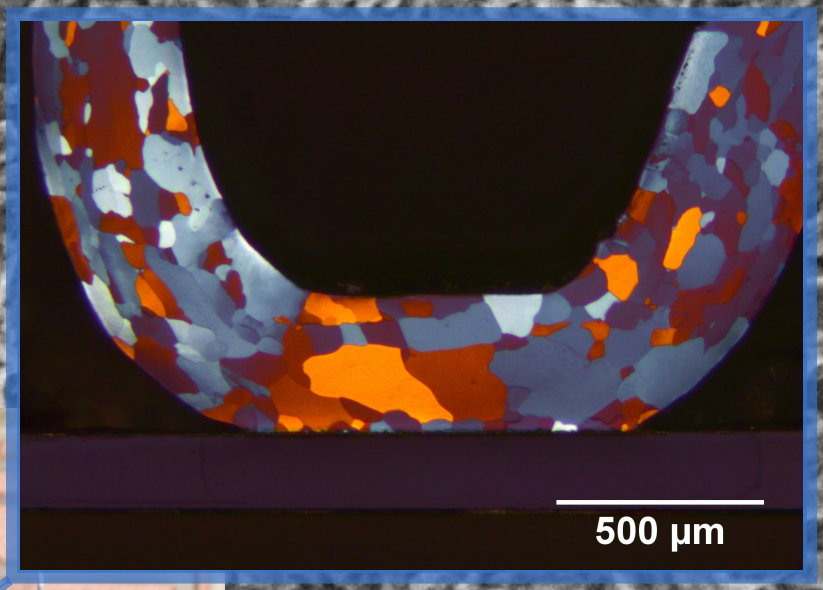
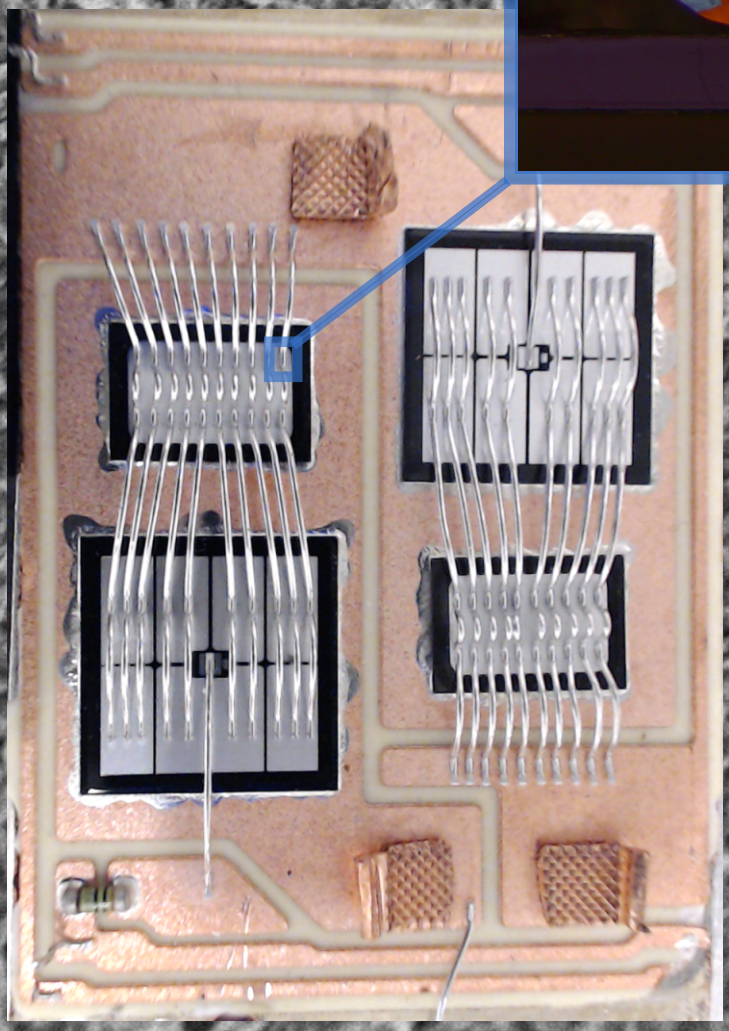
Thermomechanical Related Failures in IGBT based Power Converters

Master Project Autumn 2013 to Spring 2014





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Thermomechanical Related Failures in IGBT Based Power Converters

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Abstract

In the present work IGBT based power converters are subjected to an accelerated test. The heat transfer in the power module is simulated showing that a cyclic temperature change is present during power cycling. Stresses are thus induced at the interfaces between different materials, which causes thermomechanical related failures. Some of these failures are investigated in this project.

The topology of the metallization on the semiconductor chips are examined using scanning electron microscopy (SEM) and focused ion beam (FIB) milling. The degradation of the semiconductor chips and the wires are examined through electrical measurements with four-point probing. A study of the grains structure of the wires is carried out using micro-sectioning. These methods enables degradation mapping of the power module.

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Termomekanisk Relaterede Fejlmekanismer i IGBT Baserede Effektkonvertere

Rapport af

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Resumé

I denne rapport er IGBT baserede effektkonvertere udsat for en accelereret test. Varmetransporten i effektmodulet er simuleret og viser at der er en cyklisk temperatur ændring under operation. Dette forårsager stress i grænsefladerne mellem de forskellige materialer, hvilket resulterer i termomekanisk relaterede fejlmekanismer. Nogle af disse fejlmekanismer undersøges i dette projekt.

Topologien a metalliseringen på halvleder chipsene undersøges med skannende elektron mikroskopi og fokuseret ion stråle. Degraderingen i halvleder chipsene og wirerne studeres gennem elektriske målinger med fire-punkts probning. Kornstrukturen i wirerne er undersøgt med micro-sectioning. Disse metoder gør det muligt at kortlægge degraderingen i effektmodulet.

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Lotte Haxen Østergaard

Preface

This Master thesis was written by a master student of nanophysics and -materials at Aalborg University during the period of September 2nd 2013 - June 4th 2014.

In this work the author would like to thank Peter Kjær Kristensen for doing FIB milling, Dorthe Ankjær Rasmussen for helping with some steps in the micro-sectioning, and Kim Houtved Jensen for etching samples with Barker's reagent.

Sources are denoted by numbers in square brackets, [#]. These numbers correspond to entries in the bibliography found at the end of the paper. Page numbers are given in citations when relevant. In the bibliography, sources are listed by author and title. Publisher, ISBN, journal, and year are given where applicable.

If sources are cited prior to a period, they relate to that particular sentence. If cited after the period, they relate to the preceding paragraph or subsection unless otherwise noted. Equations, tables and figures are numbered separately. Thus the same chapter may contain both a Figure 4.1 and a Table 4.1.

List of Abbreviations

CB:	Conduction Band
CTE:	Coefficients of Thermal Expansion
DCV:	Differential Control Volume
DCB:	Direct Cu Bonded
DUT:	Device Under Test
FIB:	Focused Ion Beam
IGBT:	Insulated Gate Bipolar Transistor
IV:	Current-Voltage
HS:	High Side
LS:	Low Side
MOS:	Metal Oxide Semiconductor
MOSFET:	Metal Oxide Semiconductor Field Effect Transistor
SEM:	Scanning Electron Microscopy
VB:	Valence Band

Contents

Introduction 1

Power electronics is used to control the conversion of electrical energy and today numerous devices are running on electrical power. Due to the global awareness of climate changes there is great attention on energy efficiency. Hence, it is of interest to develop more efficient power electronics to save vast amounts of energy. Power converters are used in a wide power range depending on the application. In the low power regime (1W to 1kW) switched mode power supplies are used for battery charging, portable communication, personal computers, power tools, etc. In the high power regime (10W to 100MW) drive systems are used which control the motion of electrical machines. These are used in propulsion systems, power generation (wind turbines), heating ventilation, air conditioning systems, water pumps, etc. Power converters are a key enabling technology to make the electrical energy supply more robust and flexible. They are a step towards the realization of sustainable energy. [1, p. 1-14]

The structure of a power module is complex and the power module investigated in this project consist of several materials in a layered structure. Power cycling the power module with an AC load results in a cyclic temperature change in the module. There is a mismatch in the coefficients of thermal expansion (CTE) between the materials of the module. Thus, cyclic temperature changes will induce stress and strain in the many interfaces in the structure. This will lead to failures, which can generally be classified into two types; those caused by overstress and those caused by wearout. Failures from overstress arise from a single load, whereas wearout failures is a result of cumulative damage related to the load. Failures can also arise from other stressors which could be vibration, contamination/dust, and humidity. However, temperature changes is the major problem today as there is a trend towards high-power-density power electronics. The ability to withstand these stresses is an important factor in power electronic reliability. "Reliability is the probability of an item to perform a required function under given conditions for a given time interval"[2]. So the reliability of a power module is dependent on its application. The objective today is to find and analyse the creation of failures in order to make designs that prevent these failures. The task is however never ending as preventing one failure will only increase the lifetime of a power module until the next failure occurs. [3; 4]

Project Description

The aim of this project is to examine and map thermomechanical related degradation in IGBT based power modules subjected to accelerated load conditions. As many different failures

can occur in a power module the focus of the project evolves around the wire bonds. This is carried out using scanning electron microscopy (SEM), focused ion beam (FIB), four-point probing, and micro-sectioning. Furthermore, the heat transfer is simulated using COMSOL multiphysics.

The goals of the project can be summarized to:

- Model the heat transfer during accelerated testing through a section of the module
- Examine the surface and cross section of the metallization of the semiconductor chips using SEM and FIB
- Map the degradation of the module with a focus on the wire bonds using four-point probing
- Investigate the crack formation, delamination, and grain structure at the interface of the wire bonds using micro-sectioning

Power Modules 2

This chapter will present some subjects relevant for the power module investigated in this report. First, a description of the semiconductor chips will be given. Following this will be the configuration of the power module in question and how it is stresses will be discussed. Next, the power loss in the semiconductor components are described. Finally, the some important failure mechanism in power modules are outlined.

2.1 pn Junction

A pn junction is a boundary between two types of semiconductor materials which is p-doped at one side and n-doped at the other. If a p-doped and n-doped material are joined there will be a large gradient in the hole and electron concentrations between the regions. Thus, excess electrons will diffuse from the n-region to the p-region and excess holes will diffuse from the p-region to the n-region. The diffusing charge carriers will recombine with carriers of an opposite charge. Charged donor and accepter atoms will then be present at the interface as illustrated in Fig. 2.1. Due to the potential difference of these charges they will induce an electric field ($\mathcal{E}$). $\mathcal{E}$ will force excess electrons and holes to move from the interface and into the n-region and p-region, respectively. Hence, the $\mathcal{E}$ acts oppositely to the diffusion which induces an equilibrium with a region across the interface which is depleted of excess charge carriers. This region is called the depletion layer. The potential difference at the interface results in a build-in potential barrier (V_{bi}). When the junction is in thermal equilibrium the Fermi level is constant throughout the junction. Thus, in an energy diagram the valence- and conduction bands (VB and CB) are bend through the depletion layer since the relative position of the CB and VB with respect to the Fermi level changes between the p- and n-regions as illustrated in Fig. 2.2(a). [5, p. 242-244]

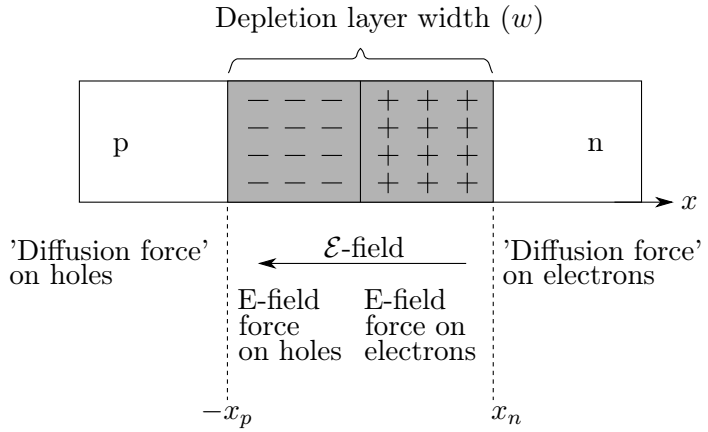
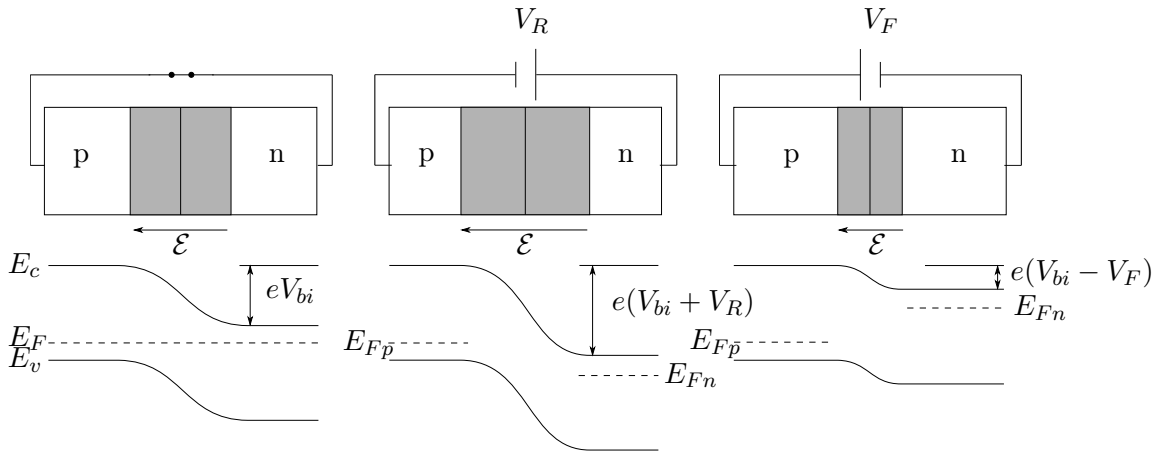


Figure 2.1. A pn junction in thermal equilibrium. From [5]

With an applied bias between the p- and n-region the pn junction will no longer be in equilibrium. When a positive bias is applied to the n-region the bias is reverse applied. The reverse applied bias (V_R) induces an electric field in the same direction as the original field as illustrated in Fig. 2.2(b). Hereby the Fermi level in the n-region is lowered compared to that of the p-region and the difference is equal to the applied voltage. The total barrier is thus increased by a factor of V_R, so the total barrier is $V_{tot} = V_{bi} + V_R$. This will increase the width of the depletion layer and the current is blocked. [5, p. 251-252]



(a) Thermal equilibrium. (b) Reverse applied bias. (c) Forward applied bias.

Figure 2.2. A pn junction and matching energy diagrams with different applied bias. $\mathcal{E}$ illustrates the relative size and direction of the electric field and E_F, E_c, and E_v is the energy of the Fermi level, CB, and VB, respectively. Inspired by [5]

If a positive bias is applied to the p-region the potential barrier will be reduced to $V_{tot} = V_{bi} - V_F$ and $\mathcal{E}$ will be reduced together with the width of the depletion layer as illustrated in Fig. 2.2(c). Excess charge carriers can thus diffuse across the depletion layer and hence, a current is running. Thus the conduction and blocking of a pn junction can be controlled with the applied bias and the current-voltage (IV) characteristics is shown in Fig. 2.3. However, if V_R is too large the diode will break down and conduct in reverse. The V_R

needed for this is called the breakdown voltage, V_{Br}. [5, p. 278]

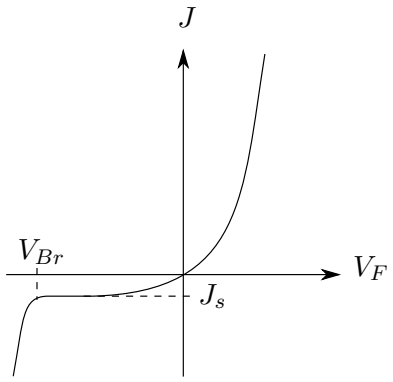


Figure 2.3. *J-V_F* dependence of an ideal diode. From [5]

2.1.1 Ideal Current in a pn Junction

Two currents are flowing in a pn junction, one is due to the concentration gradient and the other is due to the electric field. These are called diffusion and drift current, respectively.

Applying an electric field to a semiconductor will produce a force on the electron and holes causing them to move. This movement of charge is called drift and gives rise to a drift current. If charges are moving at an average drift velocity, v_d, the drift current density for holes and electrons will be

$$J_{p,drift} = epv_{dp} \quad \text{and} \quad J_{n,drift} = -env_{dn}, \tag{2.1}$$

where e is the elementary charge, p and n are the hole and electron concentrations. v_{dp} and v_{dn} are the hole and electron average drift velocities, respectively, which are given by

$$v_{dp} = \mu_p \mathcal{E} \quad \text{and} \quad v_{dn} = \mu_n \mathcal{E}, \tag{2.2}$$

where μ_p and μ_n are the hole and electron mobility, respectively. Both drifting electrons and holes contributes to the drift current density and thus the total drift current density is the sum of the two which is found by combining Eq. 2.1 and 2.2, giving

$$J_{drift} = e(\mu_n n + \mu_p p)\mathcal{E}. \tag{2.3}$$

Similarly, the diffusion current can be found from the flux of holes and electrons, which are given by

$$q''_p = D_p \frac{dp}{dx} \quad \text{and} \quad q''_n = -D_n \frac{dn}{dx}, \tag{2.4}$$

where D_p and D_n are the hole and electron diffusion coefficients, respectively. This gives a diffusion current density of

$$J_{dif} = J_{p,dif} + J_{n,dif} = eD_p \frac{dp}{dx} + eD_n \frac{dn}{dx}. \tag{2.5}$$

The total current is the sum of the individual hole and electron currents, $J_{tot} = J_p + J_n$, which are illustrated in Fig. 2.4. It is assumed that the total current is constant throughout the

entire pn structure, that the individual electron and hole currents are continuous throughout the entire pn structure, and that the individual electron and hole currents are constant throughout the depletion layer: $J_n(x_n) = J_n(-x_p)$ and $J_p(x_n) = J_p(-x_p)$. As the electric field is zero on the edge of the depletion layer the total current density can be described through the diffusion current by

$$J_{tot} = J_{n,dif}(x_n) + J_{p,dif}(-x_p). \tag{2.6}$$

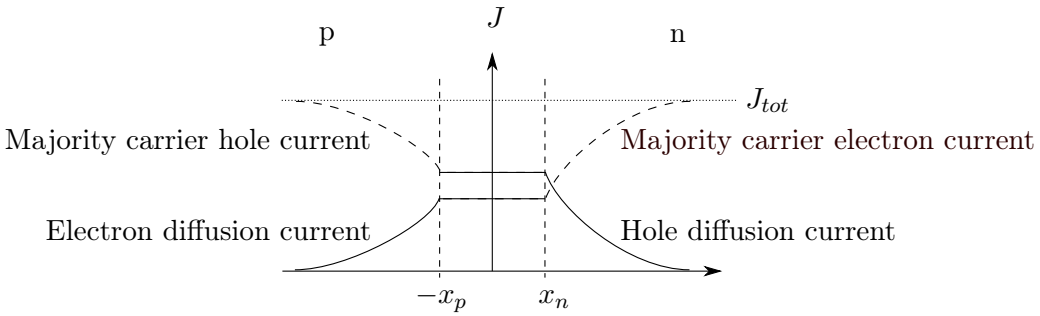


Figure 2.4. Current density through a pn junction. From [5]

As described in Eq. 2.5, the diffusion current is dependent on the concentration of excess carriers and to find this the build-in potential is needed

$$V_{bi} = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right), \tag{2.7}$$

where $V_T = kT/e$ is the thermal voltage, n_i is the intrinsic carrier concentration, and N_A and N_D are the doping concentrations of the p- and n-region, respectively. Assuming complete ionization in the depletion layer entail that

$$p_{p0} \approx N_A \quad \text{and} \quad n_{n0} \approx N_D, \tag{2.8}$$

where p_{p0} and n_{n0} is the majority carrier hole and electron concentration in thermal equilibrium, respectively. In thermal equilibrium it applies that $n_{n0}p_{p0} = n_i^2$ which entails

$$p_{n0} = \frac{n_i^2}{N_D} \quad \text{and} \quad n_{p0} = \frac{n_i^2}{N_A}, \tag{2.9}$$

where p_{n0} and n_{p0} is the minority carrier hole and electron concentrations in thermal equilibrium, respectively. Inserting Eqs. 2.8 and 2.9 into 2.7 gives the minority carrier concentrations

$$p_{n0} = p_{p0} \exp\left[\frac{-eV_{bi}}{kT}\right] \quad \text{and} \quad n_{p0} = n_{n0} \exp\left[\frac{-eV_{bi}}{kT}\right]. \tag{2.10}$$

Applying V_F gives the minority carrier concentrations outside equilibrium. As the minority carriers diffuse from the edge of the depletion layer and into the neutral semiconductor regions, recombination with majority carriers will occur. The diffusion length, L, is much shorter than the width of the depletion layer and thus the excess minority carrier

concentrations must approach zero at distances far away from the depletion layer. Hence, the minority carrier concentrations thus become

$$p_n(x) = p_{p0} \exp\left[\frac{-e(V_{bi} - V_F)}{kT}\right] \exp\left[\frac{x_n - x}{L_p}\right] \quad x \geq x_n \tag{2.11}$$

and

$$n_p(x) = n_{n0} \exp\left[\frac{-e(V_{bi} - V_F)}{kT}\right] \exp\left[\frac{x_p + x}{L_n}\right] \quad x \leq -x_p. \tag{2.12}$$

The excess carrier minority concentrations yields

$$\delta p_n = p_n - p_{n0} \quad \text{and} \quad \delta n_p = n_p - n_{p0}. \tag{2.13}$$

Incerting Eq. 2.13 into 2.5 and evaluating at $x = x_n$ and $x = -x_p$ gives a total diffusion current of

$$J_{tot} = \underbrace{\left[\frac{eD_p p_{n0}}{L_p} + \frac{eD_n n_{p0}}{L_n}\right]}_{J_s} \left[\exp\left(\frac{eV_F}{kT}\right) - 1\right], \tag{2.14}$$

where J_s is the reverse saturation current density. This equation is known as the ideal diode equation and is illustrated in Fig. 2.3. If V_R is applied and it is on the order of a few kT/eV then the current density becomes independent of the V_R and it will equal J_s until it reaches V_{Br}. [5, p. 157-158, 172-174, 279-288]

2.2 MOSFET

A metal oxide semiconductor field effect transistor (MOSFET) is a multi junction semiconductor device where an applied bias controls if the device is in a blocking or conducting state. In order to describe the operation of the MOSFET the MOS capacitor is considered first.

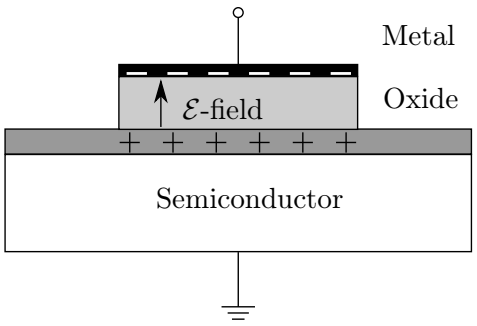
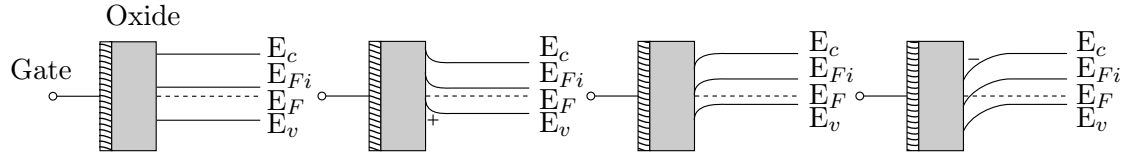


Figure 2.5. A MOS capacitor with a negative gate bias. Inspired by [5]

The MOS capacitor is similar to a parallel plate capacitor where the oxide layer separates the plates as shown in Fig. 2.5. Consider here the semiconductor material to be p-type. If the metal is at a negative bias then negative charges will exist at the metal-oxide interface inducing an electric field. If the electric field is large enough to be present in

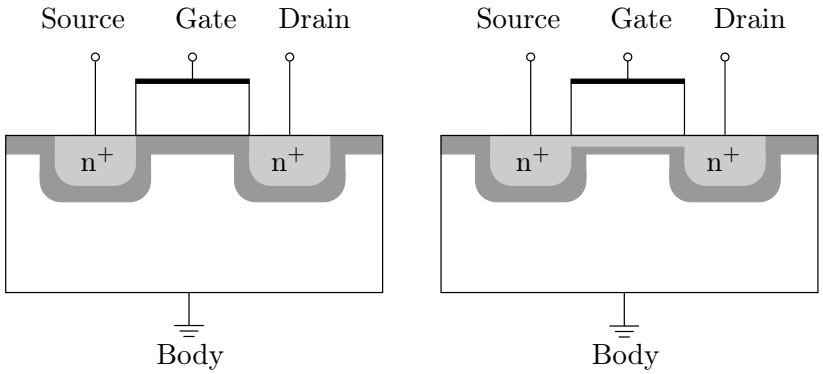
the semiconductor material the majority carrier holes experience a force towards the oxide-semiconductor interface. This creates an accumulation of holes corresponding to a positive charge on "the bottom plate" of the MOS capacitor. The energy diagram for a negative gate voltage, V_G, is illustrated in Fig. 2.6(b). If the applied bias is reversed then the induced electric field creates a negative depletion layer of fixed ionized acceptor atoms and the energy diagram will look as depicted in Fig. 2.6(c). Increasing the applied voltage will increase the induced electric field. This results in a larger depletion layer and additional band bending in the energy diagram as shown in Fig. 2.6(d). Then the intrinsic Fermi level at the surface is below the Fermi level. The CB at the interface is close to the Fermi level whereas the VB is close to the Fermi level in the bulk semiconductor. This implies that near the oxide-semiconductor interface the semiconductor has properties like an n-type semiconductor. The surface of the semiconductor is thus inverted, creating an inversion layer of electrons also called a channel. [5, p. 371-375]



(a) Zero V_G. (b) Negative V_G (accumulation). (c) Positive V_G (inversion). (d) Large positive V_G.

Figure 2.6. Energy diagrams of a MOS capacitor with p-type semiconductor with different gate voltages applied. E_{Fi} is the intrinsic Fermi level. Inspired by [5]

Now the entire MOSFET is considered in order to understand its basic operation. The current in the MOSFET is due to charge flow in the channel region near the oxide-semiconductor interface. Two types of operation exists; enhancement mode (which is discussed above), and depletion mode where a channel exists at no applied bias to the MOS, $V_G = 0$. These can be of both n- and p-type semiconductor material and are illustrated in Fig. 2.7 for a p-type MOSFET, where n^+ denotes a highly doped area.



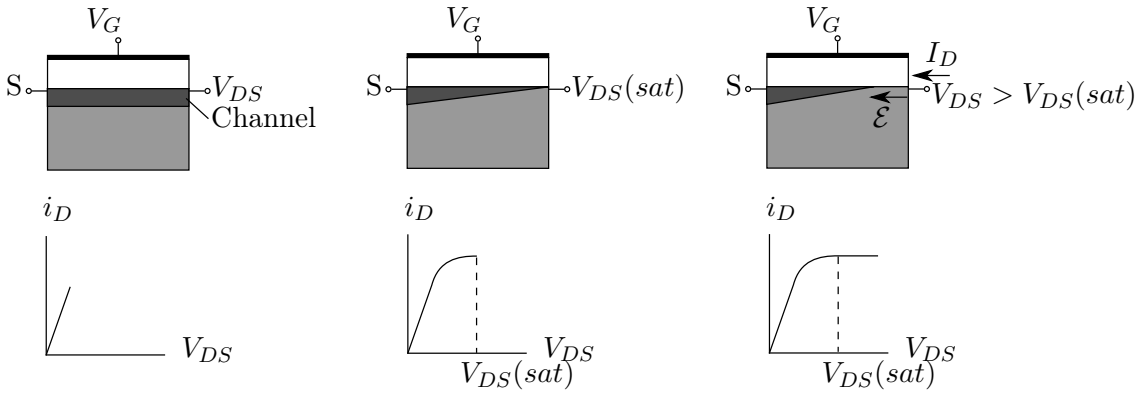
(a) Enhancement mode. (b) Depletion mode.

Figure 2.7. p-type MOSFET with an n-channel. From [5]

In the enhancement mode for a p-type semiconductor $V_G > 0$ will induce an electron inversion

layer. The inversion layer connects the n-type source to the n-type drain where the electrons will flow from the source to the drain. In the depletion mode there is a channel when $V_G = 0$. This can be because the threshold voltage, V_{th}, is negative or the region of the channel is intentionally doped. V_{th} is the V_G needed for the channel to connect the source and drain of the transistor. If the semiconductor is a n-type with a p-channel then in enhancement mode the V_G has to be negative in order to induce an inversion layer.

When $V_G < V_{th}$ the drain current (i_D) is zero. As V_G becomes larger than V_{th} the inversion charge density increases thus increasing the channel conductance (g). The basic MOS structure is shown in Fig. 2.8 for different drain-source voltages (V_{DS}) where $V_G > V_{th}$. For small values of V_{DS} the channel behaves like a resistor and thus $i_D = gV_{DS}$.



(a) Small V_{DS} (b) $V_{DS} = V_{DS}(sat)$ (c) $V_{DS} > V_{DS}(sat)$

Figure 2.8. The channels dependency on V_{DS} and the resulting i_D with $V_G > V_{th}$. From [5]

The thickness of the inversion layer illustrates the relative charge density which in Fig. 2.8(a) is essentially constant. As V_{DS} increases the voltage drop across the oxide decreases near the drain. This decreases the charge density of the inversion layer near the drain. The conductance of the channel then also decreases. When V_{DS} is increased to the point where the potential drop across the oxide at the drain is equal to V_{th} then the induced inversion charge density is zero at the drain and saturation is reached, as depicted in Fig. 2.8(b). Increasing V_{DS} even further will shorten the channel. In this case the electrons will be injected from the channel and into the depletion layer where they are swept into the drain by the electric field, as illustrated in Fig. 2.8(c). If the change in channel length is small compared to the original length then the current will be constant. For an enhancement mode n-type MOSFET the IV characteristics are illustrated in Fig. 2.9 for different V_G. [5, p. 403-410]

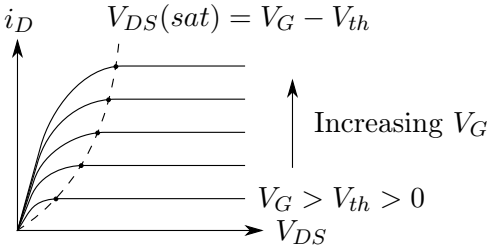


Figure 2.9. MOSFET *IV* characteristics. From [5]

2.3 IGBT

In a MOSFET only majority carriers are available to lead the current and thus it has a high internal voltage drop when conducting. Adding an extra highly doped semiconductor region to the MOSFET decrease the internal voltage drop. This structure is a so-called insulated gate bipolar transistor (IGBT), see Fig. 2.10. An IGBT can not conduct current in the reverse direction due to the changed structure and thus in a circuit a freewheeling diode needs to be placed in parallel with the IGBT.

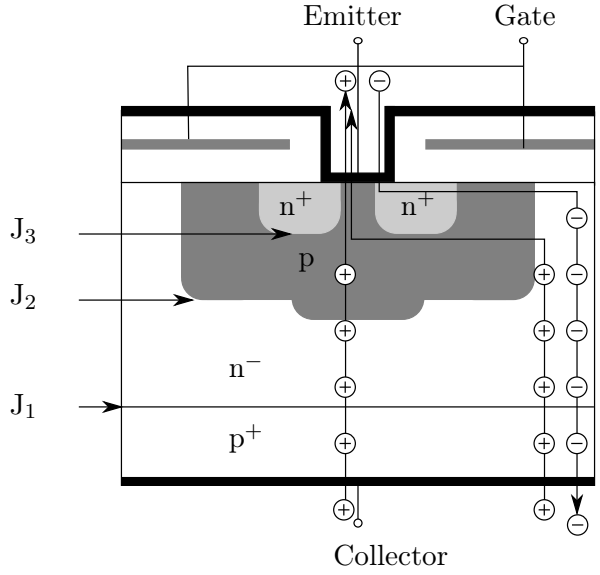


Figure 2.10. Structure and current lines of an IGBT. The signs in the doped regions denotes the doping levels. Inspired by [6]

The emitter (E) corresponds to the source and the collector (C) corresponds to the drain. If the $V_G \leq 0$V and $V_E < V_C$ the IGBT is turned off and operating in the forward blocking mode where the J_2 junction is blocking. The J_1 and J_3 junctions are on the other hand conducting as was described for pn junctions in Sec. 2.1. If $V_G > 0$ the IGBT is in forward conductive mode. First, a channel is formed beneath the oxide in the p-region by inversion, as described in Sec. 2.2. The channel enables the electrons to flow from the n^+ emitter to the n^- region which opens the J_1 junction. Holes are transported from the p^+ region to the n^- region. This exceeds the doping concentration of the n^- region by several orders of

magnitude provided that the collector current, i_C, is high enough. More electrons then flow from the n^+ emitter to the n^- region to maintain charge neutrality. The conductivity of the n^- region thus increases due to the large inflow of charge carriers which reduces the voltage drop across the IGBT making the conduction loss less than for the MOSFET. The flow of the charges are illustrated in Fig. 2.10.

If $V_G \leq 0$, then due to the high concentration of electrons in the n^- region, electrons will flow into the p^+ collector and holes flow into the p-doped region. This will result in a rapid decrease in current through the IGBT. As the electron concentration in the n^- region decreases the flow of charge carriers will eventually stop and the rest will be removed by recombination. Since the recombination is slow compared to the flow of charge carriers, it leaves behind a current tail as illustrated in Fig. 2.11.

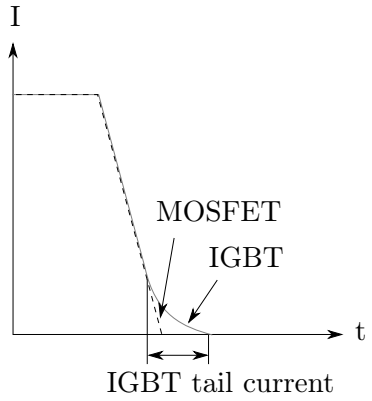


Figure 2.11. Comparison of the turn-off behaviour of MOSFETs and IGBTs. From [7]

The IV characteristics of the IGBT is similar to the MOSFET as observed in Fig. 2.12. When V_G is small the channel in the p-region is weak and the electron flow is correspondingly decreased. This decreases the conductivity across the IGBT and thus also i_C as seen in Fig. 2.12. [7, p. 39-42]

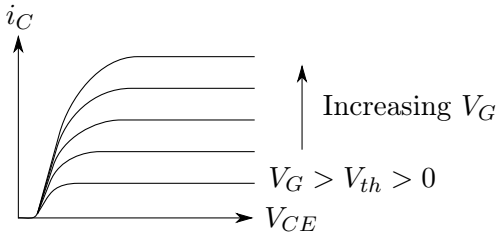


Figure 2.12. IGBT IV characteristics. From [7]

2.4 Danfoss P3 Power Module

The Danfoss P3 power module, which is the subject of study, consists of 6 sections. Each section has 2 diodes and 2 IGBT semiconductor chips which are placed on a direct Cu bonded (DCB) substrate with an Al_2O_3 ceramic. A section can be divided into two halves each with one IGBT and one diode. On a half section 10 Al wires in parallel connects the IGBT

topside, diode backside, and DCB. The 6 sections are attached to a Cu baseplate. Both semiconductor chips and DCBs are soldered onto subsequent layers using $SnAg$ (96%) solder paste. The geometry is depicted in Figs. 2.13 and 2.14 and the thicknesses of the layers can be seen in Tab. 2.1.

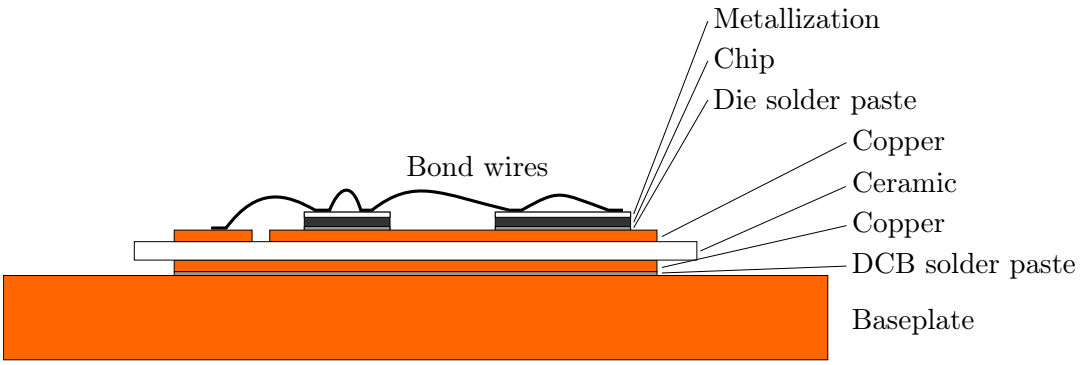


Figure 2.13. Side view of one section of a Danfoss P3 module.

Material	**Thickness [μm]**
Bond wire – Al	400
Metallization – Al	6
Chip – Diode/IGBT (Si)	200
Die attach – solder paste	100
Copper	300
Ceramic - Al_2O_3	380
Copper	300
DCB attach - solder paste	100
Baseplate – Cu	3000

Table 2.1. Thickness of the various layers in the Danfoss P3 power modules.

In order to keep track of the individual sections, chips, and wires they have been numbered according to position. Each section is given a number starting with S1 for the section closest to the module gate terminals and each section is divided into a high side (HS) and a low side (LS) as depicted in Fig. 2.14. When the module is placed in an electrical circuit, as described later in Sec. 2.5, the HS is the chip placed between the source and the load and the LS is the chip placed between the load and the ground. The wires are given a number from 1 to 10 for both the HS and LS. They are numbered starting from the edge of a section and towards the middle as depicted in Fig. 2.14.

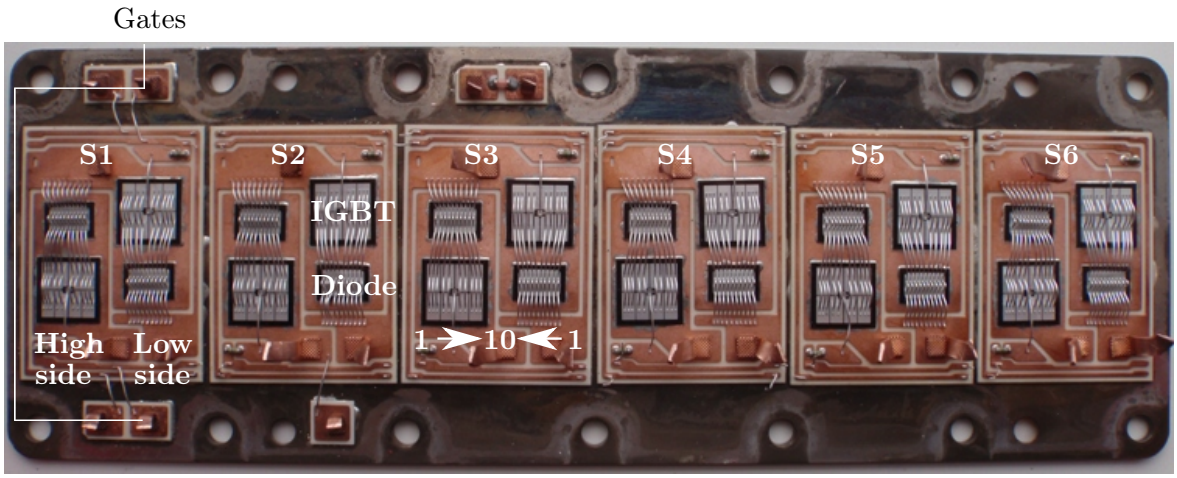


Figure 2.14. Top view of a Danfoss P3 module illustrating the naming of the sections and wires.

2.5 Accelerated Test Setup

A key part of the production of reliable power converters is robustness tests with regards to real life operation. However, it may take years to test a devices in its typical operation regime. Therefore, accelerated tests are used instead in which the device is run at a higher stress level than during normal operation. The purpose of an accelerated test setup is to investigate component robustness and identify potential mechanisms inducing failures. The conditions of the setup utilized for stressing the components in this report are close to a real wind turbine. This setup is designed and run by the Department of Energy Technology at Aalborg University, for details see [8]. There are different approaches in realization of accelerated tests. However, this subject is beyond the topic of the current report. Therefore, only the setup which was used for the P3 modules is briefly described below.

The test setup consists of an H-bridge topology as depicted in Fig. 2.15, where a DC voltage of 1000V and a sinusoidal current with a peak current of 922A is applied to the device under test (DUT). Here IGBT modules are used on each leg where one leg is used as the DUT and the other as a control side. This enables control of the power flow. On the control side the current from the DUT is shared between two legs which ensures that the DUT module wears out before the control side. In the setup large magnitudes of power is needed and the advantage of this setup is that the power is circulated, thus only losses of the system needs to be supplied.

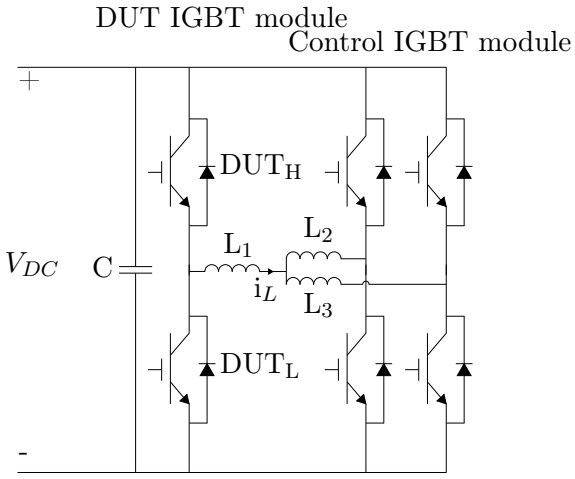


Figure 2.15. Topology of the test setup. From [8]

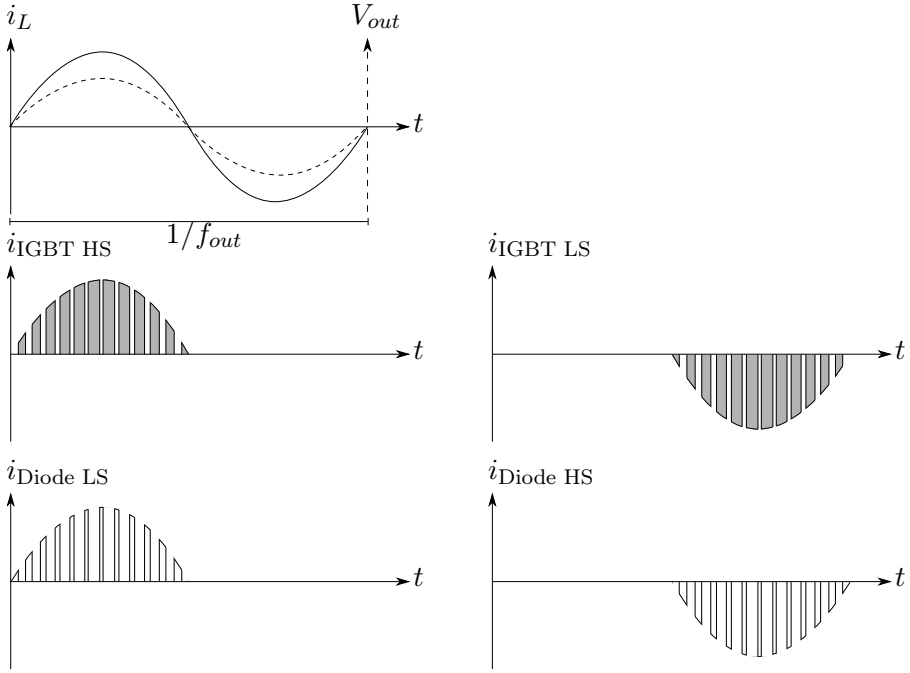


Figure 2.16. Current and voltage output together with the current in the semiconductor chips during one duty cycle. Inspired by [9]

All the sections in the power converter are connected in parallel so the module effectively has one HS and one LS, DUT_H and DUT_L respectively. The DUT_H and DUT_L will be switching at the fundamental frequency (f_{out}) of 6Hz. If the HS IGBT is turned on the current in the top loop will flow counter clockwise, through the HS IGBT. Turning off the HS IGBT will turn-on the LS diode and the current in the bottom loop will flow clockwise. The IGBT will be turned on at a switching frequency (f_{sw}) of 2.5kHz. The current output is controlled using pulse width modulation (PWM), which is illustrated along with the current in the semiconductors in one duty cycle in Fig. 2.16. The figure illustrates the aforementioned switching of the current between the semiconductor components. L_1, L_2, and L_3 are the load

inductors. On the control side the inductors L_2 and L_3 are designed to share the load evenly between the two control IGBT modules to insure that the DUT is worn out first. During the test the baseplate is kept at a temperature of 80°C ±0.5°C using Danfoss shower power. When the accelerated test is done the modules are investigated using four point probing and micro-sectioning which are both described in Chap. 4. [8; 9; 10]

2.6 Power Loss

During the accelerated test described in Sec. 2.5 there will be a power loss in the module which will turn into heat and thus stress the module. The total power loss, P_{tot}, of the semiconductor chips is the sum of the conduction, switching, and blocking loss;

$$P_{tot} = P_{cond} + P_{sw} + P_b \approx P_{cond} + P_{sw}, \tag{2.15}$$

where the P_b is normally neglected. These can be calculated for a given situation using the data-sheet of the semiconductor chip. In the following the calculation of the power loss in the diode and IGBT will be explained while considering the accelerated test.

2.6.1 Switching Process of the Diode

The diode and IGBT are connected in an H-bridge as seen in Fig. 2.15. The HS IGBT is turned on at time t_0 and turned off at time t_1. A current will flow in the load of the size

$$I_{out} = \frac{V_{DC} t_1}{L}, \tag{2.16}$$

where L is the inductance. As the IGBT is turned off at time t_1 the current I_{out} flows through the LS diode and the diode turns on. As the IGBT is turned off the voltage drop falls to a steady level of $V_{F,st}$. During the turn-on of the diode a voltage overshoot occurs. The center region of a power diode is lightly doped in order to have the required blocking capability as this region has a large resistance. When the diode is blocking a depletion layer is present and before the diode can conduct this must be removed and flooded with charge carriers to reduce the resistance. This process takes some time. Hence, as the current start flowing in the diode the voltage drop across the diode will increase to the peak value V_{FRM} at which point the depletion region is flooded with charge carriers and the voltage drop will fall to $V_{F,st}$, as illustrated in Fig. 2.17. The turn-on loss of the diodes are neglected as it is less than 1% of the turn-off loss. When the HS IGBT is turned on again at time t_4 the LS diode will turn off and the current will run through the IGBT. Before the diode can block again all the charge carriers have to be removed so the depletion layer can be established. This occurs by recombination for most charges but the rest are removed by $\mathcal{E}$, which causes a the reverse recovery current. When sufficient carriers have been removed the diode becomes reverse biased and starts to block the current, which happens at time t_6. The reverse recovery current reaches it maximum I_{RRM} at time t_7. By definition the turn-off process ends when the diode current is 20% of I_{RRM} which is at time t_8. The voltage might overshoot during turn-off as is depicted in Fig. 2.17 but that depends on the actual conditions. [6, p. 34-35] [7, p. 130-134] [11]

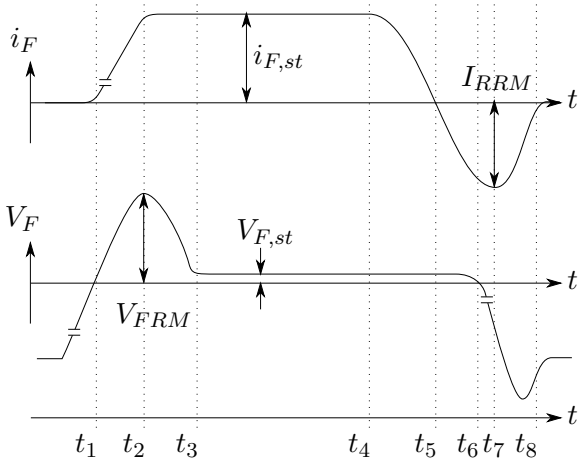


Figure 2.17. Current, i_F, and voltage drop, V_F, in a diode during switching. Inspired by [7]

2.6.2 Switching Process of the IGBT

As mentioned earlier, the load is switched between the diode and the IGBT during the accelerated test. When the IGBT is turned on at time t_2 V_G rises. At the time t_3 V_G reaches V_{th} of the IGBT and i_C starts to flow through it as illustrated in Fig. 2.18. At the time t_4 i_C have reached its nominal value but it continues to rise due to the reverse recovery behaviour of the diode. i_C will later decline and reach a steady level, $i_{C,st}$, determined by the load at time t_5. As observed in Fig. 2.18 V_{CE} have also dropped continuously until it reaches $V_{CE}(sat)$ at time t_6, which marks the end of the IGBT turn-on process. V_{CE} drops to a value equivalent to the voltage drop across the n^- region of the IGBT and as the region is flooded with charge carriers from the p^+ collector it drops to $V_{CE}(sat)$. The IGBT is turned off at time t_1 after i_C have reached the desired value, I_{out}, determined in Eq. 2.16. A voltage overshoot of V_{CE} typically on the order of δV_{CE} occurs due to parasitic inductances in the circuit. [6, p. 49-53] [7, p. 140-145]

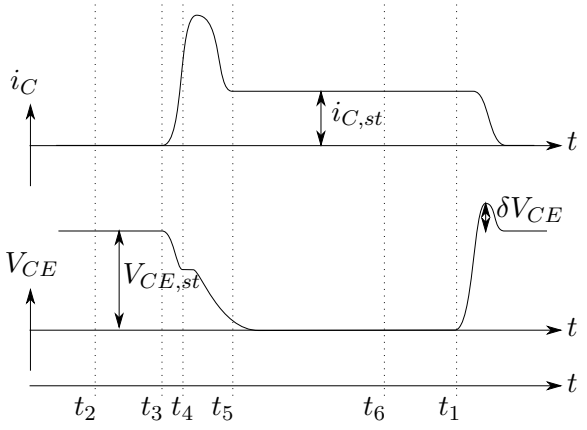


Figure 2.18. Current, i_C, and voltage drop, V_{CE}, in an IGBT during switching. Inspired by [7]

2.6.3 Power Loss in the Semiconductor Chips

The forward characteristic of the diode is illustrated in Fig. 2.19 where i_F is the forward current and r_F is the forward resistance of the diode. The average losses per period, T_{sw}, is given by

$$P_{cond,D}(t,T_j) = \frac{1}{T_{sw}} \int_0^{t'} v_F(t,T_j) i_F(t) dt, \tag{2.17}$$

where t' is the time that the diode is turned on and T_j is the junction temperature. The forward voltage of the diode can be estimated by a linear approximation to be

$$v_F(t,T_j) = V_{F0}(T_j) + r_F(T_j) i_F(t), \tag{2.18}$$

where

$$i_F(t) = \hat{i}_F \sin \omega t. \tag{2.19}$$

$\hat{i}_F$ is the amplitude of the current and ω is the angular frequency, $\omega = 2\pi/T$. Inserting Eqs. 2.18 and 2.19 into 2.17 gives

$$P_{cond,D}(t,T_j) = \frac{1}{T_{sw}} \int_0^{t'} V_{F0}(T_j) i_F(t) + r_F(T_j) i_F^2(t) dt, \tag{2.20}$$

This can be done similarly for the IGBT, where $v_{CE}(t,T_j) = V_{CE0}(T_j) + r_{CE}(T_j) i_C(t)$ and $i_C(t) = \hat{i}_C \sin \omega t$.

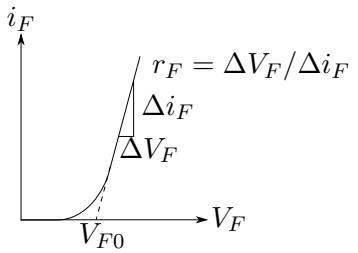


Figure 2.19. i_F and V_F relation of a diode. From [7]

The ratio between the time the IGBT is turned on and off is described with a modulation factor which is given by

$$m = \frac{\hat{V}_{out}}{V_{DC}/2}. \tag{2.21}$$

The on-state power dissipation for the diode and IGBT for a sinusoidal PWM can then be calculated according to

$$P_{cond,D}(t,T_j) = \left(\frac{1}{2\pi} + \frac{m \cos \varphi}{8} \right) V_{F0}(T_j) i_F(t) + \left(\frac{1}{8} - \frac{m \cos \varphi}{3\pi} \right) r_F(T_j) i_F(t)^2 \tag{2.22}$$

$$P_{cond,T}(t,T_j) = \left(\frac{1}{2\pi} + \frac{m \cos \varphi}{8} \right) V_{CE0}(T_j) i_C(t) + \left(\frac{1}{8} + \frac{m \cos \varphi}{3\pi} \right) r_C(T_j) i_C(t)^2, \tag{2.23}$$

where φ is the phase shift between the current and voltage (which in the accelerated test is zero, see Fig. 2.16). However, to calculate the conduction loss from Eqs. 2.22 and 2.23 requires to know the threshold voltages and the resistances at all T_j. They can be approximated by the use of the data from the data-sheet provided by the manufacturer of the semiconductor component, which is given for a T_j of 25°C:

$$V_{F0}(T_j) = V_{F0(25°C)} + TC_V(T_j - 25°C) \tag{2.24}$$

$$r_F(T_j) = r_{F(25°C)} + TC_r(T_j - 25°C), \tag{2.25}$$

where TC_V and TC_r are calculated from IV-characteristic at 25 and 125°C in the data-sheet:

$$TC_V = \frac{V_{F0(125°C)} - V_{F0(25°C)}}{125°C - 25°C} \tag{2.26}$$

$$TC_r = \frac{r_{F(125°C)} - r_{F(25°C)}}{125°C - 25°C}. \tag{2.27}$$

The total switching loss for the diode and IGBT can be calculated by

$$P_{sw,D} = f_{sw}E_{rr} \tag{2.28}$$

$$P_{sw,T} = f_{sw}(E_{on} + E_{off}), \tag{2.29}$$

where E_{rr} is the reverse recovery energy of the diode and E_{on} and E_{off} are the turn-on and turn-off energies of the IGBT. However, to calculate the switching loss from Eqs. 2.28 and 2.29 requires to know switching energies at all currents and temperatures. As this is unknown an approximation can be made using the data from the data-sheet:

$$P_{sw,D}(t, T_j) = f_{sw}E_{rr}\left(\frac{\sqrt{2}}{\pi}\frac{I_{out}(t)}{I_{ref}}\right)^{K_i}\left(\frac{V_{DC}}{V_{ref}}\right)^{K_v}(1 + TC(T_j - T_{ref})) \tag{2.30}$$

$$P_{sw,T}(t, T_j) = f_{sw}(E_{on} + E_{off})\frac{\sqrt{2}}{\pi}\frac{I_{out}(t)}{I_{ref}}\left(\frac{V_{DC}}{V_{ref}}\right)^{K_v}(1 + TC(T_j - T_{ref})), \tag{2.31}$$

where T_{ref}, I_{ref} and V_{ref} are the reference temperature, current and voltage of the switching loss measurements taken from the data-sheet. TC is the temperature coefficients of the switching loss $\sim 0.006\text{K}^{-1}$ for the diode and $\sim 0.003\text{K}^{-1}$ for the IGBT. K_i is the exponents for the current dependency of switching losses ~ 0.6 and K_v is the exponents for the voltage dependency of switching losses ~ 0.6 for the diode and ~ 1.3-1.4 for the IGBT. [6, p. 279-281, 283-285] [7, p. 127-130, 137-140]

2.7 Failure Mechanisms

The lifetime of a power module is dependent on its application profile as well as on the design, materials used, and production quality. When running the power module the power loss in the semiconductor chips causes them to heat-up. This results in a local heat-up in the module causing an inhomogeneous temperature distribution in the module, which will be discussed further in Chap. 3. This will induce stresses which can cause damage to the module. Typical elements to fail in power modules are the packaging interconnects. The failures are often caused by cracks forming in the interfaces. In the following some of the failure mechanisms of power modules are presented.

2.7.1 CTE Mismatch

The semiconductor chips and the metallization have significantly different coefficients of thermal expansion (CTE). For Al it is $24.0 \cdot 10^{-6}$/K and for Si it is $2.49 \cdot 10^{-6}$/K at 25°C. Since these two materials are interconnected their expansion due to the thermal cycling is limited at the interface. This leads to thermo-mechanical stress and strains. Induced stress primarily originate from the physical processes of thermal expansion. The situation is illustrated in Fig. 2.20 with a simple two layer model.

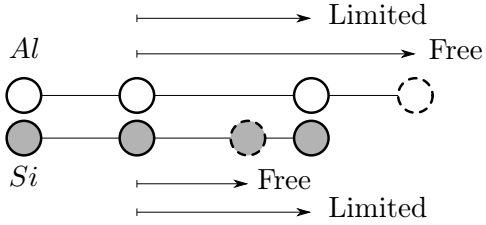


Figure 2.20. Two layer model of an Al/Si interface illustrating the free and limited expansion. From [12]

Si is a brittle material whereas Al is ductile and they have a yield stress of 5000-9000MPa and 15-20MPa, respectively. Thus, Al will experience a plastic strain at a lower induced stress compared to the Si. A deformation of Al can thus occur. As the wires are bonded to the thin metallization layer the deformation will form cracks in the wire bond. The bond wire will thus gradually lift-off which decreases the electrical and thermal conductivity. After a certain number of cycles the interface will be destroyed and the wire will lift-off. This will increase the current load on the remaining wires causing further self heating and an acceleration of the degradation process. [12; 13]

Solders

The CTE mismatch also occurs in all the other interfaces of the device. Thus, the temperature fluctuations will contribute to the degradation of these. Si chips are soldered onto the DCB and the DCB is soldered onto the baseplate. Significant amounts of heat dissipating through the module needs to flow through the structure from the chip to the baseplate. As the temperature fluctuates a strain is induced in the solder. This will eventually cause crack formation in the solders thus increasing the power loss in the solder and with it increase the temperature. This will cause the module to fail. As cracks grow from voids and impurities it is preferable to limit their presence from the production. [14; 15]

Metallization

When the Al metallization is subjected to temperature fluctuations Al will reconstruct, especially at high temperatures. This happens due to the CTE mismatch between the Al metallization and Si chip. The stiffness of Si is large compared to Al and thus, the induced stresses in the Al can exceed the elastic limit. Depending on the temperature and the stress conditions this can cause plastic deformation such as sliding of grain boundaries and dislocations. Hence, a reconstruction will occur. As the metallization reconstructs the

resistance will increase causing a degradation in the metallization. S. Pietranico et al. [16] found that the resistance increase with increasing temperature and with increasing number of cycles. Furthermore, the reconstruction appears only at the surface of the metallization, however, large cracks are propagating into the metallization towards the chip. The stresses between the Si chip and the Al metallization induced by the temperature changes might result in a bending deformation which can cause the Si and Al to crack. [2; 14; 16]

2.7.2 Al Wire Bonds

The Al wires are ultrasonically wedge bonded in the P3 modules. This process is considered to be a solid state process as it is done at room temperature and only small temperature changes occur during the bonding. The bonding begins with hardening of the wire by applying a force through the wedge. The yield and tensile strength of the wire is then reduced by ultrasonic vibrations, which is normally called ultrasonic softening. These two processes creates a deformation which enables diffusion and removes impurities. The diffusion typically occur if the Al is not pure. In the end the wire is ultrasonically hardened, which results in a polycrystalline interface. When an Al wire is bonded to an Al metallization a refinement area is present around the interface. Here the grain structure of the wire and metallization is refined depending on both the original structure and the applied power. It is observed that an increase in the ultrasonic power decreases the grains size in the wires near the interface and that the reformation area increases in the wire bulk. This reformation area has an elliptical shape. [12; 17]

While the module is running it experiences a thermal cycling which creates stress in the structure. The design of the structure is thus important and for the wires this includes the curvature of the wire and the geometrical positioning of the bonding interface. Depending on the application of the module different processes may be significant, these include diffusion, recrystallization, and material expansion. Hence the strength of the wire is limited by its microscopical structure. The elastic limit can be exceeded in some regions due to the geometry and the temperature cycles. This leads to plastic deformation which over time leads to cracks. The cracks are initiated at natural locations like voids or at the interface heel of the wire. They are expected to propagate along the boundary of the crystallized grains due to the strength of these grains. Hence the cracks are observed to initiate near the interface and propagate into the wire where the grain size increases. This can be explained by the Hall-Petch relation

$$\sigma_y = \sigma_0 + k_y d^{-1/2}, \tag{2.32}$$

where σ_y is the yield strength, σ_0 is the yield strength for dislocation along slip planes, k_y is the dislocation locking term, and d is the grain diameter. This relation says that the fracture toughness decreases with increasing grain size which increases the propagation of a crack from the interface and inwards the wire. However, normally the effective stress decreases when moving away from the interface. Thus an equilibrium will occur between the fracture toughness and the effective stress at a given distance from the interface. This limits further propagation inwards the wire and the crack should thus move parallel to the interface until the wire lifts-off. So according to the Hall-Petch relation a wire with a smaller grain size will

have a stronger bond. However, more power is also needed to bond it and there is a risk of damaging subjacent layers while applying additional force. [12; 14; 15; 17]

During the power cycling the curvature of the Al wires is important as the temperature oscillations will cause the wires to expand and contract according to the temperature. It is observed experimentally and through simulations that the wire curve will displace vertically under operation [18]. It was found that the amplitude of the displacement increases with decreasing fundamental frequency. This is expected as the displacement is directly related to the heat. The heat is mainly generated in the semiconductor chips and a lower fundamental frequency will result in a longer running time of one chip in one period, generating more heat. This displacement of the wire contributes to the wire lift-off. [14; 18]

2.7.3 Hard and Soft Degradation

The degradation of a power module can be divided into hard and soft degradation. Soft degradation comes from a gradual loss in performance which is caused by general wear. This includes the reconstruction of the metallization and void formation in the solders. Hard degradation comes from failures that deviates a lot from the nominal value causing early failure. Thus, any degradation that causes a sudden and significant change in the module are considered to be hard failures, which could be a result of delamination of the wire bonds. [3]

Heat Transfer Simulation 3

This chapter contains a description of the concept heat transfer. The heat transfer of a simplified structure in one section of the P3 module is subsequently simulated using COMSOL Multiphysics.

3.1 Heat Transfer

Heat transfer is thermal energy in transit due to a spacial temperature difference. One distinguishes between three heat transfer processes; conduction, convection, and thermal radiation. Conduction mode is when a temperature gradient is present in a stationary solid or fluid. Convection mode is when the heat transfer occurs between a surface and a moving fluid with different temperatures. Thermal radiation mode is energy radiated in the form of electromagnetic waves from a surface with a finite temperature, thus there will be a net heat transfer between two surfaces even with vacuum between them. In this section only convection and conduction will be considered. [19, p. 2-3]

3.1.1 Convection

Convection consists of two processes; energy transfer due to random molecular motion (diffusion) and macroscopic motion of liquids or gases. In this work the convection heat transfer between a fluid in motion and a surface with different temperatures is considered to understand the heat transfer due to the liquid cooling of the power module baseplate.

When a fluid is flowing on a surface there will be an interaction between these. The shear stress will cause the velocity of the fluid to decrease from a finite value u_∞ to zero as illustrated in Fig. 3.1. The surface has a temperature T_s and as the fluid has a different temperature there will be a temperature distribution throughout the fluid. The temperature in the fluid will vary from T_s at the surface to T_∞ in the outer flow. If $T_s > T_\infty$ the convection heat transfer will occur from the surface to the outer flow. At the surface, where the velocity is zero, the diffusion is the only heat transfer process.

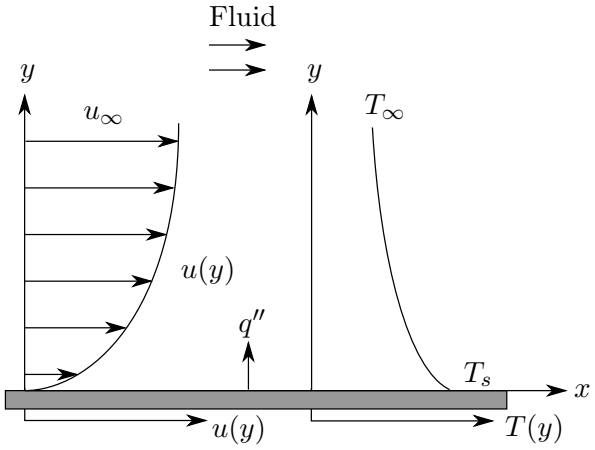


Figure 3.1. Velocity and temperature distribution in a liquid flowing on a surface due to convection, from [19].

Convection is separated into force and free according to the flow. These relate to whether the flow is caused by external forces (fan or pump) or buoyancy forces (density difference caused by temperature gradient in the fluid). An equation for heat transfer due to convection is given by

$$q'' = h(T_s - T_\infty), \tag{3.1}$$

where q'' is the heat flux and h is the convection heat transfer coefficient. The latter describes the type of convection and the problem is reduced to determining h as it is a dependent on the flow. [19, p. 6-8]

3.1.2 Conduction

Conduction is the transfer of energy from more energetic to less energetic particles of a substance due to interactions. These interactions are primarily collisions and lattice vibrations. For electrical conducting materials translational motion of the free electrons dominate. All these processes combined leads to a diffusion of energy. It is possible to quantify the heat transfer processes in terms of appropriate rate equations, which will be done below.

First Fourier's law of heat conduction will be considered for one dimension.

$$q''_x = -k_x \frac{dT(x)}{dx}, \tag{3.2}$$

where q''_x is the heat flux, $T(x)$ is the temperature, and k_x is the thermal conductivity for the given material in the x direction. The minus sign is a consequence of the fact that heat transfers in the direction of decreasing temperature. The heat flux is the heat transfer rate in the x direction per unit area perpendicular to the direction of transfer and it is proportional to the temperature gradient in that direction. Under steady state conditions, with a linear temperature distribution, the heat flux is then

$$q''_x = -k_x \frac{T_2 - T_1}{L} = k_x \frac{T_1 - T_2}{L} = k_x \frac{\Delta T}{L}, \tag{3.3}$$

where L is the length the heat is traveling. The heat rate is then

$$q_x = q''_x A_x, \tag{3.4}$$

where A_x is the area the heat is conducting through. [19, p. 3-5]

The first law of thermodynamics states that the total energy of a system is conserved. Hence, the only way that the energy of a system can change is if energy crosses the boundaries of the system or if work is canceled out by the system. For a closed system the change in the total energy stored in the system is

$$\Delta E_{st}^{tot} = Q - W, \tag{3.5}$$

where Q is the net heat transferred to the system and W is the net work done by the system. This law also applies to a control volume, a region of space bounded by a control surface through which mass may pass. If the particles that enters and leaves the control volume have different energies, this is called advection. For a differential control volume (DCV) it applies that the amount of energy stored in the DCV must equal the amount of energy that enters minus the amount that leaves the DCV.

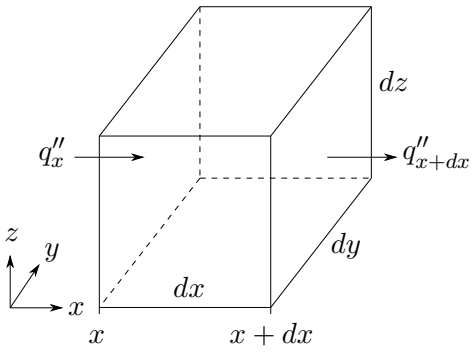


Figure 3.2. Differential control volume.

It has to be noted that the sum of thermal and mechanical energy is not conserved, as there can be a conversion between other forms of energy to thermal energy. This conversion can be seen as a thermal energy generation. A source of thermal energy could be through resistive heating. As the first law of thermodynamics must apply for all instants of time one has

$$\frac{dE_{st}}{dt} = \frac{dE_{in}}{dt} - \frac{dE_{out}}{dt} + \frac{dE_g}{dt}, \tag{3.6}$$

where E_{st} is the energy stored in the DCV, E_{in} is the energy entering the DCV, E_{out} is the energy leaving the DCV, and E_g is the thermal energy generated in the DCV. Now it is a matter of choosing the appropriate DCV and its control surface to which an analysis is applied. In order to simplify Eq. 3.6 a DCV as illustrated in Figure 3.2 is considered. Making a Taylor expansion of the heat flux gives

$$q''_{x+dx} = q''_x + \frac{\partial q''_x}{\partial x} dx, \tag{3.7}$$

which is the heat flux leaving the DCV. The energy stored in the DCV can be found from the equation for the specific heat capacity $E_{st} = mc_p\Delta T$ where m is the mass, c_p is the pressure

specific heat capacity, and ΔT is the change in temperature. The rate of change in E_{st} can those be written as

$$\frac{\partial E_{st}}{\partial t} = \rho c_p \frac{\partial T}{\partial t} V_{DCV}, \tag{3.8}$$

where ρ is the density of the material and $V_{DCV} = dxdydz$ is the volume of the DCV. The generated heat rate is given by

$$\frac{\partial E_g}{\partial t} = \frac{\partial q_n}{\partial t} V_{DCV}, \tag{3.9}$$

where n denotes the direction. Inserting Eqs. 3.7-3.9 into Eq. 3.6 and using Eq. 3.4 for the x direction yields:

$$\rho c_p \frac{\partial T}{\partial t} V_{DCV} = q''_x - q''_x - \frac{\partial q_x}{\partial x} dx A_x + \frac{\partial q_x}{\partial t} V_{DCV}, \tag{3.10}$$

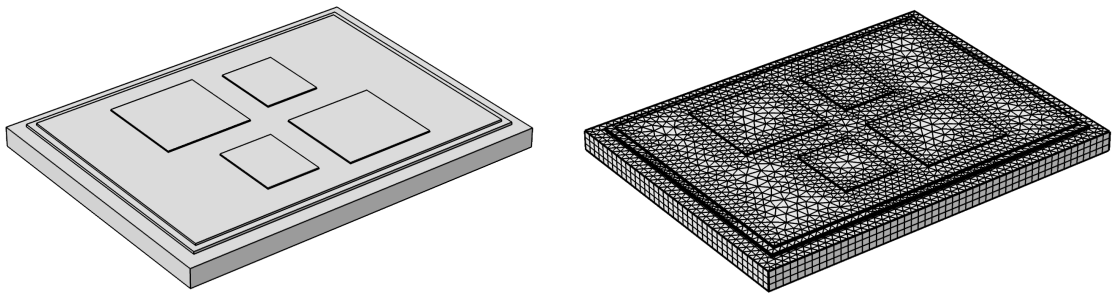
where $A_x d_x = V_{DCV}$ and those V_{DCV} cancels out. Eq. 3.10 also applies for the y and z direction which combined with Eq. 3.2 yields

$$\rho c_p \frac{\partial T(\vec{r}, t)}{\partial t} = \vec{\nabla} \cdot \left(\vec{k} \vec{\nabla} T(\vec{r}, t) \right) + \frac{\partial q(\vec{r}, t)}{\partial t}. \tag{3.11}$$

Eq. 3.11 is a partial differential equation (PDE) which with well-defined boundary conditions can be solved. [19, p. 13-16] However, the structure of the module is complex and as a result the current distribution is inhomogeneous throughout the structure. The approach utilized in this report is to use the multiphysics program COMSOL to calculate the heat transfer in a section of the module.

3.2 Temperature Field of the Module

The goal of simulating the temperature field is to obtain the distribution on the semiconductor chips. To simplify the simulation only a single section is regarded, see Fig. 3.3(a). The top Cu layer of the DCB is approximated to be one solid, the Al wires and metallizations are removed, and the semiconductor chips are approximated to be composed entirely of Si.



(a) Simplified structure (b) Fig. 3.3(a) with a mesh

Figure 3.3. Simplified structure of the Danfoss P3 module.

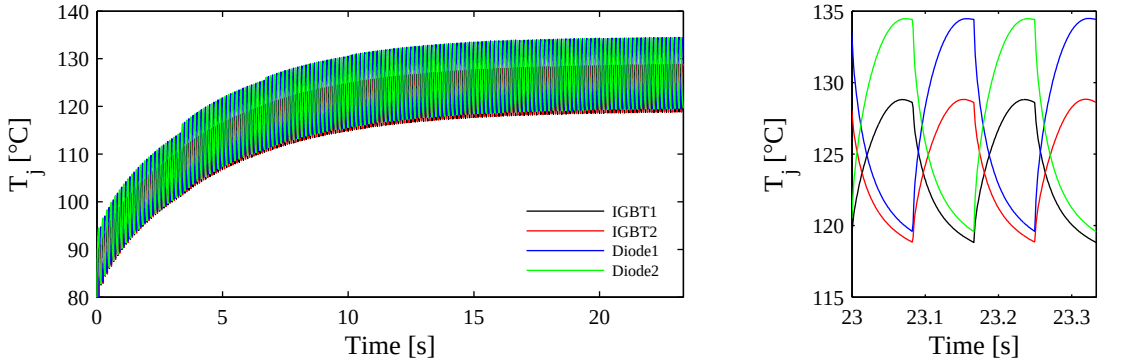
A mesh is applied to the structure, see Fig. 3.3(b), and Eq. 3.11 is solved in the nodes of this mesh. The power loss in the semiconductor chips is described by Eqs. 2.22, 2.23,

2.30, and 2.31. This results in heat generated in the semiconductor chips. The simulation is running for 140 number of cycles to insure that a steady temperature level is reached. Initially, the temperature of the structure is set to 80°C, the same as the cooling water. However, the power loss is temperature dependent, so in order to correct for this, T_j of each chip is extracted for every 20 cycles, which is then used as T_{ref} in the following 20 cycles. The boundaries of the structure are regarded as thermally isolating except for the bottom side of the baseplate which is cooled through convection. As described in Sec. 3.1.1 a suitable convection heat transfer coefficient must be found. P. Ghimire et. al [9] found that the peak junction temperature (T_{peak}) of the IGBT's during the accelerated test is 131.6°C. Thus, a suitable h should result in a T_{peak} in that range.

Initially, h is set to 4000 and the resulting T_{peak} of the IGBT's is found to be 120°C, which is well below the desired value. Setting h to 3000 results in temperatures presented in Tab. 3.1. T_{peak} of the IGBT's is in the range of the desired value and thus, it is concluded that a suitable $h = 3000$. The results in Tab 3.1 states that ΔT_j, T_m, and T_{peak} for the HS and LS diodes are equal and likewise for the IGBT's. However, it should be noted that the structure is simplified so this might not be the case if all details where included. In Tab. 3.1 and Fig. 3.4 it is observed that the diodes have a higher ΔT_j, T_m, and T_{peak} than the IGBT's during a cycle. As described in Sec. 2.7 a higher T_m and ΔT_j will increase the stress on the surrounding interconnects. Thus, the results of this heat transfer simulation indicates that the diodes will fail prior to the IGBT's.

	ΔT_j	T_m	T_{peak}
Diodes	14.9°C	127.2°C	134.4°C
IGBT's	10°C	123.9°C	128.8°C

Table 3.1. Results of the heat transfer simulation, where ΔT_j is the change in junction temperature and T_m is the mean junction temperature.



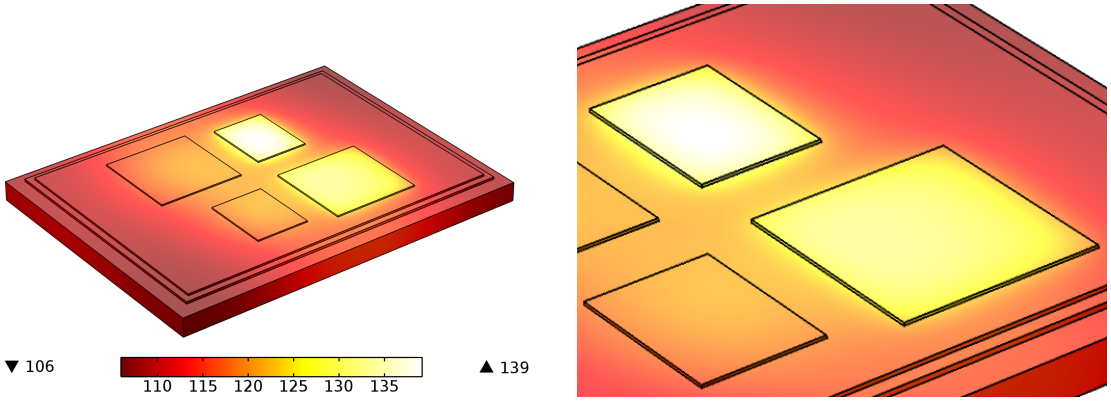
(a) T_j.

(b) The last two cycles of Fig. 3.4(a).

Figure 3.4. T_j of the four chips with $h = 3000$

The temperature distribution in the section is illustrated in Fig. 3.5. It is observed that

during the first half of the duty cycle the HS IGBT and LS diode have a higher temperature than the rest of the section, which is expected as the heat is generated in these. Likewise, the LS IGBT and HS diode has an equivalent high temperature in the second half of the duty cycle. Furthermore, in Fig. 3.5(b) it is observed that the semiconductor chips has a higher temperature at the center compared to the edge. For the diodes the difference in temperature between center and edge is 13°C and for the IGBT's it is 8°C. This temperature field results in a higher stress at the center of the chips compared to the edge. Thus, a higher degree of degradation should be present at the center.



(a) First half of the duty cycle.

(b) Magnification of Fig. 3.5

Figure 3.5. Heat distribution in a section of the module at the peak of the first half of the duty cycle given in °C.

Experimental Methods 4

This chapter describes how the Danfoss P3 modules are investigated after undergoing an accelerated test. There is an overview of the steps in the investigation and afterwards each step is described in detail.

4.1 Module Investigation

Post-failure sample investigation is the commonly used approach for analyzing failure mechanisms in power electronic components. Through this approach, however, one risk losing valuable information in the final stages of the component lifetime, e.g. through explosions or burn-out [12]. To prevent catastrophic module failure and to investigate the degradation as a function of number of cycles, modules were removed from operation prior to failling at selected lifetime stages. The modules are loaded for 0, 1.3, 2.5, 3.5, and 4.5MC (mega cycles) under the circumstances explained in Sec. 2.5. It needs to be noted that the load of the 1.3MC module stands out, as the temperature was not monitored during the accelerated test. Thus, it can not be directly compared to the other modules. The investigation is based on the following approach:

- Module disassembly - the module housing (plastic cover and silicone gel) is removed and the module is separated into sections.
- Four-point probing measurement are carried out on selected sections and chips of the modules, as presented in Tab. 4.1. Five types of measurements are carried out: section, chip wires, semiconductor chips, wire current distribution, and wire voltage drop. The different approaches are explained in detail in Sec. 4.2. The used setup is developed by K. B. Pedersen et al. [20].
- The metallization of the chips are examined using scanning electron microscopy (SEM) images and focused ion beam (FIB) milling when needed.
- The wire bonds of selected samples are investigated using micro-sectioning. This involves casting the sections into epoxy, cutting out the semiconductor chips, and polishing to the desired interface. Afterwards the samples are electro-chemically etched using Barker's reagent to make the grain structure of the Al visible. The samples are investigated in a DMI3000M top down microscope from LEICA using polarized light.

For details of the procedures see Secs. 4.2 and 4.3.

Module	Section	Chip wires	Semiconductor chip	Wire current	Wire voltage
0MC	S2, S4, S6	S2, S4, S6	S2, S4, S6	S2, S4, S6	S2, S4, S6
1.3MC	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6
2.5MC	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6	S4 + LS diode S1-S6	S4 + LS diode S1-S6
3.5MC	S1-S6	S1-S6	S1-S6	S1-S6	S1-S6
4.5MC	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6	S2, S4, S6 + LS diode S1-S6	S4 + LS diode S1-S6	S4 + LS diode S1-S6

Table 4.1. Overview of four-point probing measurements carried out.

4.2 Four-Point Probing

Four-point probing is an electrical measuring technique for measuring the voltage drop across a material or structure. Two of the probes are current carrying and the other two measures the voltage as depicted in Fig. 4.1.

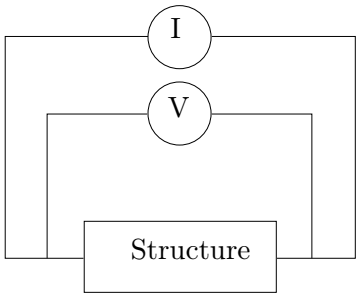


Figure 4.1. Principle of four point probing.

The advantage of using four probes is that the two voltage probes only carry an infinitesimal current. This removes unwanted signal since the resistance of the probes is eliminated along with the contact resistance. In the present setup the voltage probes are thin sharpened tungsten needles to ease the probing. A Matlab program is controlling the setup and collecting the data. Since the resistance of a material is dependent on temperature the sample is kept at a desired temperature T_0 with a deviation below a given ΔT. The temperature is controlled using two Peltier elements together with a thermocouple attached to the sample surface. If the temperature deviate more than ΔT from T_0 the current through the Peltier elements is modulated accordingly. This is known as PID (proportional-integral-derivative) control. For measurements in this project T_0 is set to 50°C and ΔT is set to 0.1°C. [20]

When measuring on a section of a power module the current carrying probes are placed at the Cu terminals which are illustrated in Fig. 4.2. These are connected to a power supply

which is controlled by the program. When measuring across the IGBTs a fifth probe is in use which opens the gate at 15 V. A DC current is applied from 0.2A to 5.0A in an interval of 0.4A. The current is kept low to reduce the electro-thermal heat-up. In general each section consist of two sides as described in Sec. 2.4. The placement of the measuring probes is identical for each side and is illustrated in Fig. 4.2.

Section: from terminal to terminal (from T_1 to T_2 for diode and IGBT)

Chip wires: from terminal to the corner of the chip surface through the wires connected to the chip (from $C_{1,2}$ to T_2 for the diode and from T_1 to $C_{1,2}$ for the IGBT)

Semiconductor chip: from terminal to the corner of the chip surface through the chip (from $C_{1,2}$ to T_1 for the diode and from T_2 to $C_{1,2}$ for the IGBT)

Wire current: through the wire curve of all 10 wires (between the blue for the diode and between the green for the IGBT)

Wire voltage: from chip surface to the wire curve of all 10 wires (between the red for the diode and between the yellow for the IGBT)

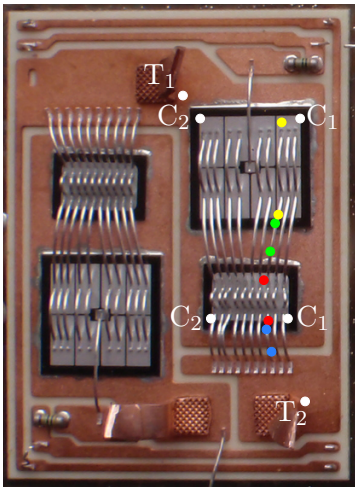


Figure 4.2. Four point probing on a section showing the measuring points for the diode and the IGBT.

As follows from the circuit shown in Fig. 2.15 the diode is placed as a freewheeling diode, accordingly, it conducts in the opposite direction of the IGBT. This is handled in the four-point measurements by interchanging the current carrying probes.

Section

The measurement from terminal to terminal gives the voltage drop through the entire half of a section: chip, chip solder, metallization, copper, and wires. Thus a few measurements can give an overview of the degradation in the individual sections of the module. This is carried out for both diodes and IGBTs.

Chip Surface

Chip surface to terminal measurements are carried out two places on the chip. These are referred to as C1 and C2 respectively. These measurements are carried out in order to locate any degradation further, that was found in the measurement between terminals. Thus, the measurement between terminals is split into two. The first measurement is through the 10 wires connected to the chip which includes the wires, wire bonds, copper, and metallization. The second measurement is through the semiconductor chip, which includes the chip, chip solder, copper, and metallization.

Wires

The current distribution is not necessarily even across the wires. Measurements on the wire curves are carried out with a known distance between the needles (3.5mm for the diode and 5mm for the IGBT). The wires are of slightly different length due to the geometry, as can be seen in Fig. 4.2. This is accounted for in the calculations of the resistance of a piece of wire, which is given by

$$R_{\text{wire}} = \rho \frac{L}{A}, \tag{4.1}$$

where ρ is the resistivity of the wire, L is the length of the wire piece, and A is the cross sectional area of the wire. As the measurements on the wire curves are done over the same length of wire for all 10 wires the resistance should be equal for all wires. Thus, measuring the voltage drop across the wire curve will give the current distribution of the wires. Measurements from the chip surface to the curve of the wire gives the voltage drop across the wire bond interface. These measurements are carried out with the same distance between the needles for all 10 wires. As the current distribution is known, the resistance in the wire bonds can be calculate. During these measurements the needle at the chip surface is always placed as close as possible to the wire without actual contact. The results may then be able to show which wire is failing if any.

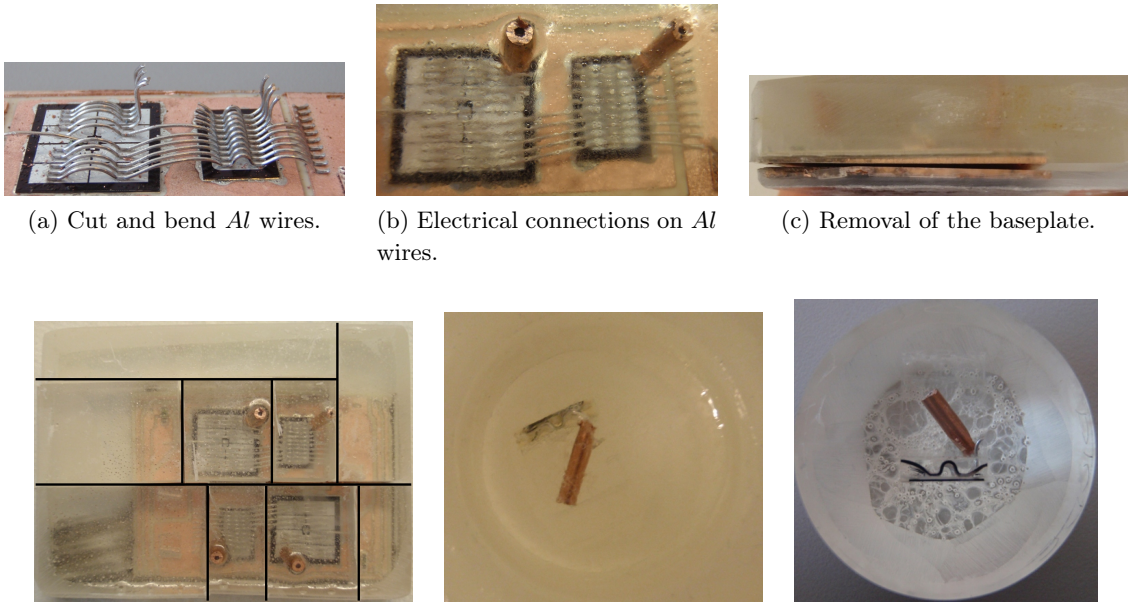
4.3 Micro-sectioning

Micro-sectioning is a technique for acquiring sample cross-sections in regions of interest. In particular the bonding interfaces of the *Al* wires are of interest in this project. An introduction to the method may be obtained in detail in [21], however, in the following the used steps are introduced:

Initially, the plastic cover is gently removed from the module. The sections are separated from each other and the silicone gel is removed with a silicone remover (C105HF). This process should be limited in time as the silicone remover does react slightly with the metals. Now the SEM and FIB investigation of the sections can be carried out along with the four-point probing measurements.

The micro-sectioning steps are described below with selected images from the process in Fig. 4.3.

1. The Al wires are cut and bend upwards to enable electrical connectivity after epoxy molding, see Fig. 4.3(a).
2. The section is cleaned and cast into epoxy - make sure not to cover the upwards pointing Al wires.
3. A Cu rod is attached to an Al wire on each chip, see Fig. 4.3(b).
4. The sections are re-cast into epoxy after a sample cleaning for protection of the Cu connectors.
5. Removal of the baseplate - precision is here paramount, as the 3mm baseplate is removed by placing the sample in upright position an cutting from the side. An image of a partly cut baseplate is seen in Fig. 4.3(c).
6. The section is cut into smaller pieces separating the semiconductor chips. These smaller pieces are then cast into epoxy. Fig. 4.3(d) illustrates the separation lines of a section.
7. The Cu, Al_2O_3 ceramics, and die solder paste is removed by polishing, leaving only the semiconductor chip and the wires.
8. The samples are re-cast in epoxy and the polishing towards the desired interface can begin. This is done using finer and finer grain SiC and DiaDuo 3μm diamond suspension polishing.
9. The lines from the polishing are removed by polishing with OP-U colloidal silica suspension.
10. Finally, the samples are cleaned and are investigated in a LEICA DMI3000M topdown microscope.



(a) Cut and bend Al wires.

(b) Electrical connections on Al wires.

(c) Removal of the baseplate.

(d) Separation lines of a section.

(e) Chip, wires, and Cu connection.

(f) Cross-section of the wire/metallization interface.

Figure 4.3. Selected steps of the micro-sectioning.

To visualize the grain structure of the Al wire the sample is electro-chemically etched using Barker's reagent at 30V for 3min [21]. Barker's reagent is designed to promote the grain

structures in pure Al. In order to due so an electrical connection is needed throughout the sample. A hole is thus drilled from the top of the sample and down to the Cu rod where a screw is placed making the electrical connection. The setup is illustrated in Fig. 4.4.

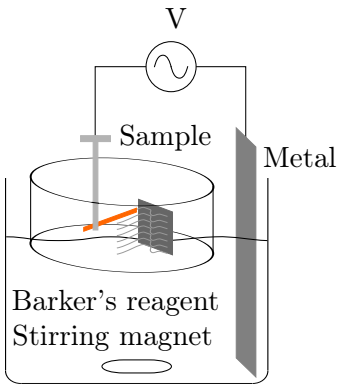


Figure 4.4. Setup for the electro-chemical etching.

After the etching the sample is investigated in the topdown microscope. There is two polarizers in the microscope. The first is placed between the light source and the sample and the second between the sample and the camera, see Fig. 4.5. The etching process is an anodization and thus, an oxide film is grown on the surface of the grains. As the grains have different sizes and crystal orientations, the oxide layers are not of an even thickness between the grains. Hence, due to Bragg diffraction the reflected light will interfere and thus, different wavelengths of light are reflected from different grains. As the light is reflected of the etched area of the sample the polarization changes. Hence, as the two polarizers are set to extinction only light reflected form the etched area will be detected by the camera. When the sample is etched the individual grains are anodized differently due to the size of the grains. Thus, the change in polarization of the reflected light is individual for the grains making them visual. [22]

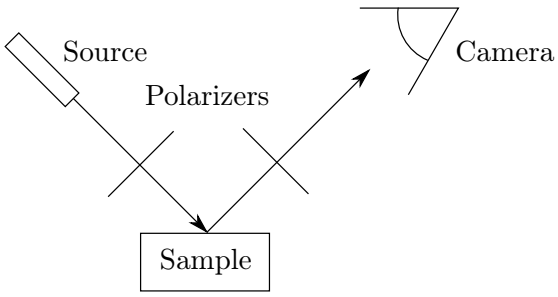


Figure 4.5. Placement of polarizers in the top down microscope.

Experimental Results 5

This chapter contains a description of relevant results and observations of all the experimental work performed in this paper. This includes examination of the metallization with SEM and FIB, electrical measurements on the power modules using four-point probing, and an investigation of the wire bonding interfaces using micro-sectioning.

5.1 Initial Observations

Prior to the four-point probing measurements on the modules any visual observations are recorded. Pictures are taken of the different chips where a clear wire lift-off is observed. Furthermore, SEM images are obtained of the metallization to see its condition. These observations will be given in the following, starting with the wires lifted off.

Wire lift-off is found for the following wires on the different modules:

1.3MC One wire bond of wire 5 on the LS diode on S6 is lifted off.

2.5MC Wire 1 on the HS diode on S6 has what seems to be a production error in the bonding.

3.5MC Many wires are lifted off.

- One wire bond of wires 1 and 8 together with both wire bonds of wires 2-7 on the HS diode on S1 are lifted off.
- One wire bond of wires 1, 6, and 7 together with both wire bonds of wires 8-10 on the LS diode on S3 are lifted off.
- One wire bond of wires 8-10 on the LS diode on S4 are lifted off.

4.5MC Nothing to note.

Pictures showing the wire lift-offs are presented in Fig. 5.1. The many lift-offs of the 3.5MC module will be discussed further in Chap. 6. Generally, it was observed that during the preparation of the samples to micro-sectioning the wire bonds on the diodes are easily pulled off compared to the wire bonds on the IGBT. This indicates that the bonding on the diode are weaker than on the IGBT after the modules have been stressed.

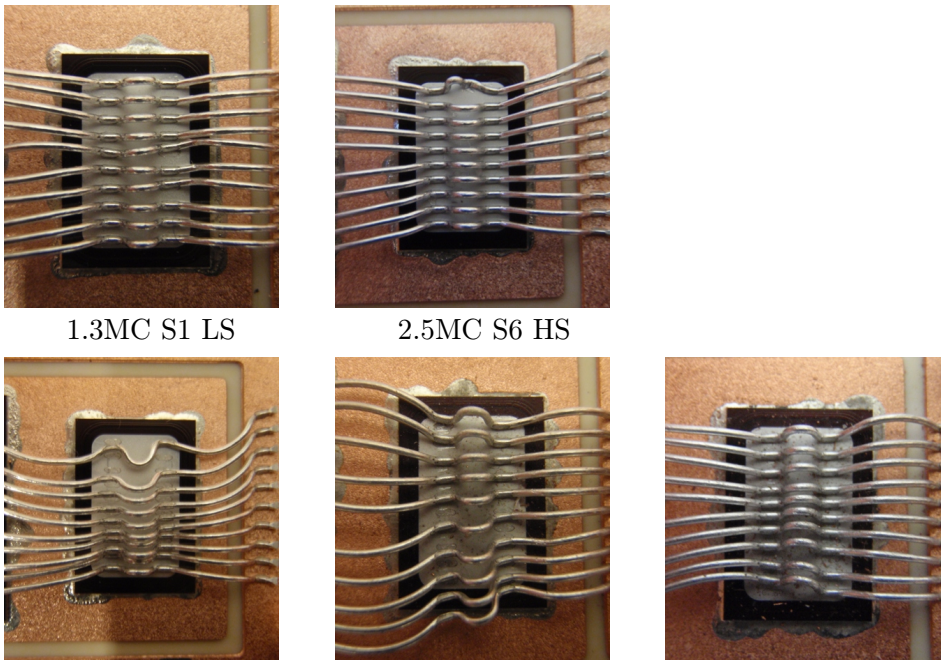


Figure 5.1. Top view of diodes with some wires clearly lifted off. For all pictures the wire in the top is wire 1.

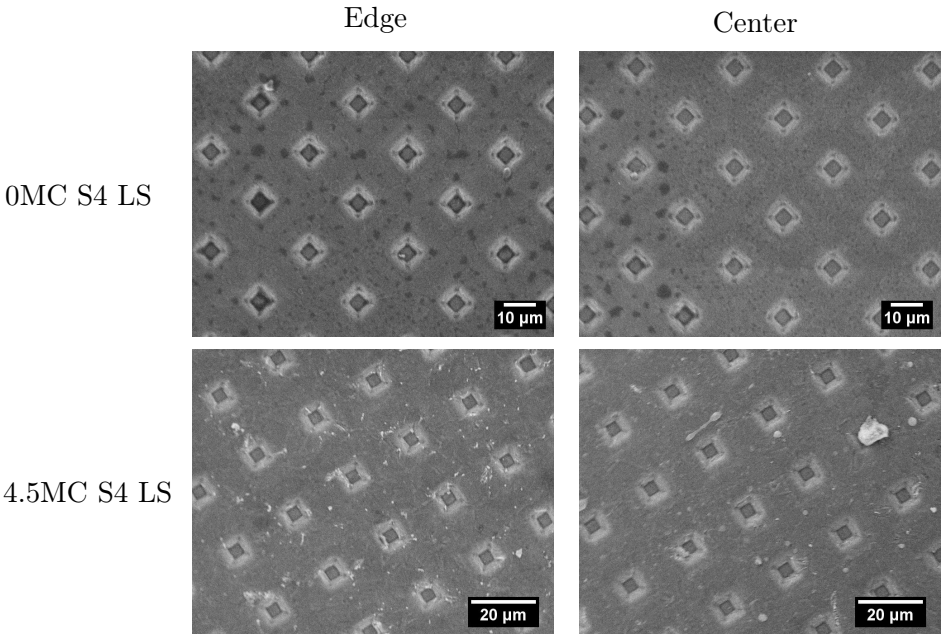


Figure 5.2. SEM images showing the topology of the metallization of the IGBTs. The first column shows the topology at the edge of the IGBTs and the second column shows topology of the center of the IGBTs.

The metallization have been examined with SEM near the edge and at the center of the chips. Considering the IGBTs there are no visible difference in the topology of the metallization

between the edge and the center of the chip, as shown in Fig. 5.2. Furthermore, there is no difference in the topology of the metallization between the modules.

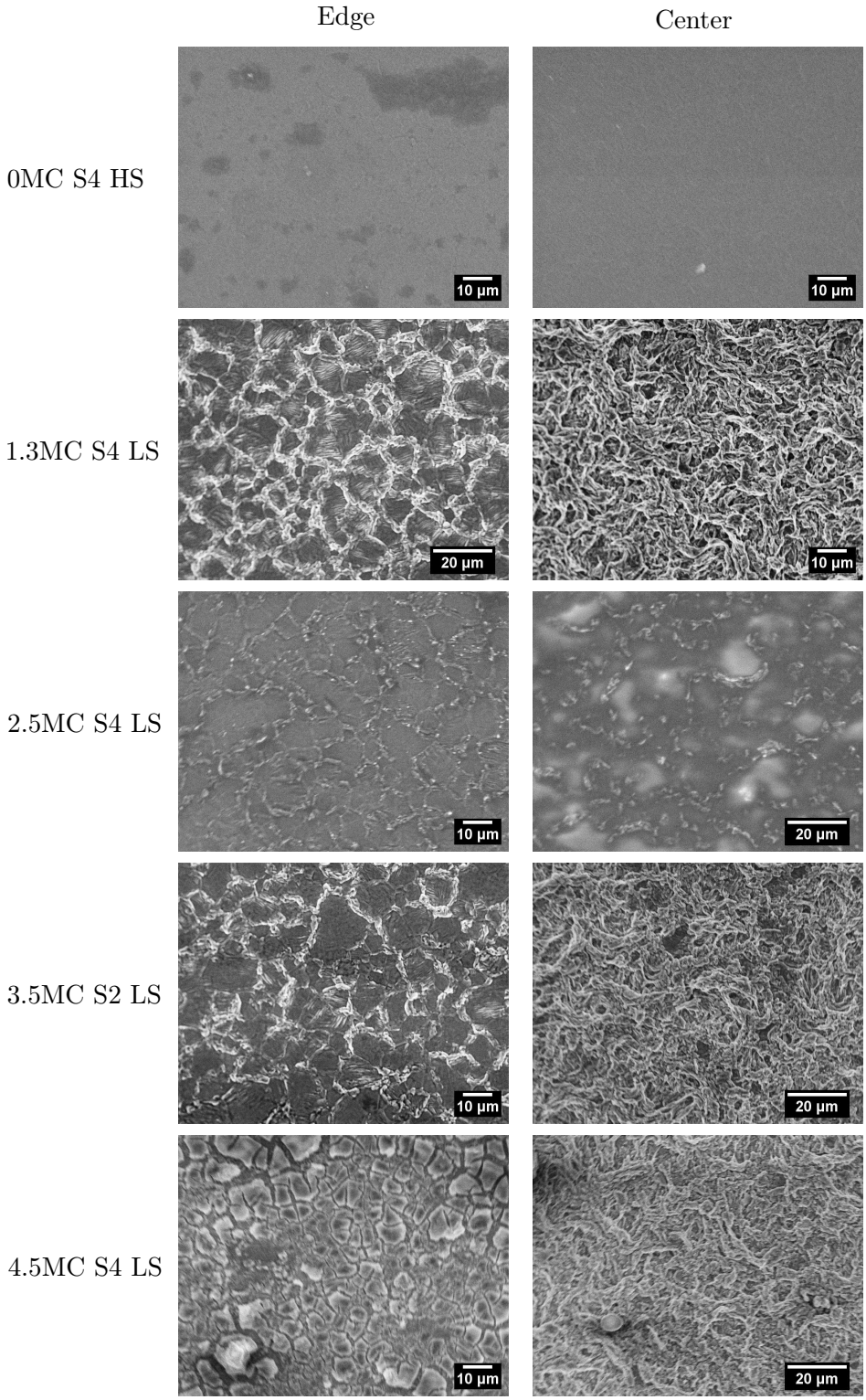
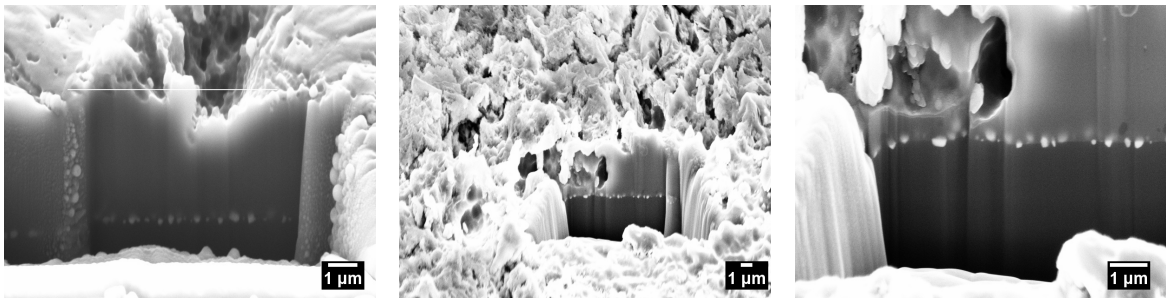


Figure 5.3. SEM images showing the topology of the metallization of the diodes. The first column shows the topology at the edge of the diodes and the second column shows topology of the center of the diodes.

For the diodes the metallization does change proportionally to the number of cycles disregarding the 1.3MC module. It is seen in Fig. 5.3 that the metallization on the new module is smooth whereas a structure is starting to form on the stressed modules. Furthermore, a difference in this structure is observed across the diodes. Comparing the edge and the center of the chip it is observed that the structural growth is more significant in the center. The metallization of all sections of the 3.5MC module have also been examined and here no significant difference have been observed between the sections, i.e. they degrade in a similar manner. This observation applies for both the HS and LS diodes.

In order to examine the depth of the structuring on the diodes they are investigated using FIB. FIB is used to cut into the diode so a cross section of the metallization becomes visible, as seen in Fig. 5.4. From Fig. 5.4 the reconstruction is seen to reach deep into the metallization and for the 4.5MC module it seems to go all the way through the metallization. This will increase the current density locally in the metallization which will cause additional heat-up.



(a) 2.5MC HS diode. (b) 4.5MC HS diode. (c) Zoom of Fig. 5.4(b).

Figure 5.4. Cross sectional view of the metallization of the diodes.

In Fig. 5.4 white dots are present in the interface between the diode and the metallization. These dots are platinum which are recombination centers in the diode that reduces the charge carrier lifetime. [6, p. 34]

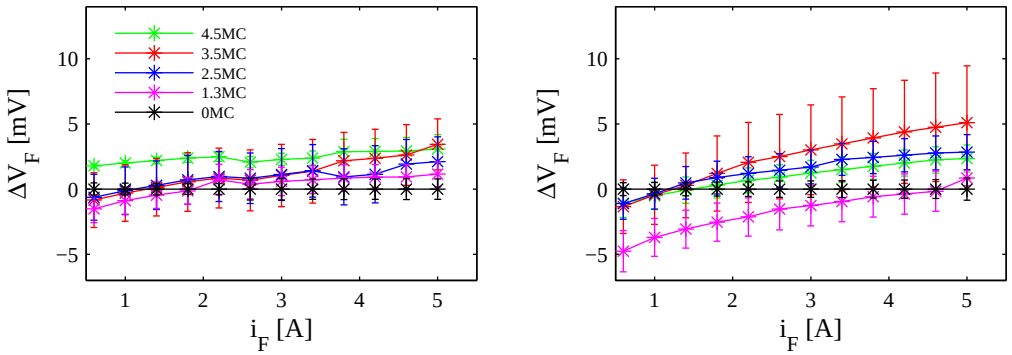
5.2 Four-Point Probing Results

Four-point probing measurements are performed on 5 modules. A new module, a 1.3MC, a 2.5MC, a 3.5MC, and a 4.5MC stressed module on selected sections as described in Sec. 4.1. In order to give a better overview of the results for the diodes and IGBT's they will be presented separately. Results of the same type are plotted on the same scale when convenient in order to make it easier to compare the results. The mean value of the sections and the deviation between sections is included as errorbars. For the new module these errorbars illustrate the variation in the production and the measurement method and for the stressed modules they also contain the spread in the degradation. As explained earlier the 1.3MC module has not been stressed similarly to the other modules and they can thus not be directly compared. However, the results of the 1.3MC module are still included in the following as they might contribute to an overall tendency of the degradation. Furthermore, it should be noted that the line between the points are not an interpolation. They are only included to

make the difference between points more visible. In the following only relevant results are presented. The reference measurements of the new module are presented in App. A and the remaining measurements of the stressed modules are available in App. B.

5.2.1 Section - Diode

The voltage drop across the diode is measured from terminal to terminal. The average voltage drop of the new module is subtracted from the stressed modules giving the relative difference in voltage drop (ΔV_F) which is plotted in Fig. 5.5. Here it is seen that only a minority of the measurements of are within the spread of the sections of the new module for both the HS and LS diodes. This indicates that the stressed modules are degrading. Disregarding the 1.3MC module, it is observed that ΔV_F increases with the number of cycles the modules have been stressed for the HS diodes. However, no relation is found for the LS diodes. Below 2A a negative ΔV_F is observed for both the HS and LS diode. Except for the 1.3MC module this small negative value is attributed to dissimilar sample heat-up, which can cause a small change in the resistance of the diode. For the 1.3MC module the temperature was not monitored during the accelerated test, thus explaining the negative values as this module have experienced diffferent loading conditions.

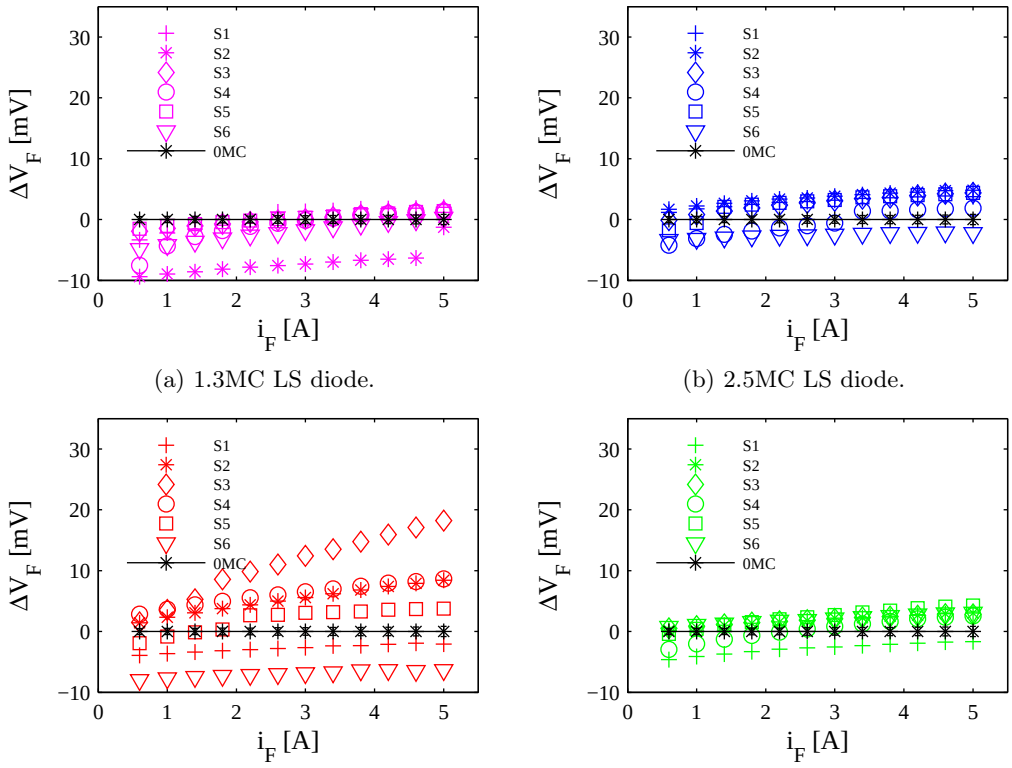


(a) HS diode.

(b) LS diode.

Figure 5.5. The relative difference in voltage drop across the diode as a function of forward current measured from terminal to terminal for both HS and LS of the sections.

The change in the voltage drop compared to a new module is illustrated in Fig. 5.6 for the individual sections. It is observed that there is a difference in ΔV_F between the sections of the same module. If the slope of ΔV_F as a function of i_F is approximately 0 the difference is attributed to diverse sample heat-up. However, a change in the slope indicates a change in the resistance and thus a degradation. From this a measure of the degradation is found for each module.



(a) 1.3MC LS diode.

(b) 2.5MC LS diode.

(c) 3.5MC LS diode.

(d) 4.5MC LS diode.

Figure 5.6. The relative difference in voltage drop across the diode as a function of forward current measured from terminal to terminal for LS of the individual sections.

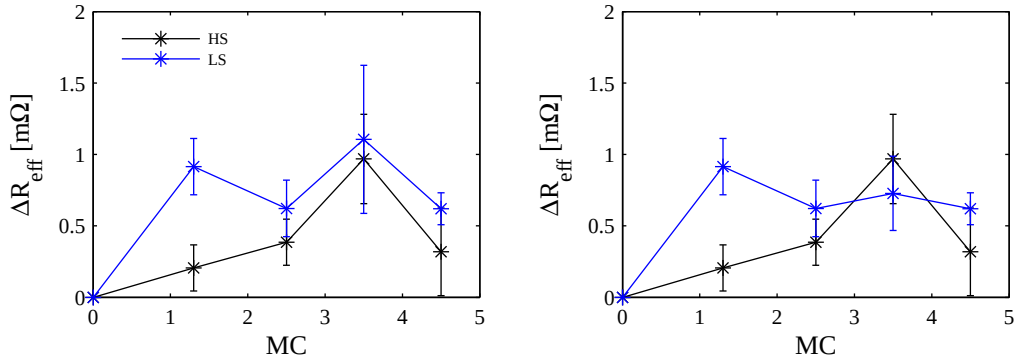
Degradation of a power module can be divided into hard and soft degradation as described in Sec. 2.7. The relation between the forward voltage and current can be described with an effective resistance (R_{eff}):

$$V_F = R_{eff} i_F. \tag{5.1}$$

The change in effective resistance (ΔR_{eff}) can be used as a measure of the degradation. Since

$$\frac{d\Delta V_F}{di_F} = \frac{dV_F}{di_F} - \frac{dV_{F,0}}{di_F} = R_{eff} - R_{eff,0} = \Delta R_{eff} \tag{5.2}$$

it is found through the results in Fig. 5.6 as the slope of these curves, where $V_{F,0}$ and $R_{eff,0}$ are the reference forward voltage and effective resistance, respectively. Degradation can be divided into hard and soft degradation as described in Sec. 2.7. Thus, to remove the hard degradation all sections with a large ΔR_{eff} are disregarded to give the soft degradation, which are both illustrated in Fig. 5.7. It is observed that the hard degradation of the 3.5MC module has a large spread, which is caused by the LS diode on S3. Unfortunately, in general the data presented in the four-point probing results suffer from low statistics. Thus, one can conclude that there is a tendency that the LS diode is damaged a bit more than the HS. However, the ΔR_{eff} is small and thus, only general wear appears from these results.

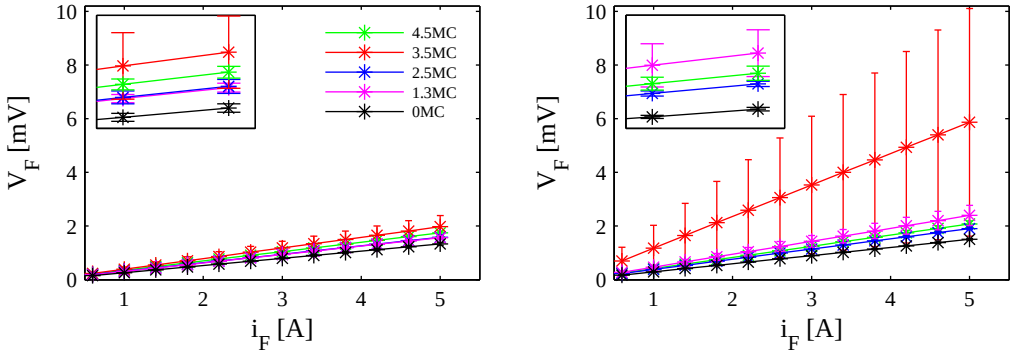


(a) Hard degradation. (b) Soft degradation.

Figure 5.7. Hard and soft degradation of the HS and LS diode.

5.2.2 Chip Surface - Diode

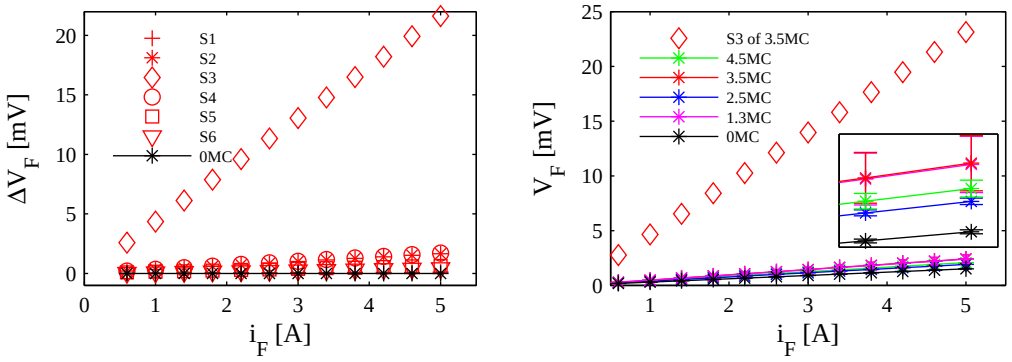
The voltage drop through the wires from the chip surface of the diode at C2 to the terminal is plotted in Fig. 5.8. From the figure it is seen that the stressed modules have a higher voltage drop than the new module which is attributed to normal wear. However, the increase in the voltage drop is more significant for the LS than the HS diode, indicating a more significant degradation at the LS. No relation between the effective resistance of the modules and the number of cycles they have been stressed is found, as seen in the zooms. Furthermore, the 3.5MC module has a large spread which is examined further below.



(a) C2 HS diode. (b) C2 LS diode.

Figure 5.8. The voltage drop through the wires as a function of forward current measured from the chip surface of the diode at C2 to the terminal for both HS and LS of the sections. The small figures inside are a zoom of the last two measurements.

Because of the large spread of the 3.5MC module for the LS diode the measurements at C2 are plotted for the individual sections in Fig. 5.9(a). It is observed that S3 is standing out from the other sections of this module. Separating S3 of the 3.5MC module from the rest of the module is illustrated in Fig. 5.9(b). In the zoom it is observed that there still is no correlation found between the effective resistance and the number of cycles.

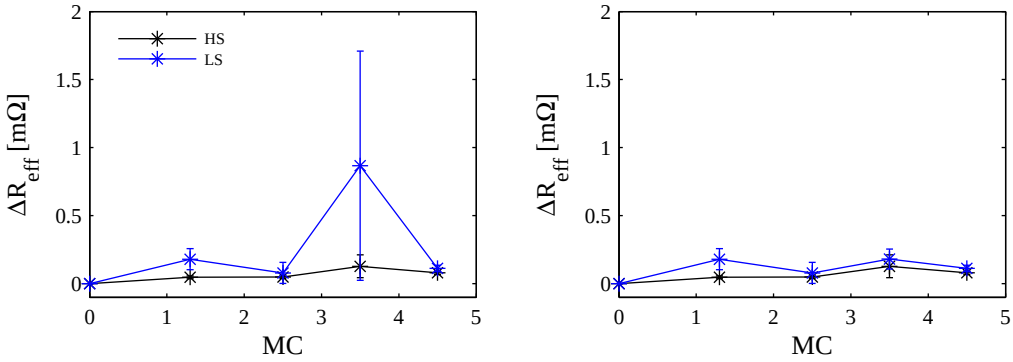


(a) 3.5MC LS diode individual sections.

(b) S3 of the 3.5MC module separated.

Figure 5.9. The voltage drop through the wires as a function of forward current measured from the chip surface C2 of the LS diode to the terminal. (a) Measurements of the LS diode of the 3.5MC module are plotted for the individual sections. (b) The voltage drop through the wires is plotted with S3 of the LS diode of the 3.5MC module separated. The small figure inside is a zoom of the last two measurements.

The hard and soft degradation through the wires of the diode are presented in Fig. 5.10. It is observed that the hard degradation of the 3.5MC module has a large spread, which is caused by the LS diode on S3. For the HS of the diode it is observed that the soft degradation increases slightly with the number of cycles the modules have been stressed, as is expected. Furthermore, it is noticed that the soft degradation and thus the general wear is a bit larger for the LS than for the HS of the diode.



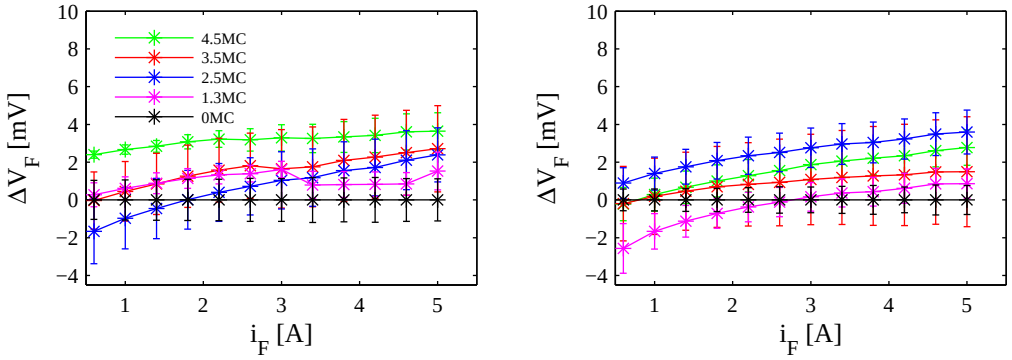
(a) Hard degradation.

(b) Soft degradation.

Figure 5.10. Hard and soft degradation through wires of the diode.

The voltage drop through the diode from the chip surface of the diode at C2 to the terminal is measured. ΔV_F as a function of forward current is plotted in Fig. 5.11. As for the measurements between terminals in Sec. 5.2.1 it is observed that only a minority of the measurements of are within the spread of the sections of the new module for both the HS and LS diodes. This indicates that the stressed modules are degrading. The effective resistance of the stressed modules is increasing with the number of cycles the modules have been stressed

for the HS diodes when disregarding the 1.3MC module. However, this is not the case for the LS where no correlation is found.

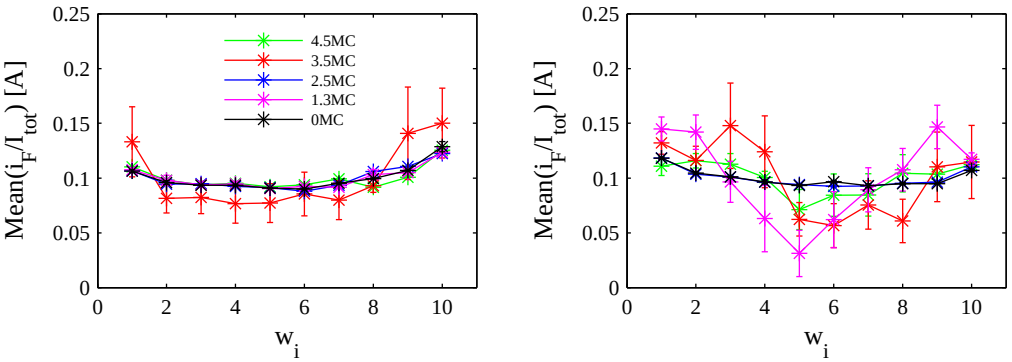


(a) C2 HS diode. (b) C2 LS diode.

Figure 5.11. The relative difference in voltage drop through the diode as a function of forward current measured from the chip surface of the diode at C2 to the terminal for both HS and LS of the sections.

5.2.3 Wires - Diode

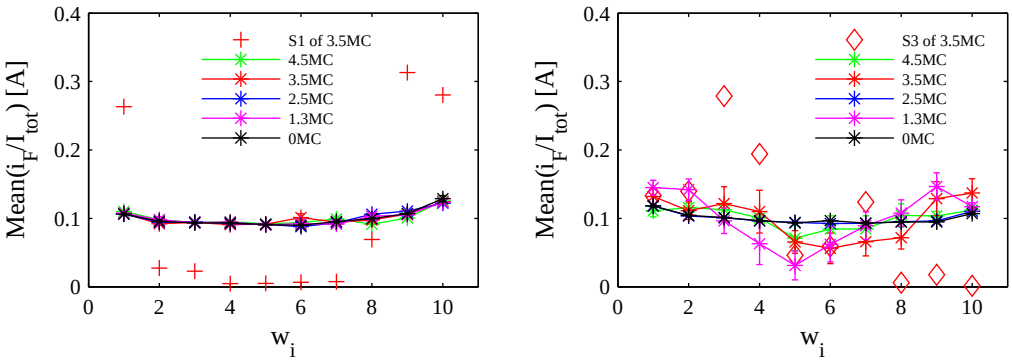
The current distribution of the 10 wires from each half of a section is plotted in Fig. 5.12. For a new module it is seen that the current distribution is almost homogeneous except for the edges, which is consistent for the reference measurements as seen in Fig. A.4. This must be caused by geometry of the wire bonds to the chip surface. There is an even spacing between the wires bonds on the chip, but wires 1 and 10 have more surface area of the chip available as seen in Fig. 2.14. The current distribution for the 1.3MC and 3.5MC modules on the LS has a large spread and the mean values are distinct from the new module. The 4.5MC modules also deviate from the new module but it still has the same overall shape. For the HS the 3.5MC module has a large spread and the current through a few of the wires deviate significantly from the new module.



(a) HS diode. (b) LS diode.

Figure 5.12. The current distribution of the wires on the diode for both HS and LS of the sections.

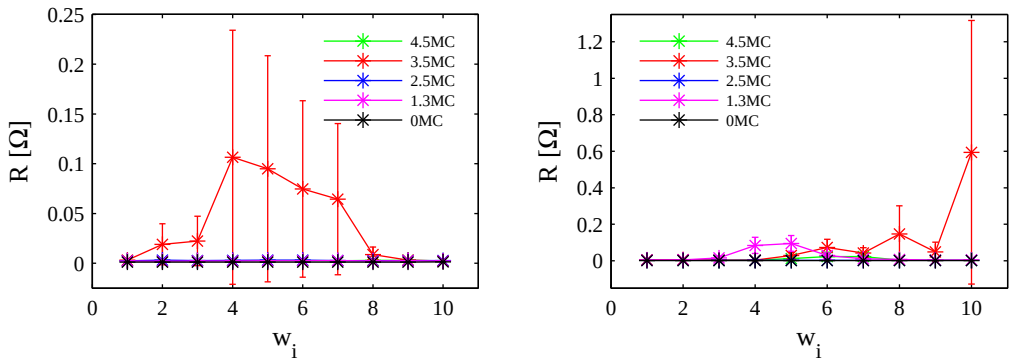
Due to the large spread of the 3.5MC module it is plotted with the S1 and S3 separated for the HS and LS, respectively, as shown in Fig. 5.13. It is observed that S1 of the HS and S3 of the LS are the main contributors to the spread between the sections, indicating that the degradation is most severe in the wires of those diodes. However, for the LS a general degradation is still observed.



(a) HS diode. (b) LS diode.

Figure 5.13. The current distribution of the wires on the diode for both HS and LS of the sections with the S1 and S3 separated for the HS and LS, respectively.

The resistance through the wire bonds is plotted in Fig. 5.14. A large resistance is observed for the 3.5MC module along with a large spread. This is studied further in Fig. 5.15.



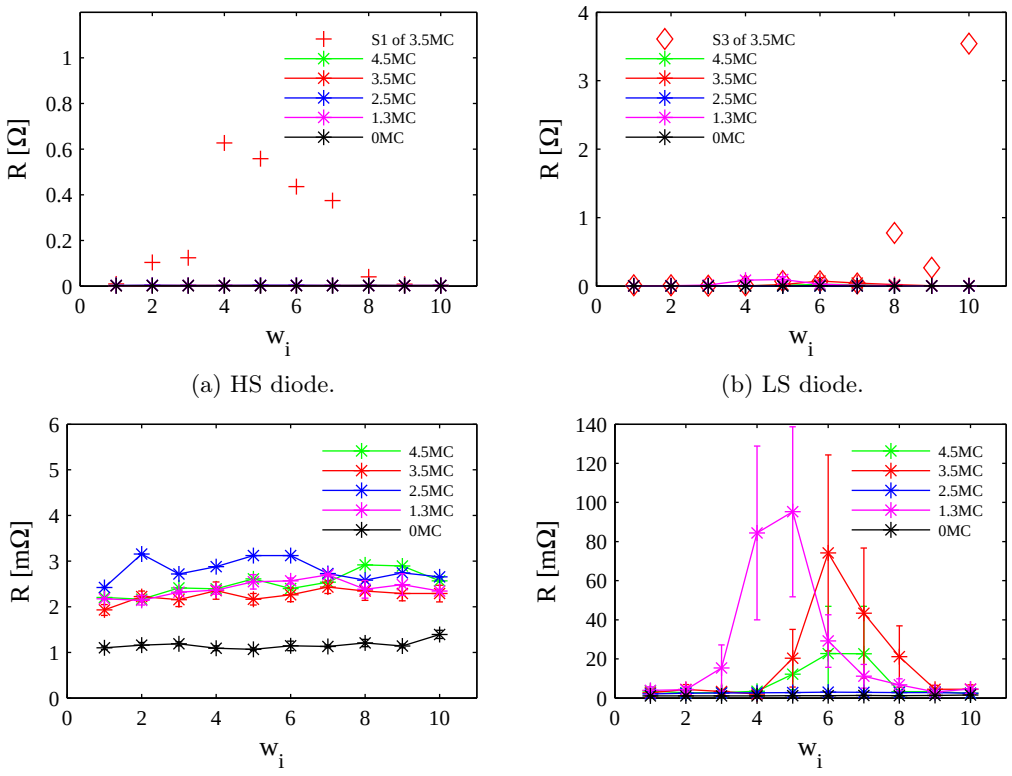
(a) HS diode. (b) LS diode.

Figure 5.14. The resistance through the wire bonds in the diode measured from the chip surface to the wire curve for both HS and LS of the sections.

As for the current distribution it is observed that S1 of the HS and S3 of the LS are the main contributors to the spread between the sections. Disregarding these sections the increase in resistance is now about even for all the wires of the different modules for the HS, see Fig. 5.15(c), which is attributed to general wear. However, this is not the case for the LS, where a degradation is found for the 1.3MC, 3.5MC, and 4.5MC modules, see Fig. 5.15(d).

Furthermore, no relation between the number of cycles the modules have been stressed and the increase in resistance is found.

Considering the resistance in the new module, it is observed that there is a small increase in resistance in wire 10 compared to the other wires, which is evident from Fig. 5.15(c). This originates from the placement of the measuring probes. When measuring for wire 1-9 the needle on the chip surface is placed in between two wires whereas for wire 10 it is not, which is also evident from Fig. A.5.



(a) HS diode.

(b) LS diode.

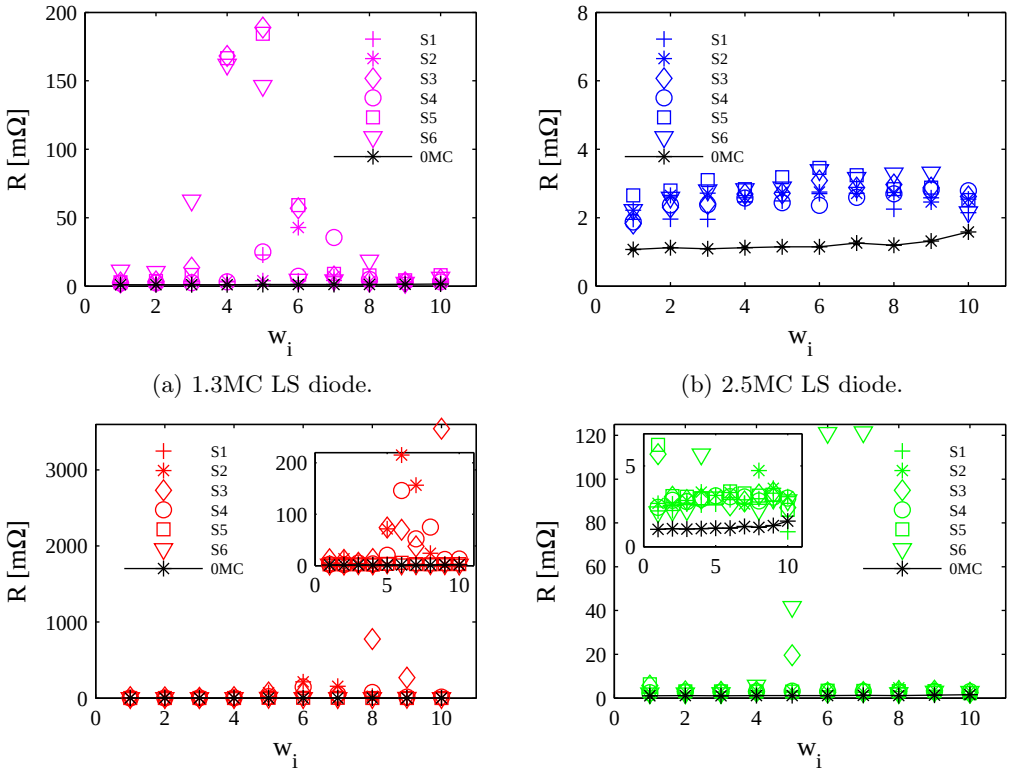
(c) Zoom of Fig. 5.15(a).

(d) Zoom of Fig. 5.15(b).

Figure 5.15. The resistance through the wire bonds in the diode measured from the chip surface to the wire curve for both HS and LS of the sections with the S1 and S3 separated for the HS and LS, respectively.

The resistances through the wire bonds for the individual sections of the 1.3MC, 2.5MC, 3.5MC, and 4.5MC modules are plotted for the LS in Fig. 5.16. It should be noted that in order to make the difference between the sections in each plot visible the axis of these plots are not of the same size. The resistance through the wire bonds of the HS of all the modules is increased slightly with respect to the new module apart from the S1 of the 3.5MC module, see Fig. B.7. In the LS diode there is a significant difference in the resistance between the sections of a module except for the 2.5MC module. Furthermore, it is observed that the 3.5MC module has a significantly higher resistance than the rest of the modules as seen in Fig. 5.16(c). This suggests that the wire bonds of the LS diode are degraded more than the HS, which is also evident from the degradation in Fig. 5.17. The large spread found in the

hard degradation of the 3.5MC module is caused by the LS diode of S3. Degradation is found to increase with the number of cycles the modules are stressed for the HS, but for the LS no tendency is obvious. However, only one module have been examined for each point in the graph, so more data is needed to make any conclusions on the relation between degradation and number of cycles.



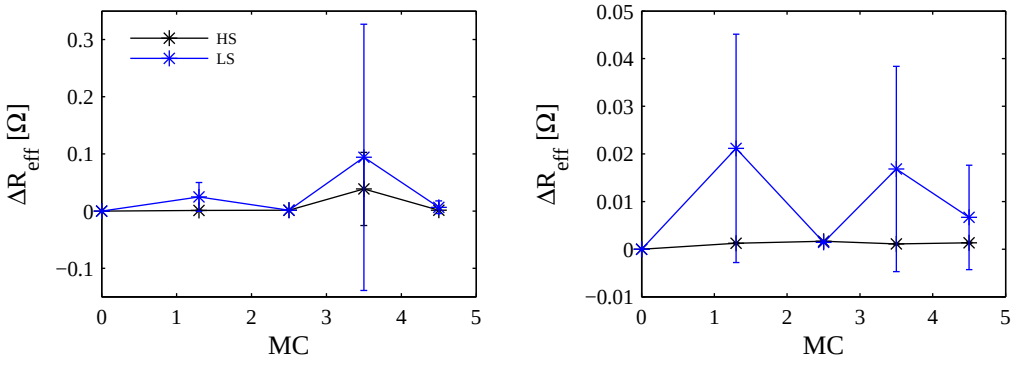
(a) 1.3MC LS diode.

(b) 2.5MC LS diode.

(c) 3.5MC LS diode.

(d) 4.5MC LS diode.

Figure 5.16. The resistance through the wire bonds in the diode measured from the chip surface to the wire curve for the individual sections of the 1.3MC, 2.5MC, 3.5MC, and 4.5MC modules. The small figure inside (c) and (d) are a zooms of the measurements.



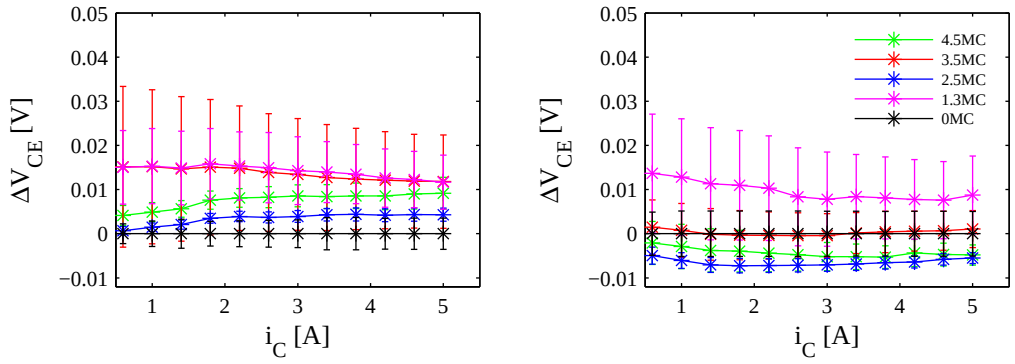
(a) Hard degradation.

(b) Soft degradation.

Figure 5.17. Hard and soft degradation of the resistance through the wire bonds of the diode.

5.2.4 Section - IGBT

The voltage drop across the IGBT is measured from terminal to terminal. The average of the new module is subtracted from the stressed modules giving the relative difference in voltage drop (ΔV_{CE}), which is plotted in Fig. 5.18. Here it is observed that the voltage drop is increased for the stressed modules except for the 2.5MC and 4.5MC modules on the LS which are decreased compared to the new module. However, the magnitude is only 5mV. Since the difference in the voltage drop of the modules during the accelerated test varies on the order of 10mV, see [8], no significance is attributed to this. For the HS IGBT's the small increase in ΔV_{CE} is attributed to general wear. However, a large spread i present for the 3.5MC module. For the LS diodes it is found that ΔV_{CE} is negative for the 2.5MC module. This indicated the R_{eff} is decreased in the LS IGBT's of this module, thus decreasing its power loss. There is found no relations between the effective resistance of the modules and the number of cycles they have been stressed.

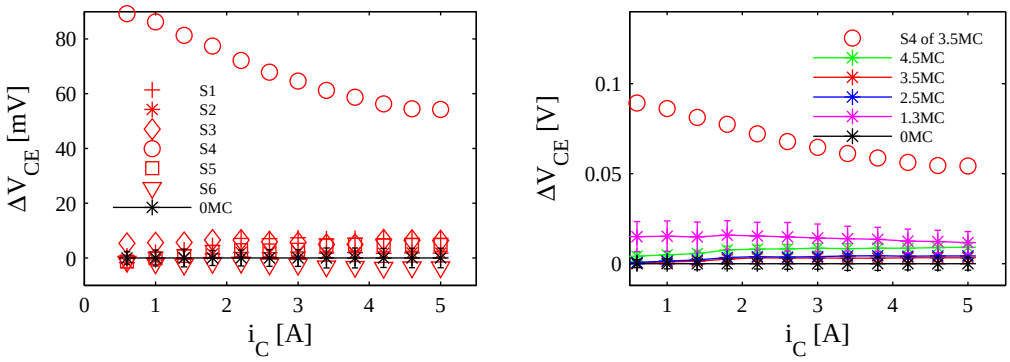


(a) HS IGBT.

(b) LS IGBT.

Figure 5.18. The relative difference in voltage drop across the IGBT as a function of collector current measured from terminal to terminal for both HS and LS of the sections.

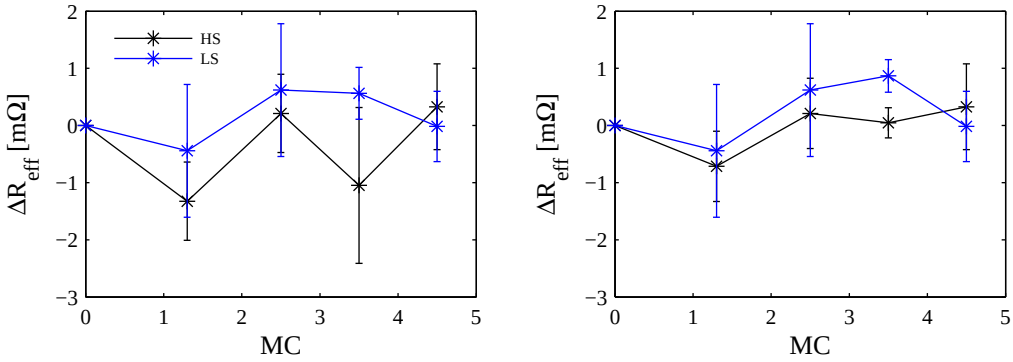
The large spread of the HS of the 3.5MC module is examined further for the individual sections in Fig. 5.19(a). It is evident that S4 is significantly different from the other sections. Separating S4 removes the spread of the 3.5MC module, see Fig. 5.19(b). This indicates that S4 of the IGBT is degraded more than the other sections. The degradation illustrated in Fig. 5.20 shows a tendency that the LS is degraded more than the HS of the IGBT. However, the degradation is limited as ΔR_{eff} is small and is thus attributed to general wear.



(a) 3.5MC HS IGBT individual sections.

(b) S4 of the 3.5MC separated.

Figure 5.19. The relative difference in voltage drop across the IGBT as a function of collector current measured from terminal to terminal for HS of the sections. (a) for the individual section of the HS of the 3.5MC module. (b) with S4 of the 3.5MC module separated from the other sections.



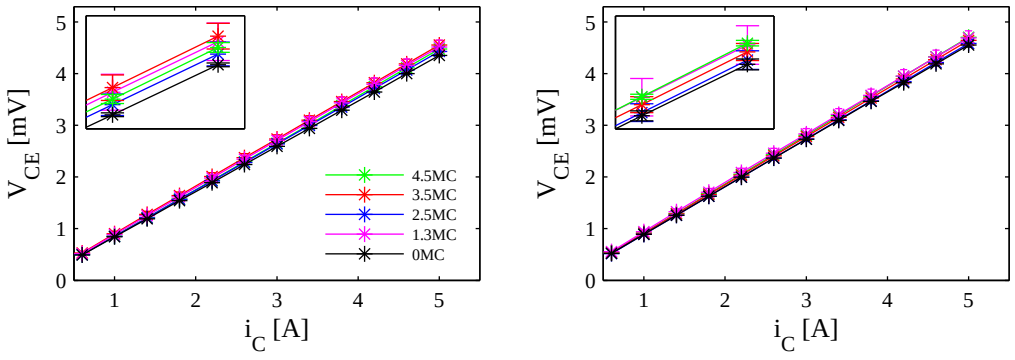
(a) Hard degradation.

(b) Soft degradation.

Figure 5.20. Hard and soft degradation of the IGBT.

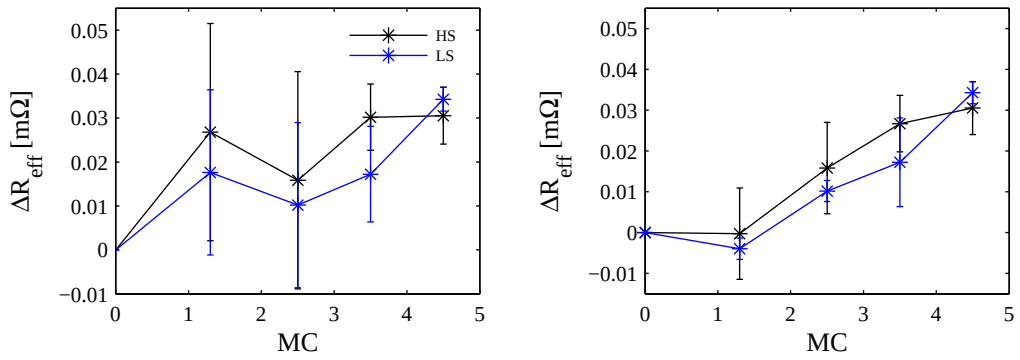
5.2.5 Chip Surface - IGBT

The voltage drop through the wires from the chip surface of the IGBT at C2 to the terminal is plotted in Fig. 5.21. Here only a small increase in the voltage drop is observed for the stressed modules, which is attributed to general wear. The measure of the degradation is presented in Fig. 5.22, where it is evident that ΔR_{eff} is almost zero.



(a) C2 HS IGBT. (b) C2 LS IGBT.

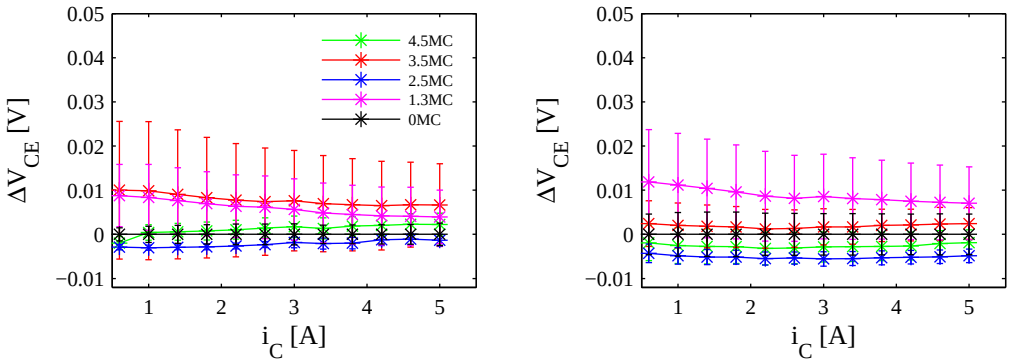
Figure 5.21. The voltage drop through the wires as a function of collector current measured from the chip surface of the IGBT at C2 to the terminal for both HS and LS of the sections. The small figures inside are a zoom of the last two measurements.



(a) Hard degradation. (b) Soft degradation.

Figure 5.22. Hard and soft degradation through wires of the IGBT.

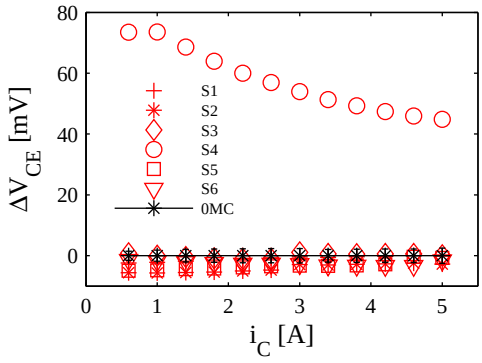
The voltage drop through the IGBT from the chip surface of the IGBT at C2 to the terminal is measured. The average of the new module is subtracted from the stressed modules which is plotted in Fig. 5.23. It is observed that these measurements are about identical to the measurements between terminals presented in Fig. 5.18. Thus, the individual sections of the HS of the 3.5MC module is investigated further, see Fig. 5.24. Again it is observed that S4 is distinct from the other sections. This indicated that S4 of HS IGBT of the 3.5MC module is degraded more compared to the other sections.



(a) C2 HS IGBT.

(b) C2 LS IGBT.

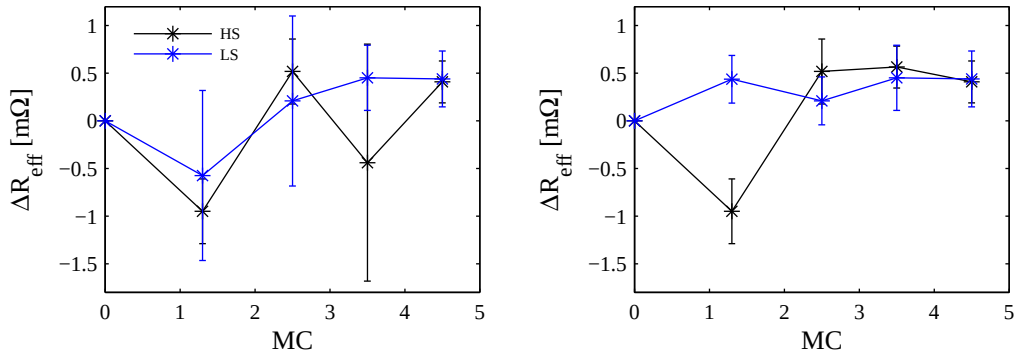
Figure 5.23. The relative difference in voltage drop through the IGBT as a function of collector current measured from the chip surface of the IGBT at C2 to the terminal for both HS and LS of the sections.



(a) 3.5MC HS IGBT individual sections.

Figure 5.24. The relative difference in voltage drop through the HS IGBT for the individual sections of the 3.5MC module.

A measure of the degradation through the chip of the IGBT is presented in Fig. 5.25. It is observed that there is a small degradation in the IGBT's, which is attributed to general wear. Furthermore, there is a tendency that the degradation increases with the number of cycles that the modules have been stressed when disregarding the 1.3MC module.

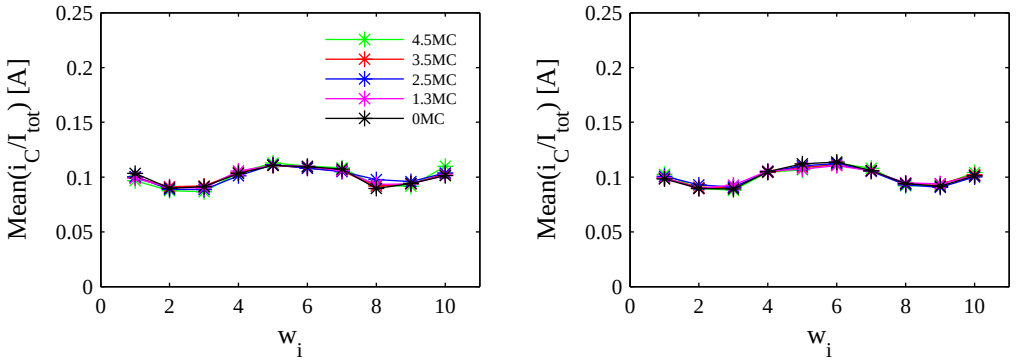


(a) Hard degradation. (b) Soft degradation.

Figure 5.25. Hard and soft degradation through the chip of the IGBT.

5.2.6 Wires - IGBT

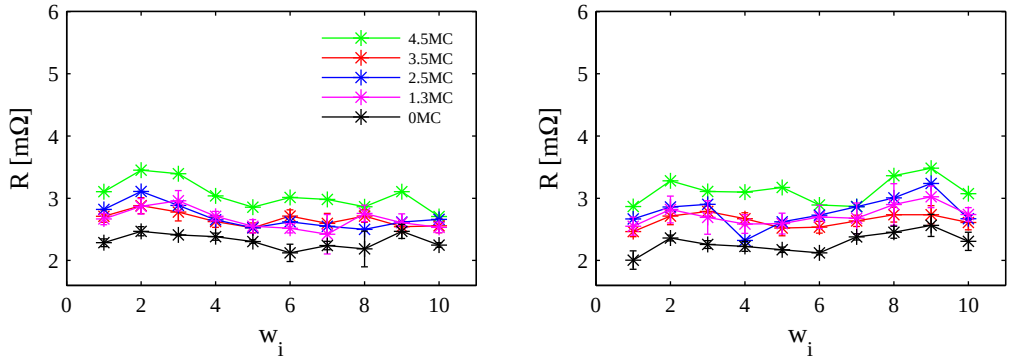
The current distribution of the 10 wires from each half of a section is plotted in Fig. 5.26. As for the diode the current distribution for the IGBT is not homogeneous. This is due to an uneven distance between the wire bonds on the chip surface as seen in Fig. 2.14. Generally it is observed that the current distribution of the stressed modules is similar to that of a new module.



(a) HS IGBT. (b) LS IGBT.

Figure 5.26. The current distribution of the wires of the IGBT for both HS and LS of the sections.

The resistance through the wire bonds is plotted in Fig. 5.27. Only a small increase in the resistance is observed which is attributed to general wear. No difference between the HS and LS is observed and no clear correlation between the degradation and the number of cycles is present.



(a) HS IGBT. (b) LS IGBT.

Figure 5.27. The resistance through the wire bonds in the IGBT measured from the chip surface to the wire curve for both HS and LS of the sections.

A measure of the degradation through the wire bonds is plotted in Fig. 5.28. No hard degradation was present through the wire bonds of the IGBT's. The small ΔR_{eff} is attributed to general wear. There is a tendency of the degradation increasing with the number of cycles that the module is stressed.

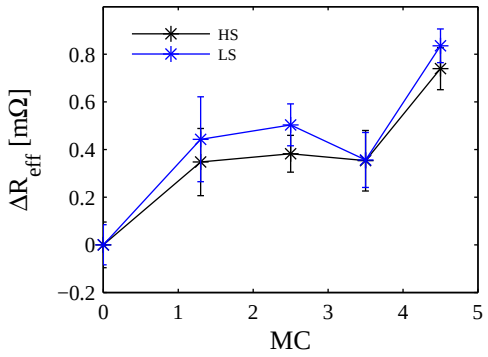


Figure 5.28. Soft degradation of the resistance through the wire bonds of the IGBT.

5.2.7 Summary of the Four-Point Probing Results

The results of the four-point probing are numerous and thus an overview is difficult to maintain. Important results are presented above and the remaining can be found in App. B. In this section a summary of the four-point probing results will be presented.

The results of the four-point probing measurements clearly point out that the LS diode is degrading as presented in Secs. 5.2.1, 5.2.2, and 5.2.3. The measurements through the diode shows no degradation which is contrary to the measurements through the wires as seen from Figs. 5.8 and 5.11. Thus the degradation must be present in the wire bonds and to a limited degree the metallization. This is then confirmed in the current distribution and the resistance through the wire bonds, as seen in Figs. 5.12 and 5.14. A significant degradation is found for S1 and S3 of the HS and LS diode, respectively, as seen in Fig. 5.15. Similarly for the

S4 of the HS IGBT a significant degradation is observed. Otherwise no degradation is found for the IGBT's except for general wear.

5.3 Micro-sectioning Results

The interface of the *Al* wire bond is investigated using the micro-sectioning technique described in Sec. 4.3. In order to keep track of the bonding interfaces they are numbered B1-4 as illustrated in Fig. 5.29. Micro-sectioning is time consuming and thus only one section of each module is investigated. In this section the results are presented with illustrative examples and further images that support the statements are presented in App. C. Unfortunately, a few samples broke while attaching the electrical contact before the etching. Thus, the grain structure of these samples are not available.

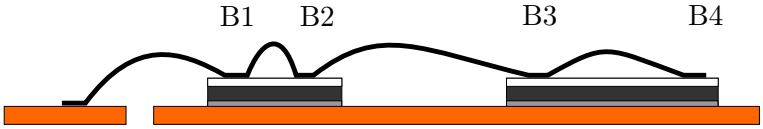
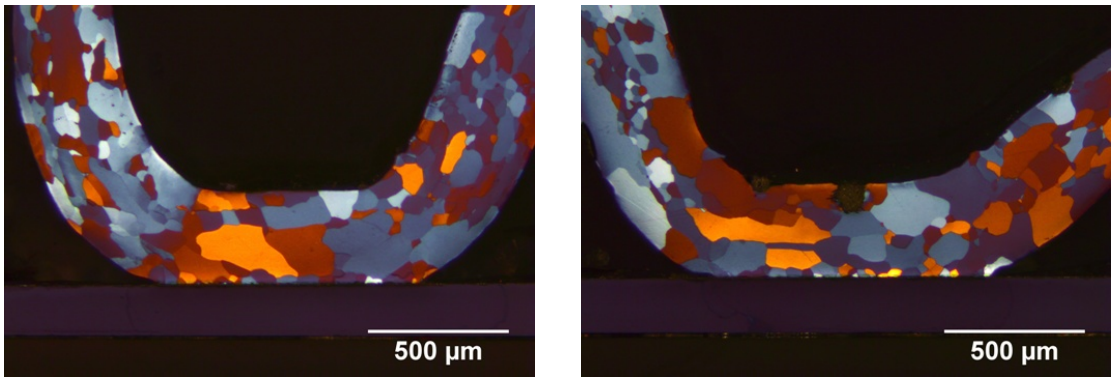


Figure 5.29. Numbering of the bonding interfaces.

5.3.1 Reference Module

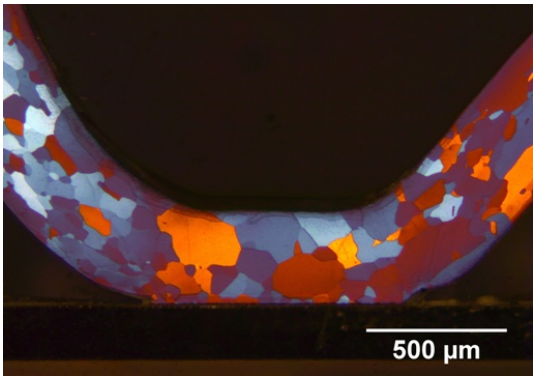
Initially a new module is investigated giving a reference to the stressed modules, see Fig. 5.30. At the interface it is observed that the refinement area is very small which show that the fracture strength of the grains inside the wires is weak as described in Sec. 2.7.2. By magnifying the edges of the interface, see Fig. 5.31, it is observed that there is no delamination or cracks in the wire bonds of the new module.



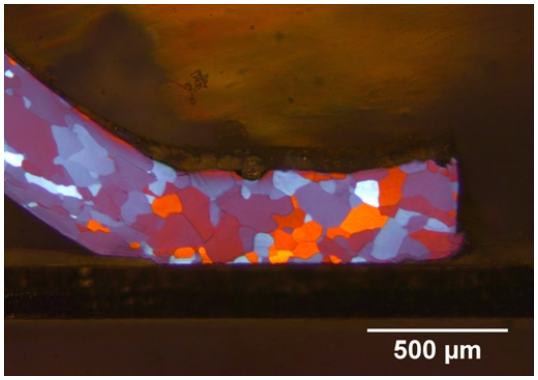
(a) Wire bond B1 diode.

(b) Wire bond B2 diode.

Figure 5.30. Grain structure of the wire bonds of the new module.

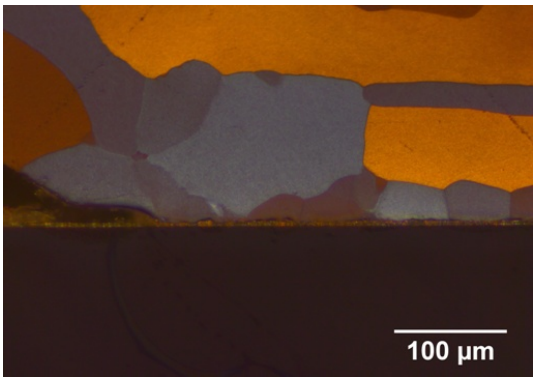


(c) Wire bond B3 IGBT.

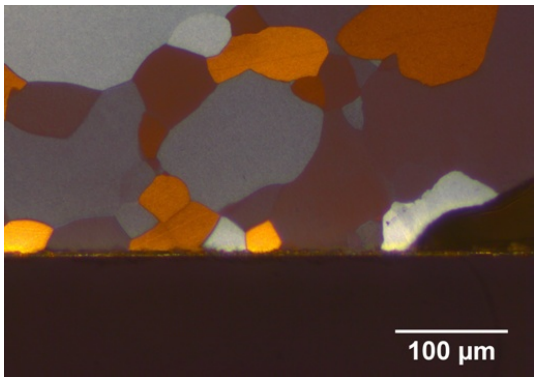


(d) Wire bond B4 IGBT.

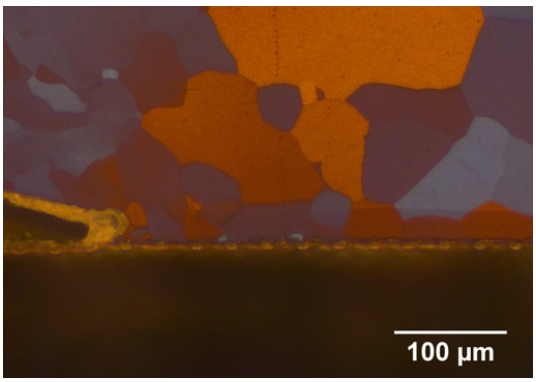
Figure 5.30. Grain structure of the wire bonds of the new module.



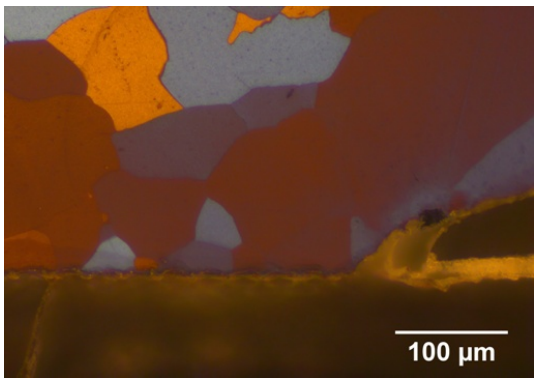
(a) Wire bond B2 left side of the bond on the diode.



(b) Wire bond B2 right side of the bond on the diode.



(c) Wire bond B3 left side of the bond on the IGBT.



(d) Wire bond B3 right side of the bond on the IGBT.

Figure 5.31. Magnification of the grain structure of the wire bonds of the new module.

5.3.2 Stressed Modules

It was difficult to reach an interface of the wires on the diodes of the stressed modules that was actually bonded to the diode. This is an indication that for many wire bonds on the

diodes the bonding area is small and thus it is difficult during the polishing to stop at the correct time to reach this small area. Thus, for the HS and LS diodes of the 1.3MC, 2.5MC, and 4.5MC modules the interfaces reached are where no wire bond is visible as illustrated in Fig. 5.32. Here it is clearly seen that the wire has once been bonded in this cross sectional cut as the delamination of the wire is visible with remains of the wire present on top of the diode. Images of the other samples can be found in App. C.

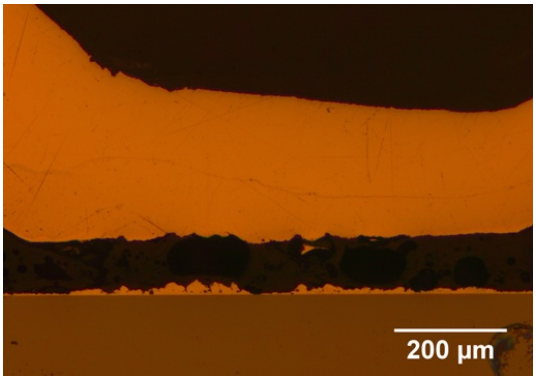
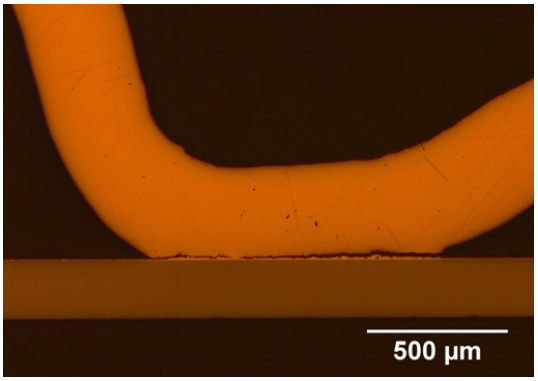
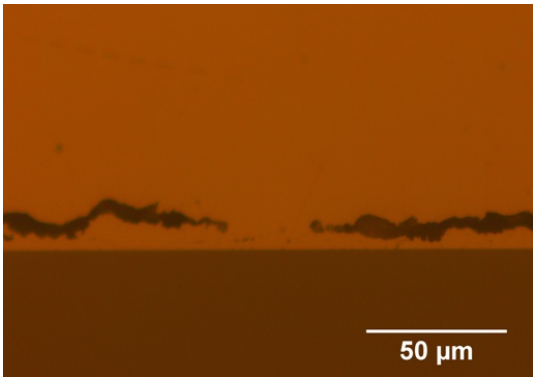


Figure 5.32. Delaminated B2 wire bond on the LS diode of S2 of the 4.5MC module.

Only a wire bond on the HS and LS diode of the 3.5MC module is found, see Fig. 5.33. It is clearly observed that most of the bonding area of the wire bonds is delaminated. From the samples examined it appears as if there is no difference between the bonding of the HS and LS diode. However, since only a few samples are examined no conclusion can be drawn on the basis of these results.

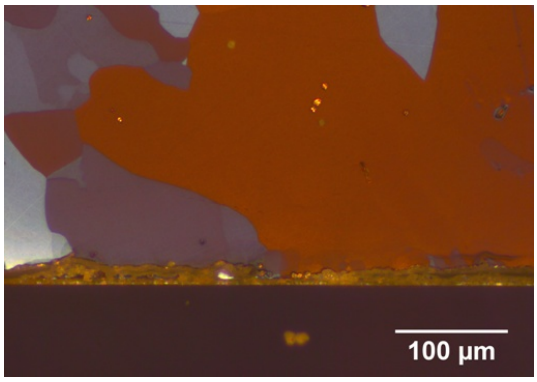


(a) Wire bond B2 of S2 on the HS diode of the 3.5MC module.

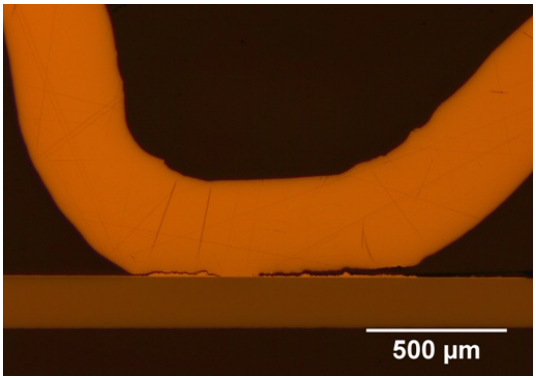


(b) Zoom of Fig. 5.33(a).

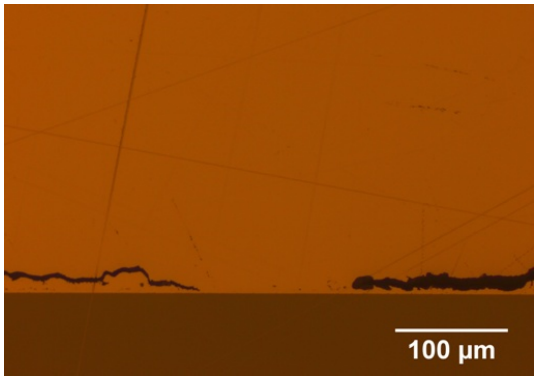
Figure 5.33. Wire bonds of the HS and LS diode of the 3.5MC module.



(c) Zoom of Fig. 5.33(a) after etching.



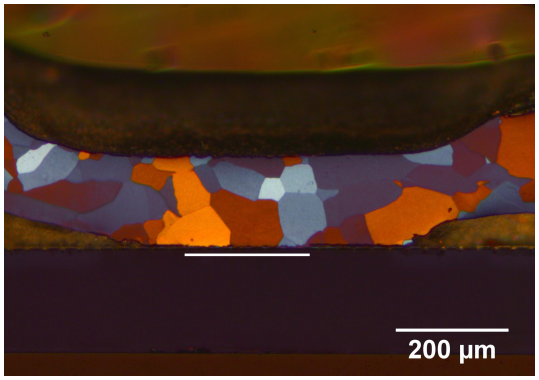
(d) Wire bond B2 of S2 on the LS diode of the 3.5MC module.



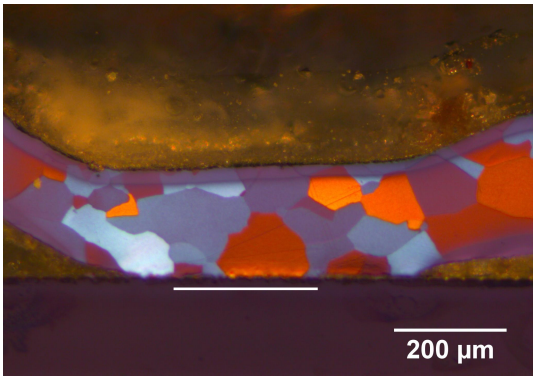
(e) Zoom of Fig. 5.33(c).

Figure 5.33. Wire bonds of the HS and LS diode of the 3.5MC module.

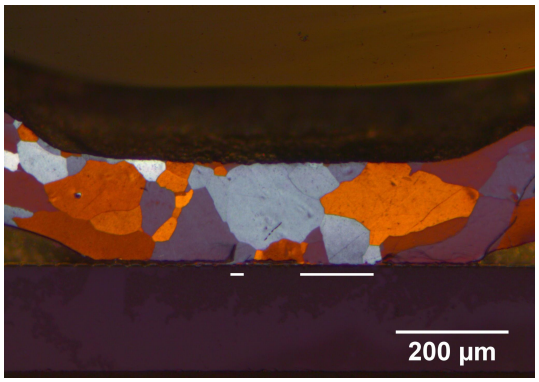
Considering the wire bonds on the IGBT, illustrated in Fig. 5.34, it was found that it was easier to reach an interface where the wires were attached compared to the diodes. The height of the wire in the cross sectional cut can give an idea of how far into the wire the cross sectional cut is. The cross sectional cut of the wires of the 1.3MC, 2.5MC, and 3.5MC modules in Figs. 5.34(a,b,c) are approximately in the same position inside the wire, since the height is about 200μm. Whereas, the wire bond of the 4.5MC module in Fig. 5.34(d) has a height of about 400μm. Knowing that the height of the wire is 400μm it is estimated that the cross sectional cut of the wire bond of the 4.5MC module is close to the center of the wire, while the other wires are closer to the side of the wire. The wire bond has an elliptical shape as described in Sec. 2.7.2, and thus the length of the wire bond in the cross sectional cut is larger in the center compared to the edges of the wire. Taking this into consideration it is observed that there is an increasing delamination of the wire bonds on the IGBT's with an increasing number of cycles the modules have been stressed.



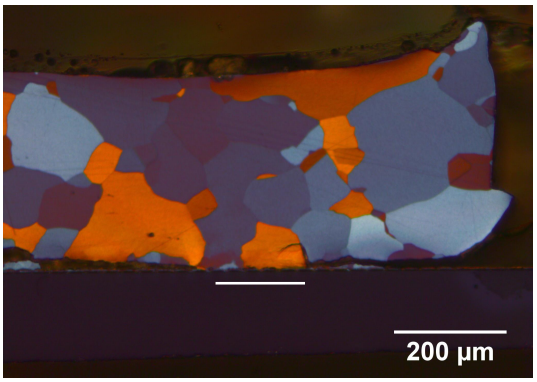
(a) Wire bond B4 of S4 on the HS IGBT of the 1.3MC module.



(b) Wire bond B4 of S4 on the LS IGBT of the 2.5MC module.



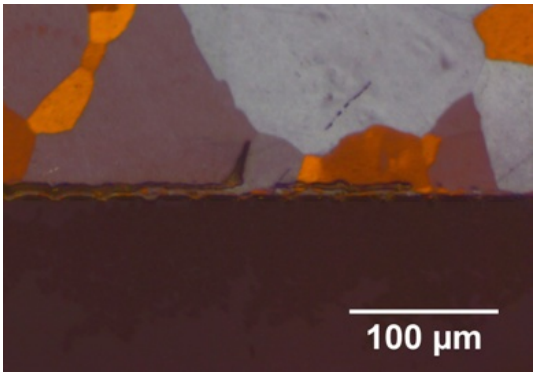
(c) Wire bond B4 of S2 on the HS IGBT of the 3.5MC module.



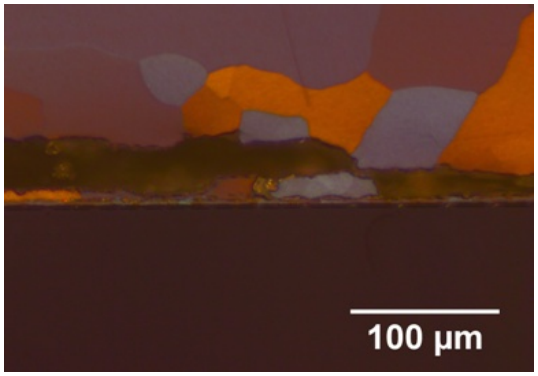
(d) Wire bond B4 of S4 on the LS IGBT of the 4.5MC module.

Figure 5.34. Grain structure of the wire bonds on the IGBT of the stressed modules. The white line under the wire bonds illustrates the length of the bonded part of the wire.

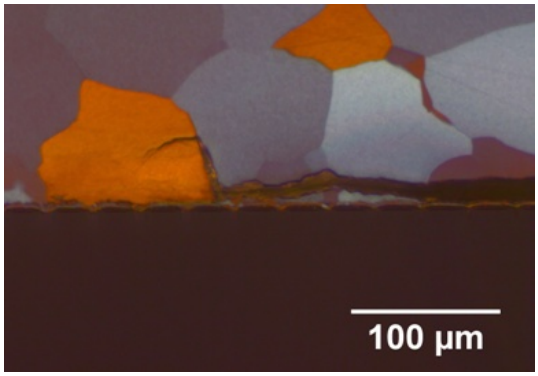
Magnifications of wire bonds of the 3.5MC and 4.5MC modules of Fig. 5.34(c,d) shows that both delamination and crack growth occurs, see Fig. 5.35. For the 3.5MC module it is observed that the delamination ends in a crack that propagates between two grains in the Al, see Fig. 5.35(a). However, the formation of a crack does not stop the delamination further inside the wire bond. In Fig. 5.35(b) the delamination in a wire bond of the 4.5MC module shows the refinement area is still bonded to the metallization, but only for a few grains. This is because the general size of the grains are very large also in the small refinement area, see findings in [17]. At the other side of this bond there is a crack propagating initially between two grains but it terminates into a grain, see Fig. 5.35(c). As described in Sec. 2.7.2 it is expected that the cracks should propagate between grains. The effective stress decreases when moving away from the bonding interface. Thus, at some point the effective stress normal to the interface will be smaller than the fracture toughness and the crack stop propagating away from the interface. However, the fracture toughness of large grains is smaller than that of small grains. As the stress parallel to the interface is still present in the wire at some point the crack will again move parallel to the bonding interface.



(a) Wire bond B4 of S2 on the HS IGBT of the 3.5MC module.



(b) Wire bond B4 left side of S4 on the LS IGBT of the 4.5MC module.



(c) Wire bond B4 right side of S4 on the LS IGBT of the 4.5MC module.

Figure 5.35. Cracks and delamination of the wire bonds on the IGBT of the 3.5MC and 4.5MC module.

Discussion and Conclusion 6

The Danfoss P3 power modules were subjected to an accelerated test for a different number of power cycles. During the power cycling heat is generate in the module and a cyclic temperature change is experienced in the module, see Sec. 3.2. This causes stress in the interconnections which can eventually lead to failures. The state of the metallization is examined using SEM and FIB and the Al wires are investigated with four-point probing and micro-sectioning. The results obtained using these methods are discussed below.

The heat transfer in a structural simplified version of the power module has successfully been simulated in Sec. 3.2. It is found that T_j, T_{peak}, and T_m are higher for the diode compared to the IGBT during the accelerated test. Furthermore, it shows that a temperature distribution is present on the semiconductor chips, as presented in Fig. 3.5(b), where it is seen that the temperature is higher in the center compared to the edge. The variation in the temperature between the center and edge of the diode is 13°C and of the IGBT is 8°C. Metallization reconstruction found on the diodes and not the IGBT (see Sec. 5.1) could be caused by the higher temperature that the diodes experiences compared to the IGBT. Additionally, the temperature field accounts for the finding presented in Fig. 5.3 that diode center experience a higher degree of reconstruction compared to the edges. Furthermore, it is found that the degree of the reconstruction increases with increasing number of cycles the modules were stressed. Using FIB to cut into the metallization, it is observed that the structural growth results in cavities in the metallization, see Fig. 5.4. Some of these are on the size of the thickness of the metallization, causing the current density to increase locally. This results in additional stress at these locations.

Four-Point probing measurements were carried out on selected samples as described in Sec. 4.1. Initially, the voltage drop between the terminals was measured for both the diodes and the IGBT's, see Figs. 5.5 and 5.18. In order to narrow down the location of possible failures this measurement was split into two; one giving the voltage drop across the semiconductor chip (Figs. 5.11 and 5.23) and the other across the wires (Figs. 5.8 and 5.21). For the IGBT's only a small ΔR_{eff} is found which is attributed to general wear, see Figs. 5.20, 5.22, and 5.25. Particularly the measurement through the wires of the IGBT's effectively showed zero change in the effective resistance. Considering the measurement through the chip of the IGBT a significant ΔV_{CE} was observed for the HS IGBT on S4 of the 3.5MC module. For the diode small ΔR_{eff} is found when measuring through the diode and the wires of the diode, see Figs. 5.7, 5.10, and B.6, which is attributed to general wear. Furthermore, a

significant degradation is found through the wires in the HS diode on S1 and LS diode on S3 of the 3.5MC module. Considering the results presented in the aforementioned figures, it is found that a change in the power module can be located using four-point probing. Thus, initially a measurement between terminals can be used to locate which halves of the sections are significantly degraded. Afterwards, it can be specified whether it is the semiconductor chips or the wires that are degraded. In future work this could save of lot of time as the measurements can be focused.

The current distributions through the wires bonded to the semiconductor chips are presented in Figs. 5.12 and 5.26 for the diodes and IGBT's, respectively. It is found that the current distribution is dependent on the geometry of the wire bonds on the semiconductor chips. Thus, the wire bonds with a larger surface area of the chip available has a higher current. The resistance through the wire bonds are presented in Figs. 5.14 and 5.27 for the diodes and IGBT's, respectively. For the IGBT only a small increase in resistance in the wire bonds is found in the stressed modules compared to a new module. This is attributed to general wear. However, for the diode Fig. 5.15 clearly shows a significant increase in the resistance of wires 2-8 on the HS of S1 of the 3.5MC module and of wires 8-10 on the LS of S3 of the 3.5MC module. This is in correlation with the initial observations presented in Sec. 5.1, that those wires are observed to be lifted off. Furthermore, it is evident that only the wires observed to have both bonds lifted off show this significant increase in resistance. Thus, four-point probing can be used to determine wire lift-off of individual wires. Disregarding the HS diode of S1 and the LS diode of S3 of the 3.5MC module, it is found that the HS diode only show a small increase in the resistance through the wire bonds relative to a new module, which is attributed to general wear, see Fig. 5.15(c). Still, the LS diodes show a large increase in the resistance through the wire bonds. Thus, the wire bonds on the LS diodes are highly degraded. It is found that the wires placed in the center of the LS diode are more degraded compared to those at the edge as evident from Fig. 5.15(d). This is in correlation with the temperature field found on the semiconductor chips in the heat transfer simulation. The fact that the degradation is found in the wire bonds on the diode and not the IGBT is presumably caused by the higher T_j, T_{peak}, and T_m of the diode compared to the IGBT, which will cause additional stress on the diodes. However, as the four-point probing results shows a difference between the HS and LS diode, this reveals that this difference is not included in the simulation, probably due to the simplification of the structure.

The significant degradations found for the 3.5MC module could be caused by a production fault in just one wire bond on the HS diode of S1 and the LS diode of S3. It is assumed that the fault will cause a wire to fail early which will increase the resistance in this wire bond and thereby increase the current through the neighboring wires, thus increasing the stress. The extra generated heat will then transfer in the module due to the temperature difference to the rest of the module. This might cause the degradation found in S4 of the HS IGBT as this IGBT is located next to the LS diode of S3, see Fig. 2.14. However, the HS IGBT of S3 is in closer thermal contact with the LS diode of S3 and here no significant degradation is found. Thus, it is suspected that there is a production fault in the HS IGBT of S4 or perhaps in its solder.

In Sec. 5.3 the bond wire interfaces were examined using micro-sectioning. In Figs. 5.30 and

5.31 cross-sectional images of interfaces from a new module is presented. The grain diameter is estimated to be in the range of 100-250μm in the wire and in the range of 25-50μm in the refinement area. As described in Sec. 2.7.2 the large grain size indicates that the fracture strength of the grains in the wire is weak. This is confirmed in Fig. 5.35 showing a crack propagating inside a grain. Delamination is found in both diodes and IGBT's in the stressed modules and in the IGBT's cracks are observed to propagate in the wires. For the IGBT's it is found that there is a higher degree of delamination of the wires with increasing number of cycles the modules were stressed, see Fig. 5.34. On the diodes it was difficult to reach an interface where the wire was still bonded. This indicates that the bonding areas of the diodes are small. Furthermore, this is supported by the fact that the wires on the diodes were found to lift-off easily during the sample preparation. However, if the wire bonds of the diode were weakened considerably before the disassembling, it is speculated that the mechanical module disassembly and dissolving of the silicone gel has actually contributed to the wire lift-off.

From the results of the heat transfer simulation, initial observations, four-point probing, and micro-sectioning it is concluded that with the load provided by the accelerated test (see Sec. 2.5) the wire bonds on the LS diodes are most probable to fail first. This is presumably caused by the high temperature and temperature fluctuations in the this part of the power module. To continue this work it would be interesting to investigate the module further, e.g. the metallization and solder. Additional examinations of the metallization could be carried out. A useful supplement to SEM and FIB would be to use the four-point probing technique to map the degradation in the metallization. In order to do this, it is necessary to modify the setup. Loading additional samples with the conditions of the accelerated test would give a better statistical basis of the results. Furthermore, changing the loading conditions e.g. the frequencies f_{out} and f_{sw} would perhaps affect the degradation of the module, which would be interesting to study.

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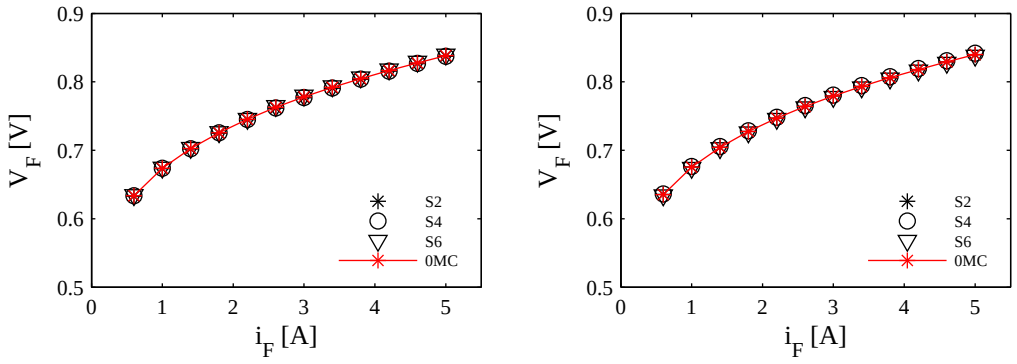
Four-Point Probing References

A

The four-point probing reference measurements are presented in the following chapter.

A.1 Diode

The voltage drop across diode of a new module measured from terminal to terminal is presented in Fig. A.1.

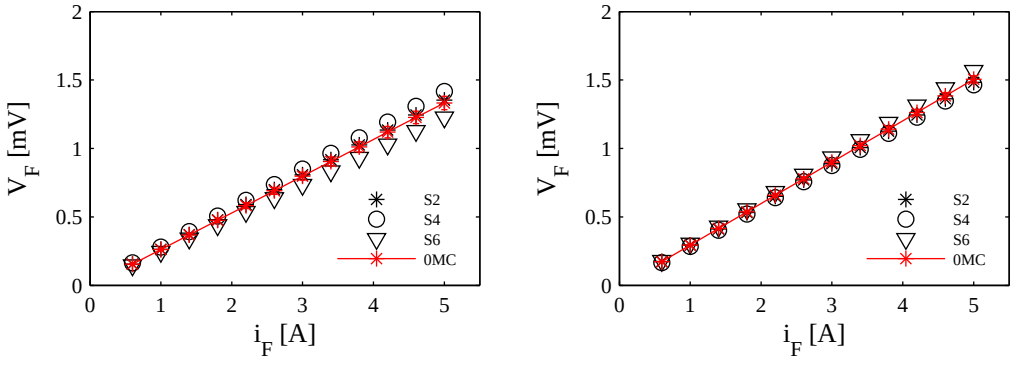


(a) HS diode.

(b) LS diode.

Figure A.1. The voltage drop across the diode as a function of forward current measured from terminal to terminal for both HS and LS of the sections of the new module.

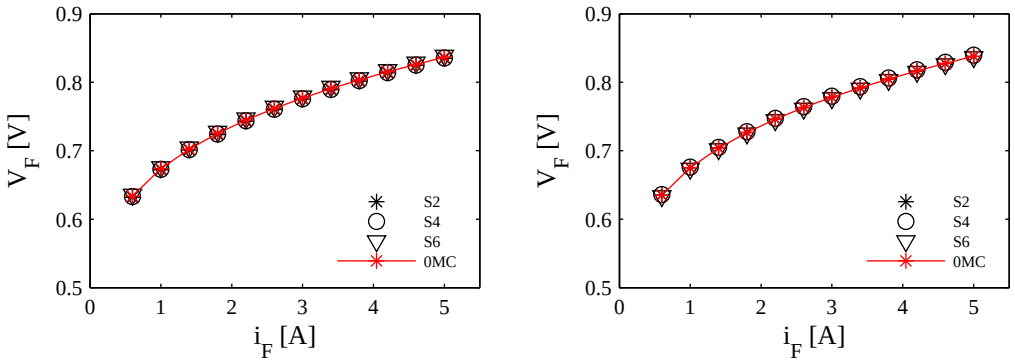
The voltage drop across wires of the diode of a new module measured from terminal to chip surface C2 is presented in Fig. A.2. The variation in these measurements originates from the difficulty in placing the probes at the exact same position of the chip surface. As the metallization is a thin layer a small change in probe position will cause a noticeable difference in the measured voltage drop.



(a) HS diode. (b) LS diode.

Figure A.2. The voltage drop across the wires of the diode as a function of forward current measured from terminal to chip surface C2 for both HS and LS of the sections of the new module.

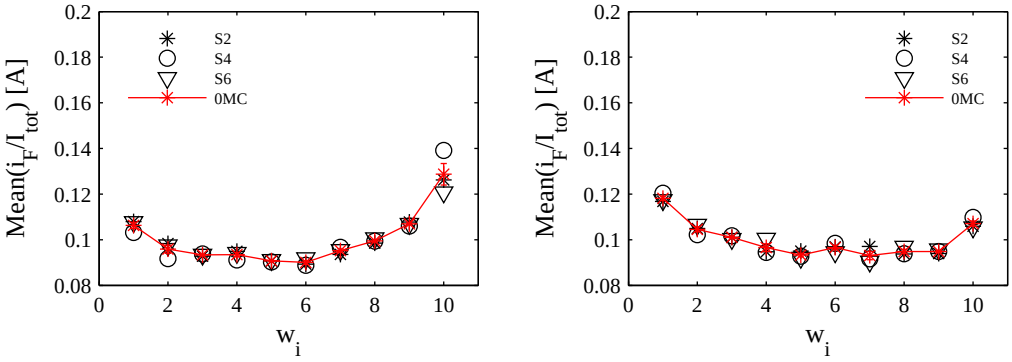
The voltage drop across the diode chip of a new module measured from terminal to chip surface C2 is presented in Fig. A.3.



(a) HS diode. (b) LS diode.

Figure A.3. The voltage drop across the diode chip as a function of forward current measured from terminal to chip surface C2 for both HS and LS of the sections of the new module.

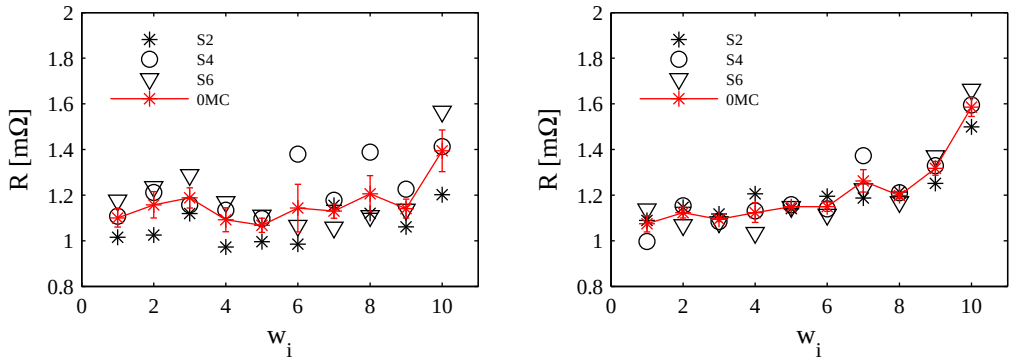
The current distribution of the wires of the diode of a new module is presented in Fig. A.4.



(a) HS diode. (b) LS diode.

Figure A.4. The current distribution of the wires of the diode measured for both HS and LS of the sections of the new module.

The resistance through of the wire of the diode of a new module is presented in Fig. A.5. The large resistance of wire 10 originates from the placement of the measuring probes. When measuring for wire 1-9 the needle on the chip surface is placed in between two wires whereas for wire 10 it is not.

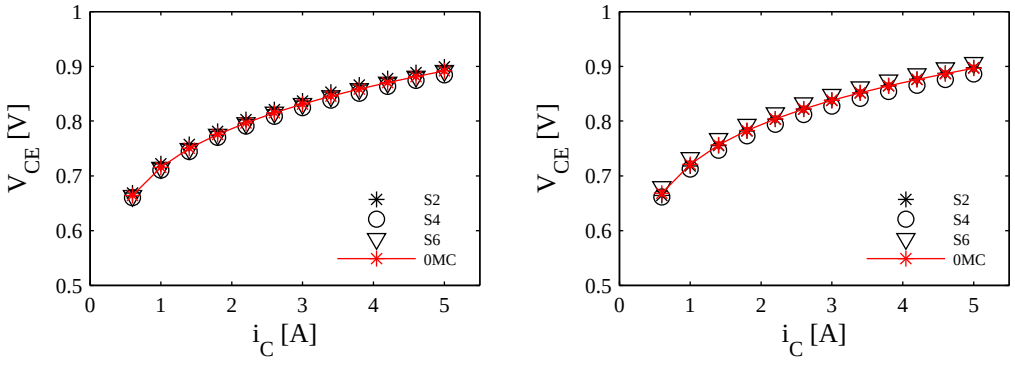


(a) HS diode. (b) LS diode.

Figure A.5. The resistance through the wire bonds of the diode measured for both HS and LS of the sections of the new module.

A.2 IGBT

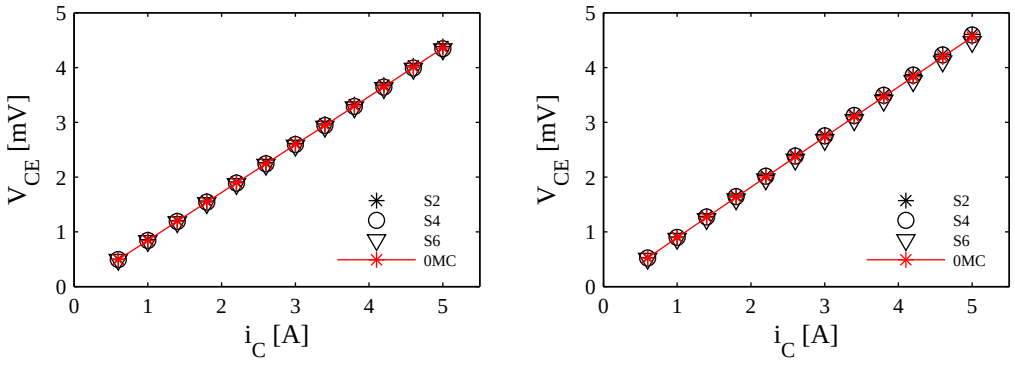
The voltage drop across the IGBT of a new module measured from terminal to terminal is presented in Fig. A.6.



(a) HS IGBT. (b) LS IGBT.

Figure A.6. The voltage drop across the IGBT as a function of collector current measured from terminal to terminal for both HS and LS of the sections of the new module.

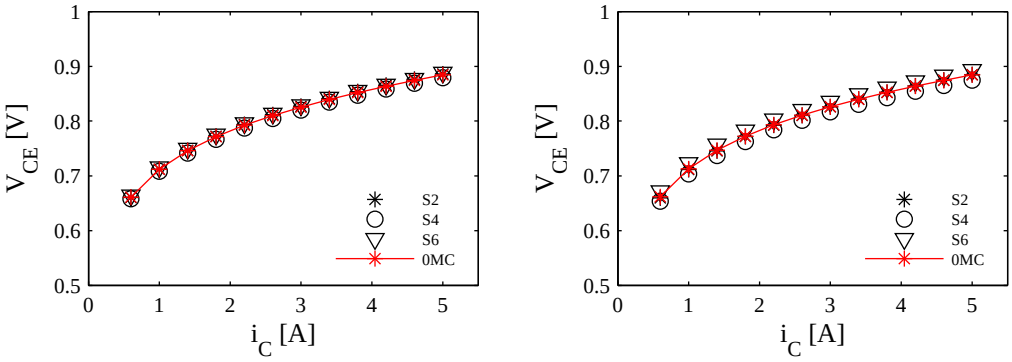
The voltage drop across wires of the IGBT of a new module measured from terminal to chip surface C2 is presented in Fig. A.7.



(a) HS IGBT. (b) LS IGBT.

Figure A.7. The voltage drop across the wires of the IGBT as a function of collector current measured from terminal to chip surface C2 for both HS and LS of the sections of the new module.

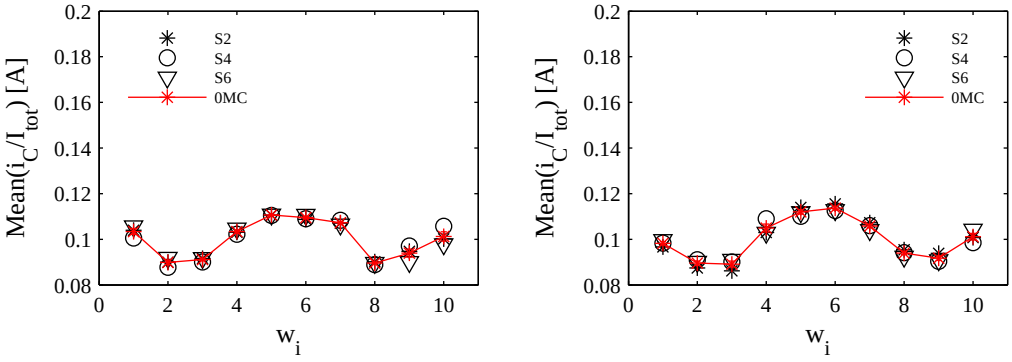
The voltage drop across the IGBT chip of a new module measured from terminal to chip surface C2 is presented in Fig. A.8.



(a) HS IGBT. (b) LS IGBT.

Figure A.8. The voltage drop across the IGBT chip as a function of collector current measured from terminal to chip surface C2 for both HS and LS of the sections of the new module.

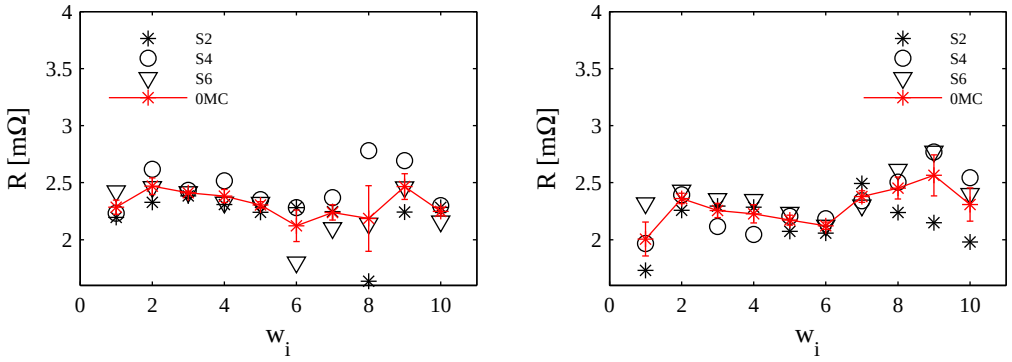
The current distribution of the wires of the IGBT of a new module is presented in Fig. A.9.



(a) HS IGBT. (b) LS IGBT.

Figure A.9. The current distribution of the wires of the IGBT measured for both HS and LS of the sections of the new module.

The resistance through of the wire of the IGBT of a new module is presented in Fig. A.10. The difference in the measurements from the individual sections come from the difficulty in placing the probe at the surface of the chip in the same distance from the wire bond at each measurement.



(a) HS IGBT. (b) LS IGBT.

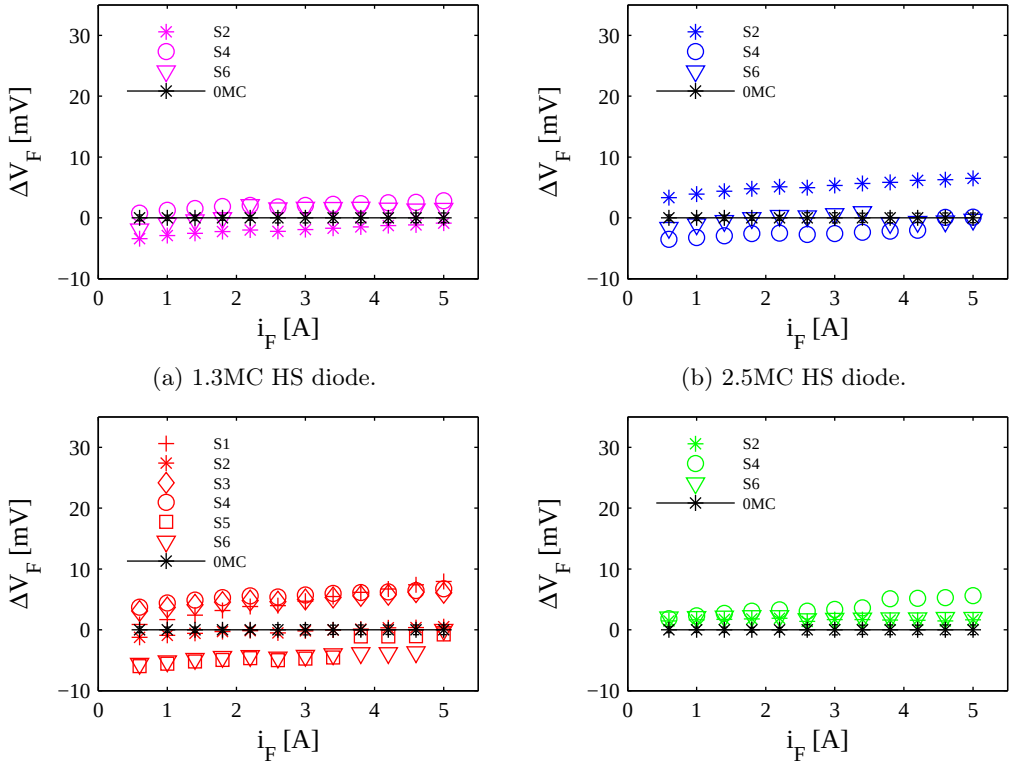
Figure A.10. The resistance through the wire bonds of the IGBT measured for both HS and LS of the sections of the new module.

Four-Point Probing Results B

In the following the results from the four-point probing which are not included in Sec. 5.2 are presented.

B.1 Section - Diode

The voltage drop across the diode is measured from terminal to terminal. The average of the new module is subtracted from the stressed modules which is plotted in Fig. B.1 for the individual sections.



(a) 1.3MC HS diode.

(b) 2.5MC HS diode.

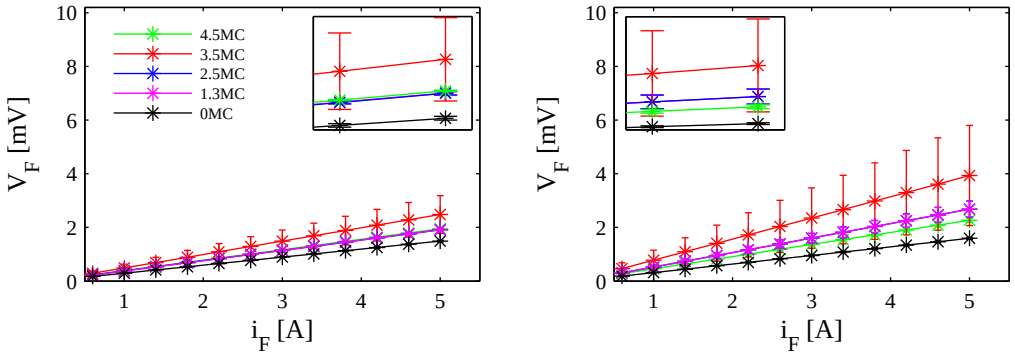
(c) 3.5MC HS diode.

(d) 4.5MC HS diode.

Figure B.1. The relative difference in voltage drop across the diode as a function of forward current measured from terminal to terminal for HS of the individual sections.

B.2 Chip Surface - Diode

The voltage drop through the wires from the chip surface of the diode at C1 to the terminal is plotted in Fig. B.2.

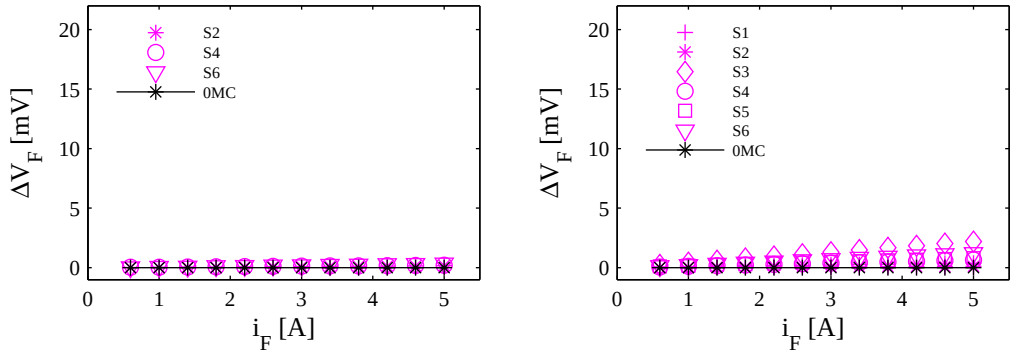


(a) C1 HS diode.

(b) C1 LS diode.

Figure B.2. The voltage drop through the wires as a function of forward current measured from the chip surface of the diode at C1 to the terminal for both HS and LS of the sections. The small figures inside are a zoom of the last two measurements.

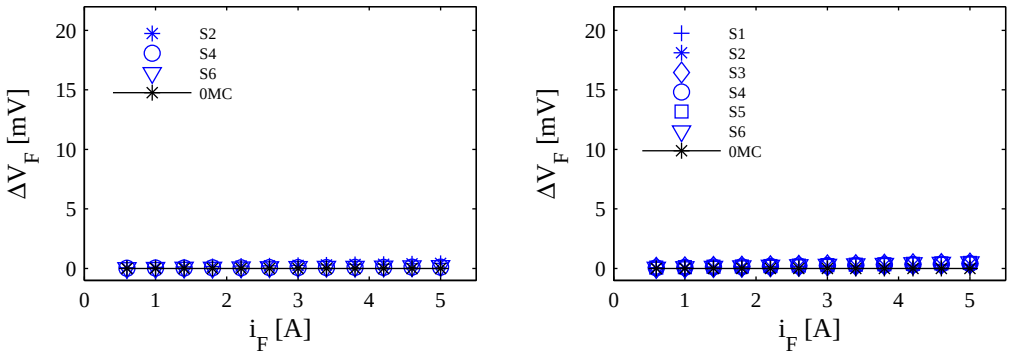
The voltage drop through the wires from the chip surface of the diode at C2 to the terminal is plotted in Fig. B.3 for the individual sections.



(a) 1.3MC HS diode.

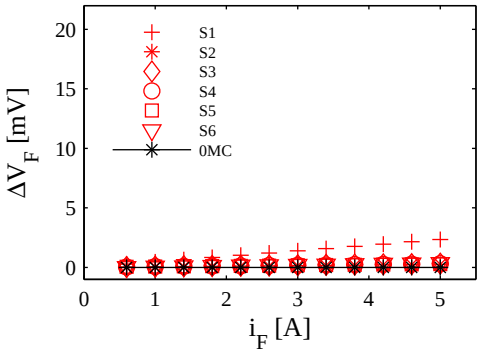
(b) 1.3MC LS diode.

Figure B.3. The voltage drop through the wires as a function of forward current measured from the chip surface of the diode at C2 to the terminal for both HS and LS of the individual sections.

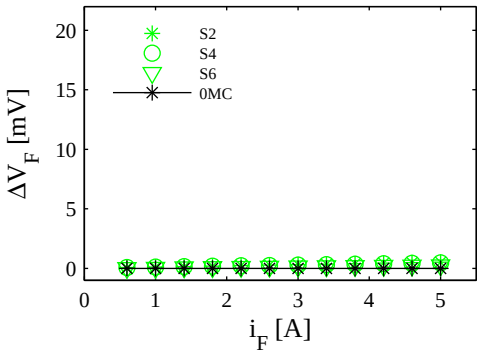


(c) 2.5MC HS diode.

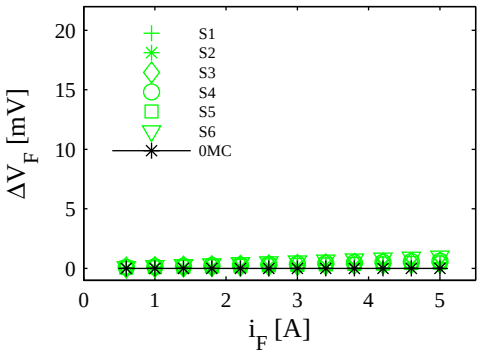
(d) 2.5MC LS diode.



(e) 3.5MC HS diode.



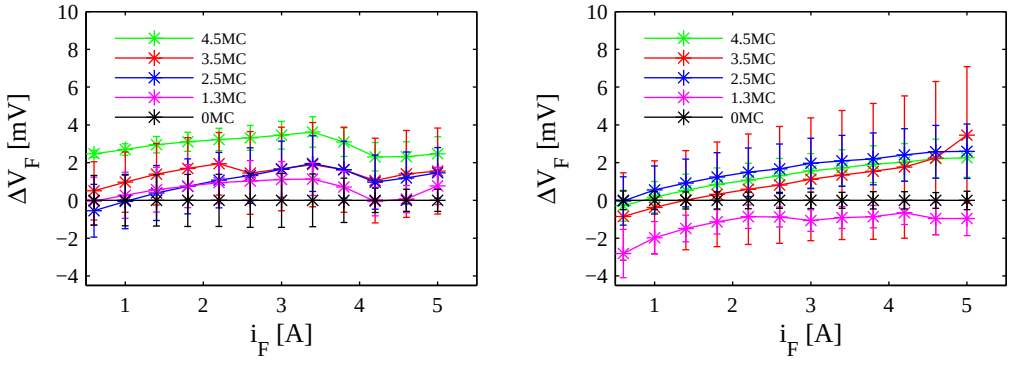
(f) 4.5MC HS diode.



(g) 4.5MC LS diode.

Figure B.3. The voltage drop through the wires as a function of forward current measured from the chip surface of the diode at C2 to the terminal for both HS and LS of the individual sections.

The relative voltage drop through the diode from the chip surface of the diode at C1 to the terminal is plotted in Fig. B.4.

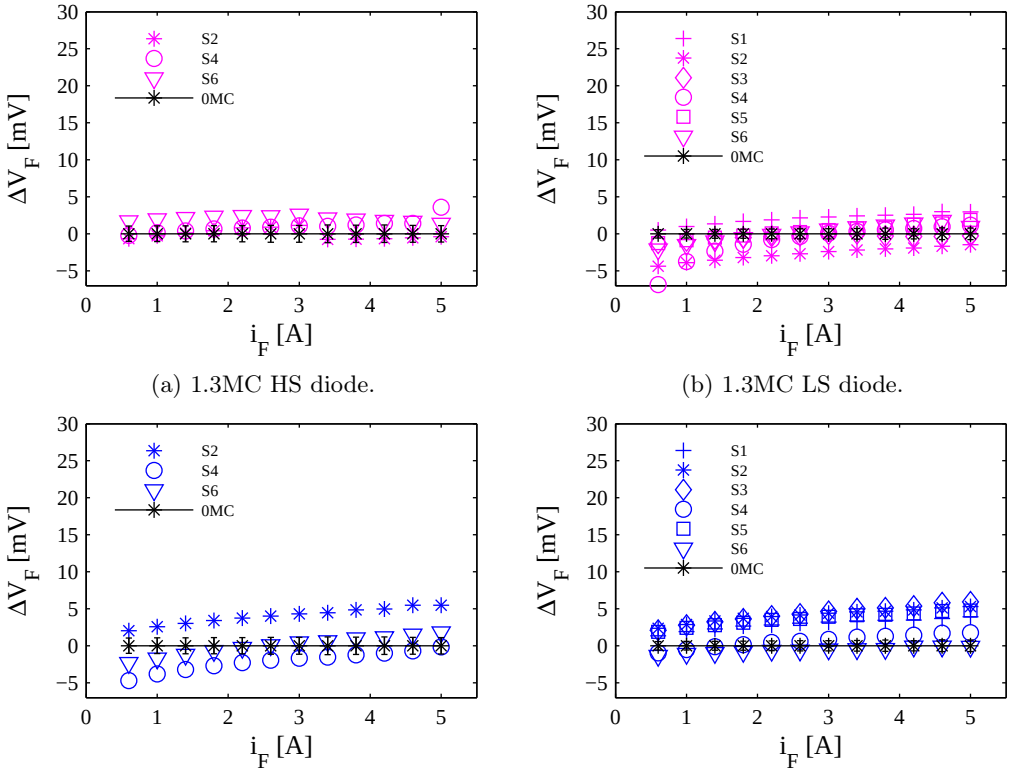


(a) C1 HS diode.

(b) C1 LS diode.

Figure B.4. The relative difference in voltage drop through the diode as a function of forward current measured from the chip surface of the diode at C1 to the terminal for both HS and LS of the sections.

The voltage drop through the diode from the chip surface of the diode at C2 to the terminal is plotted in Fig. B.5 for the individual sections.



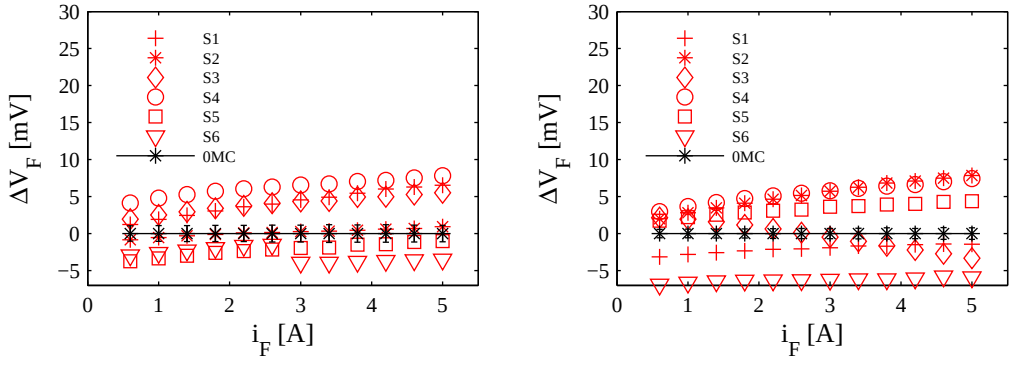
(a) 1.3MC HS diode.

(b) 1.3MC LS diode.

(c) 2.5MC HS diode.

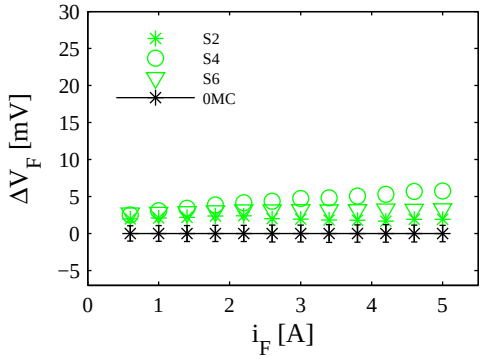
(d) 2.5MC LS diode.

Figure B.5. The voltage drop through the diodes as a function of forward current measured from the chip surface of the diode at C2 to the terminal for both HS and LS of the individual sections.

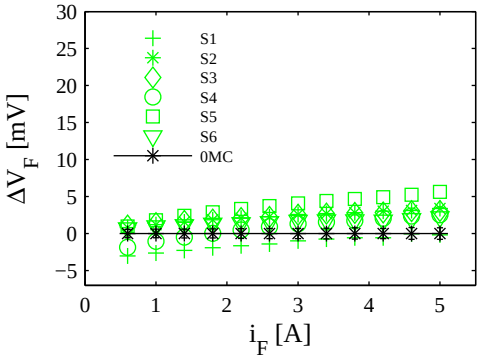


(e) 3.5MC HS diode.

(f) 3.5MC LS diode.



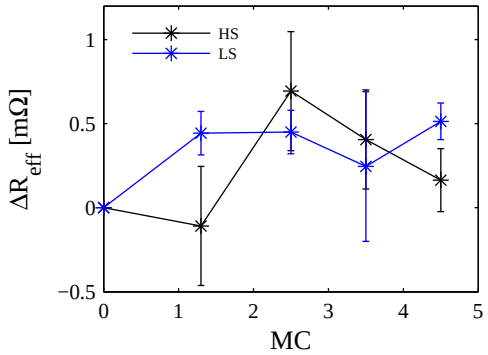
(g) 4.5MC HS diode.



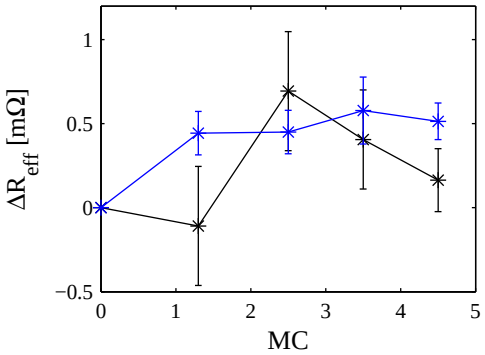
(h) 4.5MC LS diode.

Figure B.5. The voltage drop through the diodes as a function of forward current measured from the chip surface of the diode at C2 to the terminal for both HS and LS of the individual sections.

A measure of the degradation through the diode is plotted in Fig. B.6.



(a) Hard degradation.

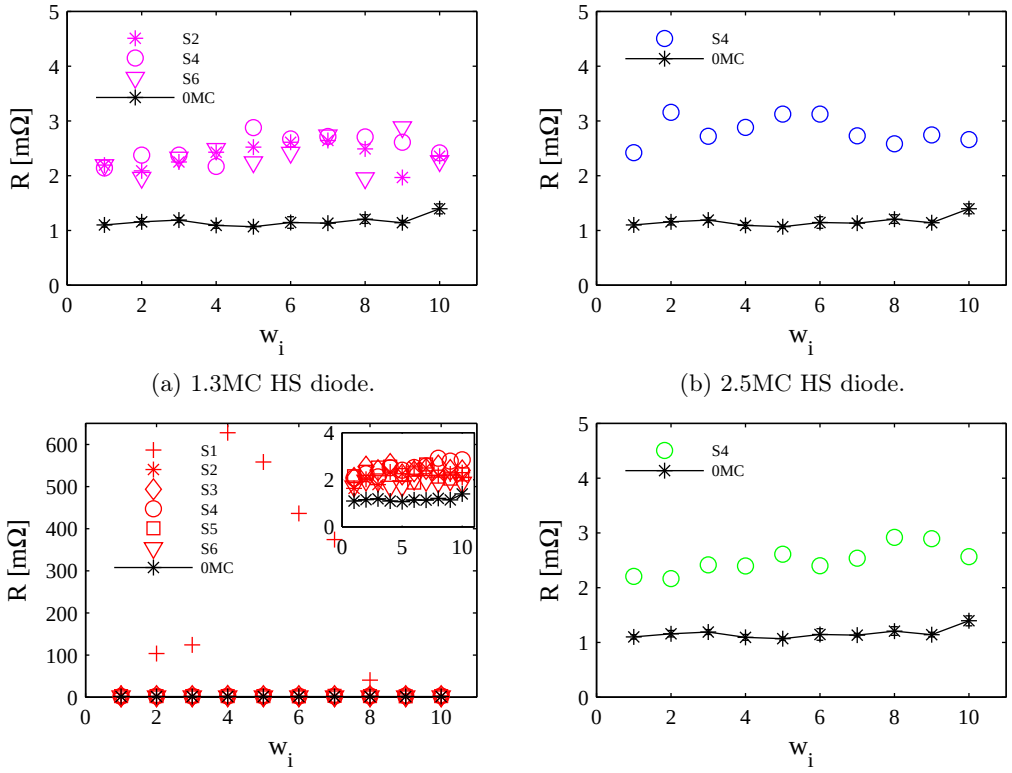


(b) Soft degradation.

Figure B.6. Hard and soft degradation through the chip of the diode.

B.3 Wires - Diode

The resistance through the wire bonds on the diode for the individual sections is plotted in Fig. B.7.



(a) 1.3MC HS diode.

(b) 2.5MC HS diode.

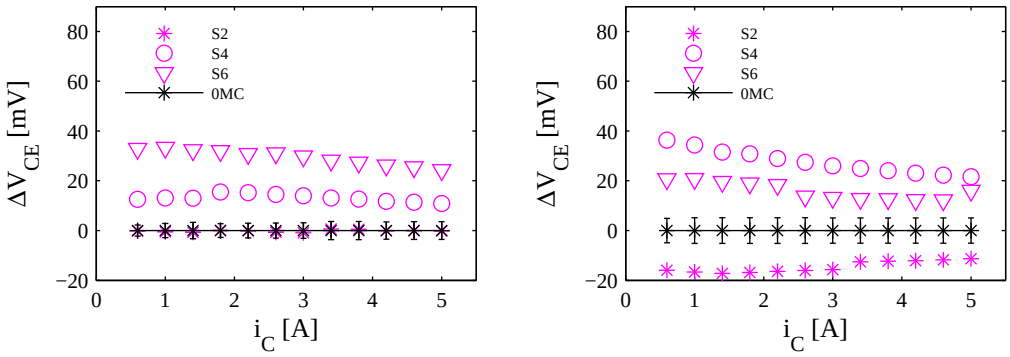
(c) 3.5MC HS diode.

(d) 4.5MC HS diode.

Figure B.7. The resistance through the wire bonds on the diode measured from the chip surface to the wire curve for the individual sections of the 1.3MC, 2.5MC, 3.5MC, and 4.5MC modules.

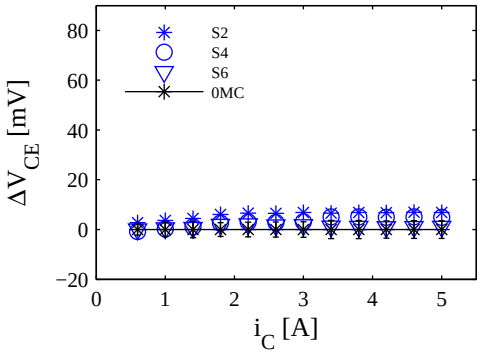
B.4 Section - IGBT

The voltage drop across the IGBT is measured from terminal to terminal. The average of the new module is subtracted from the stressed modules which is plotted in Fig. B.8 for the individual sections.

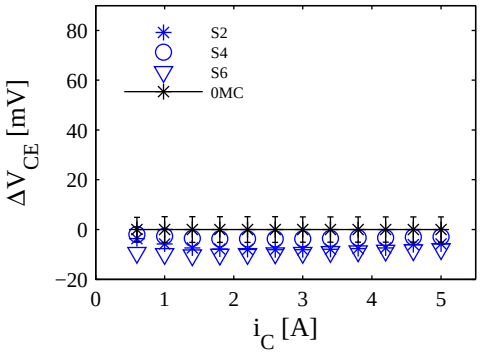


(a) 1.3MC HS IGBT.

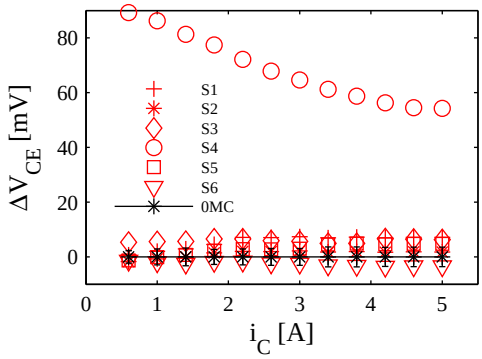
(b) 1.3MC LS IGBT.



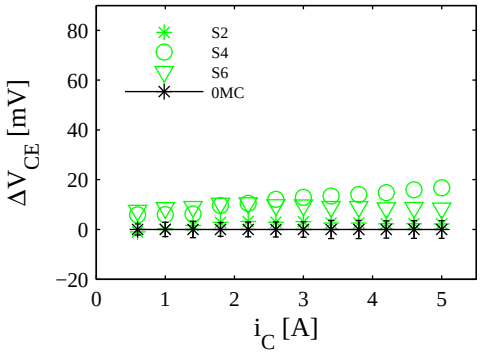
(c) 2.5MC HS IGBT.



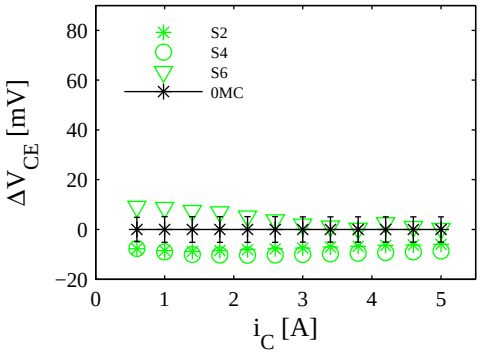
(d) 2.5MC LS IGBT.



(e) 3.5MC HS IGBT.



(f) 4.5MC HS IGBT.

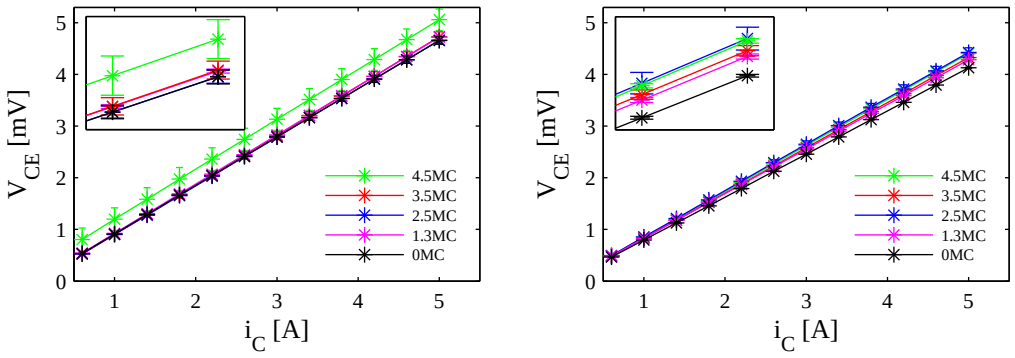


(g) 4.5MC LS IGBT.

Figure B.8. The relative difference in voltage drop across the IGBT as a function of collector current measured from terminal to terminal for both HS and LS of the individual sections.

B.5 Chip Surface - IGBT

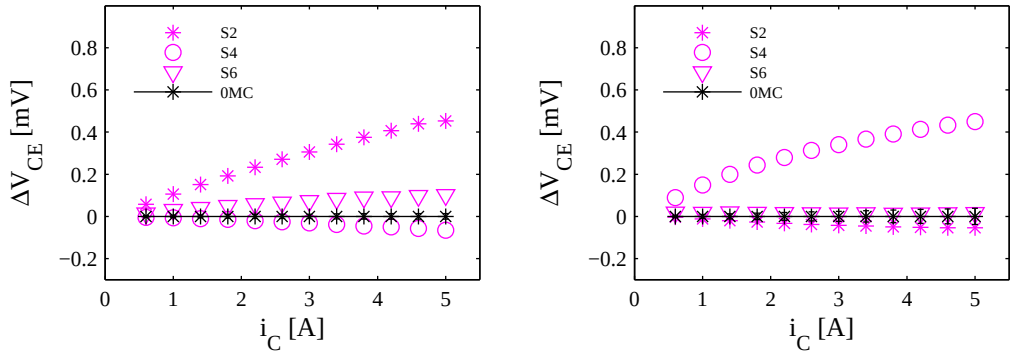
The voltage drop through the wires from the chip surface of the IGBT at C1 to the terminal is plotted in Fig. B.9.



(a) C1 HS IGBT. (b) C1 LS IGBT.

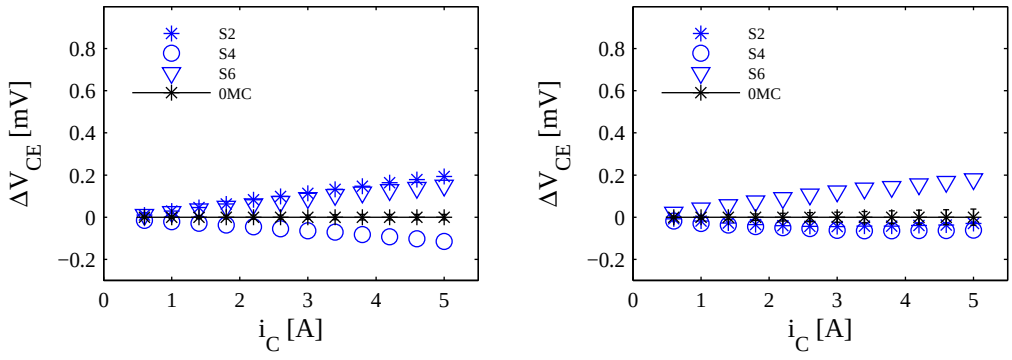
Figure B.9. The voltage drop through the wires as a function of collector current measured from the chip surface of the IGBT at C1 to the terminal for both HS and LS of the sections. The small figures inside are a zoom of the last two measurements.

The voltage drop through the wires from the chip surface of the IGBT at C2 to the terminal is plotted in Fig. B.10 for the individual sections.



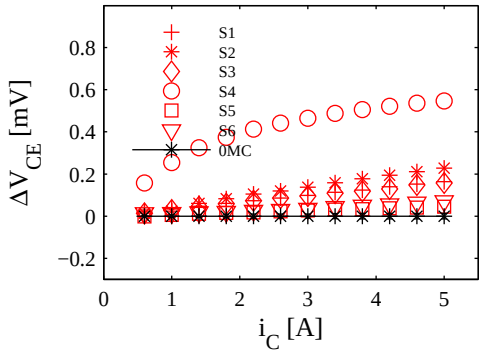
(a) 1.3MC HS IGBT. (b) 1.3MC LS IGBT.

Figure B.10. The voltage drop through the wires as a function of collector current measured from the chip surface of the IGBT at C2 to the terminal for both HS and LS of the individual sections.

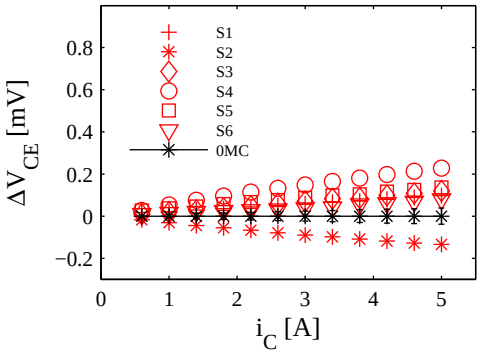


(c) 2.5MC HS IGBT.

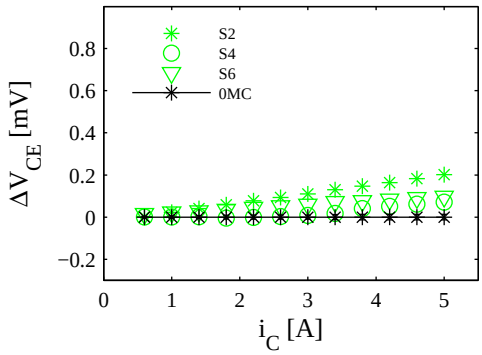
(d) 2.5MC LS IGBT.



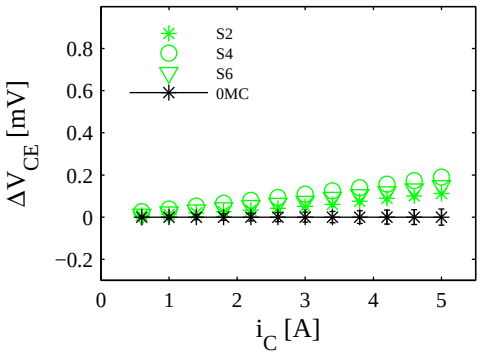
(e) 3.5MC HS IGBT.



(f) 3.5MC LS IGBT.



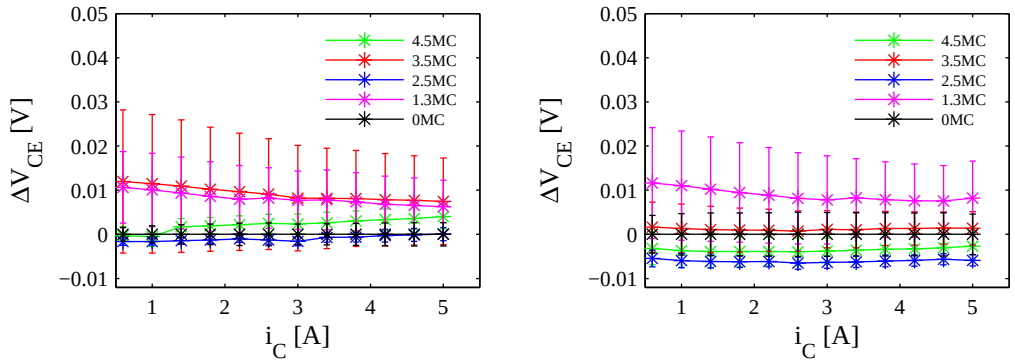
(g) 4.5MC HS IGBT.



(h) 4.5MC LS IGBT.

Figure B.10. The voltage drop through the wires as a function of collector current measured from the chip surface of the IGBT at C2 to the terminal for both HS and LS of the individual sections.

The relative voltage drop through the IGBT from the chip surface of the IGBT at C1 to the terminal is plotted in Fig. B.11.

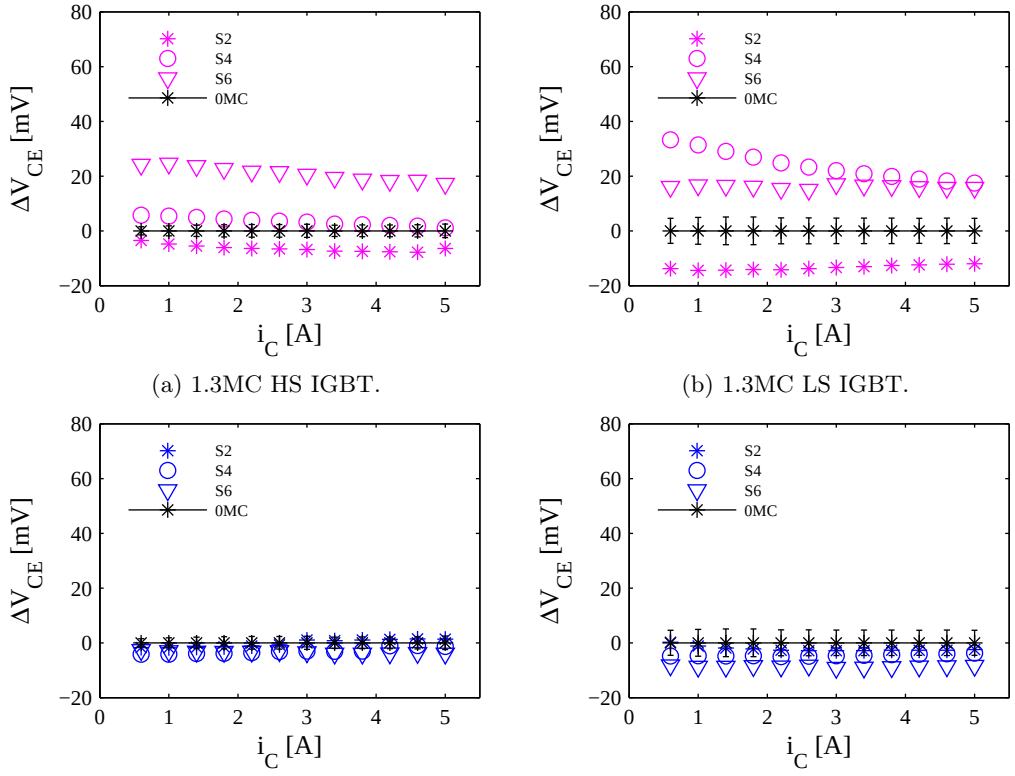


(a) C1 HS IGBT.

(b) C1 LS IGBT.

Figure B.11. The relative difference in voltage drop through the IGBT as a function of collector current measured from the chip surface of the IGBT at C1 to the terminal for both HS and LS of the sections.

The voltage drop through the IGBT from the chip surface of the IGBT at C2 to the terminal is plotted in Fig. B.12 for the individual sections.



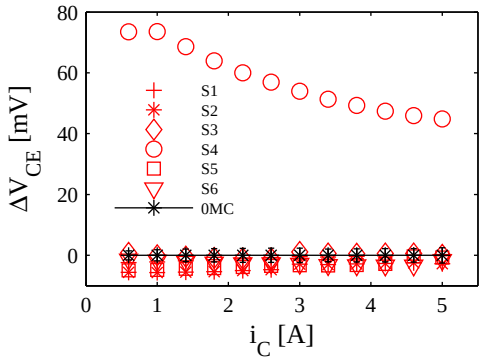
(a) 1.3MC HS IGBT.

(b) 1.3MC LS IGBT.

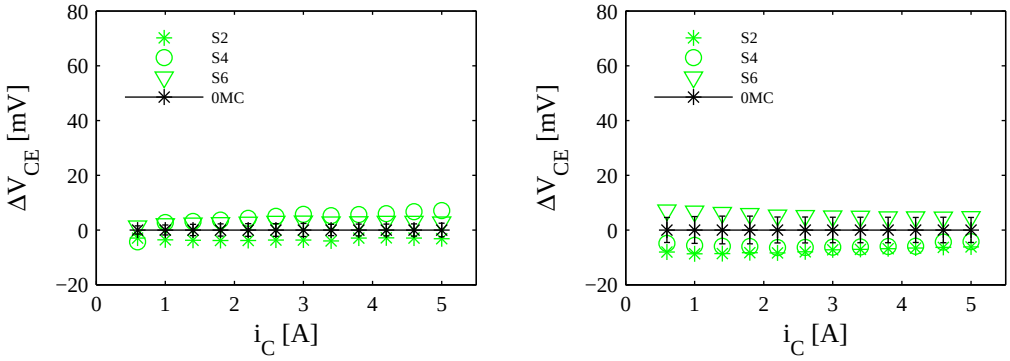
(c) 2.5MC HS IGBT.

(d) 2.5MC LS IGBT.

Figure B.12. The relative difference in voltage drop through the IGBT as a function of collector current measured from the chip surface of the IGBT at C2 to the terminal for both HS and LS of the individual sections.



(e) 3.5MC HS IGBT.



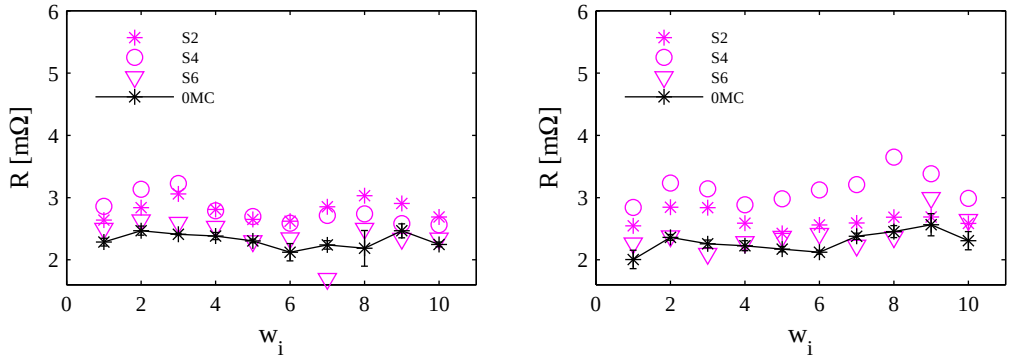
(f) 4.5MC HS IGBT.

(g) 4.5MC LS IGBT.

Figure B.12. The relative difference in voltage drop through the IGBT as a function of collector current measured from the chip surface of the IGBT at C2 to the terminal for both HS and LS of the individual sections.

B.6 Wires - IGBT

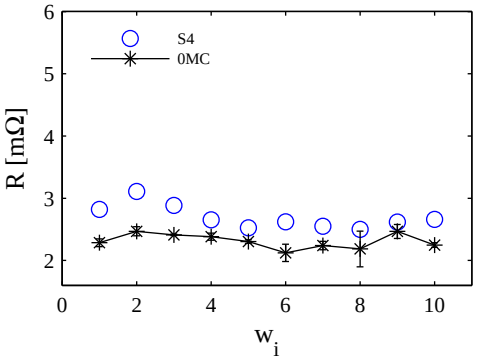
The resistance through the wire bonds on the IGBT for the individual sections is plotted in Fig. B.13.



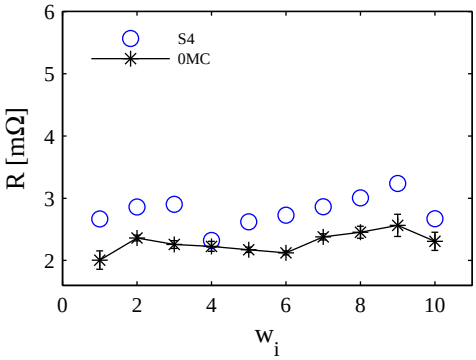
(a) 1.3MC HS IGBT.

(b) 1.3MC LS IGBT.

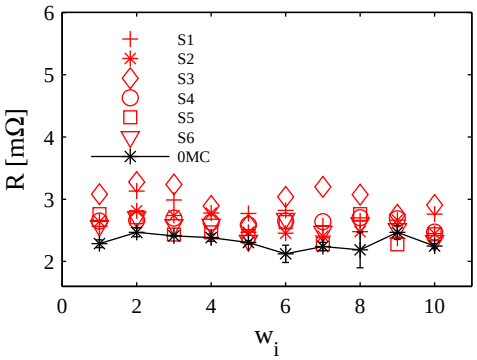
Figure B.13. The resistance through the wire bonds in the IGBT measured from the chip surface to the wire curve for the individual sections of the 1.3MC, 2.5MC, 3.5MC, and 4.5MC modules.



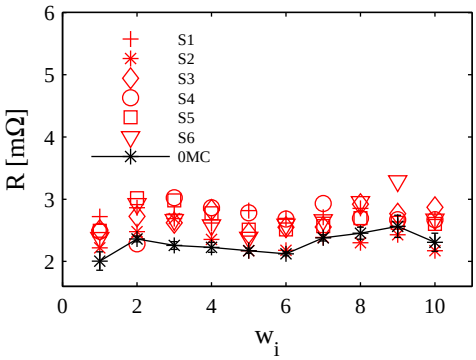
(c) 2.5MC HS IGBT.



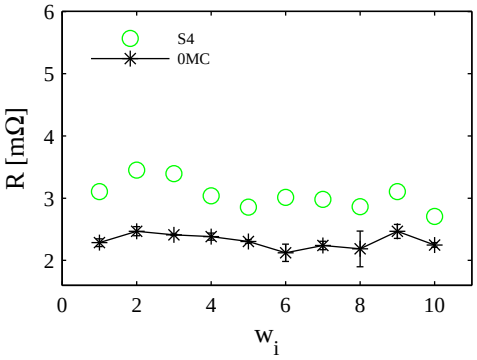
(d) 2.5MC LS IGBT.



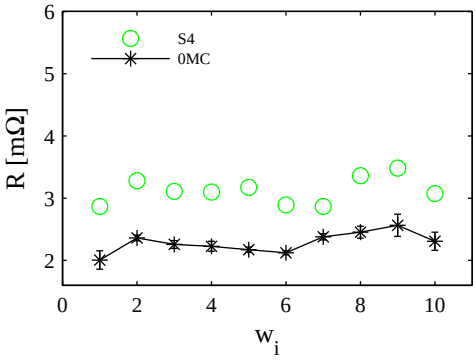
(e) 3.5MC HS IGBT.



(f) 3.5MC LS IGBT.



(g) 4.5MC HS IGBT.



(h) 4.5MC LS IGBT.

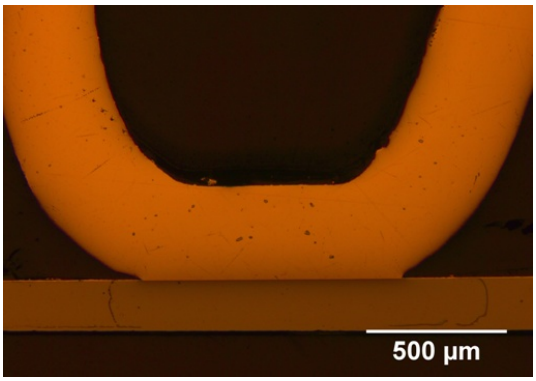
Figure B.13. The resistance through the wire bonds in the IGBT measured from the chip surface to the wire curve for the individual sections of the 1.3MC, 2.5MC, 3.5MC, and 4.5MC modules.

Micro-sectioning Results C

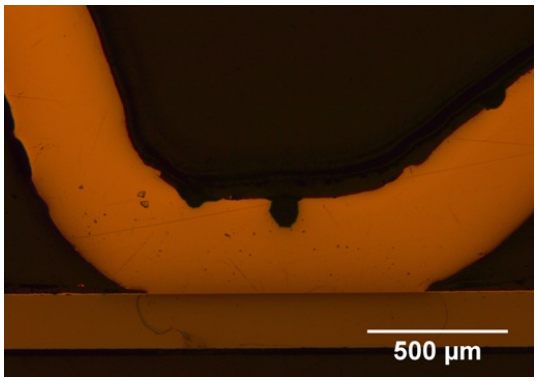
In the following the results from the micro-sectioning which are not included in Sec. 5.3 are presented.

C.1 New Module

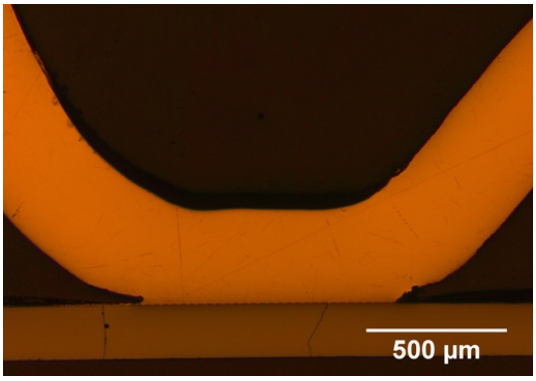
Additional images from the micro-sectioning results of the new module can be found in Fig. C.1.



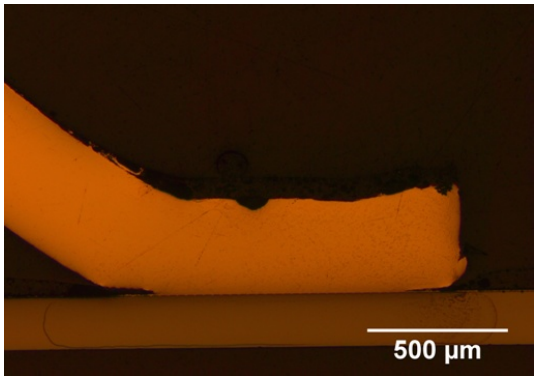
(a) Wire bond B1 of S2 on the HS diode.



(b) Wire bond B2 of S2 on the HS diode.



(c) Wire bond B3 of S2 on the HS IGBT.

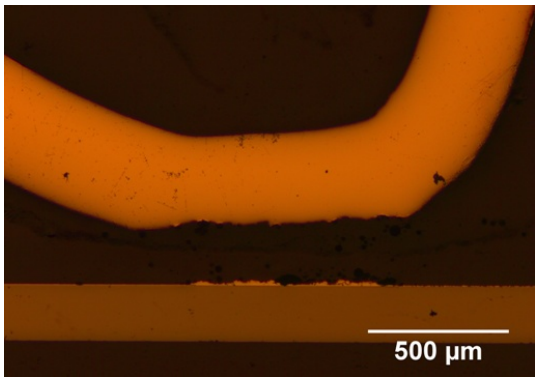


(d) Wire bond B4 of S2 on the HS IGBT.

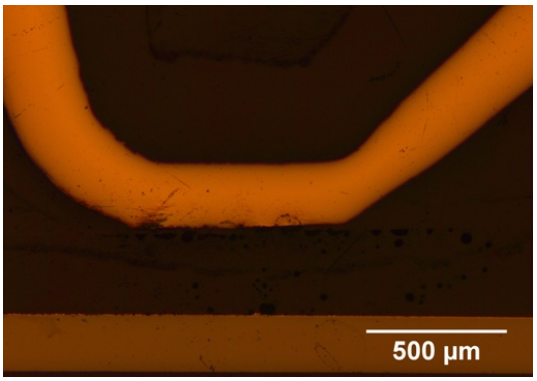
Figure C.1. Wire bonds of the HS diode and IGBT of the new module before etching.

C.2 1.3MC Module

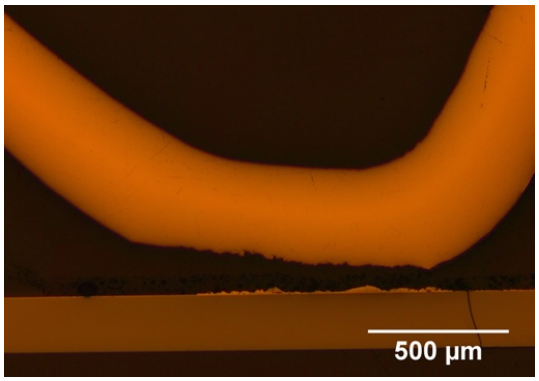
Additional images from the micro-sectioning results of the 1.3MC module can be found in Figs. C.2, C.3, and C.4.



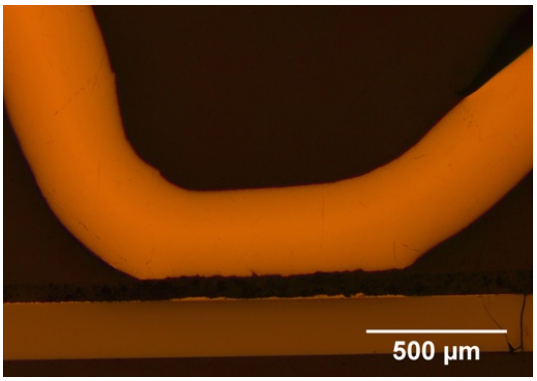
(a) Wire bond B1 of S4 on the HS diode.



(b) Wire bond B2 of S4 on the HS diode.

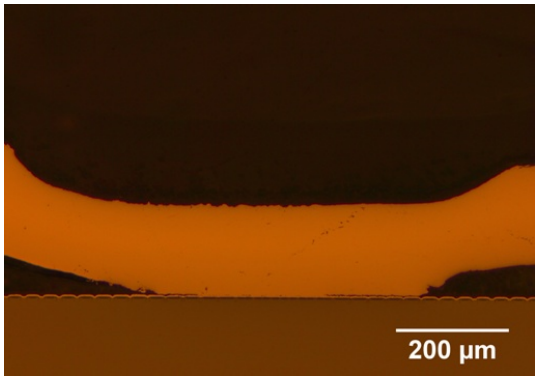


(c) Wire bond B1 of S4 on the LS diode.

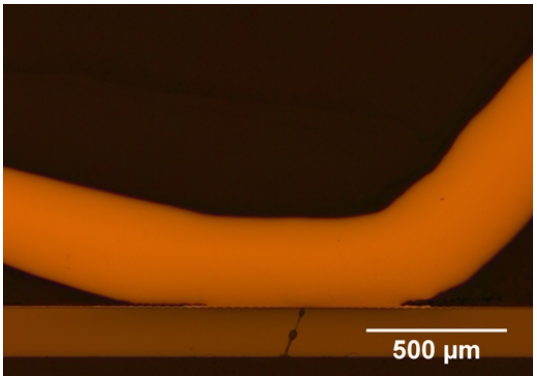


(d) Wire bond B2 of S4 on the LS diode.

Figure C.2. Wire bonds of the HS and LS diode of the 1.3MC module before etching.

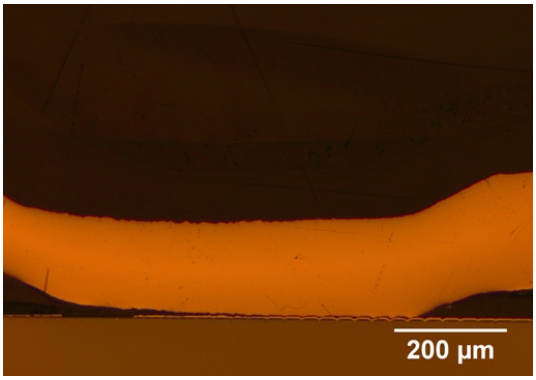


(a) Wire bond B3 of S4 on the HS IGBT.

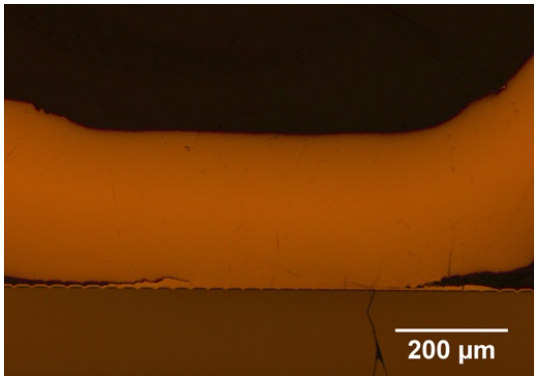


(b) Wire bond B4 of S4 on the HS IGBT.

Figure C.3. Wire bonds of the HS and LS IGBT of the 1.3MC module before etching.

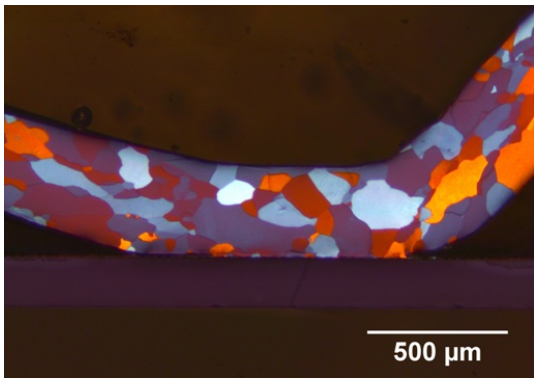


(c) Wire bond B3 of S4 on the LS IGBT.

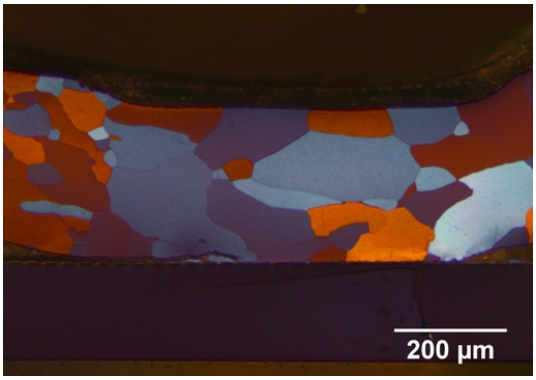


(d) Wire bond B4 of S4 on the LS IGBT.

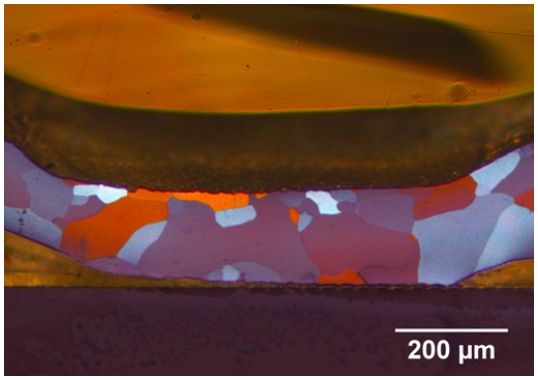
Figure C.3. Wire bonds of the HS and LS IGBT of the 1.3MC module before etching.



(a) Wire bond B3 of S4 on the HS IGBT.



(b) Wire bond B3 of S4 on the LS IGBT.

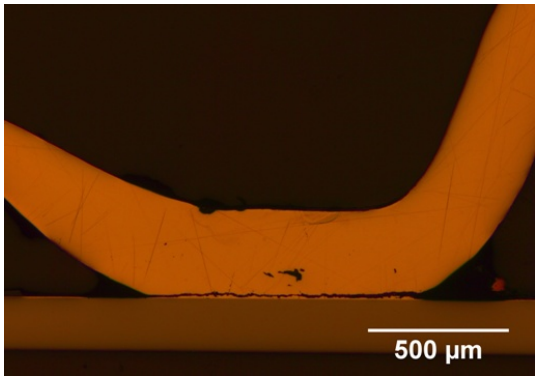


(c) Wire bond B4 of S4 on the LS IGBT.

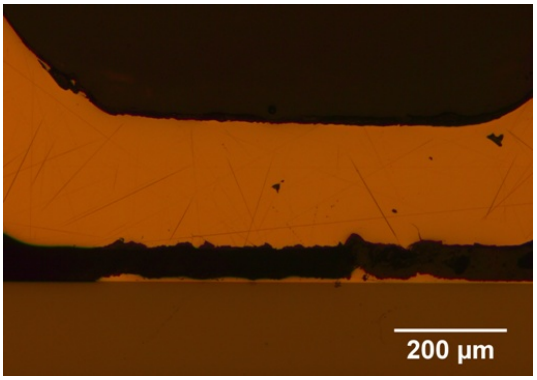
Figure C.4. Grains structure in the wire bonds of the HS and LS IGBT of the 1.3MC module.

C.3 2.5MC Module

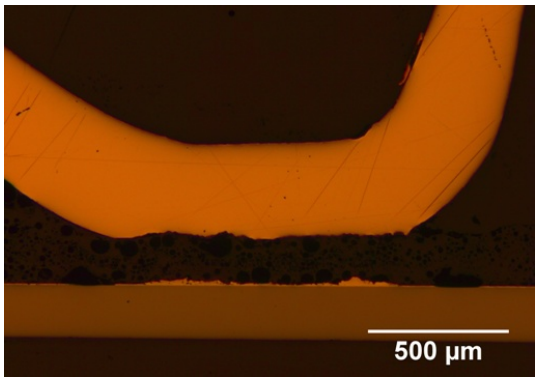
Additional images from the micro-sectioning results of the 2.5MC module can be found in Figs. C.5, C.6, and C.7.



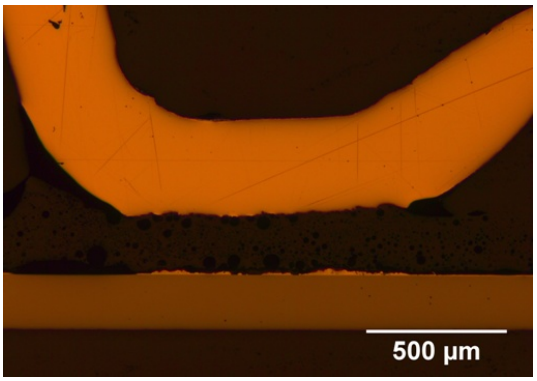
(a) Wire bond B1 of S2 on the HS diode.



(b) Wire bond B2 of S2 on the HS diode.

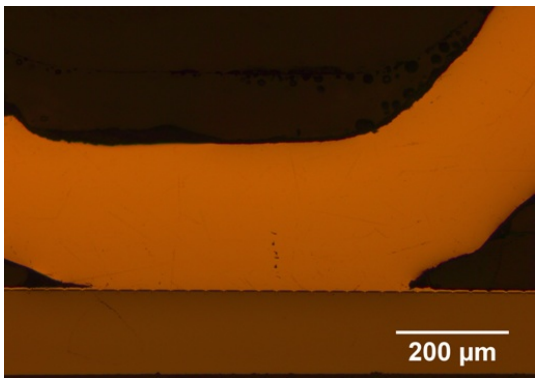


(c) Wire bond B1 of S2 on the LS diode.

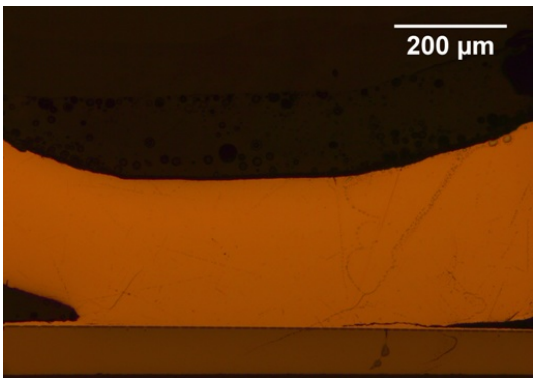


(d) Wire bond B2 of S2 on the LS diode.

Figure C.5. Wire bonds of the HS and LS diode of the 2.5MC module before etching.

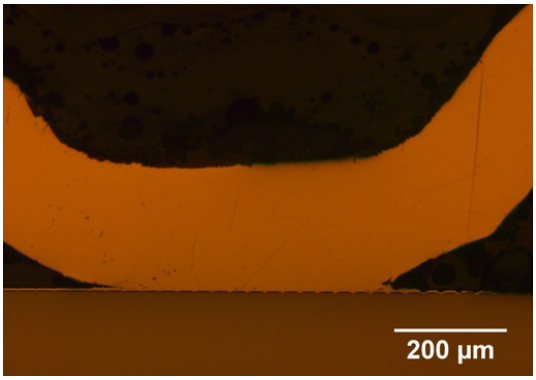


(a) Wire bond B3 of S4 on the HS IGBT.

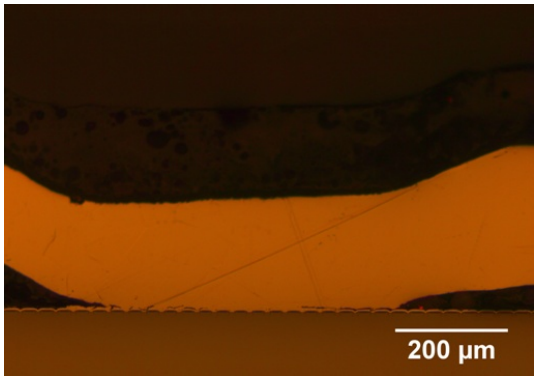


(b) Wire bond B4 of S4 on the HS IGBT.

Figure C.6. Wire bonds of the HS and LS IGBT of the 2.5MC module before etching.

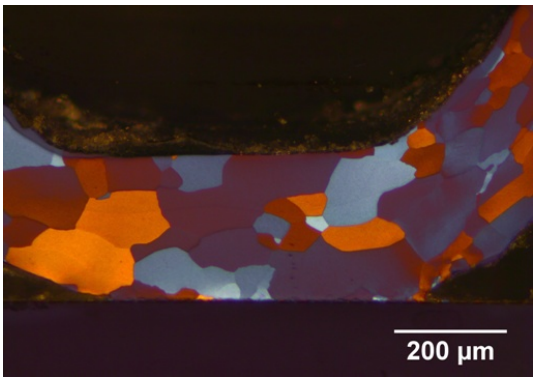


(c) Wire bond B3 of S4 on the LS IGBT.

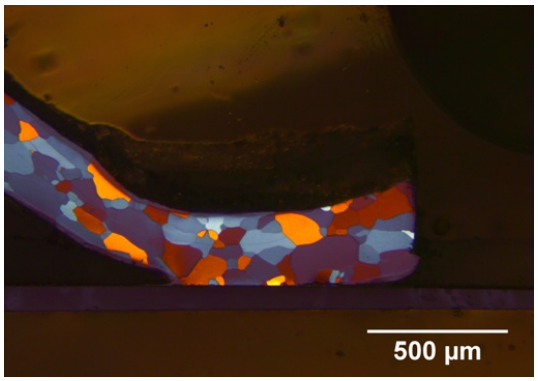


(d) Wire bond B4 of S4 on the LS IGBT.

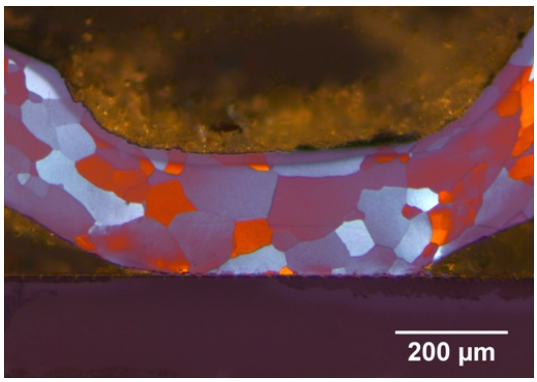
Figure C.6. Wire bonds of the HS and LS IGBT of the 2.5MC module before etching.



(a) Wire bond B3 of S4 on the HS IGBT.



(b) Wire bond B4 of S4 on the HS IGBT.

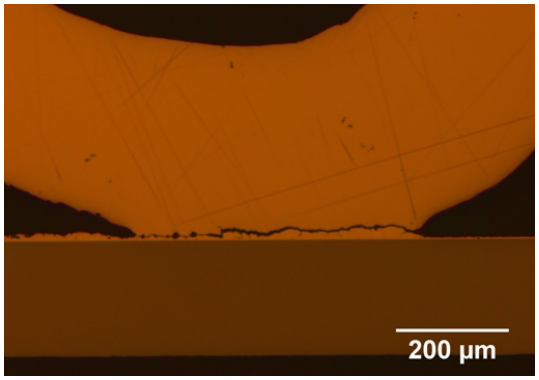


(c) Wire bond B3 of S4 on the LS IGBT.

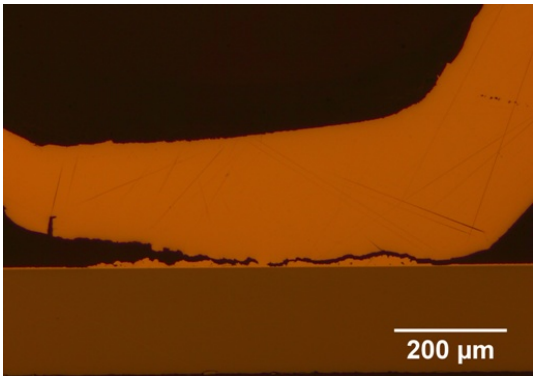
Figure C.7. Grains structure in the wire bonds of the HS and LS IGBT of the 2.5MC module.

C.4 3.5MC Module

Additional images from the micro-sectioning results of the 3.5MC module can be found in Figs. C.8, C.9, C.10, and C.11.

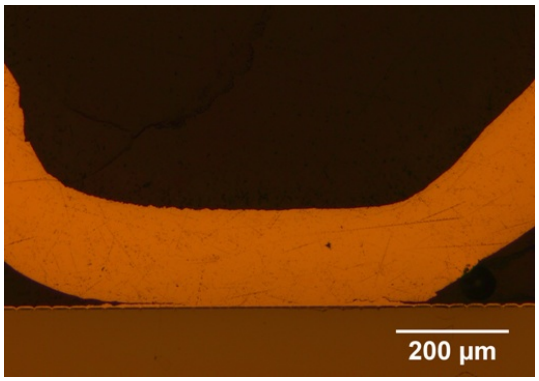


(a) Wire bond B1 of S2 on the HS diode.

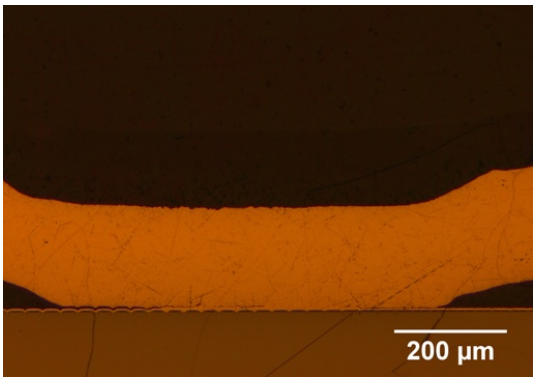


(b) Wire bond B2 of S2 on the LS diode.

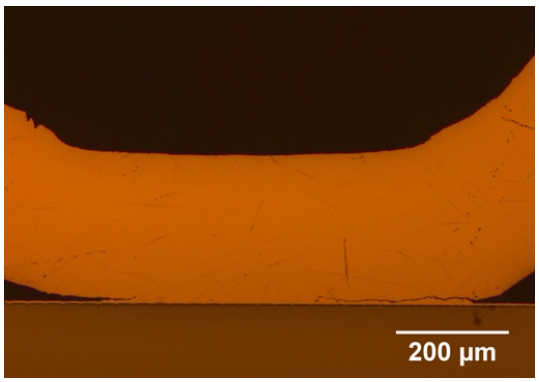
Figure C.8. Wire bonds of the HS and LS diode of the 3.5MC module before etching.



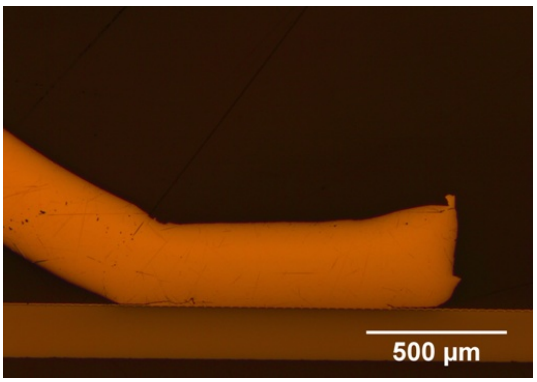
(a) Wire bond B3 of S2 on the HS IGBT.



(b) Wire bond B4 of S2 on the HS IGBT.

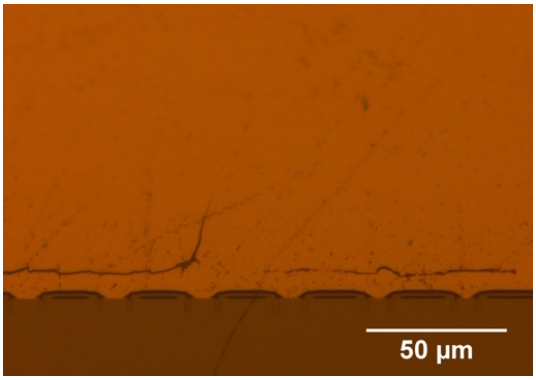


(c) Wire bond B3 of S2 on the LS IGBT.

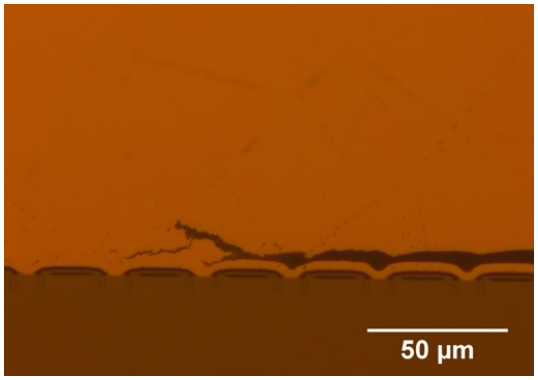


(d) Wire bond B4 of S2 on the LS IGBT.

Figure C.9. Wire bonds of the HS and LS IGBT of the 3.5MC module before etching.

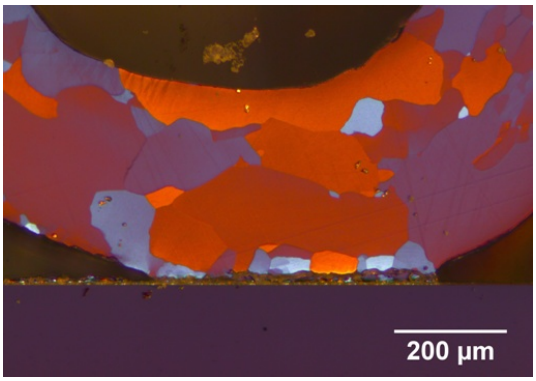


(e) Zoom of Fig. C.9(b).

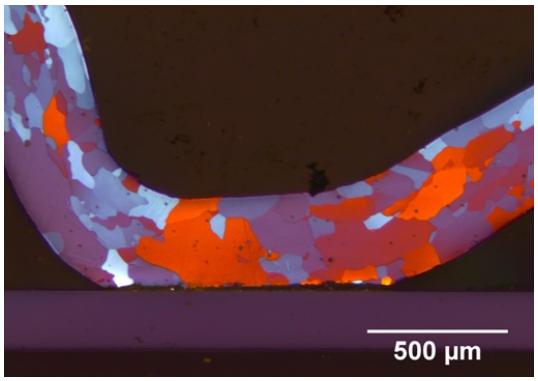


(f) Zoom of Fig. C.9(d).

Figure C.9. Wire bonds of the HS and LS IGBT of the 3.5MC module before etching.

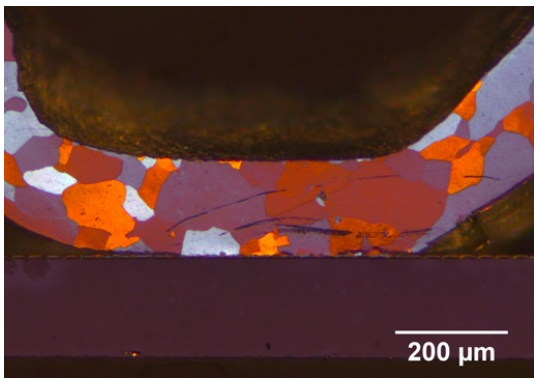


(a) Wire bond B1 of S2 on the HS diode.



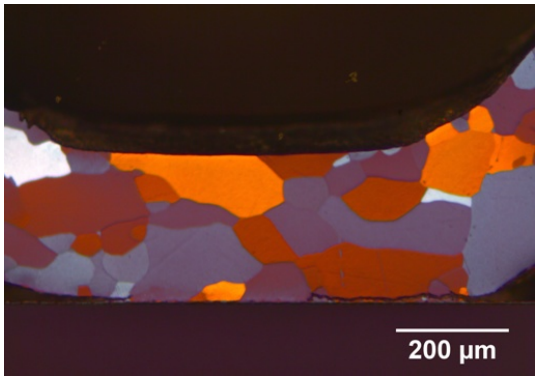
(b) Wire bond B2 of S2 on the HS diode.

Figure C.10. Grains structure in the wire bonds of the HS diode of the 3.5MC module.

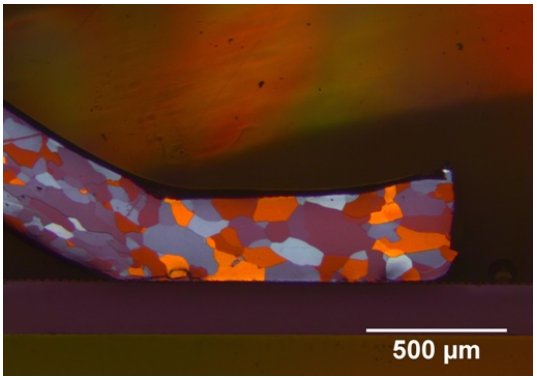


(a) Wire bond B3 of S2 on the HS IGBT.

Figure C.11. Grains structure in the wire bonds of the HS and LS IGBT of the 3.5MC module.



(b) Wire bond B3 of S2 on the LS IGBT.

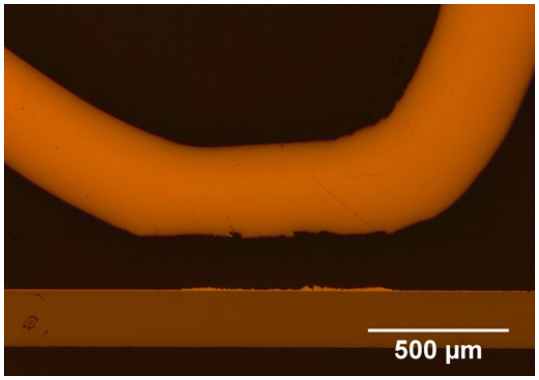


(c) Wire bond B4 of S2 on the LS IGBT.

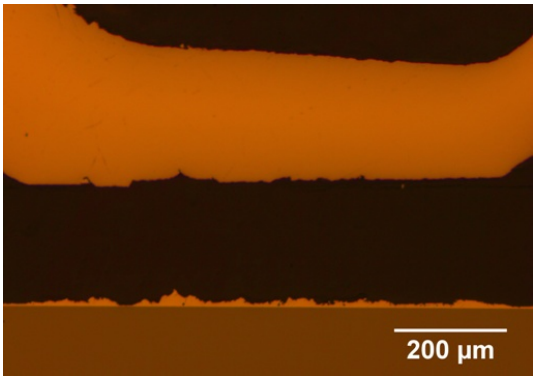
Figure C.11. Grains structure in the wire bonds of the HS and LS IGBT of the 3.5MC module.

C.5 4.5MC Module

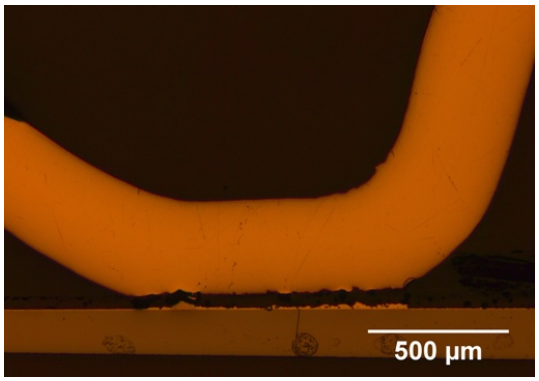
Additional images from the micro-sectioning results of the 4.5MC module can be found in Figs. C.12, C.13, and C.14.



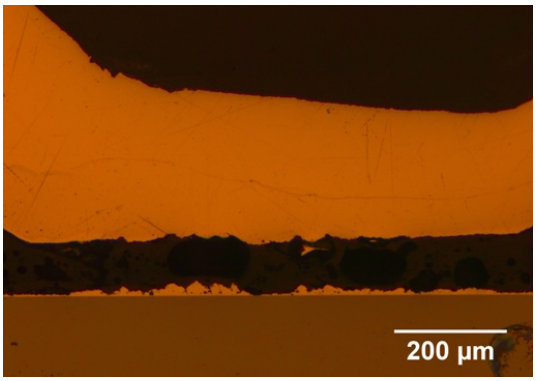
(a) Wire bond B1 of S2 on the HS diode.



(b) Wire bond B2 of S2 on the HS diode.

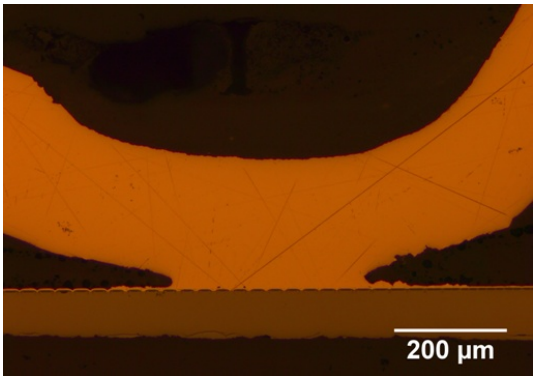


(c) Wire bond B1 of S2 on the LS diode.

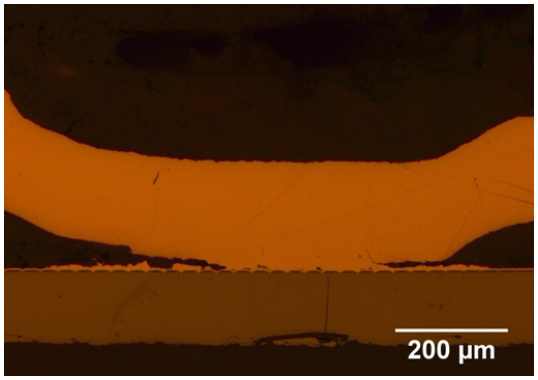


(d) Wire bond B2 of S2 on the LS diode.

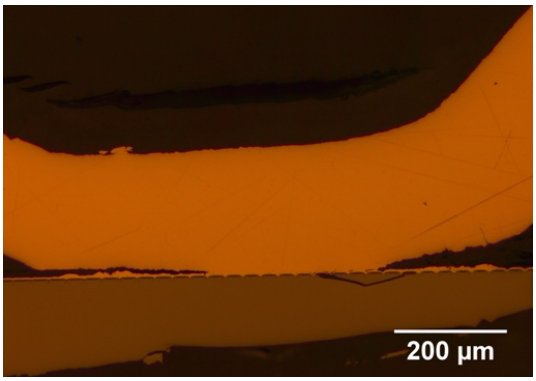
Figure C.12. Wire bonds of the HS and LS diode of the 4.5MC module before etching.



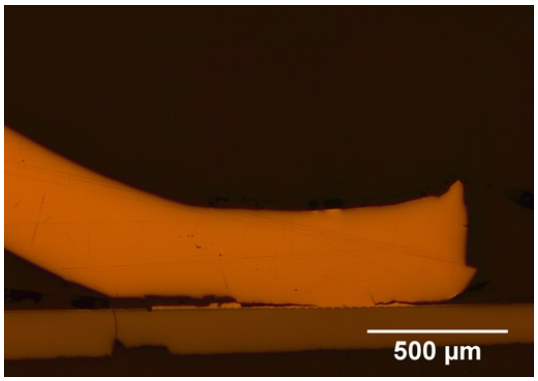
(a) Wire bond B3 of S4 on the HS IGBT.



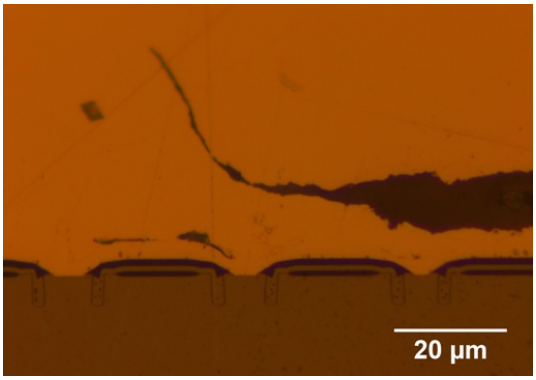
(b) Wire bond B4 of S4 on the HS IGBT.



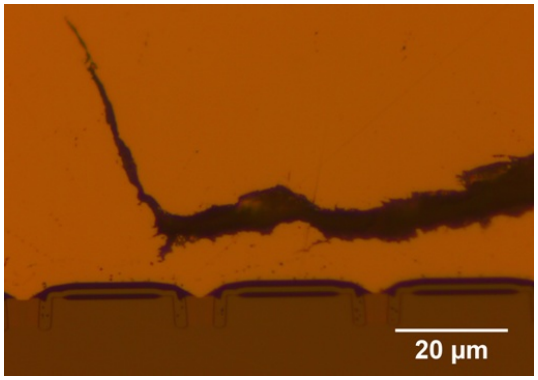
(c) Wire bond B3 of S4 on the LS IGBT.



(d) Wire bond B4 of S4 on the LS IGBT.

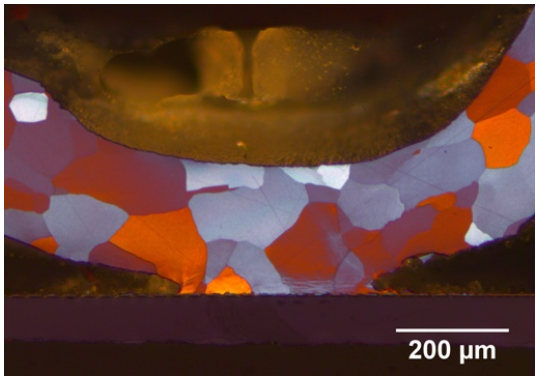


(e) Zoom of Fig. C.13(b).

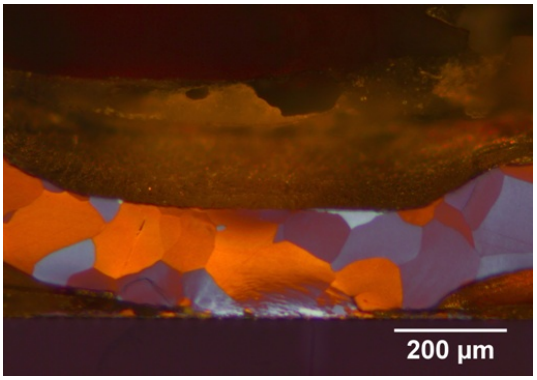


(f) Zoom of Fig. C.13(d).

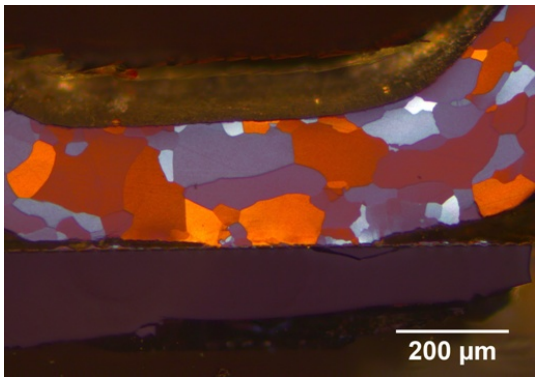
Figure C.13. Wire bonds of the HS and LS IGBT of the 4.5MC module before etching.



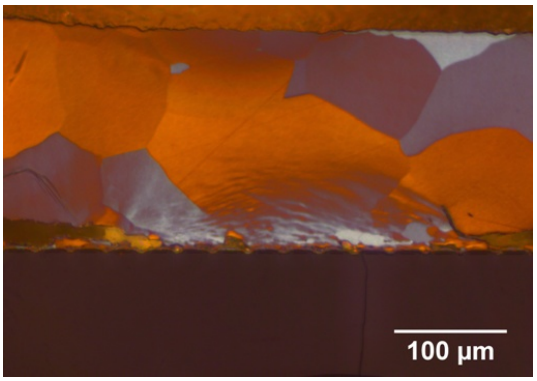
(a) Wire bond B3 of S4 on the HS IGBT.



(b) Wire bond B4 of S4 on the HS IGBT.



(c) Wire bond B3 of S4 on the LS IGBT.



(d) Zoom of Fig. C.14(a).

Figure C.14. Grains structure in the wire bonds of the HS and LS IGBT of the 4.5MC module.