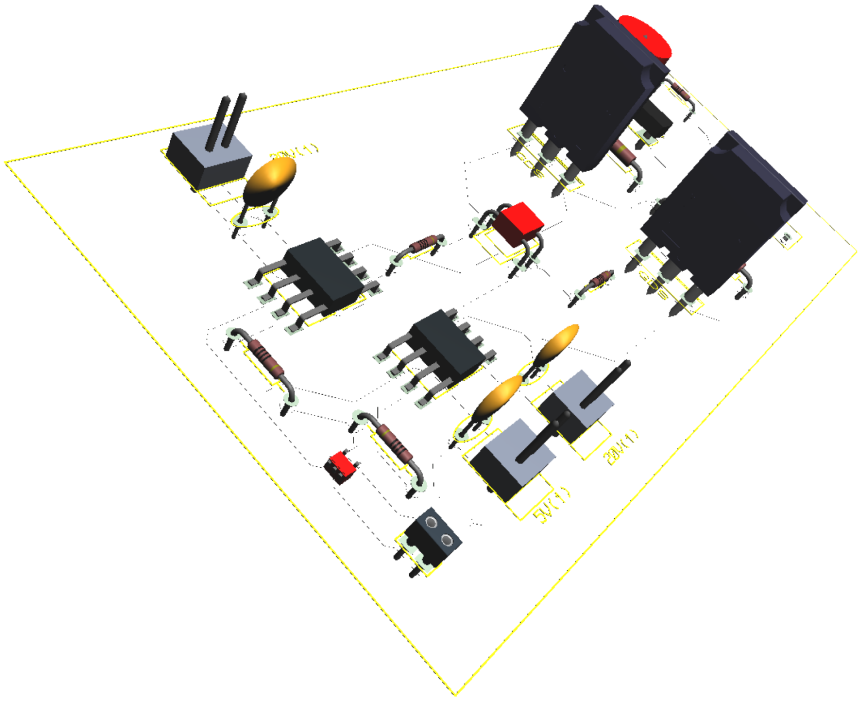
Bidirectional Flyback Converter for Dielectric Electro Active Polymer

Harvesting energy via a novel Dielectric Electro Active Polymer Generator

TAHİR LAĞAP



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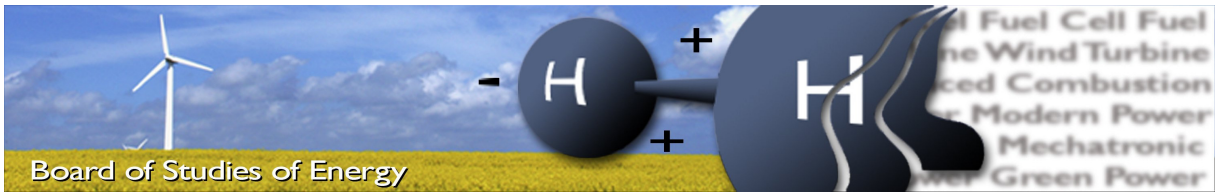

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SYNOPSIS:

Abstract :

In this student project the efforts during the fall and spring semester 2013-2014, which corresponds to 9^{th} and 10^{th} semester of the education, have been introduced.

The project deals with design of a bi-directional flyback converter for Dielectric Electro Active Polymer Generator (DEAP). Firstly an introduction to the energy harvesting cycles has been made. Afterwards, the converter is discussed theoretically and in order to enhance the efficiency of the converter two SiC MOSFET employed to work in series. Therefore, a brief discussion on series connection techniques are done and gate balancing core technique was utilized to provide balanced voltage distribution at switching transients. Finally the converter has been built at laboratory of AAU and experiments have been performed which are different voltage levels.

Number of reports:	3 (Three)
Number of pages:	54 pages
Appendix:	25 pages
DVD:	3 (Three)

By signing this document, each member of the group confirms that all participated in the project work and thereby that all members are collectively liable for the content of the report.

Preface

This report has been prepared as a final step of master program Wind Power Systems (WPS) offered by Aalborg University (AAU) Institute of Energy Technology and it covers 9^{th} and 10^{th} semester, being 50 ECTS. The thesis is direct continuation of 8^{th} semester project which is titled same 'Harvesting energy via a novel Dielectric Electro Active Polymer Generator' and it can be found in Digital Library of AAU or in the attached CD.

Reading Instructions

According to "*procedure for project work*" of Energy department at School of Engineering and Science, maximum number of the Master thesis is limited to 90 which was calculated by the formula provided. The number of pages is counted from the first content page, including appendix excluding the blank pages prior to the beginning of a new chapter.

Each chapter and appendix is ended by 'references' section, due to this, citations, which are given in brackets, are re-enumerated in each chapter. Figures, tables and equations are enumerated by first chapter number then relevant sequence number. For example Table X.Y means X^{th} chapter Y^{th} table. It should be noted that equations given in parenthesis.

Finally, 'conventional current direction' is followed in the entire thesis. Additionally, a compact disc is annexed to provide, references, simulation files, datasheets, scripts, circuit schematics and PCB layouts.

Acknowledgements

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Last but not least, I would like to give heartfelt thanks to Ewen Ritchie who is associate professor and Lisbeth Holm Nørgaard who is senior secretary at Department of Energy Technology, because of their kind suggestion to be "tuition waiver" which enabled me to study the master education at Aalborg University.

Tahir Lağap, 27/05/2014

Summary

The master thesis is direct continuity of 8^{th} semester report which has the same name as "Harvesting energy via a novel Dielectric Electro Active Polymer Generator". While in the second mentioned report design of the converter was handled, in this report, analysis of the converter as well as the snubber network, is done.

The thesis consist of 6 chapters and 5 appendices. In the first chapter, an introduction to the thesis is done in this chapter. Basics of the DEAP technology as well as motivation, limitation and objectives are defined.

Then in the second chapter, one switching period of proposed bidirectional flyback converter is given. Proposed RCDD snubber is experimentally compared with typical RCD snubber and a paper based on this chapter was submitted to the conference IECON 2014. Understanding that used IGBT has significant influence on converter efficiency, it was decided to employ two MOSFET by series connection.

In chapter of 'Series connection of MOSFETs' which is number three, the problems that are encountered while stacking MOSFETs and the theory of series connection methods are briefly discussed. The most representative method "gate balancing core" is chosen to apply for series connection of SiC MOSFETs.

Then in the following chapter, experiments and efforts for the selected method are demonstrated. The next chapter, number six, deals with the bidirectional flyback converter which is modified with two SiC MOSFET in series. The issue with desynchronised gate signals and approach to over come this issue at turn-off transition is exhibited. Lastly, conclusion to entire thesis as well as future works are discussed.

The modification on the bidirectional flyback converter with stacked MOSFET in the high voltage side, shows a notable change in the converter efficiency i.e. change from the range of 65% to range of 90% with 5 A in the primary side.

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CHAPTER 1

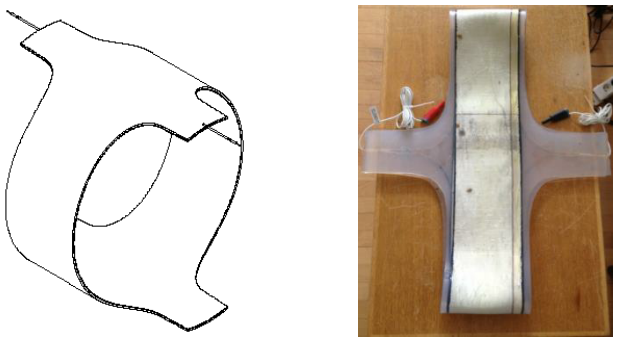
Introduction

In this chapter an introduction to the entire thesis is done. In order for a better understanding, basics of the DEAP are given, its state of the art are discussed, as well as motivation, limitations and objectives are defined.

1.1 Introduction

Massive increment in world's energy demand during the last century, especially the oil crisis in 1970s, caused the countries to feel the shortage of the oil and go towards to the renewable energy sources such as wind, solar energy and etc. In order to be able to use alternatives to these sources, new techniques and materials have been introduces.

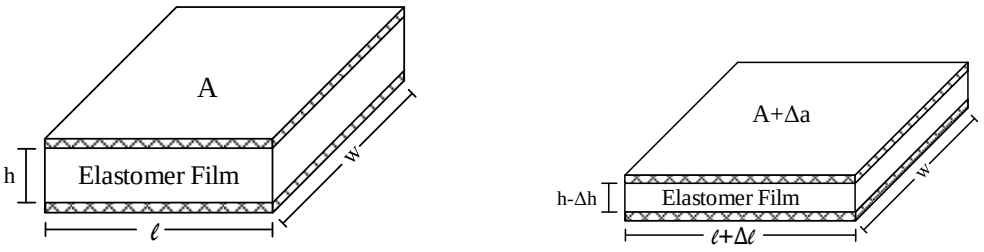
Dielectric Electro Active Polymer (DEAP, see Fig. 1.1) is one of these mentioned alternatives. Furthermore dielectric elastomers received developments being focus of research early in 1900s. However the journey of these kind of actuators (electrode-free) has begun back in 1800 by Wilhelm Röntgen [1].



(a) (b)

Figure 1.1: Single DEAP ring generator (a) schematic (b) product.

DEAPs are utilized in three mode; actuator, generator and sensor. A DEAP's shape and size change when it is excited by electric field (see Fig. 1.2). To provide this electric field, silver electrodes are coated to the both surface of the polymer material. While as a result of this structure, material becomes a parallel plate capacitor, the mentioned change in size and shape brings the feature of being variable capacitor.



(a) (b)

Figure 1.2: DEAP working in actuator mode (a) initial state (b) final state.

1.1.1 Actuator mode

In this mode of operation, applied voltage creates an electric field by means of electrodes and due to Maxwell stress tensor occurred, the material acts in favour of electrostatic forces mentioned, thus it gets compressed in the thickness and enlarged in the surface area, converting electrical energy into mechanical energy.

In Fig. 1.2, l denotes the length of the material, h thickness w width and A surface area. In this representation, it is assumed that the volume of the material is constant due to incompressible feature of the element [2] and width is not changing.

1.1.2 Generator mode

It has previously been mentioned that a DEAP is a parallel plate capacitor, as it can be realized from the equation (1.1), capacitance depends on thickness and the surface area and change in the capacitance is given by (1.2) which is derivative of the capacitance equation.

$$C(t) = \frac{\varepsilon_r.\varepsilon_0.A(t)}{h(t)} = \frac{\varepsilon.A(t)}{h(t)} \ \text{[F]} \ \Rightarrow \tag{1.1}$$

$$\frac{dC}{dt} = \frac{\varepsilon}{h} \cdot \frac{dA}{dt} - \frac{\varepsilon.A}{h^2} \cdot \frac{dh}{dt} \ \text{[F]} \tag{1.2}$$

In this mode the material is elongated and pre-charged then let to contract. The process can be visualized from Fig. 1.2 but this time from (b) to (a). Neglecting the leakage losses and assuming the charge of the material remains the same following charge equation (1.3) is considered. Subsequently, electric potential energy of the DEAP material is given in (1.4).

$$Q = C(t).V(t) \tag{1.3}$$

$$E_e(t) = \frac{1}{2}.C(t).V^2(t) \tag{1.4}$$

In energy harvesting process, elongation and contraction is done consecutively which is named as "*energy harvesting cycles*" and three methods are applied during these cycles [2] i.e. Constant Charge (CC), Constant Voltage (CV) and Constant E-Field (CE). As it is fundamental in this project CC is applied and will basically be explained in the following section.

1.1.2.1 Constant charge cycle

This is the fundamental operation of the DEAP material. The main idea of the cycle is, as it has been mentioned, neglecting the losses, charge of the DEAP remains constant. One operation cycle is given in the Fig. 1.3. Next the transitions between the points, which are given in the figure, will be explained.

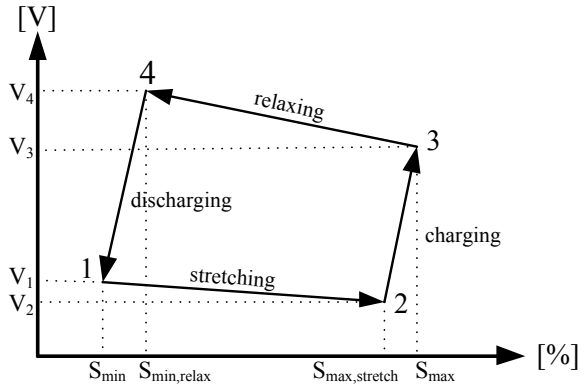


Figure 1.3: DEAP voltage vs. strain in constant cycle operation.

Transition 1 $\rightarrow$ 2

Point 1 is the initial position for this cycle and as it can be realized from Fig. 1.3 DEAP is stretched to $S_{\min}$ which is pre-stretch value as well as V_1 initialization voltage. Then the material is elongated to point 2 by utilization of a mechanical force. Here it can be seen that the voltage of the material drops to V_2. By equating of the charges (Q_1=Q_2), the voltage V_2 and substituting that into (1.4) following equation can be found. Here equation (1.5) gives the amount of energy that has been converted into mechanical energy during the transition. It should be remembered that the capacitance of the DEAP has increased.

$$\Delta E_{1\rightarrow 2} = \frac{1}{2}.C_1.V_1^2.(\frac{C_1}{C_2} - 1) \tag{1.5}$$

Transition 2 $\rightarrow$ 3

At this transition, the voltage of the DEAP V_2 is boosted to V_3 by means of a power electronic converter. The transition is called charging and at the end of this transition, i.e. point 3, DEAP is ready to generate energy.

Transition 3 $\rightarrow$ 4

This transition is the one makes the differences between energy harvesting cycles. Since this is CC,

the charge remains constant until point 4. DEAP voltage V_3 gives its place to V_4 and for CC cycle this value is higher than V_3. Equation (1.6) represents the mechanical energy converted into electrical energy.

$$\Delta E_{3\to4} = \frac{1}{2}.C_3.V_3^2.(\frac{C_3}{C_4} - 1) \tag{1.6}$$

For CE and CV cycles, this transition occurs while the converter tries to keep either the voltage or e-field between a pre-defined hysteresis band.

Transition 4 $\rightarrow$ 1

Point 4 means that it is time to harvest energy for CC cycle and the converter discharges the DEAP generator to its initialization voltage V_1 meaning that the generator is now ready for a new energy harvesting cycle.

1.2 State of the art

DEAP's lightness, cheapness and low power consumption have made it convenient for a large number of applications. In this field three operation modes of the material have been introduced which are actuator mode, generator mode and using the material as a sensor.

For actuation it is known as artificial muscle and have been used in such applications like pumps, sound generations, valves, massaging sleeves, enhanced pc-mouse and varifocal lens [3, 4]. In [5] several practical applications (structural health monitoring, actuator positioning, alignment and tension monitoring and wearable devices) have been introduced as a sensor.

As it is also one of the focal point of this report, several energy generation applications have been performed. In [6], 0.26 J energy harvested at 0.5 Hz cycling frequency and 60% delta-strain. The highest energy generation record is being hold by SBM as the results were reported in [7] that with 10-70% deformation, 0.7 Hz cycling frequency 4 joules of energy has been extracted being 0.89 J/kg of active material.

1.3 Motivation

It was previously mentioned that the energy demand of the world is increasing day after day so that newer and cleaner energy sources are becoming a focal point of the research. DEAP technology has a place in the market as either actuator, generator or sensor and share is still growing. In [4] it was explained as "*The recent years' growth of the field of EAP has been quite well reflected in the number of papers that were submitted for presentation at the 2014 SPIE EAPAD Conference. It is pleasing to see that it reached a record of 138 papers. Also, there is growing number of emerging companies that produce EAP and related products*."

This developing technology, enabling energy harvest from renewable energy sources, needs direct collaboration with power electronics. Thus, process of energy scavenging, conversion and interaction

with load has to be made in a safe, reliable and controlled way. All in all, design of a highly efficient, low-cost power electronics converter is not an easy task which motivates the researchers high.

1.4 Limitations

Initially, in [8] a bidirectional flyback converter was designed and tested. Even though the final goal was to test the converter with DEAP generator, eventually lack of the generator resulted the tests to be done with a constant capacitive load.

Similarly, in this thesis, for debug and test process of the converter, a 2.26 μF constant capacitive load was used instead of actual DEAP generator. Upgrade in production department of Danfoss PolyPower A/S between November 2013 and February 2014 and reasons beyond the control, delayed the delivery of DEAP generator so that the converter was tested with constant capacitive load.

1.5 Objectives

The main objectives of this master thesis are defined in this section. Indeed, sorted in a non-hierarchized manner, the project's objectives were:

- Analyse the bidirectional flyback converter together with the snubber network and determine the biggest influence on converter efficiency.
- Make a comparison between different snubber networks and experimentally validate the employability of RCDD snubber network in terms of converter efficiency and over-voltage suppress capability.
- Test the connectivity of SiC MOSFETs in series and if feasible rebuild the flyback converter.
- Make an efficiency comparison with new and old configuration of bidirectional flyback converter.

1.6 Project Outline

The master thesis consist of 6 chapters. In this section the main lines of these chapters are given in order to create a big picture in readers mind.

- **Chapter 1: 'Introduction'** An introduction to the thesis is done in this chapter. Basics of the DEAP technology as well as motivation, limitation and objectives are defined.
- **Chapter 2: 'Analysis of the Bi-directional Flyback Converter and Snubber'** In this chapter, one switching period of proposed bidirectional flyback converter is given. Proposed RCDD snubber is experimentally compared with typical RCD snubber and a paper pased on this chapter was submitted to the conference IECON 2014. Understanding that used IGBT has significant influence on converter efficiency, it was decided to employ two MOSFET by series connection.
- **Chapter 3: 'Series Connection of MOSFETs'** This chapter deals with the theory of series connection methods for MOSFET/IGBT and various approaches has been briefly mentioned.

- **Chapter 4: 'Experiments with gate balancing core'** In this chapter experiments and debug process regarding to series connection of MOSFETs by means of gate balancing core method are conducted.
- **Chapter 5: 'Bidirectional Flyback Converter with Series Connected SiC MOSFETs'** In this chapter experiments done bidirectional flyback converter which has two SiC MOSFET connected in series in the high voltage side. Efficiency measurements of the converter with SiC and IGBT based version is also given in this chapter.
- **Chapter 6: 'Conclusions and Future Works'** Here, all in all conclusions and future works for the thesis is discussed.
- **Chapter 7: 'Appendices'** This part of the thesis contains, a brief theory on capacitance estimation of multilayer parallel plate capacitor, as well as publications, PCB layouts, schematics, microcontroller and simulation scripts.

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CHAPTER 2

Analysis of the Bidirectional Flyback Converter and Snubber

In this chapter a thorough analyse of the bidirectional flyback converter and the implemented snubber is done step-by-step. It should be mentioned that a scientific article has been written and submitted based on this chapter in IECON 2014 conference.

2.1 Introduction

In industrial applications it is possible to encounter systems that need high voltage power supply such as laser, X-ray and space applications. As it is in this study, some of these mentioned applications need charging of high voltage capacitors.

Furthermore it has been mentioned in Section 1.1.2 that the DEAP generator operation needs both charging and discharging functions. In line with the requirement, bidirectional flyback converter was chosen among various converter options in [1], due to its main advantages of simplicity, galvanic isolation, low component count and well known dynamic behaviour [2]. On the other hand, low power capability and energy loss because of the leakage inductances presented by flyback transformer can be mentioned as drawbacks. Although in 8^{th} semester project, design of bidirectional flyback converter was examined step-by-step, only its basic operation was studied.

This chapter is dedicated to analysis of the bidirectional flyback converter together with the implemented RCDD snubber, in detail. Even though 'design' of the mentioned converter is not a content of this chapter, in the light of analysis, selection of the snubber components will be discussed for the sake of optimality.

2.2 Bidirectional flyback converter

In bidirectional DC/DC converters, power flow is attained by way of bidirectional current flow, so that in these converter the polarity of the electric potentials at either end stay the same [3]. As it is given

in Fig. 2.1, very basic bidirectional flyback converter consist of two power electronics switches, 2 diodes and a flyback transformer. Energy flow from one to the other end is obtained by switching on and off at one side and subsequently diode on the other side .

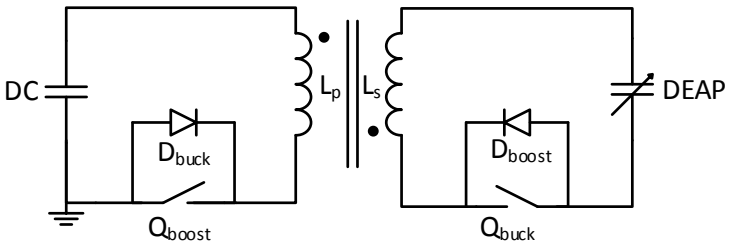
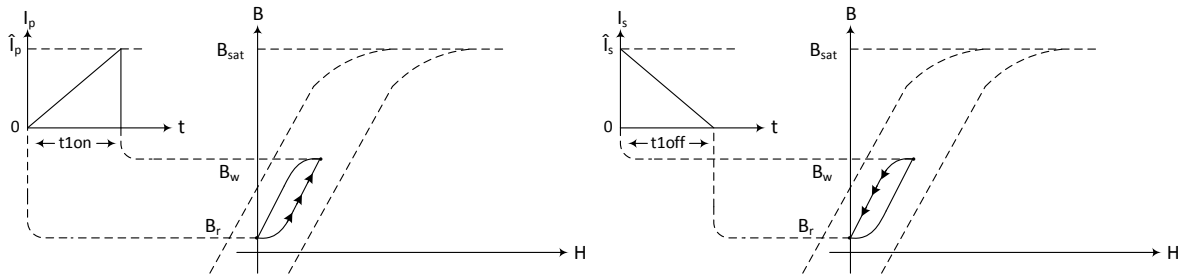


Figure 2.1: Bidirectional flyback converter.

In Fig. 2.2 current waveform and flyback transformer magnetization are illustrated. Supposing that the energy flow will occur from DC to DEAP side (Fig. 2.1), Fig. 2.2a represents the duration called 'energy storage' phase where $\mathrm{Q_{boost}}$ is conducting and $\mathrm{D_{boost}}$ is reverse-biased. At the end of this phase $\mathrm{Q_{boost}}$ is turned-off and right after 'flyback phase' starts where uncontrolled semiconductor $\mathrm{D_{boost}}$ conducts, transferring energy to the output load i.e. DEAP generator. It should be mentioned that given operation in Fig. 2.2 demonstrates boundary conduction mode.



(a) (b)

Figure 2.2: Current waveform and magnetization of the flyback transformer at (a) energy storage (b) flyback phase.

Here in Fig. 2.2a flux density starts from its residual value $\mathrm{B_r}$ and reaches to its peak value $\mathrm{B_w}$, then in Fig. 2.2b vice versa occurs. $\mathrm{t_{1on}}$ is the duration of energy storage phase and $\mathrm{t_{1off}}$ is duration of flyback phase. As assumed that energy flow from DC to DEAP side, the slope of the currents as well as the peak values can be computed by means of (2.1). For example, in energy storage phase, to find peak current substitution must be done as; V by $\mathrm{V_{DC}}$, L by $\mathrm{L_p}$, di by switching period of $\mathrm{Q_{boost}}\times$duty cycle.

$$\frac{V}{L} = \frac{di}{dt} \tag{2.1}$$

Similarly, change in flux regarding to Fig. 2.2, is expressed by (2.2) where N is number of turns in the relevant winding.

$$B_w - B_r = \Delta B = \frac{V \cdot dt}{N} \tag{2.2}$$

2.3 Snubber network

Snubber networks are often located across high-voltage power semiconductors for the purpose of switching stress and EMI reduction during turn-off and turn-on transitions [4].

Practically, windings in a transformer cannot be perfectly coupled to the core. This arises from physical separation between the windings where a small amount of energy is stored, introducing leakage inductance to the circuit [5]. In a flyback converter, care must be taken for the overshoot caused by high di/dt in leakage inductances and its resonance with output capacitances C_{OSS} of the power switches in order not to exceed limits of the 'safe operating area (SOA)'. To ensure the operation in SOA, passive and active snubber networks for flyback converters, are used. In the following subsections these will briefly be over-viewed.

2.3.1 Passive snubbers

Passive snubber networks qualified to resistors, capacitors, inductors and diodes. As they can control either voltage or current they can also be dissipative or non-dissipative. Accordingly, it is possible to utilize a passive snubber for voltage spike clamping or to damp the ringing for noise reduction in the system or both. In [5], these snubbers are generally classified into three:

- Rate-of-rise control snubber
- Voltage clamp snubber
- Damping snubber

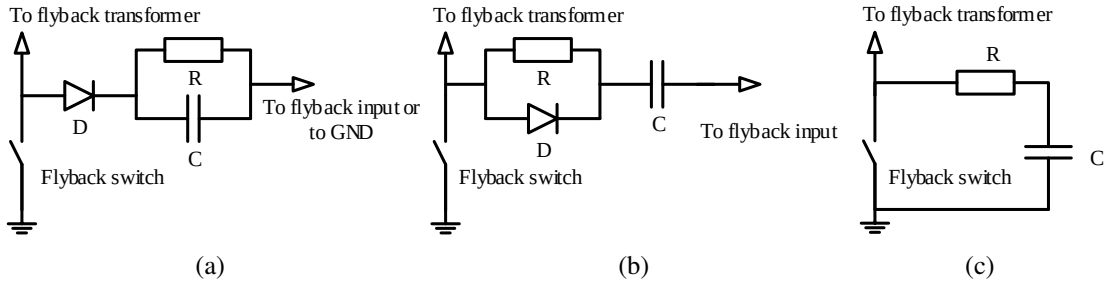


Figure 2.3: RCD snubber network with the configuration of (a) voltage clamp (b) rate-of-rise and (c) RC snubber network.

The RCD snubber configuration in Fig. 2.3a is used in order to clamp the voltage at drain of the power semiconductor to the capacitor voltage V_C in turn-off transition. The value of the capacitor C and resistor R are basically determined by means of the energy stored in leakage inductance. Here in this snubber, at each turn-off, snubber capacitor voltage rises to the value that is sum of clamp voltage and snubber capacitor voltage ripple which is relatively a small change since the capacitor voltage is the clamp level. It discharges to the clamp voltage on snubber resistor until next turn-off meaning the time constant of RC clamp is bigger than switching period. In short, the energy that is needed to be dissipated in the snubber is the energy stored in the leakage inductance causing the snubber capacitor voltage ripple [5, 6].

In Fig. 2.3b RCD snubber network configuration for rate-of-rise control is demonstrated. As an operation principle, the snubber capacitor here charges and discharges completely at each cycle so that the RC time constant should be much smaller than switching period. In this network, the snubber capacitor value is estimated by choice of rise time at maximum inductor current and supply voltage by means of current-voltage relation of capacitance. One important thing here is that power dissipation of the resistor is independent of its value because of very small RC time constant compare to switching period. Thus it depends on the capacitor size, since all the energy stored in capacitor is dissipated on each cycle [5, 6].

Simple RC voltage snubber in Fig. 2.3c is commonly used and feasible for both rate-of-rise control and damping. By controlling rate-of-rise at drain, peak power dissipation may be reduced. It is mainly used to damp the resonance of parasitic elements. Snubber capacitance value must be higher than resonance circuit capacitance and lower enough to minimise the power dissipation on resistor as well as the resistor value being close to characteristic impedance of the parasitic resonance.

Passive snubber networks given in Fig. 2.3 are dissipative. On the other, it is possible to achieve non-dissipative passive snubbers as well. While energy transferred to capacitor in dissipative snubbers are turned into heat, in non-dissipative snubbers a way is found to transfer energy either back into the source or output [6].

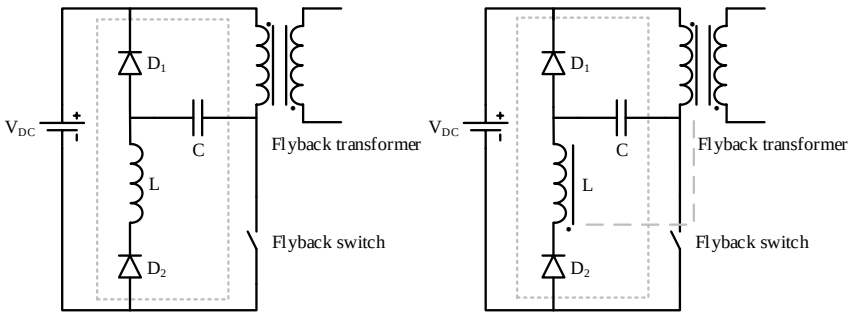


Figure 2.4: Passive (a) non-dissipative (b) regenerative snubber networks.

In Fig. 2.4 non-dissipative passive snubber networks are given. The circuit in Fig. 2.4a is know as non-dissipative LC turn-off snubber and it has been studied in [7]. This configuration can be used as a rate-of-rise control or voltage clamp snubber [6]. In Fig. 2.4b a modified version of this snubber is given, being energy regenerative snubber studied in [8]. Operation of the snubber network starts at turn-off of the semiconductor switch. Energy in the leakage inductance moves to snubber capacitor C through diode D_1. At turn-on of the switch, the voltage rings with inductance L until the snubber current goes to zero or diode D_1 turns-on again [6]. However in Fig. 2.4b, the snubber inductor is coupled to the flyback transformer enabling the energy return to the source [8] Another benefit of these networks is lowered ringing.

2.3.2 Active clamp

Active clamp in a flyback converter is demonstrated in Fig. 2.5. It is utilized to recycle the energy stored in leakage inductance of the flyback transformer and to minimise the voltage overshoot at drain of the flyback (main) switch. Configuration can also help both main and snubber switches to perform zero voltage switching (ZVS) [9, 10]. Some other benefits of this technique are, using lower voltage semiconductor compare to RCD, reduced EMI/RFI and actively resetting main transformer to third quadrant of BH curve [11].

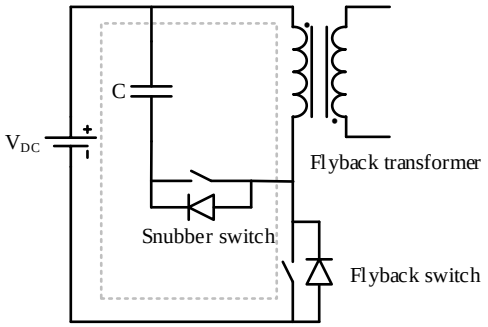


Figure 2.5: Active clamp snubber network in flyback converter.

Drawbacks of this technique can be mentioned as; necessity of an additional high voltage switch and an isolated gate driver for this clamp switch and modified control technique to achieve ZVS.

2.4 Bidirectional flyback converter with snubber network

In previous section 'Snubber network' (2.3), the origin of the problem that brings the requirement of snubber networks and the most typical snubbers have been discussed briefly. However, for particular applications care must be taken in decision making process. In this study, not only the bidirectional energy flow increases the complexity of the problem, but also load type i.e. DEAP.

To start with, simple RC snubber can be applied to rate-of-rise control and damping. However, this snubber is dissipative by definition [6]. It absorbs energy at each voltage transition lowering the efficiency [5]. It also decrease the switching speed of the semiconductor. It concludes that this technique is not unsuitable for this study.

To talk about RCD clamp, first DEAP energy harvesting cycles should be noted. In typical DC-DC converters, considering a constant load, a transient period occurs until output smoothing capacitor reaches to desired output voltage. On the contrary, in DEAP application energy flow direction reverses soon after the desired voltage achieved. This cycle can clearly be realized in Section 1.1.2. The key point here is that, while energy storage phase occurs in one end of the transformer, the snubber resistor will draw energy on the other end. Besides, since energy flow direction and voltage levels changes, clamp voltages are also not fixed.

In RCD rate-of-rise configuration, snubber capacitors absorb energy at both turn-on and turn-off of the switches on both side of the converter.

Active clamp technique has been used for bidirectional flyback converter in [12, 13] and for low power, low voltage applications high efficiency (above 90%) was measured. However, using this snubber for bidirectional converter doubles the disadvantages that was mentioned in the previous section. One of the main constrain in this study is high voltage switches and using active clamp for bidirectional flyback converter doubles the requirement of high voltage switch in the DEAP side as well as the complexity of the control circuit increases.

Lastly, passive non-dissipative snubber network becomes a strong candidate. Still, it needs to be justified and discussed. By different component values this voltage snubber can act as either rate-of-rise control or clamp mode. In [6], it has been mentioned that clamp mode is normally used in current snubber. Snubber capacitance value is chosen by means of (2.3).

$$i = C\frac{dv}{dt} \tag{2.3}$$

Here, rate-of-rise i.e. $\Delta v/\Delta t$ needs to be known. Typically, change in voltage can be taken as voltage rating of the switch and time interval has to be shorter than the smallest pulse-width of the switch gate signal which is duty cycle$\times$switching period. The trade-off here is that higher the capacitance lower voltage spike.

The proposed snubber in Fig. 2.6 is an modified version of non-dissipative snubber. The snubber capacitor size is minimised by series connected damping resistor, sacrificing the stored energy in leakage inductance. As in RC snubber, energy dissipation of the snubber network depends on the capacitance.

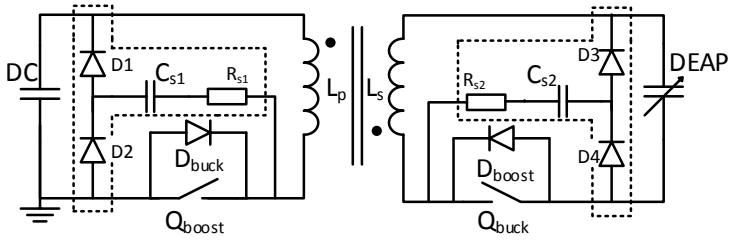


Figure 2.6: Proposed snubber together with the bidirectional flyback converter.

2.5 Principle of operation

In this section, one period of operation in boost mode working will be discussed by division of seven intervals (see Fig. 2.7), since it is basically the same in either boost or buck mode. It should be noted that this analysis was done for ideal components.

Firstly, secondary side of the converter is reflected to the primary side for the purpose of simplification. Variable DEAP capacitance is substituted by a fixed capacitor, C_D, since it can be considered constant during a boost or buck cycle. Besides, DC-link capacitor is also replaced by a constant DC voltage source, V_{CD}, names of switches changed from Q_{boost} and Q_{buck} to Q_1 and Q_2 respectively, and

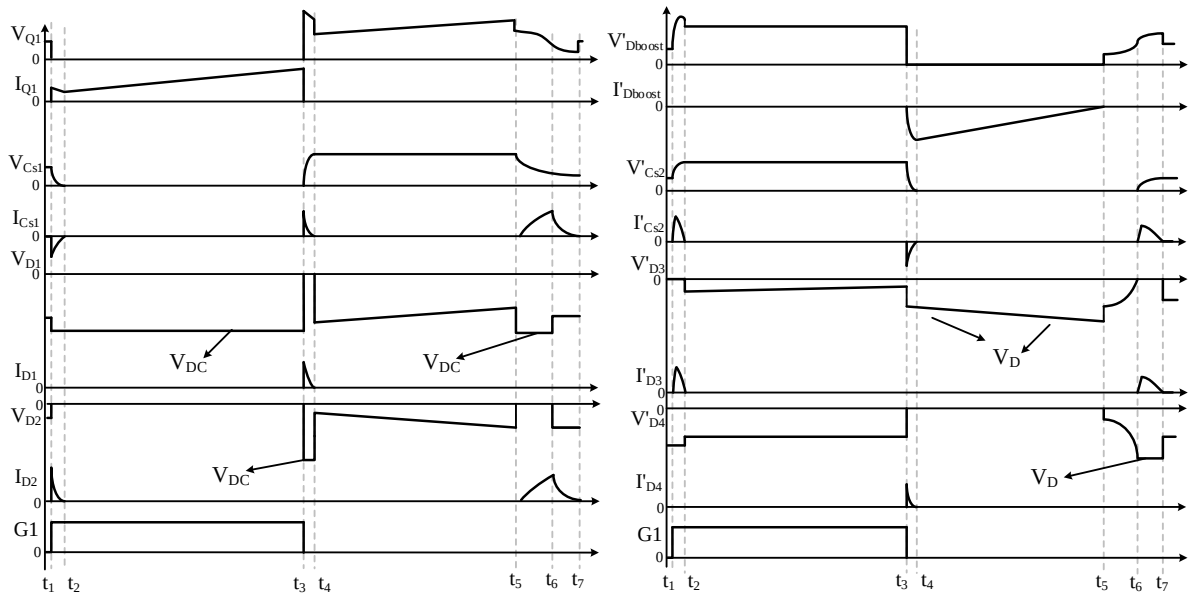


Figure 2.7: Voltage and current waveforms of one boost period.

reflected passive components renamed by adding prime ($'$) to their name. Applying these changes to Fig. 2.6; Fig. 2.8 is obtained.

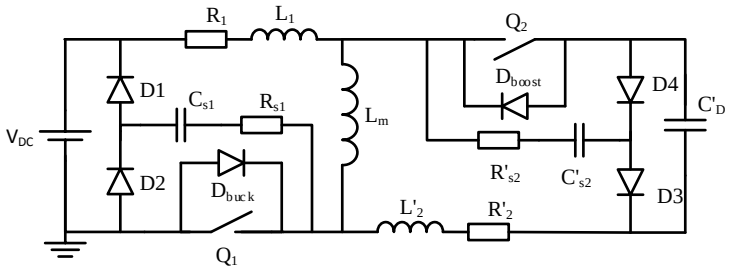


Figure 2.8: Proposed bidirectional flyback converter with all the components are reflected to the primary side.

Here, denoting n turns ratio of the transformer (N_{prim}/N_{sec}), reflected inductances and resistances must be multiplied by n^2 and while capacitances must be divided by the same term.

Subsequently, in relation with the states of the switches, that is listed in Table 2.1, current paths are demonstrated and components which no current flows in are given in grey colour. Analysis is done by primary and secondary side leakage inductances current $I_{L1}(t)$ and $I_{L'2}(t)$ respectively.

Table 2.1: States of the switches.

	t_1-t_2	t_2-t_3	t_3-t_4	t_4-t_5	t_5-t_6	t_6-t_7	t_7-t_1
Q1	ON	ON	OFF	OFF	OFF	OFF	OFF
Q2	OFF	OFF	ON	ON	OFF	OFF	OFF
D1	OFF	OFF	ON	OFF	OFF	OFF	OFF
D2	ON	OFF	OFF	OFF	ON	ON	OFF
D3	ON	OFF	OFF	OFF	OFF	ON	OFF
D4	OFF	OFF	ON	OFF	OFF	OFF	OFF

2.5.1 Interval t_1-t_2 (Q_1, D_2 and D_3 are ON)

At the beginning of this interval there is no current flowing in the converter. The interval starts with the gate signal, G_1. Snubber capacitor C_{s1} discharges and C'_{s2} charges, so the section lasts when $I_{D2}(t)$ and $I_{L'2}(t)$ reach to zero ampere again. States of the switches are given in Table 2.1 as well as the equivalent circuit is given in Fig. 2.9. Here, mesh current method is applied and equations are rearranged as in (2.4) and (2.5) which represent voltages that can be used to estimate primary and secondary side leakage inductor currents.

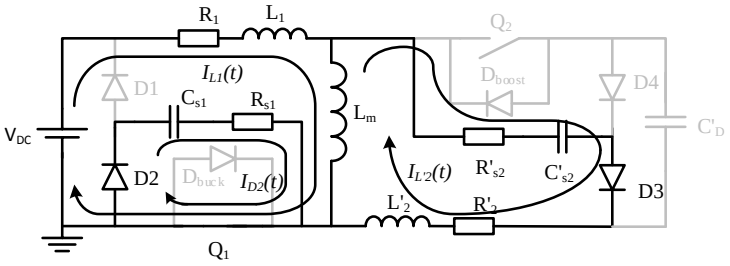


Figure 2.9: State of the converter in interval t_1-t_2.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -L_m\frac{dI_{L'2}(t)}{dt} - R_1 I_{L1}(t) - V_{DC} \tag{2.4}$$

$$(L'_2 + L_m)\frac{dI_{L'2}(t)}{dt} = -L_m\frac{dI_{L1}(t)}{dt} - I_{L'2}(t)(R'_{s2} + R'_2) - V_{C's2}(t) \tag{2.5}$$

$$I_{D2}(t_{1-2}) = I_{D2}(t_1)\, e^{-t/R_{s1}C_{s1}} \tag{2.6}$$

To talk about the steady-state work, C_{s1} is completely discharged and C'_{s2} is charged to its final value at the end of each period and no current flows due to snubbers in this interval of t_1-t_2. Hence $I_{L'2}$ is substituted as zero value in (2.4) and (2.5) resulting $V_{C's2}$ to be constant at steady-state. Besides, before steady-state $I_{D2}(t)$ flows through Q_1 and it can be obtained by (2.6).

2.5.2 Interval t_2-t_3 (Q_1 is ON)

When the converter is in this state, it means that primary side capacitor is completely discharged on Q_1 and secondary side capacitor is charged to $\geq n \cdot V_{DC}$ that it does not draw current from the flyback

transformer. This interval can be named as main energy storage phase to the transformer. The state ends when gate signal goes low at switch Q_1. The only current flowing in the circuit is $I_{L1}(t)$, illustrated in Fig. 2.10 and it can be obtained by solution of (2.7) for $I_{L1}(t)$.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -R_1 I_{L1}(t) - V_{DC} \tag{2.7}$$

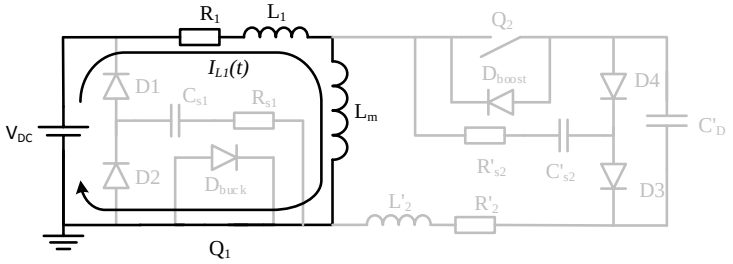


Figure 2.10: State of the converter in interval t_2-t_3.

2.5.3 Interval t_3-t_4 (Q_2, D_1 and D_4 are ON)

In this interval Q_1 is no longer conducting. A high di/dt occurs at both end of the transformer, inductances L_1 and L_m changes their polarity, $I_{L1}(t)$ drops and $I_{L'2}(t)$ rises. The interval finalizes when $I_{L1}(t)$ and $I_{D4}(t)$ reach to zero ampere. The voltage spike which brings the necessity of the snubber on primary side switch, Q_1 arises at this very section. As it is illustrated in Fig. 2.11, primary side snubber network creates a path for the leakage inductance current I_{L1}, and the voltage spike is suppressed to acceptable level.

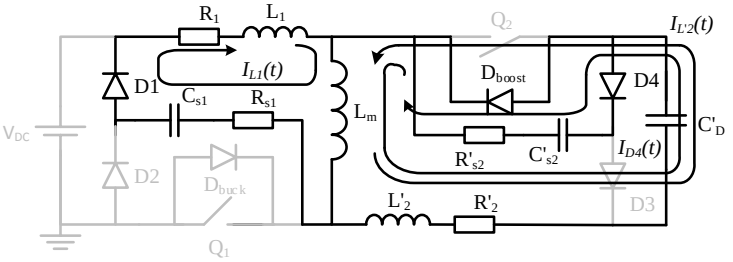


Figure 2.11: State of the converter in interval t_3-t_4.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -L_m\frac{dI_{L'2}(t)}{dt} - I_{L1}(t)(R_1 + R_{s1}) + V_{Cs1}(t) \tag{2.8}$$

$$(L'_2 + L_m)\frac{dI_{L'2}(t)}{dt} = -L_m\frac{dI_{L1}(t)}{dt} - R'_2 I_{L'2}(t) + V_{C'D}(t) \tag{2.9}$$

Currents flowing in the converter can be obtained by solution of (2.8) and (2.9). Here, since C'_{s2} is very small compare to C_D, a simplification is made that, energy stored by itself is dissipated on R'_{s2}, R'_2 and series resistance of C'_D meaning that $I_{D4}(t)$ is not expressed.

2.5.4 Interval t_4-t_5 (Q_2 is ON)

This period can be named as flyback period. Energy stored in the transformer is moved to the output in this interval. $I_{L'2}(t)$ is the only current flowing in the converter which is illustrated in Fig. 2.12 and can be calculated by solution of (2.10) for $I_{L'2}(t)$.

$$(L'_2 + L_m)\frac{dI_{L'2}(t)}{dt} = -R'_2 I_{L'2}(t) + V_{C'_D} \tag{2.10}$$

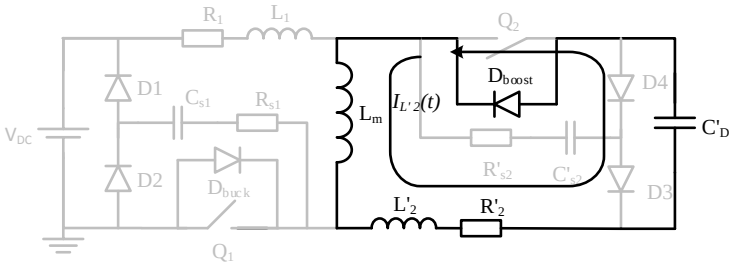


Figure 2.12: State of the converter in interval t_4-t_5.

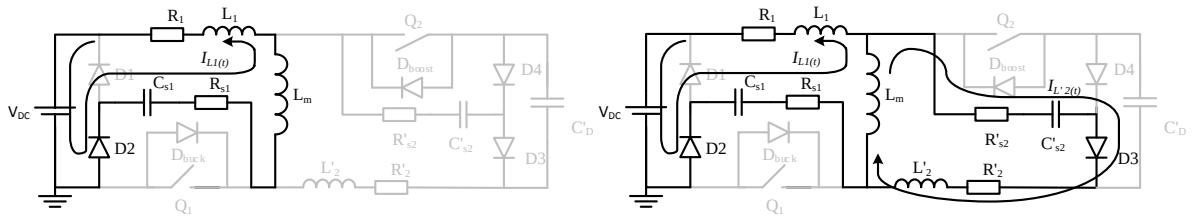
2.5.5 Interval t_5-t_6 (D_2 is ON) and t_6-t_7 (D_2 and D_3 are ON)

When converter steps into stage t_5-t_6, energy transfer is already done and the only current that flows in the converter is due to primary side snubber capacitor C_{s1}.

C_{s1} is at the voltage that was charged in interval t_3-t_4 and in Fig. 2.13a it is shown that an RLC circuit occurs, however D_2 restricts the oscillation. The current flows as follows: First $I_{L1}(t)$ builds up and at the very moment that it crosses its peak value, interval t_5-t_6 ends. So now it is interval t_6-t_7.

According to inductor voltage expression $v = Ldi/dt$, when slope of current changes its sign, i.e. di/dt changes sign, accordingly inductor changes its polarity. Then a second current $I_{L'2}(t)$ flows as in Fig. 2.13b. In case C'_{s2} charges high enough ($\geq V_{DC}/n$) then it does not draw current in interval t_1-t_2.

Equation (2.11), (2.12) and (2.13) can be solved in order to calculate the currents in intervals t_5-t_6 and t_6-t_7 respectively.



(a) (b)

Figure 2.13: State of the converter in interval (a) t_5-t_6 and (b) t_6-t_7.

(2.11) associates with interval t_5-t_6 as well as (2.12) and (2.13) with interval t_6-t_7.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = V_{C1}(t) - I_{L1}(t)(R_1 + R_{s1}) + V_{DC} \tag{2.11}$$

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -L_m\frac{dI_{L'2}(t)}{dt} - I_{L1}(t)(R_1 + R_{s1}) - V_{DC} + V_{C1}(t) \tag{2.12}$$

$$(L'_2 + L_m)\frac{dI_{L'2}(t)}{dt} = -L_m\frac{dI_{L1}(t)}{dt} + V_{C'2}(t) - I_{L'2}(t)(R_2 + R_{s2}) \tag{2.13}$$

2.5.6 Interval t_7-t_1 (all is OFF)

In this interval all the switching devices are turned-off thus there is ideally no current flowing.

2.5.7 Snubber component selection

So far, one switching period of the converter in boost mode working has been analysed. The intervals that snubber network shows its function and influence have been observed. Converter state at interval t_3-t_4 where voltage spike is being suppressed, can be a start point to size the components.

Here, the components will be sized based on energy in leakage inductance and damping. It starts with sizing the snubber capacitances. At this point energy stored in the leakage inductances was considered. Equation (2.14) is derived from equalizing energy expressions of a capacitor and inductor, correspondingly writing the expression with respect to capacitance. By this, a capacitor value is found to be minimum. Measured transformer parameters to use in the expression, are given in Table 2.2.

$$C_{s1,s2} \geq \frac{L_{L1,L'2}\,\hat{I}^2_{L1,L'2}}{V^2_{Q1,Q2(\max\_CE\_stress)}} \tag{2.14}$$

In this case, with 15 A peak current ($\hat{\mathrm{I}}_{\mathrm{L1}}$) value on the primary side, according to (2.14) $\mathrm{C_{s1}}$ and $\mathrm{C_{s2}}$ are found to be 2.96 nF and 0.8 nF respectively. In practice, $\mathrm{C_{s1}}$ and $\mathrm{C_{s2}}$ are chosen to be 4.7 nF and 2.2 nF respectively. It should be noted that maximum voltage stress on the switches were found by (2.16) and (2.17).

To continue with sizing the resistors, it can be done by (2.15). Here ζ is the damping factor and it is chosen to be $1/\sqrt{2}$ (≈ 0.707). This makes $\mathrm{R_{s1}}$ and $\mathrm{R_{s2}}$, 100 and 333 ohm respectively.

$$R_{s1,s2} = 2\zeta\sqrt{\frac{L_{L1,L2}}{C_{s1,s2}}} \tag{2.15}$$

Lastly, diodes on the primary side must be able to block maximum DC-link voltage, as well as the ones on the secondary side must be able to block maximum output voltage. Therefore GP02-40 diodes were used which has maximum DC blocking voltage of 4000 V and 15 A peak forward surge current.

Table 2.2: Converter Component Parameters.

L_1	25.86 μH	Cs1	4.7 nF
L_2	111.34 μH	Rs1	100 Ω
R_1	0.55 Ω	Cs2	2.2 nF
R_2	3.74 Ω	Rs2	333 Ω
L_m	6.22 mH	D1-D4	GP02-40 (4 kV)
n	0.5	$D_{buck,boost}$	GP02-40 (4 kV)
Q_{boost}	IXGF25N300 (3 kV)	Q_{buck}	IXGF25N300 (3 kV)
C_{DC}	53.3, 77.5, 117.5 μF	C_D	2.26 μF

2.5.8 Summary

In this section one period of boost operation has been examined. By division of the period to seven intervals, not just well-known flyback operation but also the proposed snubber have been analysed.

In Section 2.4, it has been mentioned that snubber capacitor value is minimised. It is because not to seize the output energy in snubber part. Section 2.5.1 validates that secondary side snubber absorbs energy during energy storage period to the transformer and the same process arises in buck mode operation for primary side snubber as well. In intervals t_1-t_2 and t_3-t_4 this absorbed energy is dissipated. On the other hand choosing a low value snubber capacitor penalizes its ability to suppress over-voltages. So it is a trade-off between voltage spike and energy waste.

It can straightforwardly be seen in intervals t_5-t_6 and t_6-t_7 that diodes D_2 and D_4 create path not only to discharge of C_{s1} but also charge of C_{s2}. This means that energy absorption in the secondary side during intervals t_1-t_2 decreases while primary side snubber becomes ready for next energy take of from leakage inductance L_1.

Ideally, in a boost operation as long as duration of conduction of primary side switch Q_1 remains the same, peak primary side current, accordingly energy stored in leakage inductance remains the same. It has also been observed that at the end of each period, C_{s1} discharges more than previous period; eventually in steady-state zero volt so that voltage overshoots ratio due to primary side components gets lower. However increasing stress caused by the load capacitance voltage, keeps the all in all voltage spike getting higher but with less increment ratio.

Lastly, current paths created by diodes D_2 and D_4 (Fig. 2.13a and Fig. 2.13b) make the snubber network to involve in and lower the ringing caused by C_{OSS} of the switching devices and leakage inductances and so that ringing during the interval t_7-t_1 has lower amplitude and frequency.

2.6 Experimental Setup

To start with, firstly the design criteria then components of the converter are required to be selected. The converter is designed to work in discontinuous conduction mode boosting the voltage of DEAP generator from 500 V to 2 kV and then bucking it back to 500 V with maximum 15 A in the primary

side. Considering these criteria, maximum stress on the switching devices is found by (2.16) and (2.17).

$$V_{Q_{1(max\_CE)}} = nV_{C_D} + V_{DC} \tag{2.16}$$

$$V_{Q_{2(max\_CE)}} = \frac{V_{DC}}{n} + V_{C_D} \tag{2.17}$$

IGBTs that were used, are given in Table 2.2. According to (2.17) maximum voltage rating of secondary switch must be higher than maximum output voltage so that selected component fulfils the requirement.

Going on with the efficiency measurements, it is done by replacing the DC voltage source with a pre-charged capacitor as in Fig. 2.6 and estimating the energy flow in both end of the converter. Since the values of the capacitors are known, only needed parameters for the efficiency measurement are their voltages. Equation (2.18) is used to estimate the input and output energy of the converter during both boost and buck modes so that efficiency can be calculated by E_{out}/E_{in}.

$$\Delta E = \left| \frac{1}{2} C_{DC,D} (V_{\text{start}}^2 - V_{\text{end}}^2) \right| \tag{2.18}$$

In Table 2.2 three different capacitance values are given for $\mathrm{C_{DC}}$. It should be mentioned that depending on the amount of energy being transferred, different sized capacitors were used.

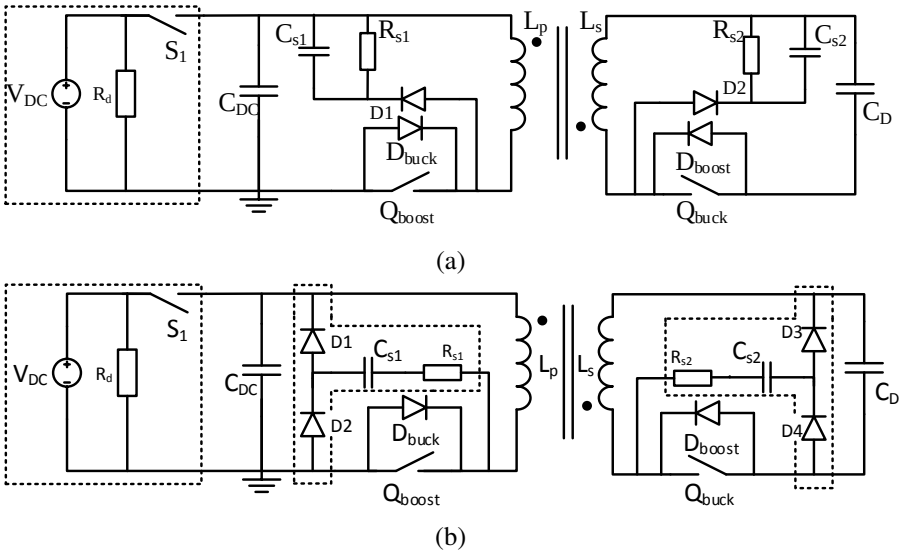


Figure 2.14: Circuit diagram of the test setup (a) with RCD (b) RCDD snubber network.

Fig. 2.14 illustrates the circuit diagram of the test setup and mechanical switch $\mathrm{S_1}$ is used to charge $\mathrm{C_{DC}}$ up to $\mathrm{V_{start}}$ voltage that was 400 V and after it is opened, boost and buck operations are performed successively.

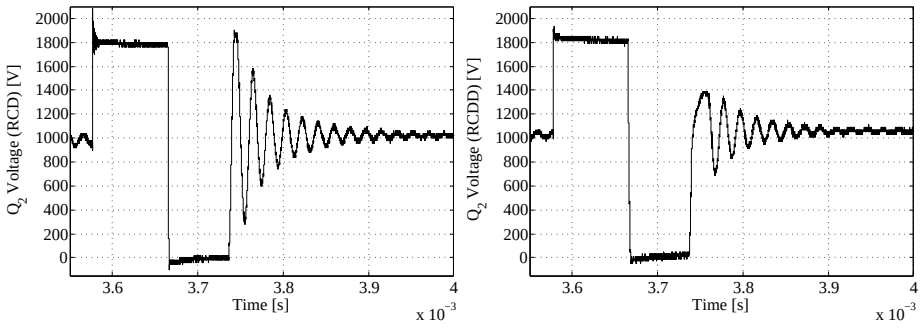
In order to operate the converter, a MATLAB® model was implemented and number of pulses were obtained at desired duty cycle, voltage and frequency. In this way the converter was run in open-loop

mode.

2.7 Test Results

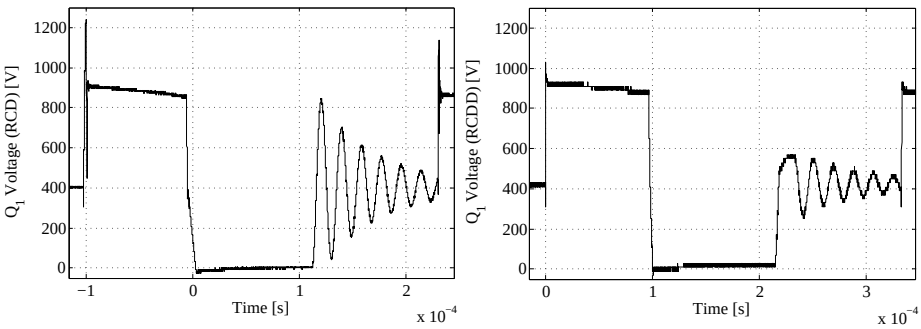
In this section along with the voltage waveforms of power switches, experimentally obtained converter efficiency by operating voltages at boost and buck mode working with 3 primary peak-current values (5, 10 and 15 A) are presented.

In Fig. 2.15 and Fig. 2.16 switching waveforms of IGBTs are given with RCD and RCDD snubber. For boost mode operation, last switching period of the secondary side IGBT Q_2 and accordingly for buck mode operation, first switching period of primary side IGBT Q_1 are illustrated, since the highest overshoot ratio occurs at these periods. It is clear in the figures that in spite of higher snubber capacitance in RCD snubber voltage spikes are higher. Herein series damping resistor of RCDD snubber plays a significant role. Another important point to realise in the figures, is ringing. Both frequency and amplitude of the ringing is dropped with RCDD network (Table 2.3).



(a) (b)

Figure 2.15: Experimental voltage waveforms of the secondary side switch Q_2 with (a) RCD snubber (b) RCDD snubber at boost mode operation.



(a) (b)

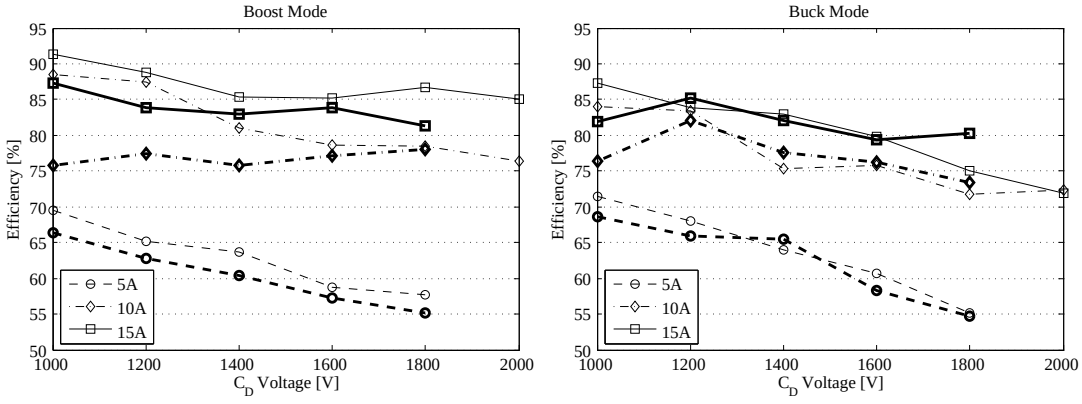
Figure 2.16: Experimental collector-emitter voltage waveforms of the primary side switch Q_1 with (a) RCD snubber (b) RCDD snubber at buck mode operation.

Table 2.3: Foremost values regarding to Fig. 2.15 Fig. 2.16.

	Fig. 2.15a		Fig. 2.15b		Fig. 2.16a		Fig. 2.16b	
Overshoot	2080	V	1930	V	1240	V	1030	V
Voltage	1800	V	1820	V	904	V	925	V
Ratio	15.5	%	6	%	37.16	%	11.35	%
Osc freq	48	kHz	26.6	kHz	52.7	kHz	35.94	kHz

In Fig. 2.17a and Fig. 2.17b, efficiency maps of the converter with RCD and RCDD snubber, are illustrated and maximum energy conversion efficiency for the boost mode is found to be 91.34 % and 87.3 % for the buck mode (with RCDD snubber). Before the operation starts, input voltage V_{DC} and output voltage V_{C_D} were set to 400 V and 500 V respectively. After every boost operation, converter working reference for buck operation was to lower the V_D voltage back to 500 V.

In the efficiency maps it can straightforwardly be noticed that at higher primary peak-current values efficiency is higher and it decreases by increasing operating voltage. This behaviour arises from decreasing number of pulses for higher current values and increasing number of pulses for higher voltage values. Switching losses of the used IGBT is remarkable.



(a) (b)

Figure 2.17: Experimentally obtained energy transfer efficiency map of the converter at (a) boost (b) buck mode operation. Thick lines and markers shows RCD snubber as well as thin ones RCDD.

Lastly, RCD snubber network passive component parameters are respectively 420 kΩ and 33 nF for primary side and 1.5 MΩ and 16 nF for secondary side. The parameters are based on 50 V clamp voltage ripple, in order to minimise energy waste by the clamp capacitor. Just as it is in interval t_1-t_2 of RCDD snubber, RCD snubber also draws energy during the energy storage period of flyback transformer. Furthermore the clamp voltage changes by the change of energy flow direction so that capacitor value is needed to be kept low. Eventually, the size of the capacitor is a trade-off between the energy loss and voltage spike.

2.8 Conclusion

Bidirectional flyback converter with proposed RCDD snubber has been presented and analysed in detail. The converter has demonstrated high efficiency at specific working point promising future. Decrement in efficiency by increasing number of pulses showed that for this particular converter, performance of switching devices plays a significant role.

On the other hand, proposed RCDD snubber exhibited expected behaviour by protecting the switching devices against voltage spikes and allowing them to work safely in the designed operating area. The experimental results shows that RCDD snubber network demonstrates better over voltage protection than RCD snubber with slightly higher converter efficiency in most of the operation points.

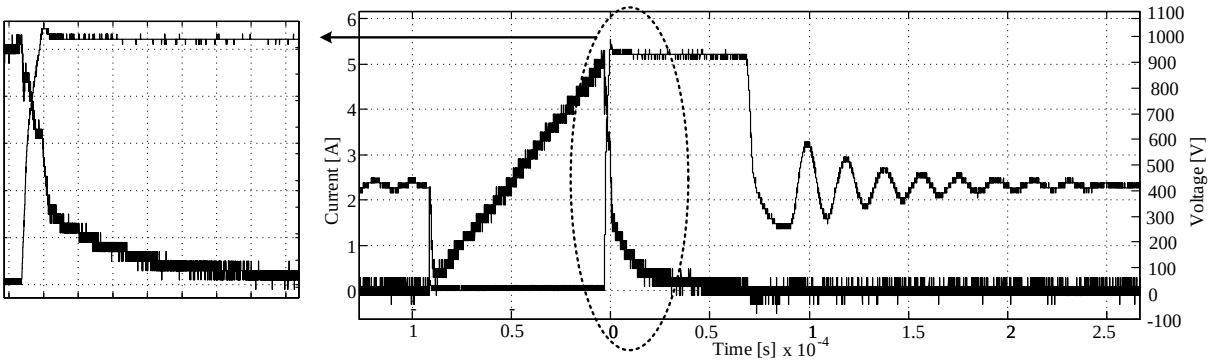


Figure 2.18: Turn-off voltage and current waveforms of used IGBT in bidirectional flyback converter. A magnification is done in the figure left to exhibit the tail current.

To return to the efficiency of the converter, as mentioned switching behaviour of IGBT has significant effect on the energy loss. In Fig. 2.18, experimental collector-emitter voltage waveform of primary side switch Q_1 with transformer current is shown. This measurement was taken while output voltage was 1040 V and peak collector current 5.2 A. Tail current that arises at IGBT turn-off can be seen clearly. Moreover this tail current flows while there is high voltage across the switch; in this example it is 920 V.

Therefore, in order to avoid this energy loss in the converter it was decided to replace the IGBTs with MOSFETs. In the following chapter, disadvantages of high-voltage MOSFETs are briefly mentioned and approaches to overcome, are treated.

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CHAPTER 3

Series Connection of MOSFETs

This chapter deals with the theory of series connection methods for MOSFET/IGBT. Note that the text will follow as if the methods are for MOSFET. Moreover the main source for this chapter is [1].

3.1 Introduction

It has been discussed in the previous chapter that some industrial applications requires high voltage power supplies. In some of these applications for example for electro active polymer, in spite of high voltage requirement, the current range is relatively low. Off-the-shelf power semiconductors that fulfil the voltage rating are normally designed for high power applications and introduces high switching losses that seize the big part of the energy transferred in DEAP application. These were mostly IGBTs and recently high-voltage MOSFETs, up to 4500 V, started being encountered in the shelf of electronic component distributors. However, cost of these MOSFETs are high and most importantly their on-state resistance which are typically in the range of several hundred ohms up to kilo ohms, makes them to become disinterested.

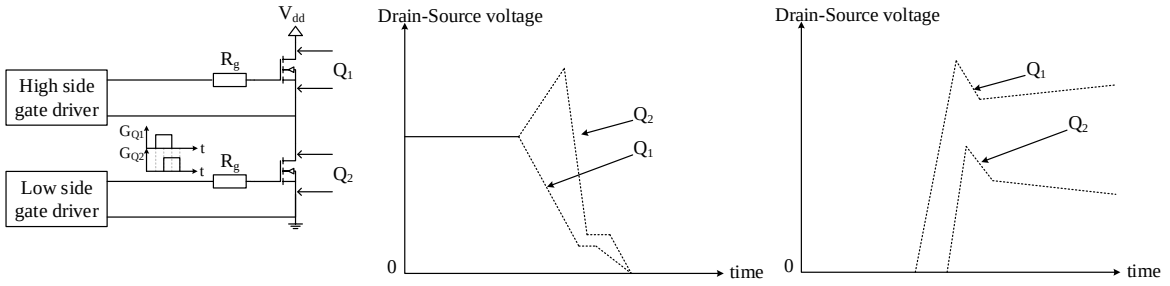
Eventually either for high or low power applications, various techniques have been used in order to use the low voltage rating switches in high voltage applications by means of series connection. In [1] a review and comparison of these techniques are discussed. In this study, while the most reasonable of these techniques are briefly mentioned, the utilized technique is handled in detail.

The main problem arises in series connection of the power semiconductors is unequal voltage share. Since the operating voltage would be higher than individual voltage rating of each switch, unequal voltage share may firstly cause failure of one or more, subsequently all the switches in the stack.

This voltage unbalance is mainly due to device parameter spread and gate signal mismatches [1]. Device parameter spread issues originate from deviation of parasitic parameters of semiconductor switch

such as gate-to-source or gate-to-drain capacitance or both [2]. Gate signal mismatches may arise from various reasons for example, parasitics and response of gate drive units, propagation delays, parasitic leakage inductances, EMI and so on.

Voltage share of series connected semiconductors can be discussed under two category as transient and steady-state voltage sharing. In Fig. 3.1 both of these problems are illustrated. Firstly, in Fig. 3.1a a simplified schematic of two series connected MOSFET is given. It is assumed that there is a delay between gate signals i.e. gate signal of the upper switch Q_1, is leading. In this case, as in Fig. 3.1b, turn-on transition of Q_1 starts earlier than Q_2 and while drain-source voltage of Q_1 is dropping, rest of the supply voltage V_{dd} is blocked by delayed switch. Depending on length of the delay, this situation may cause failure of, first delayed then the leading switch. In turn-off transition of the switches as in Fig. 3.1c similar problem is also a matter of discussion but this time the hazard is there for leading switch.



(a) (b) (c)

Figure 3.1: Series connected (a) two MOSFET and (b) turn-on (c) turn-off transient drain-source voltage waveforms of the switches.

In Fig. 3.1c, unbalanced steady-state voltage sharing can also be seen after the switch turn-off transition. While drain-source voltage of one switch increasing, the other ones is decreasing. This unrestrained ascent across Q_1 may eventually end up with the switch failure.

3.2 Steady-state voltage sharing

The steady-state unbalanced voltage share is due to unequal off-state impedance of semiconductor switch [3]. Mainly, off-state impedance depends on drain-to-source voltage and the junction temperature of the MOSFET device. If this impedance is considered in terms of leakage current, they are inversely proportional to each other. In this case, examining the leakage current would be much clear. In Fig. 3.2a equivalent circuit of two stacked MOSFETs is illustrated.

In [4] it has been stated that a common rule of thumb for leakage current is, it doubles for every 10°C. Mathematically sub-threshold leakage current can be expressed by (3.1).

$$I_{sub} = I_0 e^{\frac{V_{gs}-V_{th}}{nV_T}} \left[1 - e^{-\frac{V_{ds}}{V_T}}\right] \tag{3.1}$$

$$I_0 = \frac{W\mu_0 C_{ox} V_T^2 e^{1.8}}{L} \tag{3.2}$$

Substituting (3.2) into (3.1) and assuming V_{GS} is zero[1] OFF state leakage current yields;

$$I_{off} = \frac{W\mu_0 C_{ox} V_T^2 e^{1.8}}{L} \frac{1}{e^{\frac{V_{th}}{nV_T}}} \left[1 - \frac{1}{e^{\frac{V_{ds}}{V_T}}}\right] \tag{3.3}$$

Here, I_0 is the reverse saturation current, V_T=KT/q is the thermal voltage, V_{th} is threshold voltage of MOSFET, V_{ds} and V_{gs} are respectively drain-to-source and gate-to-source voltages, W and L are effective transistor width and length, C_{ox} is gate oxide capacitance, μ_0 is carrier mobility and finally n is the sub-threshold swing coefficient. As well as dependency of leakage current to drain-to-source voltage, it can be seen that I_0 is responsible for exponential temperature dependence. It can be concluded that higher the junction temperature means higher leakage current. And considering the parasitic diode of MOSFET which is reverse biased, therefore substituting V_{DS} with negative polarity makes the conclusion in (3.4).

$$I_{off1} < I_{off2} \Leftrightarrow V_{DS1} > V_{DS2} \tag{3.4}$$

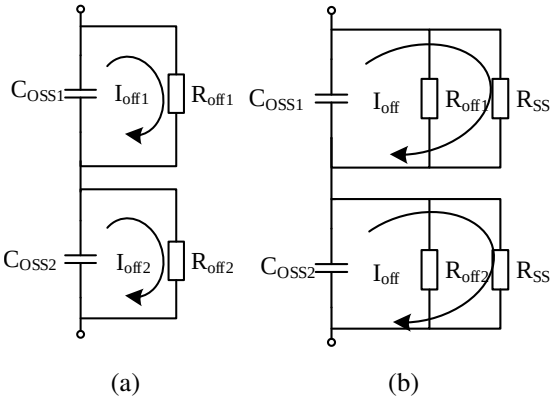


Figure 3.2: Equivalent circuit of two MOSFETs (simplified) connected in series (a) with no balancing resistor (b) with steady-state balancing resistor.

From the analysis it can be understood that, if one of the MOSFET in the stack senses lower voltage than the other one, output capacitances of the MOSFETs will dis/charge and with the tendency of equalizing their leakage current, so that a huge voltage unbalance will occur. In order to avoid this situation, steady-state balancing resistors are used in parallel with serialized switching devices as in Fig. 3.2b. The value of this resistor must be such that it will dominate the parallel impedance. A rule of thumb is to use resistors with the value of 10% of the minimum off-state impedance in order to obtain dominance [5].

[1]Even though gate-to-source voltage is not zero but below threshold voltage V_{th}, it means the MOSFET is in OFF state, prime of exponential part becomes negative so that it can be written as denominator by changing the prime sign to positive as it is done in (3.3).

3.3 Transient voltage sharing

Looking to voltage transients of serialized semiconductor switches, two main things stand out. Beginning of the transients and the slope of the voltages. Either of them may cause switch failures individually.

To start with, a mismatch in gate signal timing will start the turn-on voltage transition of the leading signal switch, earlier than lagging one, resulting to have risk of failure. This was illustrated in Fig. 3.1. On the other hand, in spite of synchronised gate signals, a mismatch in voltage transition slope means different rate of voltage change. Eventually slope mismatch ends up again failure.

There are several factors that effect the voltage transition slope in a MOSFET. They can be named as differences in MOSFET parasitic capacitances (see Fig. 3.3), transfer characteristics, mismatched gate resistance; current and voltage. By means of (3.5) these factors are more apparent [6].

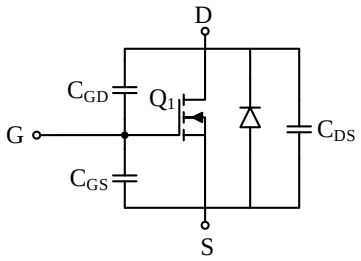


Figure 3.3: A simple representation of MOSFET with parasitic capacitances.

$$\frac{dv_{DG}}{dt} = \frac{dv_{DS}}{dt} = \frac{i_G}{C_{GD}} = \frac{V_{GG} - V_{GS,I_0}}{R_G C_{GD}} \tag{3.5}$$

Here, V_{GG} is applied gate voltage, V_{GS,I_0} is gate source voltage at full load current, C_{GD} is gate-to-drain (Miller) capacitance, R_G is gate resistance and i_G is gate current.

3.4 Methods for series connection of MOSFETs

In industry and research area different methods are encountered for series connection of MOSFETs. These methods can be classified as passive snubber, voltage clamping and active gate control circuits. A review of them is given in [1]. In the following subsections, main ideas behind these three classes are treated.

3.4.1 Passive snubber methods

Passive snubber methods are the most popular ones among the serialization techniques [1]. Just as in RC snubber that has been discussed in Chapter 2, snubber network controls the rate-of-rise of the voltage across the MOSFETs. In one side this method is reliable, introducing good voltage balance and easy to

use, on the other side snubber network losses are very high, switching characteristics are slowed down and the operation frequency is limited [1].

3.4.2 Voltage clamping methods

This method is based on limiting the maximum allowable drain-to-source voltage by means of zener diode. The technique introduce higher power loss since the first clamped device is exposed both higher current and voltage until the turn-off of the other switches. In spite of improved techniques in order to lower the power loss of the devices, method is limited by zener diode voltage rating which is maximum 330 V on the shelf of suppliers.

3.4.3 Active gate control methods

There are many different approaches in this technique. Unlike the other ones, the difference in these methods is to interfere to the gate signal of the switch. The approaches could be based on gate balancing core, feedback loop or even 'resistors capacitors and a diode'. The most representative approach 'gate balancing core' is treated in the next section.

3.5 Gate balancing core method

In this method, as it is illustrated in Fig. 3.4, gate wires of the series connected switches are magnetically combined by means of a core. The technique was first proposed in [7] with 4 series connected 2.5kV/1.8kA flat-packaged IGBTs in a two level inverter. As the study demonstrated good results in transient voltage sharing, steady-state voltage sharing is done by parallel balancing resistors R_{ss} (Fig. 3.4).

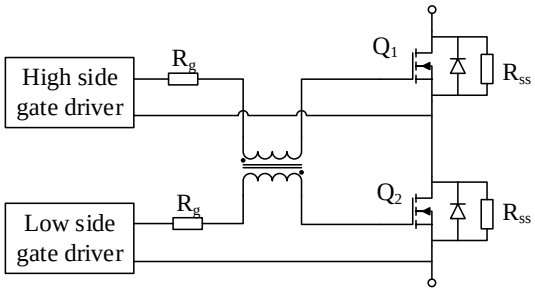


Figure 3.4: Two series connected MOSFET with gate balancing core.

The gate balancing core has windings with the turns ratio of one-to-one (1:1) and since two switch is coupled by one core, for n number of switch $(n-1)$ transformer is need. The idea of this core is to balance the gate currents whenever there is a delay between the gate signals either at turn-on or turn-off.

Assuming that gate signal of high side MOSFET Q_1 is leading by the difference in time ΔT_{on}, equivalent circuit during turn-on transition is depicted in Fig. 3.5 where; L_{lk1} and L_{lk2} are leakage inductances and L_m magnetizing inductance of the gate balancing core, C_{iss1} and C_{iss2} are input capacitances of the switches, V_F and V_R bias voltages of the gate driver units (GDU) and $R_{g(on)}$ and $R_{g(off)}$ gate resistors. It should be noted that in this figure for the purpose of clear image high side switch input capacitance is

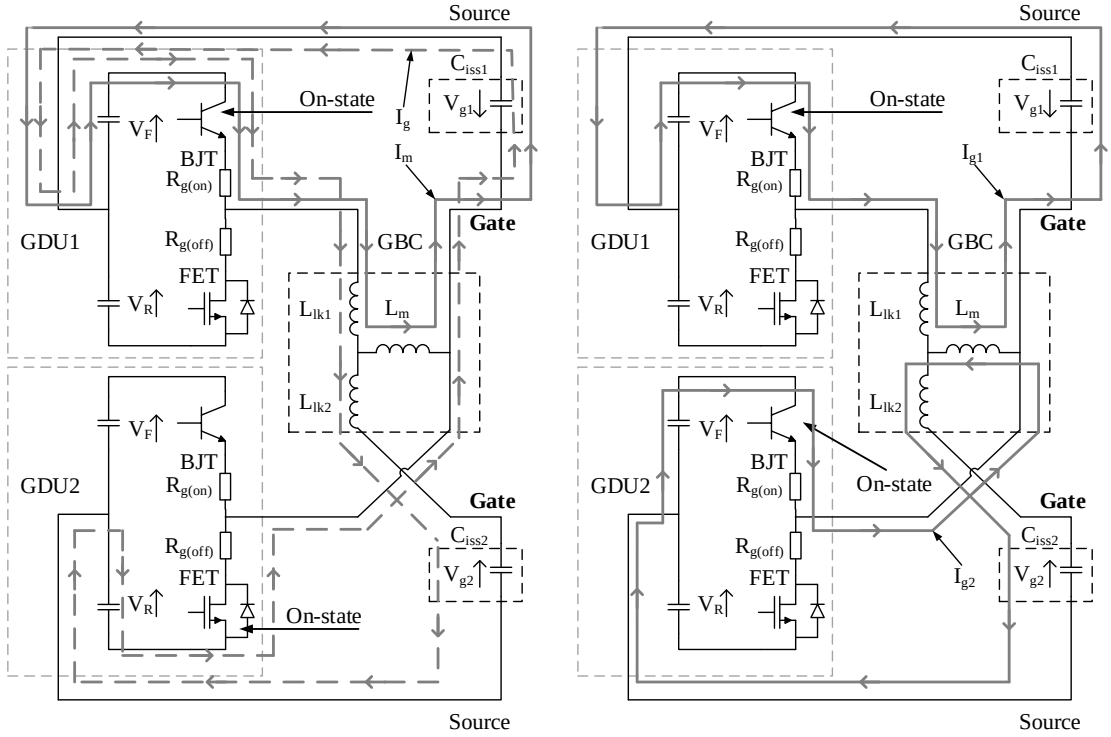


Figure 3.5: Equivalent circuit for turn-on transition of two stacked MOSFET with gate balancing core (a) during ΔT_{on} (b) after ΔT_{on}. (GBC: Gate balancing core).

represented upside-down.

To start with Fig. 3.5a, in this state, as aforementioned, the gate signal from GDU1 is leading. This means that while in GDU1, BJT is on, in GDU2 it is FET. In this case a part of the current supplied by the GDU1, I_g, charges C_{iss2} and C_{iss1} is charged by the sum of I_m and I_g resulting to be faster and causing voltage unbalance. The difference between gate-to-source voltages depends on charge of C_{iss1} by I_m [8]. In order to synchronize the signals at turn-on, the difference between gate-to-source pins should be determined as V_{GS1} nearly equals to V_{GS2} [7]. For fulfilment of the above mentioned requirement (3.6) is derived in [8].

$$L_m \geq \frac{\Delta T_{on}^2}{0.02 \cdot C_{iss}} \tag{3.6}$$

After ΔT_{on}, each switch is fed by their own gate driver unit with the currents of I_{g1} and I_{g2}. Since these currents are equal, the balance between two switches are now achieved [7]. However as this state can be seen in Fig. 3.5b, the leakage inductances of the gate balancing core create an RLC circuit where the damping ratio is given in (3.7). So, to prevent the oscillations in gate currents properly, $\zeta \leq 0.7$ should be determined. Thus (3.8) is obtained.

$$\zeta = \frac{R_g}{2}\sqrt{\frac{C_{iss}}{L_{lk1,2}}} \tag{3.7}$$

$$L_{lk1} = L_{lk2} \leq \frac{C_{iss} R_g^2}{1.96} \tag{3.8}$$

To sum up, gate balancing core method includes only one extra element to the circuitry and it does not introduce any notable losses [2]. Previous studies in [2, 7] verified that technique ensures acceptable transient voltage sharing. On the other hand, gate balancing core manages only with the gate signals without keeping an eye on the voltage across the switches. The disadvantage shines out that mismatches caused independent from gate signals, for example unequal junction temperature, cannot be prevented.

3.5.1 Effect of interwinding capacitance of gate balancing core

So far, the theory that has been documented in [8] was followed and that study was originally done for IGBTs connected in series. According to [5] where two Si MOSFETs were connected in series, it was documented that interwinding capacitance C_w, in gate balancing core has significant influence on transient voltage sharing. In Fig. 3.6[2] this interwinding capacitance is represented as a lumped component which, in reality, is distributed along the transformer windings.

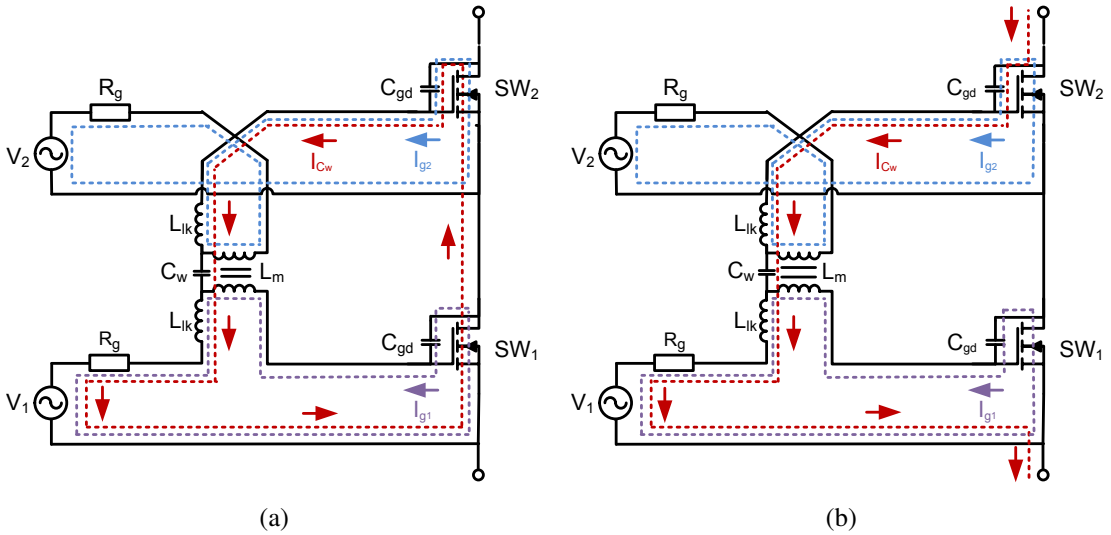


Figure 3.6: Interwinding capacitance current path during (a) turn-on (b) turn-off.

To start with turn-off, gate-to-source voltages of the switches start to decrease and when they clamped to the plateau voltage, drain-to-source voltages of the switches start to build up. The current paths regarding to this stage, are illustrated in Fig. 3.6b. As it can be seen C_w charges up thorough miller capacitance of upper-side MOSFET. Then C_w remains charged until the turn-on stage. At turn-on transition, when gate-to-source voltage is clamped to plateau voltage, interwinding capacitance is shorted through the path which is shown in Fig. 3.6a [5].

The conclusion was made in [5] that charging and discharging process of C_w, distort the gate currents of MOSFETs in switching transitions which results in distorted dynamic voltage distribution. The analysis documented that the gate balancing core should be designed such that value of interwinding

[2]Fig. 3.6 was taken from the mentioned reference [5] and arrows indicates the positive current direction.

capacitance should be less than 1% of minimum miller capacitance. Additionally, gate resistor of upper switch was placed between gate balancing core and MOSFET as an optimization in order increase the damping ratio of RLC circuit that is formed on the current path of interwinding capacitance.

3.6 Conclusions

In this chapter series connection methods for MOSFETs was handled. Factors that cause problems in stacked switches were enlighten, main ideas of solution approaches were discussed. Eventually series connection of two SiC MOSFETs was decided to be experimented by means of gate balancing core method.

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CHAPTER 4

Experiments with gate balancing core

In this chapter experiments and debug process regarding to series connection of MOSFETs by means of gate balancing core method are conducted. Two silicon carbide (SiC) MOSFET of Cree® C2M1000170D were selected for series connection due to its voltage rating of 1.7 kV.

4.1 Introduction

Before starting the test, the technique was needed to be verified. The gate balancing core technique, as mentioned, introduces only one extra component to the circuitry which is the transformer. The journey begins with the design of this transformer. Subsequently, the experiments were run with the setup that simplified version is illustrated in Fig. 4.1. The circuit is basically operating as a step-down converter that MOSFET stack senses V_{DC1} at turn-on and $V_{DC1+DC2}$ at turn-off, assuming the ideal case.

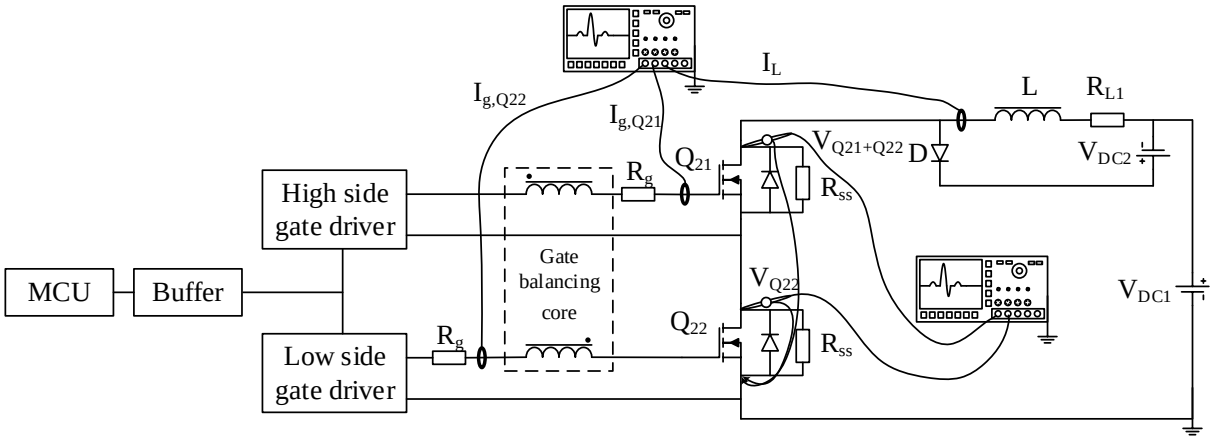


Figure 4.1: Simplified test setup for gate balancing core technique where two MOSFET is connected in series.

The inductor L, in Fig. 4.1 was gotten from laboratory of Aalborg University and its inductance and winding resistance (R_{L1}) were measured to be 5.24 mH and 3.93 ohm respectively. Diode D is Cree®

C3D10170H SiC schottky diode with the blocking voltage of 1700 V and repetitive peak forward surge current of 45 A. Selected SiC MOSFET Cree® C2M1000170D, has ratings that have been given in Table 4.1 and finally gate drivers are Avago® ACNV3130 with 2.5 A maximum peak output current and maximum working insulation peak voltage of 2262 V.

Table 4.1: Foremost parameters of Cree® C2M1000170D.

Continuous drain current	I_{ds25}	4.9 A	Input capacitance	C_{iss}	191-220pF
Drain-to-source breakdown voltage	$V_{(BR)DSS}$	1700V	Output capacitance	C_{oss}	12-170pF
Gate threshold voltage	$V_{GS(th)}$	2.0-2.4 V	Miller capacitance	C_{gd}	1.3-35pF
Zero gate voltage drain current	I_{DSS}	30-100nA	Drain-to-source on resistance	$R_{DS(on)}$	0.95-1.1ohm

Parameters regarding to gate balancing core and steady-state resistors will be discussed in the following sections.

4.2 Steady-state voltage sharing resistors

Previously it has been discussed that in order to obtain a dominant off-state impedance across each serialized switch, balancing resistors R_{ss} are required to be 10% of off-state impedance of the switch. According to the datasheet of the selected MOSFET, parameter zero gate voltage drain current I_{DSS} given in Table 4.1 was measured while drain-to-source voltage is 1700 V and junction temperature 25°C and 150°C. Assuming the worst case scenario, the off state impedance R_{off} can be estimated 17 giga-ohms as in (4.1).

$$R_{off} = \frac{V_{(BR)DSS}}{I_{DSS}} = \frac{1700}{100 \times 10^{-9}} \left[\frac{\mathrm{V}}{\mathrm{A}}\right] = 17[\mathrm{G}\Omega] \tag{4.1}$$

In this case maximum 1.7 giga-ohms or as a more practical value 1 giga-ohms would be enough. However LeCroy® probes that were used have 50 mega-ohms impedance. In Fig. 4.1 it has been shown that the measurements were done with respect to the ground so that drain-to-source voltage of Q_{21} is found by mathematical function of oscilloscope by subtraction of two measured waveforms.

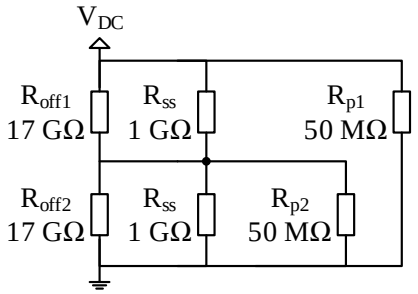


Figure 4.2: Steady-state equivalent circuit of the stacked MOSFET with probes connected.

It can straightforwardly be understood that probes will dominate the voltage sharing. The equivalent circuit of the off-state impedances is illustrated in Fig. 4.2 and this makes sum of two R_{ss} required to be less than 5 mega-ohms (2.5 MΩ each) in case probes are used. During the experiments in order to obtain

a quick steady-state voltage sharing 33 kilo-ohms power resistors were used as the focus was given to transient voltage sharing.

4.3 Design of gate balancing transformer

Design of the gate balancing transformer begins with the calculation of the necessary transformer parameters that fulfil the requirements mentioned in Section 3.5. The first aim was to obtain leakage inductance. Based on (4.2) Fig. 4.3 is generated. It can be seen that higher the gate resistance higher the leakage inductance requirement which is easier to obtain. However increasing gate resistance means increasing switching losses. Assuming 51 ohm gate resistance, needed leakage inductance is computed to be approximately 253 nH.

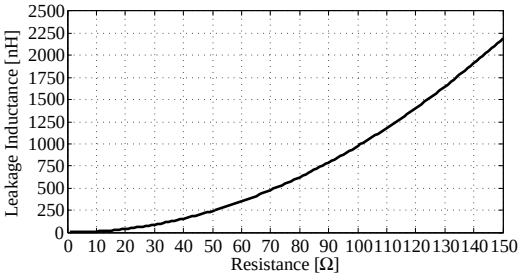


Figure 4.3: Gate balancing core leakage inductance requirement by gate resistor for ζ=0.7.

$$L_{lk1} = L_{lk2} \leq \frac{C_{iss} R_g^2}{1.96} \text{ [H]} \tag{4.2}$$

On the other hand in subsection 3.5.1 the importance of interwinding capacitance was discussed. In Table 4.1 it was given that the miller capacitance of the selected MOSFET is maximum 1.3 pF. In this case, as mentioned, 1% requirement is 13 fF. In [1] the trade-off between leakage inductance and interwinding capacitance is mentioned as "*Transformer leakage inductance and capacitance have an inverse relationship: if you decrease the leakage inductance, you will increase the capacitance; if you decrease the capacitance, you increase the leakage inductance*".

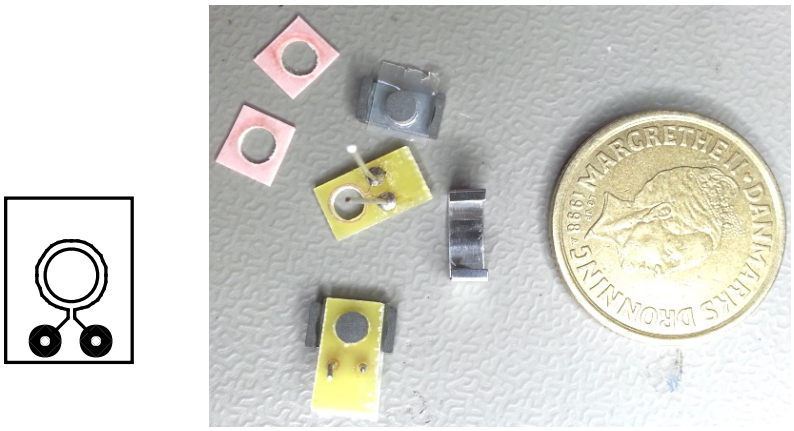
$$C = \frac{\pi . \varepsilon . \varepsilon_0 . l}{\ln\left(\frac{d}{\sqrt{r_1 . r_2}}\right)} \text{ [F]} \tag{4.3}$$

In (4.3), capacitance formula[1] of two parallel rods is given. Here, ε_0 is permittivity of free space[2], ε is relative dielectric constant of the insulation, d is center-to-center seperation of rods and $r_{1,2}$ radius of the two rods. In order to make a simple and quick approximation, this equation can be used considering only one turn in primary and secondary windings. It is now apparent that capacitance is directly correlated with dielectric constant of material between windings, which is in this case insulation and air and length of the windings while it decreases by increment of distance in between and reduction of wire radiuses. After building and measuring transformers[3] with various cores and windings final candidates were planar ER9.5 and ER11 ferrite cores (3F3). To be able to maximize the distance between windings and minimize the winding width, printed circuit board with single turn was designed (Fig. 4.4).

[1] This equation is simplified assuming that the distance from center-to-center of two rods is large compared with their radius [2].

[2] Permittivity of free space $\cong 8.85 \times 10^{-12}$ F/m

[3] The transformer parameters were measured at 5 kHz and 1 V amplitude with Wayne Kerr Precision Magnetics Analyzer - 3260B that is offering measurement range of 0.1 nH-1000 H for inductance and 5 fF-1 F capacitance



(a) (b)

Figure 4.4: (a) PCB layout and (b) a view of pieces gate balancing core.

Measured core parameters are given in Table 4.2. Even though the necessary interwinding capacitance is not reached it was decided to move on series connection experiments and investigate the effects.

Table 4.2: Measured parameters of transformer with ER11 and ER9.5 planar core.

ER11 (3F3)				ER9.5 (3F3)			
L_{lk1}	309 nH	C_w	0.21 pF	L_{lk1}	420 nH	C_w	0.26 pF
L_{lk2}	254 nH	L_m	18.3 uF	L_{lk2}	480 nH	L_m	10 uF

4.4 Experiments with gate balancing core

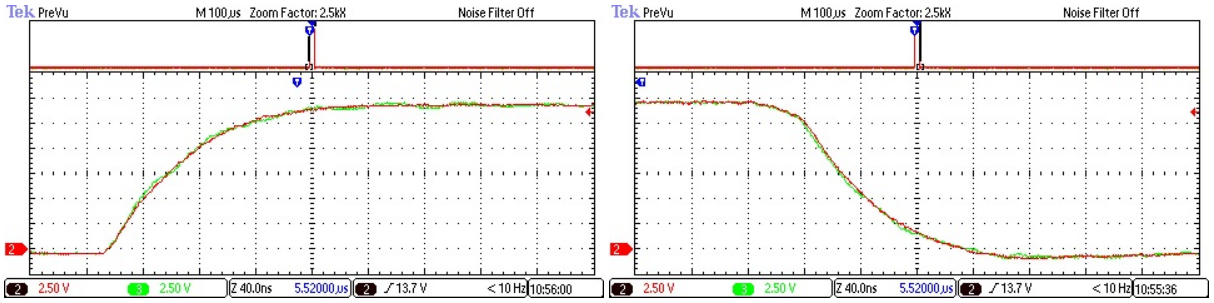
This section consists of the efforts and experiments that were performed. The simplified test setup was already given in Fig. 4.1. Following components and instruments were used which is not defined in the figure for a simple view.

- MCU—Texas Instruments® Stellaris MicroController Unit LM3S9B92
- Buffer—Texas Instruments® SN74LVC1G34 non-inverting buffer
- Gate driver—Avago® ACNV3130.
- Power supply for buffer and gate driver—GW Instek® GPS-4303

The DSP that was used has 3.3 V output voltage with 2 mA 4 mA and 8 mA pad drive for digital communication and up to 4 pads 18 mA for high-current applications [3]. However used gate driver which has maximum working insulation voltage of 2262 V, requires input forward voltage in the range of 1.2∼1.95 V (typically 1.6 V) with the current of 12∼16 mA [4]. Since two gate drivers are used a buffer was used which has 24 mA output drive current at 3.3 V [5]. Finally, the power supply has the feature of four independent isolated output which was needed [6].

4.4.1 Problem with driving high side MOSFET

When the test setup was ready to run, firstly the gate signals needed to be checked. Waveforms were observed respectively at the output of MCU, buffer and gate-to-source pins. In Fig. 4.5 captured gate-to-source voltages of the switches are shown without applying voltage across drain-to-source pins. The measurements were taken by LeCroy® high-voltage passive probes between the gate-to-common source[4].



(a) (b)

Figure 4.5: Gate-to-common source voltage waveforms of the MOSFETs (a) at turn-on and (b) at turn-off without drain-to-source voltage. Green waveform is V_{GS_{common},Q_1} and red one is V_{GS,Q_2}.

However when the setup was run, drain-to-source voltage of upper side MOSFET Q_{21} was captured so that it was switching whole DC-link voltage while the lower side MOSFET Q_{22} has almost zero voltage across its drain-source pins. Finding no error on PCB led the investigation to the gate driver and power supply.

In Fig. 4.6 it can be seen that when the MOSFET is turned-off, gate pin is connected to the source through the FET device. Speaking for inductive switching, as it is thoroughly explained in [7] that drain-to-source voltage starts to fall when gate-to-source voltage clamps to plateau voltage. This means that if source pin of MOSFET is not at zero potential, until the miller effect, the potential of gate pin must be higher then source so that gate-to-source capacitance voltage. Moreover during and after miller effect the potential difference between gate and source pins must be in the safe region in order not to fail the MOSFET. The same process must be followed during turn-off.

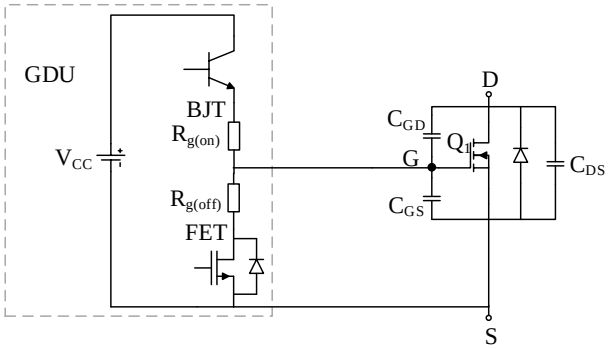
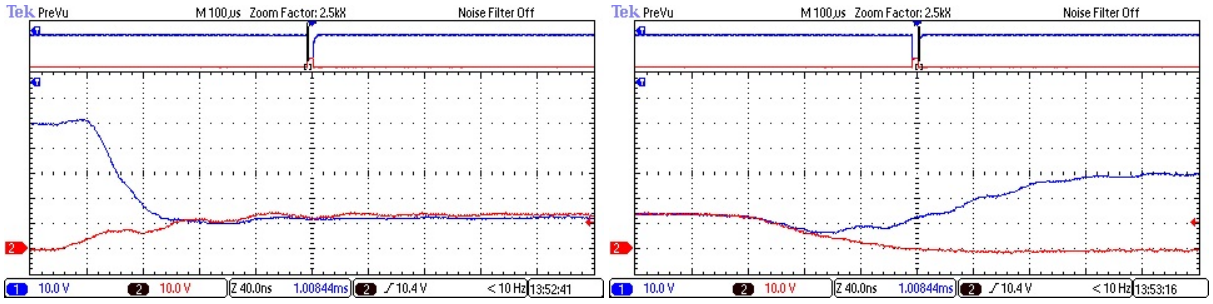


Figure 4.6: A simplified view of gate driver connected to a MOSFET.

[4]The term "common source" is used to indicate source pin of lower side MOSFET i.e. Q_{22} since passive probes were used.

After the above information, it was understood that either the power supply of gate driver must be able to float or one of high-side MOSFET driving techniques i.e. charge pump or bootstrap must be utilized. This showed that GW Instek® GPS-4303 power supply is not able to float so that it is keeping the source pin of Q_{21} switch around zero potential. It also clarifies why no voltage observed across drain-source pins of Q_{22} switch.

As a practical solution Traco Power® TMA 0515S miniature, 1 kV I/O isolated, 1 W DC/DC converter was used. New waveforms are exhibited in Fig. 4.7.



(a) (b)

Figure 4.7: Gate-to-common source voltage waveforms of the MOSFETs (a) at turn-on and (b) at turn-off with 100 V across the MOSFET stack. Blue waveform is V_{GS_{common},Q_1} and red one is V_{GS,Q_2}.

4.4.2 Voltage oscillations across MOSFET stack

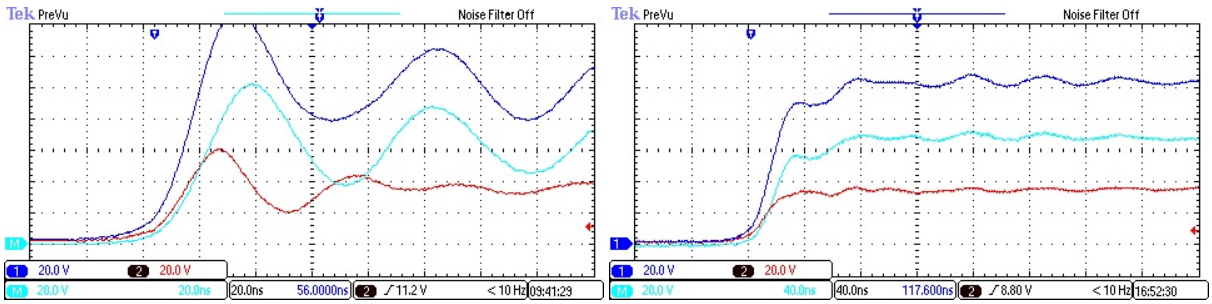
Firstly, in order to see the behaviour of test setup an experiment was conducted with 100 V at DC-link. As it can be seen from Fig.4.8a where drain-to-source voltage waveforms across the MOSFETs and stack are shown, there is a high voltage overshoot and oscillations. From (4.4) inductance was estimated as 20 μH with 6 pF capacitance[5] and 70 ns oscillation period. PCB trace length from anode of the anti-parallel diode across the inductor (see Fig. 4.1) is 5.2 cm. Following the rule of thumb as 10-15 nH/cm it was clear that issue didn't arise from PCB.

$$L = \frac{T^2}{4\pi^2.C} \tag{4.4}$$

Since the problem didn't arise from PCB, DC-link cable became the interest. Connecting 117.5 μF bypass capacitor right before the DC-link connection to the PCB minimised the oscillations that can be seen in Fig. 4.8b. Additionally, length of cables to the gate drivers from power supply and traco power was minimized and their 100 nF bypass capacitors were replaced by 2 μF non-polarized capacitors.

Even though the voltage overshoot and oscillations didn't effect the transient voltage sharing, the possibility of switch failure at higher voltage tests due to voltage spike was prevented.

[5]Here, it was assumed that output capacitance of each MOSFET which is given as 12 pF in the datasheet, are equal and connected in series being 6 pF equivalent. No doubt that the output capacitances of MOSFET are not the only parasitic capacitance in the setup. Moreover the assumtion was done in order to make a fast identification of the origin of oscillations.



(a) (b)

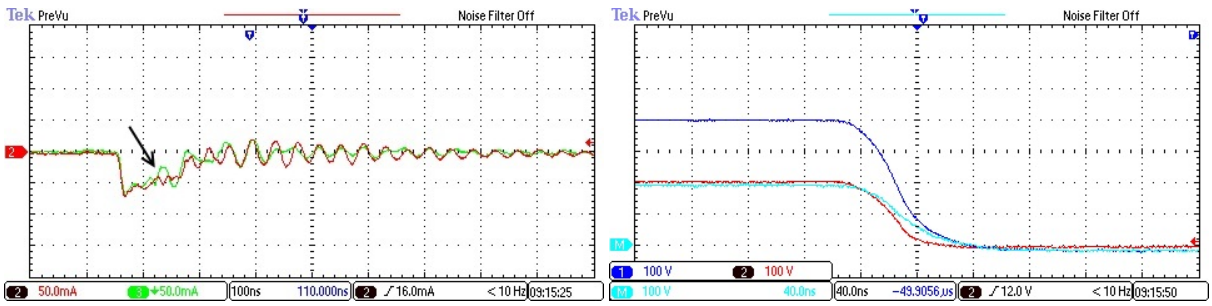
Figure 4.8: Oscillations across the MOSFETs and stack (a) before and (b) after DC-link capacitor. Blue waveform is across the stack as well as turquoise is drain-to-source voltage of Q_{21} and red is Q_{22}. R_g=100 ohm.

4.5 Low voltage tests (400 V)

This chapter houses the tests were done 400 V across the MOSFET stack with different gate balancing cores and 100 ohm gate resistors. Used Traco Power® DC/DC converter has 15 V output therefore the lower side MOSFET gate driver was fed by GW Instek® power supply with 15 V. In order to observe the gate currents, one leg of each gate resistor were extended with a winding cable. In spite of the fact that measuring gate current will increase the series inductance introduced to the gate current path due to the jaw of current probe needs a cable to pass inside, for debugging process decision was found to be fair enough.

4.5.1 Test with ER9.5(3F3) core

The parameters of gate balancing core constructed by ER9.5 (3F3) was previously given in Table 4.2. Fig. 4.9 represents the turn-on gate currents (Fig. 4.9a) and drain-to-source voltages (Fig. 4.9b). As mentioned, these current waveforms were captured on the gate resistors so that on the high side the resistor was placed between the gate balancing core and MOSFET while it was between gate driver and core in the low side. Accordingly, in Fig. 4.9a green waveform belongs to high side MOSFET Q_{21} and red one low side MOSFET Q_{22}. For the waveforms in Fig. 4.9b, blue waveform shows the voltage across the MOSFET stack as well as red one shows drain-to-source voltage of Q_{22}. Thus drain-to-source voltage waveform of Q_{21} was obtained by subtraction of these two waveforms which is turquoise.

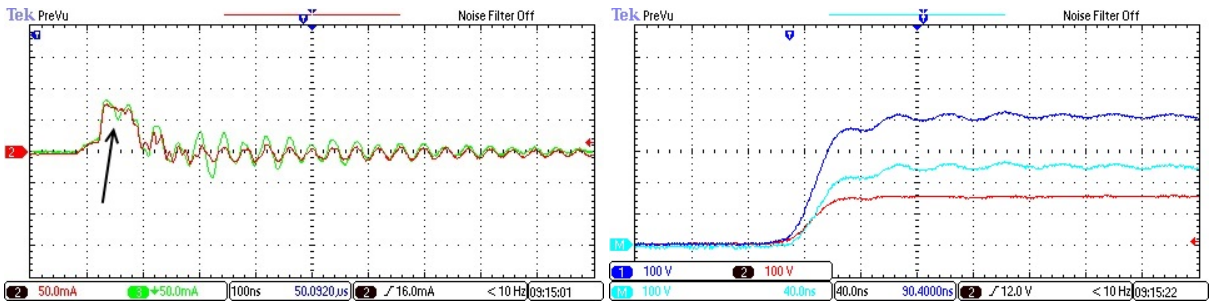


(a) (b)

Figure 4.9: Turn-on waveforms regarding to test with ER9.5 core while DC-link voltage is 400 V; (a) gate currents (b) drain-to-source voltages.

It can be straightforwardly seen that at turn-on transition voltage share was unsuccessful. The gate current unbalance, which occurred at the moment that is shown by arrow in Fig. 4.9a, resulted in unequal voltage distribution across the individual MOSFETs. Current degradation shown by arrow, causes Q_{21} to turn-on later than Q_{22}. Additionally, oscillations in current waveforms are remarkable.

Fig. 4.10 contains the current and voltage waveforms during turn-off transition. Again, as it was in turn-on, there is a current mismatch. Another point to notice in Fig. 4.10b is that drain-to-source voltage of Q_{21} starts to rise with a delay however with a bigger slope, so that the transition ends up with approximately 90 V difference across the switches.

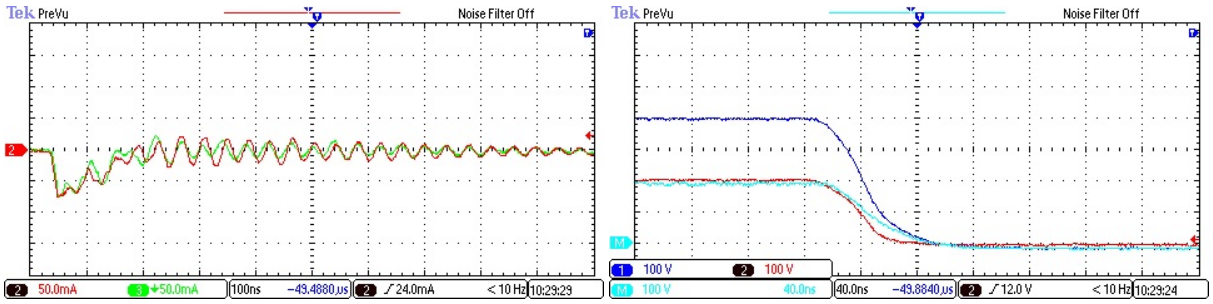


(a) (b)

Figure 4.10: Turn-off waveforms regarding to test with ER9.5 core while DC-link voltage is 400 V; (a) gate currents (b) drain-to-source voltages.

4.5.2 Test with ER11(3F3) core

In Section 3.5.1 the effect of interwinding capacitance was discussed. Even though the difference between the interwinding capacitances is not so high, it was decided to test the gate balancing core made by ER11(3F3) and experiment the possible differences. Additionally, in [8] it has been analysed that magnetizing inductance of the gate balancing core should be sized based on the delay between gate signals. Making use of the given equation (3.6) for 8 ns delay which was what measured, minimum required magnetizing inductance is found to be approximately 17 μH. As it was given in Table 4.2, magnetizing inductance of the gate balancing core with ER11 core was measured to be 18.3 μH



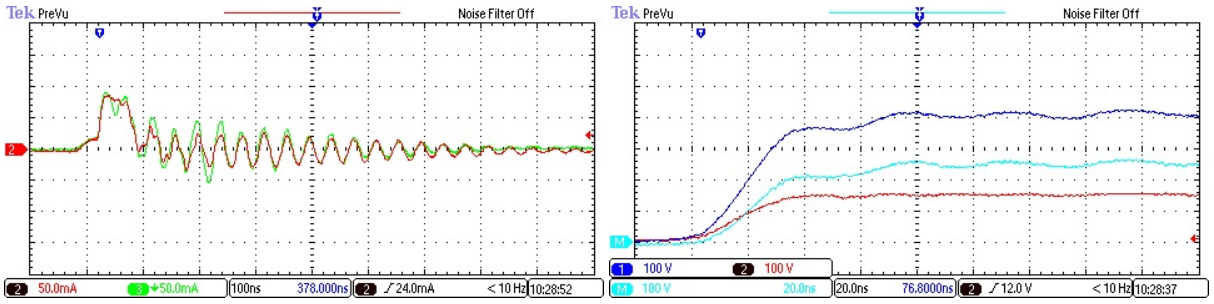
(a) (b)

Figure 4.11: Turn-on waveforms regarding to test with ER11 core while DC-link voltage is 400 V; (a) gate currents (b) drain-to-source voltages.

In Fig. 4.11 turn-on current and voltage waveforms are given. Fig. 4.11b shows that turn-on voltage

share between the switches is slightly better. However the delay between the signals still can be observed.

In Fig. 4.12 oscilloscope display images of the same test during turn-off transition are illustrated. It can be concluded that parameters of ER9.5 and ER11 core was close and didn't make any significant effect. Nevertheless, following the theory that was mentioned in [9], less interwinding capacitance and higher magnetizing inductance, it was decided to move on with this core (ER11).



(a) (b)

Figure 4.12: Turn-off waveforms regarding to test with ER11 core while DC-link voltage is 400 V; (a) gate currents (b) drain-to-source voltages.

To wrap up the progress made can be summarized as follows;

- Two gate balancing transformer made by ER9.5 and ER11 both 3F3 material were tested at 400 V volt across the MOSFET stack. Gate currents of both MOSFET were synchronised until the moment when current mismatch occurred. This moment corresponds to the plateau effect and this current unbalance seems to be the main origin of the unbalanced voltage share at turn-on and turn-off transition.

- A delay between the starting moment of voltage transitions has been observed. Increasing the magnetizing inductance didn't make a good progress in the delay, conversely the delay with ER11 slightly increased. It shows that the delay didn't arise from magnetizing inductance.

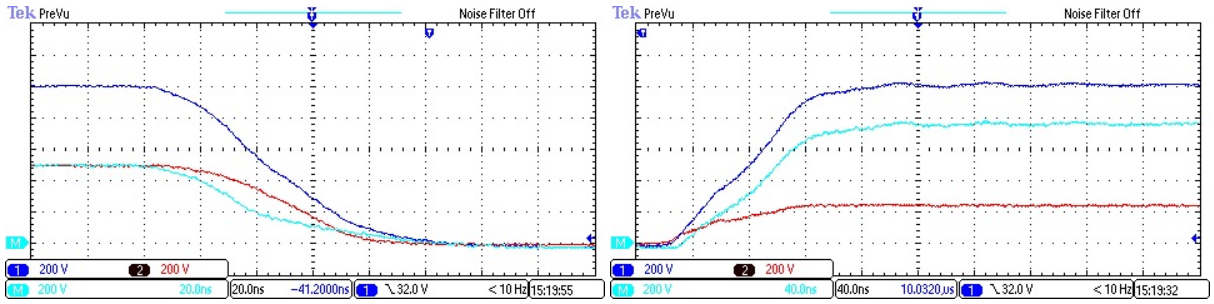
4.6 High voltage test (1000 V)

In order to see the behaviour of the system at high voltage, a test was conducted at 1000 V with ER11 gate balancing core. It should be noted that the gate resistors are lowered to the value that was estimated as being 51 ohm. The test was done by 1 kHz gate signal with 1% duty cycle, where 2 A drain current was to flow. Moreover the cable loops that were placed to the legs of gate resistors were removed to prevent any parasitics caused by.

Initially, in order to make the MOSFET stack to turn-off at high voltage, the test setup in Fig. 4.1 was decided to utilized. The experiments at 400 V were done by shorting V_{DC2} and using a 400 V DC supply for V_{DC1}. As a quicker and safer method, instead of using two power supply, Stanford PS350 power supply was used. The device has $\pm$5000 V output ($\pm$1 V accuracy) with 5 mA maximum current [10]. Power supply trips whenever a current higher than maximum set value is drawn. In this case, a

24.2 μF capacitor block with 1300 V withstand voltage was placed before the PCB connector providing high current and bypassing any oscillation that was discussed previously. Eventually, output voltage was raised step-by-step ensuring that the power supply does not trip.

In Fig. 4.13 turn-on and off voltage waveforms are depicted. The colour allocation was followed as in the previous tests. As expected the voltage share was worse. The delay mentioned before, now became more apparent. High side switch Q_{21} starts the voltage transition at turn-off later than Q_{22} with a higher dV/dt ending up 760 V across its drain-source pins. As a different behaviour from the 400 V tests, now Q_{21} turns-on faster than the lower side switch Q_{22}.



(a) (b)

Figure 4.13: (a) turn-on and (b) turn-off voltage transition waveforms at 1000 V with Rg=51 ohm.

4.7 Conclusions

Numerous tests with gate balancing core were done. In this chapter, the experiments that were found to be most reasonable, have been demonstrated and discussed.

One of the main difficulty was the parasitic components. Compare to Si MOSFETs in the similar range, the selected silicon carbide MOSFET has relatively low input capacitance. As the main purpose of gate balancing core technique is to obtain a balanced voltage share at switching transitions, for this thesis, running the converter in safe operating area has the priority as much as the former one. Even so, the experiments with gate balancing core were considered unsuccessful.

For the next chapter, it was decided to rebuilt the converter with SiC MOSFET stack and continue experiments.

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[8] K. Sasagawa, Y. Abe, and K. Matsuse. "Voltage-balancing method for IGBTs connected in series". In: *IEEE Transactions on Industry Applications* 40.4 (July 2004), pp. 1025–1030. ISSN: 0093-9994. DOI: 10.1109/TIA.2004.830794.

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CHAPTER 5

Bidirectional Flyback Converter with Series Connected SiC MOSFETs

This chapter demonstrates the efforts done with the bidirectional flyback converter which has two SiC MOSFET in series. All the experiments regardless of being considered as successful or unsuccessful, are given as well as the efficiency measurements of the converter with SiC MOSFET comparing the version with IGBT.

5.1 Introduction

As mentioned, this report is direct continuity of the 8^{th} semester project. The design of the converter was handled step-by-step in that report which can be found in the annexed compact disc. Due to this reason the converter was rebuilt with MOSFET stack and series connection tests were kept being conducted.

In Table 5.1 measured parameters of flyback transformer are listed. In this transformer, two metglas 2605SA1, C shaped core (model AMCC250) were used. Note that, the transformer was not optimally wound.

Table 5.1: Measured transformer parameters of bidirectional flyback converter.

L_1	25.86	μH	R_1	0.55	ohm
L_2	111.34	μH	R_2	3.742	ohm
L_m	6.219	mH	C_w	273	pF
N_p	52	turns	N_s	104	turns
B_{max}	1.56	tesla	Air gap	0.5	mm

To start with, in order to have a more obvious comparison and observation of the effect of the SiC devices to the system, primary side switch was kept the same which is IXGF25N300. In this case, as mentioned in Chapter 2, GP02-40 diode was placed in parallel with the IGBT.

In the secondary side, series connected MOSFETs were driven by Semikron® SKHI 22 A/B H4

dual IGBT Driver. The main reason to use this driver for the secondary side is that, it offers 4000 V I/O isolation (2 sec. AC) and it contains built-in DC/DC converter which is able to float. The Traco Power® DC/DC converter was offering only 1 kV I/O isolation. It is well-known from Chapter 2 that depending on boost or buck operation, switches senses higher voltage stress then their own converter side input/output voltage, either at turn-on or turn-off. For example, assuming that the input voltage is 400 V and output voltage is 1400 V. If the converter is running at buck mode and the end of first buck pulse output capacitor voltage (which is input for the buck operation) dropped to 1300 V, then MOSFET stack will turn-off at 400 V/turns ratio + 1300 V = 2100 V. Even if a precise voltage share had been obtained, Traco Power® would faced with the risk of failure. Additionally, Semikron® driver has +15/-7V output and demands minimum 3 ohm resistance at the output. So the gate resistors were divided as R_d=10 and R_g41 ohm[1] as it can be seen in Fig. 5.1.

Once again, to clarify the notation, Q_1 represents the primary side switch, while Q_{21} and Q_{22} are denoted for secondary side switch, high and low side respectively.

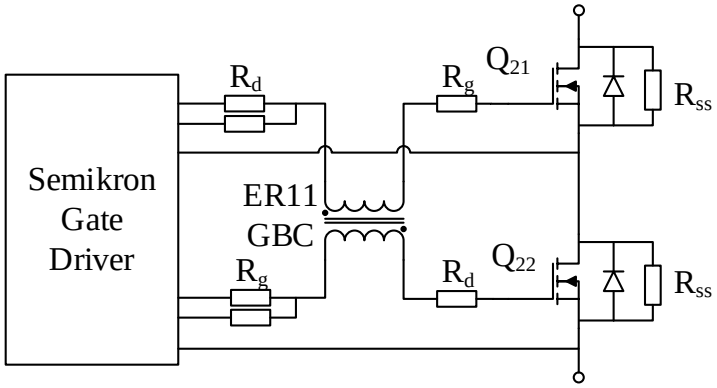


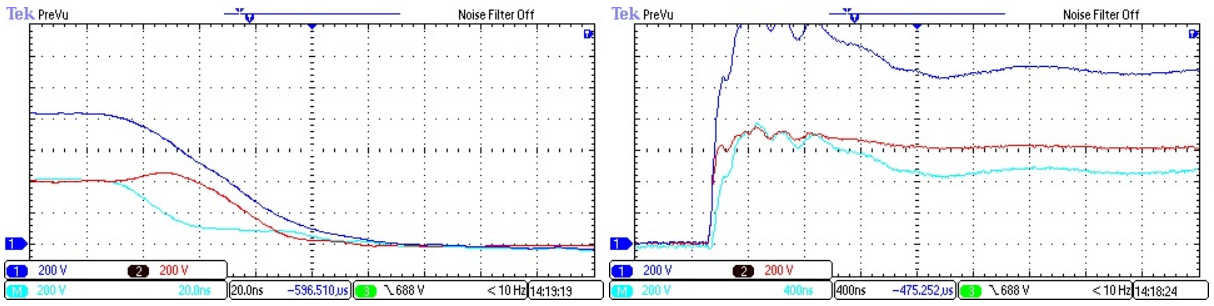
Figure 5.1: MOSFETs connected in series with Semikron® gate driver; R_d=10 and R_g=41 ohm.

5.2 High voltage test (1000 V)

To have a fair comparison with the previously test discussed in Section 4.6, a test was done so that MOSFET stack will sense similar voltage stress at turn-off for the buck operation. Referring to Section 4.2 2 mega ohms steady-state voltage sharing resistors were used.

In Fig. 5.2 turn-on and turn-off drain-to-source voltage waveforms are represented. Waveforms colours are followed as in previous experiments. In the figures it can be clearly seen that similar behaviour to the one in Section 4.6 was obtained. Especially at turn-on transition voltage unbalance has increased as well as the aforementioned delay still remains. However, in spite of voltage mismatch at turn-off transition, the steady-state voltage difference which is approximately 150 V makes the converter to run safely in limited regions.

[1] In practice 11 and 42.2 ohm resistors were used since these values were found in Aalborg University laboratory.



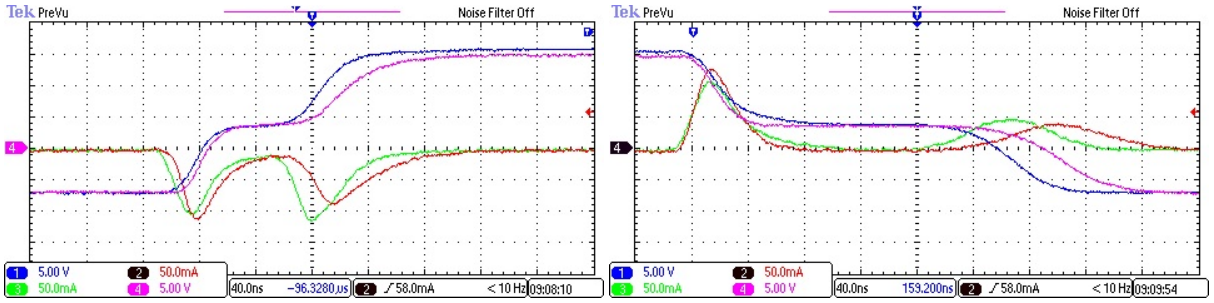
(a) (b)

Figure 5.2: (a) turn-on and (b) turn-off voltage transition waveforms at 1000 V with R_g=51 ohm obtained from the bidirectional flyback converter at buck mode operation.

5.3 Mismatch in gate currents and gate-to-source voltages

For the purpose of investigation any mismatch in gate signals, firstly the currents before the gate pins and gate-to-source voltages with differential probes were captured with zero voltage across the stack. It can be seen in Fig. 4.1 that previous current measurements of high side switch was taken just before gate pin, while for the low side switch it was between gate balancing core and and gate resistor. Regarding to the interwinding capacitance current path given in Fig. 3.6, the current measurements at these points were found to be unfair. So these current waveforms were captured right before the gate pin of each MOSFET in stack.

In Fig. 5.3 turn-on and turn-off gate currents and gate-to-source voltages of each MOSFET in stack is demonstrated. In Fig. 5.3a in spite of the fact that low side gate voltage started to build up before high side, for the currents it is vice versa and amplitude of low side MOSFET gate current is higher.



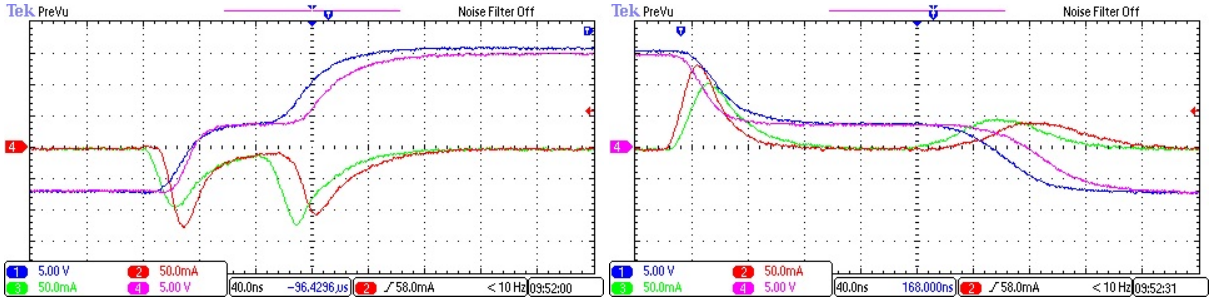
(a) (b)

Figure 5.3: (a) turn-on and (b) turn-off gate currents and gate-to-source voltages of each MOSFET in the stack where no voltage was applied across; blue and red waveforms belong to Q_{22} (low side) and green and pink waveforms belong to Q_{21} (high side).

To talk about turn-off waveforms which are given in Fig. 5.3b, until the gate-to-source voltages drop to plateau voltage although the currents have different amplitudes, they demonstrate close slopes. After the plateau effect, the mismatch continues.

This high mismatch leaded the thoughts towards to, how much the gate balancing core effects these

waveforms. Subsequently the same test was conducted without gate balancing core. The waveforms are illustrated in Fig. 5.3. As it can straightforwardly seen that the mismatch in the amplitude of gate currents, as well as the delay in between, increased. The definition ”close slopes” in gate currents until the gate-to-source voltages drops to the plateau voltage is no longer available. This test validates that the gate balancing core has an considerable effect on gate currents.



(a) (b)

Figure 5.4: (a) turn-on and (b) turn-off gate currents and gate-to-source voltages of each MOSFET in the stack with no gate balancing core and no voltage was applied across; blue and red waveforms belong to Q_{22} (low side) and green and pink waveforms belong to Q_{21} (high side).

Lastly, the gate resistors R_g, are relocated between the MOSFETs and gate balancing core as it has been depicted in Fig. 5.5. Gate current and gate-to-source voltage waveforms of turn-on and turn-off transitions can be seen in Fig. 5.6.

Speaking for turn-on transition, compare to Fig. 5.3a two difference can be realised in the figure. While balance of gate currents until plateau effect became relatively worse, from plateau till the full gate voltage, a slight improvement was obtained.

On the other hand, a significant change was observed for the turn-off waveforms which are given Fig. 5.6b. Even though gate currents are well-balanced until the end of plateau effect, after that, until turn-off, a small mismatch can still be observed.

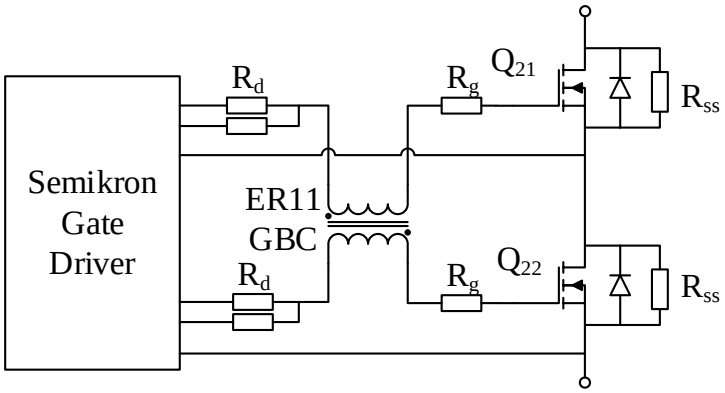
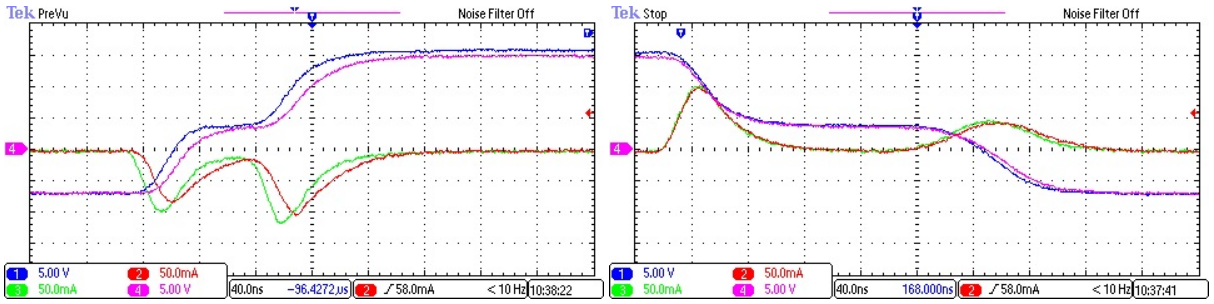


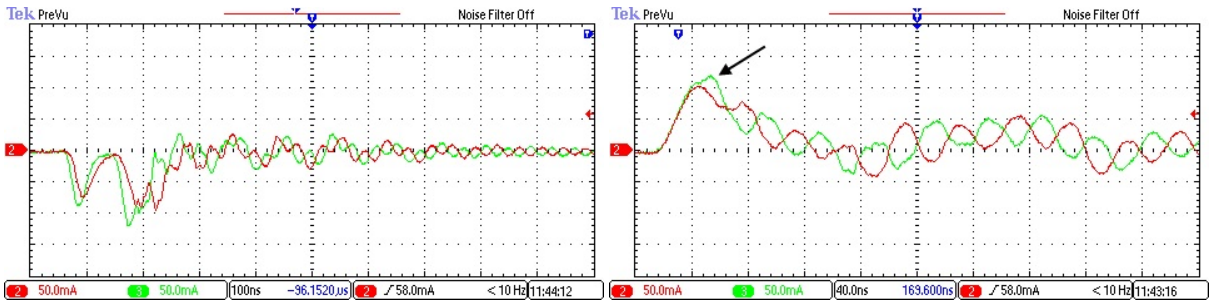
Figure 5.5: MOSFETs connected in series with Semikron® gate driver and gate resistor of low side switch is relocated; R_d=10 and R_g=41 ohm.

Right after, a test was conducted with this configuration having 1000 V at output capacitor and 2.5 A through MOSFET stack. The start point of unbalance during turn-off transition is indicated by arrow in Fig. 5.7b. Accordingly, drain-to-source waveforms are shown in Fig. 5.8.



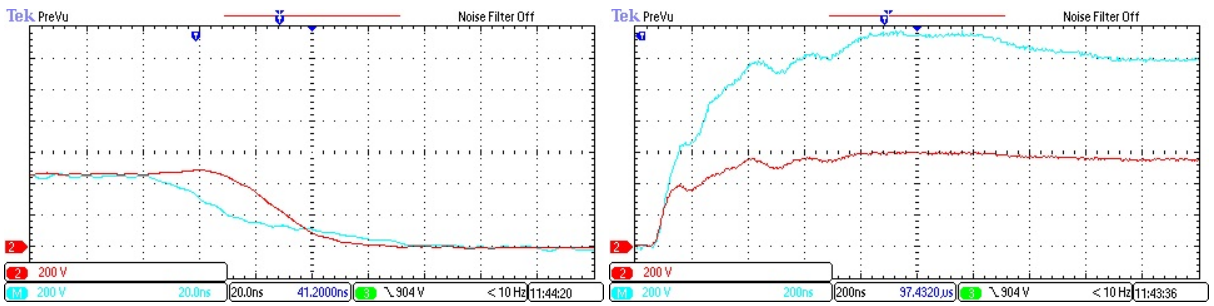
(a) (b)

Figure 5.6: (a) turn-on and (b) turn-off gate currents and gate-to-source voltages of each MOSFET in the stack with with no voltage was applied across and relocated gate resistors; blue and red waveforms belong to Q_{22} (low side) and green and pink waveforms belong to Q_{21} (high side).



(a) (b)

Figure 5.7: (a) turn-on and (b) turn-off gate currents after relocation of gate resistors; red waveforms belong to Q_{22} (low side) and green to Q_{21} (high side).



(a) (b)

Figure 5.8: (a) turn-on and (b) turn-off drain-to-source voltages after relocation of gate resistors; red waveforms belong to Q_{22} (low side) and turquoise to Q_{21} (high side).

To wrap up the progress made can be summarized as follows;

- Aforementioned delay at has been minimised for turn-off transition by relocation of the lower side MOSFET gate resistor. Nevertheless, at the end of the transition, voltage mismatch across the

switches still takes place. This relocation is against to the theory discussed in Section 3.5.1 and demands more study on it.

- For turn-on transition a significant improvement still couldn't be achieved.
- It has been validated that position of gate resistors can have remarkable influence on transient voltage sharing. More study needs to be done on this issue.

5.4 Efficiency measurements

In Chapter 2 an efficiency map with RCDD and RCD snubber network was given (see Fig. 2.17) and it was concluded that employed IGBTs has significant effect on efficiency. The proposed idea to increase the efficiency was to replace the IGBTs with SiC MOSFETs. The efforts done for series connection of SiC MOSFET showed that it is possible to have efficiency measurements in few points.

Therefore, it has been verified that the latest configuration of the converter can run safely up to 1400 V output voltage while DC-link is 400 V. In this case, using the same operation parameters (frequency, duty cycle, number of pulses, DC-link and output capacitance) efficiency measurements were done at three operating points 1000, 1200 and 1400 V output voltage with 5 A in the primary side. Note that, during these measurements, 2 mega ohms steady-state balancing resistors were replaced with 15 mega ohms and thus MOSFET voltage waveforms were not monitored.

Table 5.2: Efficiency measurements with and without SiC MOSFETs in the secondary side of the bidirectional flyback converter.

	2×IXGF25N300		IXGF25N300 + 2×C2M1000170D	
	Boost Efficiency	Buck Efficiency	Boost Efficiency	Buck Efficiency
1000 V	69.48	71.52	70.81	88.41
1200 V	65.13	68.07	64.96	90.0
1400 V	63.71	64.02	64.2	89.36

As it can be appreciated from Table 5.2, increment of converter efficiency at buck mode operation is notable. Previously, just as it is in primary side, secondary side IGBT had GP02-40 across. In the new converter, during boost operation in the secondary side parasitic diode of SiC MOSFETs were employed and converter efficiency at boost mode was not effected significantly.

5.5 Conclusions

This chapter dealt with the bidirectional flyback converter running with two SiC MOSFET in the high voltage side. For the series connection of the switches, experimental results demonstrated that series connection of SiC MOSFET needs deeper analysis opening the doors for successful voltage distribution.

For the converter efficiency, it is now verified that the main energy loss arises from switching of power semiconductors. In case a successful series connection, the converter would operate at higher

voltage levels.

In Fig. 5.9 a view of SiC based bidirectional flyback converter is given for the illustrative purpose.

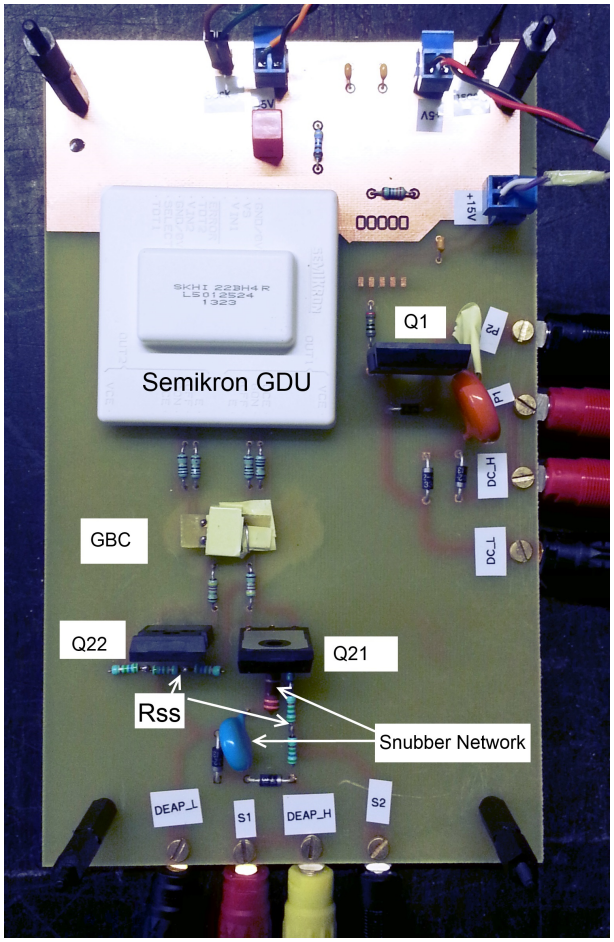


Figure 5.9: A view of SiC based bidirectional flyback converter.

CHAPTER 6

Conclusions and Future Works

In this chapter both the master thesis' conclusions and future work are presented.

6.1 Conclusions

The master thesis started with an introduction to the dielectric electro active polymers (DEAP) and continued with analysis of the bidirectional flyback converter which was designed previously in 8^{th} non-optimally. A better understanding and drawbacks of the converter were necessary in order to be able to improve and optimize it. Analysis showed that the highest influence on converter efficiency arises from switching losses. Therefore to overcome this drawback, it was decided to update the converter by replacing the IGBTs by SiC MOSFETs which are becoming more popular in recent years.

However, since the voltage rating of these switches are still not high enough to utilize in the converter, series connection techniques were reviewed and it was decided to put efforts on series connection of two SiC MOSFETs with 1700 V withstand voltage. The chosen technique is known as "gate balancing core" and parasitics of the switches as well as the other circuit components play significant role on the performance of technique. Accordingly, very low parasitic components of these switches compare to its counterparts in the same voltage range, made the operation of the technique hard to be successful.

Nevertheless, experiments which can be considered successful or not were conducted and steps were done in the true path of getting close to synchronised voltage distribution during switching transients. Yet, the work demands more research.

Efficiency measurements with SiC switches demonstrated a remarkable change in efficiency of the converter in buck mode operation i.e. change from the range of 65% to range of 90% with 5 A in the primary side. The current limitation of employed SiC devices which is 4.9 A, makes it possible to run the converter close to 10 A in the primary side, which is known from Chapter 2 that efficiency is higher

at that range due to less number of pulses.

Finally, it is authors belief that this converter can be a strong candidate to be employed in energy harvesting cycles of DEAP by following the future works to be done which will be mentioned in the next section.

6.2 Future works

Future works related to series connection of MOSFETs

After numerous experiments synchronization in turn-off voltage transient was obtained. However this synchronization was lost during plateau effect of MOSFET. More research is needed to be done on this issue. One of the main reference ”Serializing off-the-shelf MOSFETs by Magnetically Coupling” is suggesting to decrease the interwinding capacitance of gate balancing core to the level of 1% of miller capacitance, which in this case is 12 fF. A gate balancing core is required with lowest capacitance possible. Besides, alternative solutions demand research to prevent the effect of this capacitance.

Future works related to the converter

The biggest effect has been obtained on efficiency of the converter is from the switching losses. As an addition, the flyback transformer requires to be rebuilt with optimised winding techniques that lower the leakage inductance. Less leakage inductance will bring the possibility of decreasing the size of snubber network as well.

Another improvement is to find optimum operating point for the converter in terms of switching frequency and duty cycle. Additionally, after a successful series connection of MOSFETs for the secondary side, primary side switch is required to be replaced by either Si or SiC in order to minimise the switching losses in boost mode operation.

Appendices

APPENDIX A

Capacitance of parallel plates

Mainly a capacitor is an arrangement of conductors in order to store electric charge. However in many areas of electrical engineering, it is possible to encounter parasitic capacitance between conductors.

The gate balancing core in this thesis, was built by means of PCB layers. In this case a capacitance between primary and secondary layer occurs. Since two layers of PCB used, the capacitance caused by each layer can be determined separately and the result will be as capacitors connected in series or equivalent dielectric constant can be estimated and by this equivalent capacitance can also be computed.

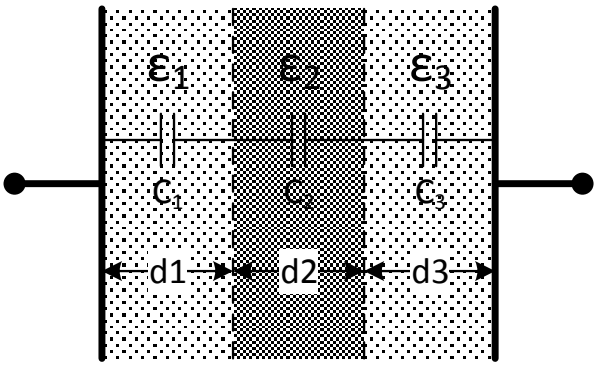


Figure A.1: Multilayer parallel plate capacitor.

In Fig. A.1 an insight view of three layer capacitor is illustrated. In order to calculate the equivalent capacitance, firstly equivalent dielectric constant of layer materials should be found by means of (A.1). Accordingly, the equivalent capacitance can be computed by (A.2) [1].

$$\varepsilon_{eq} = \sum_{m=1}^{n} \frac{d_m}{d_T \varepsilon_{rm}} \tag{A.1}$$

$$C = \frac{\varepsilon_0 \cdot \varepsilon_r \cdot A}{d_1} \tag{A.2}$$

Where d_T is total distance between plates, d_m is thickness of each material and ϵ_{rm} is the dielectric constant of m^{th} layer.

It has been mentioned that used PCB was employed to form the windings. In Fig. A.2 [2] dielectric constant of FR4 material by frequency is given. To have it more precise, prediction can be done by (A.3)

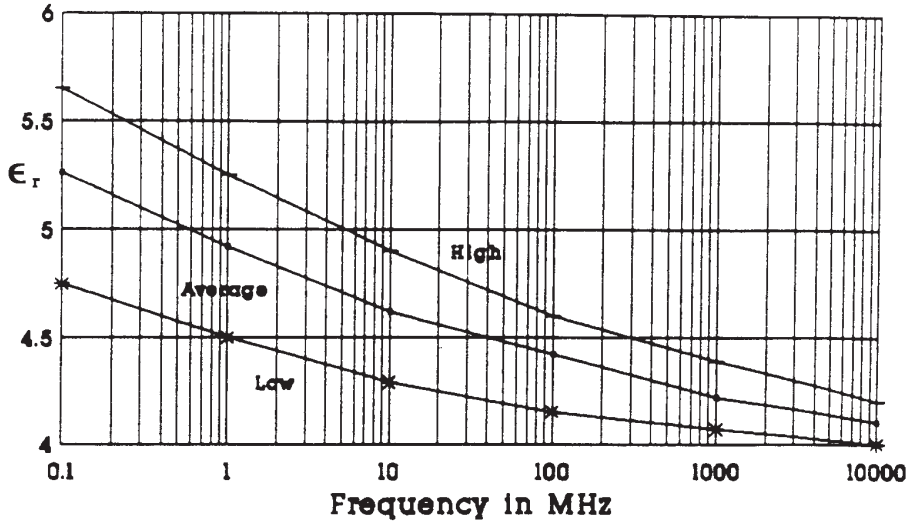


Figure A.2: ϵ_r versus frequency, FR4 material.

$$\varepsilon_r = 4.97 - 0.257 \log\left(\frac{f}{10 \times 10^6}\right) \tag{A.3}$$

In this case, using two single sided PCB with 1 mm thickness that the copper layers face up and down to maximise the distances between each other and 1 mm Mylar A sheet in between two PCB, capacitance can be calculated as follows;

Surface area (Fig. A.3),

$$A = 19 \times 0.25 = 4.75\, mm^2 \tag{A.4}$$

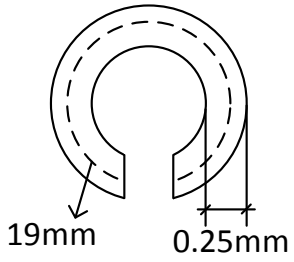


Figure A.3: Illustration of PCB layer as winding.

According to ϵ_r of FR4 at 5000 Hz is 5.82 and ϵ_r of Mylar A=3.3. Making use of A.1, equivalent dielectric constant is approximately 0.2155. Note that total distance between the plates is 3 mm. Finally,

capacitance

$$C = \frac{8.85 \times 10^{-12}\ [\mathrm{F/m}] \times 0.2155 \times 4.75 \times 10^{-6}\ [\mathrm{m}^2]}{3 \times 10^{-3}\,[\mathrm{m}]} = 3fF \tag{A.5}$$

From Table 4.2 it is known that, measured capacitance does not match with this estimation.

References

[1] I.J. Bahl. *Lumped Elements for RF and Microwave Circuits*. Artech House microwave library. Artech House, 2003. ISBN: 9781580536615. URL: http://books.google.dk/books?id=91UsWxk1CYkC.

[2] *Controlled Impedance Circuit Boards and High Speed Logic Design*. IPC-2141. The Institute for Interconnecting and Packaging Electronic Circuits. April 1996.

APPENDIX B

Circuit schematics and PCB layouts

In this appendix schematics and PCB layouts are given. It should be noted that PCB layouts are not scaled to 100%.

B.1 Schematics

B.1.1 Gate balancing core test schematic

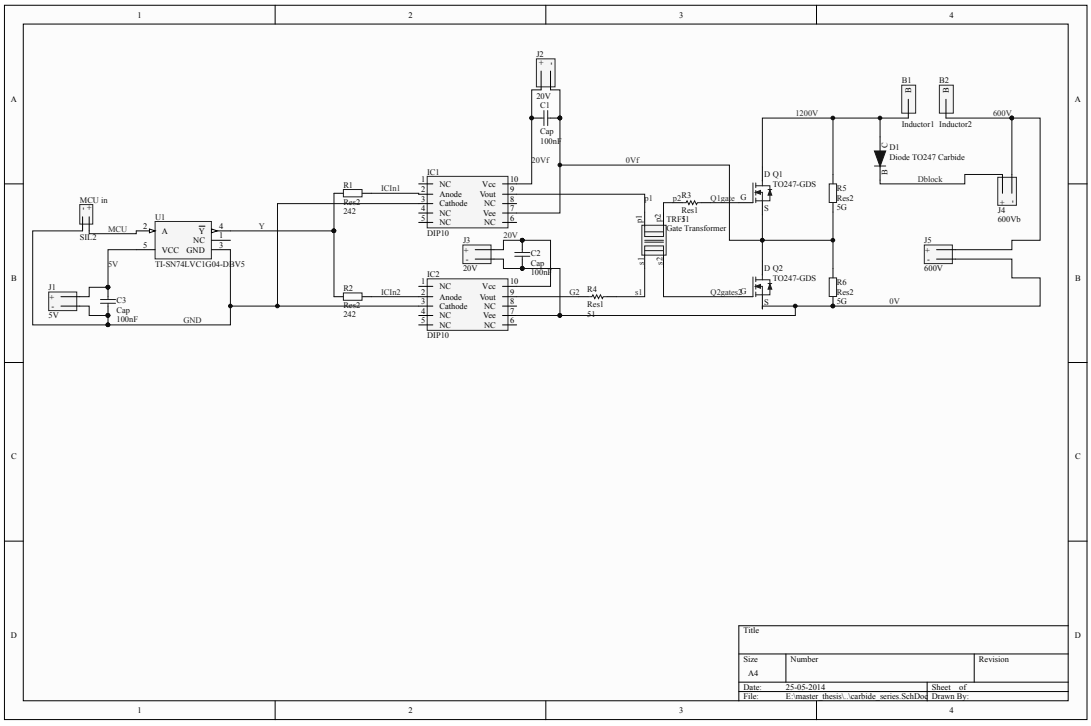


Figure B.1: Gate balancing core test schematic.

B.1.2 Bidirectional flyback converter with GBC schematic

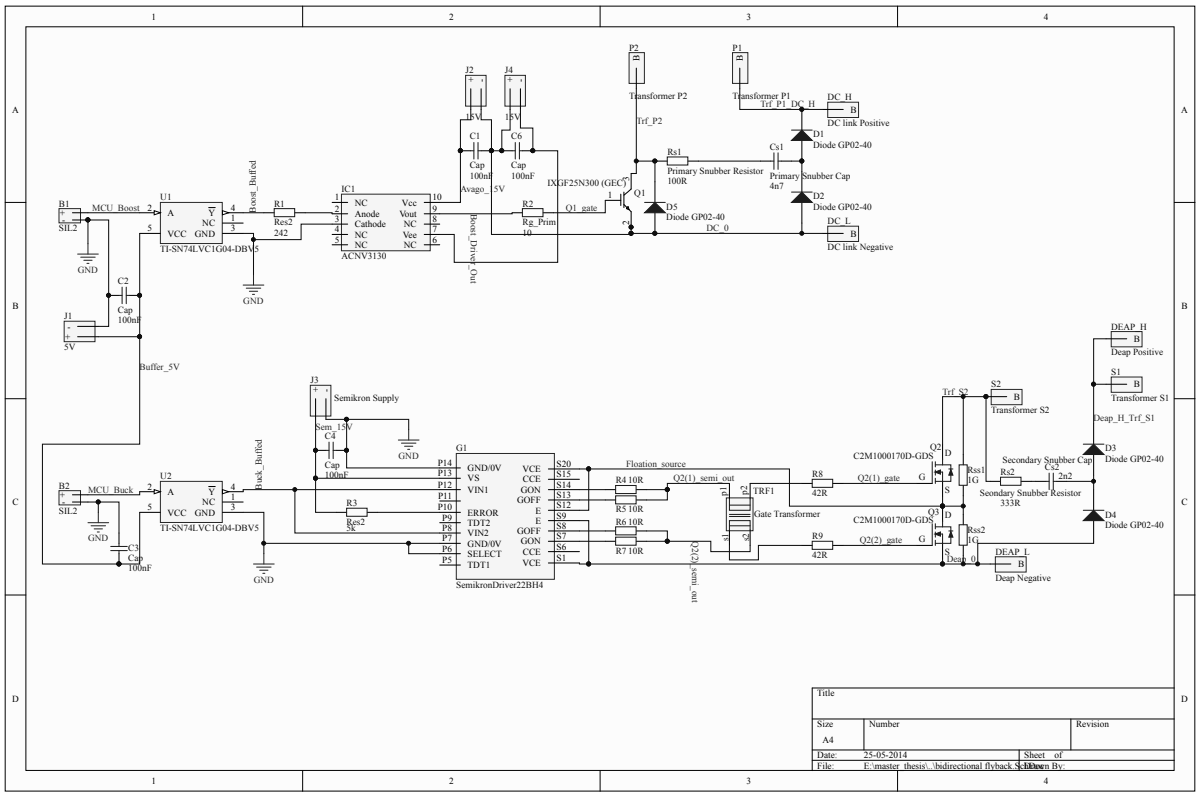


Figure B.2: Bidirectional flyback converter with GBC schematic.

B.2 PCB Layouts

B.2.1 Gate balancing core test PCB Layout

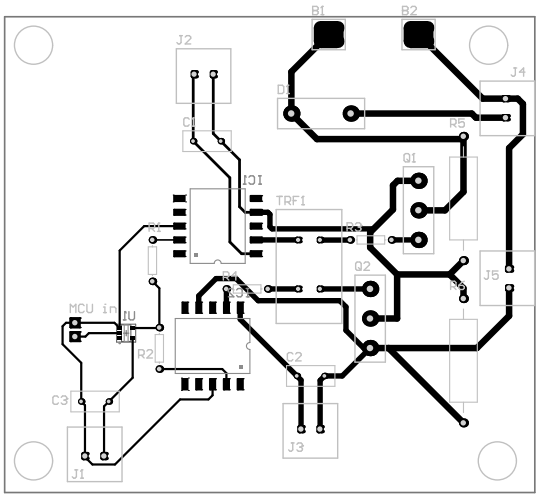


Figure B.3: Gate balancing core test PCB Layout.

B.2.2 Bidirectional flyback converter with GBC PCB layout

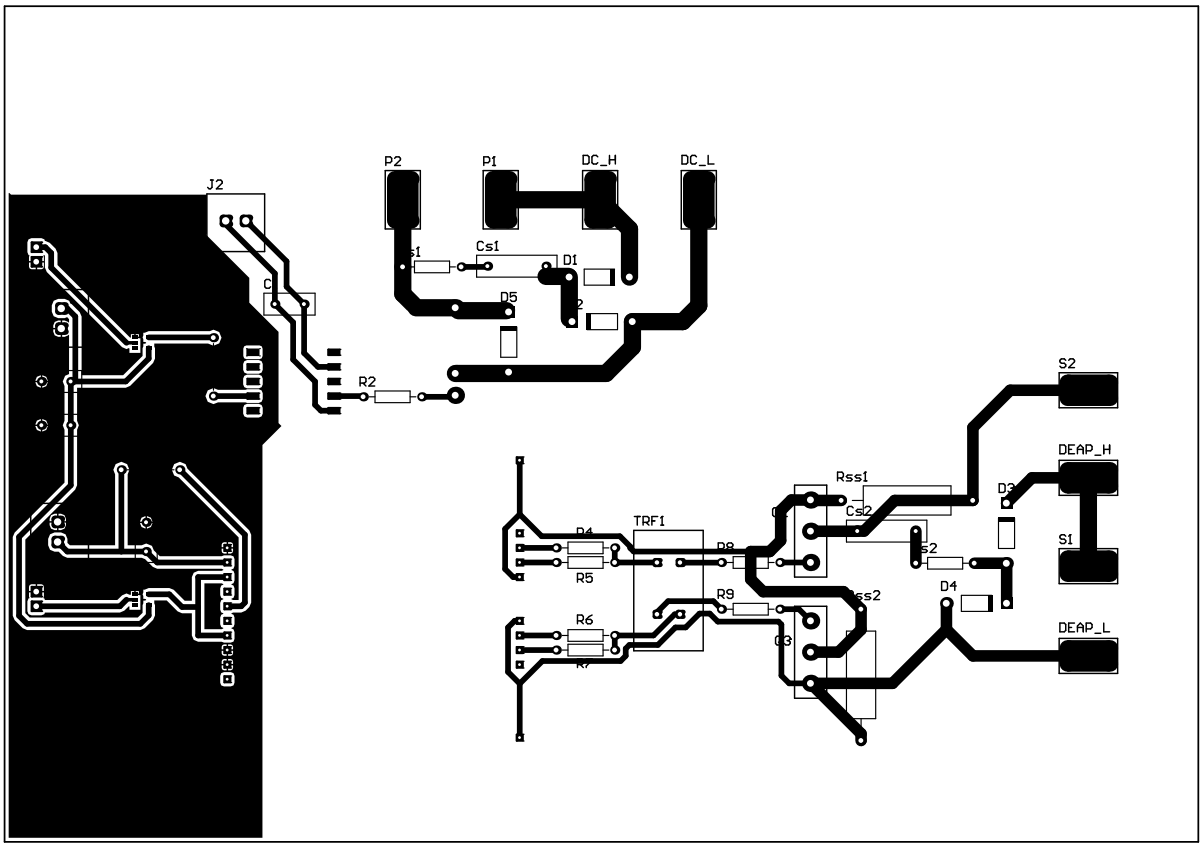


Figure B.4: Bidirectional flyback converter with GBC PCB layout.

APPENDIX C

MATLAB® Scripts

Listing C.1: Source code of MATLAB® script for number of pulses.

```
clear all
clc
%%
Vboost=1200;            % [V]
Vbuck=500;
Vdeap=500;
Vdc=400;

Ceapmax=2.26e-6;        % [F] D-EAP element capacitance
Ceapmin=2.26e-6;        % [F] D-EAP element capacitance
Cdc=53.3e-6;
%Cdc=240;                % Instead of DC-supply very high capacitance value.
fboost=3000;            % [Hz] switching frequency
dboost=0.265;           % [percent/100] duty cycle
Tsw=1/fboost;           % [second] switching period
t1sw=dboost*Tsw;        % [second]

fbuck=3000;             % [Hz] switching frequency
dbuck=0.29;            % [percent/100] duty cycle
Tbuck=1/fbuck;          % [second] switching period
t1swbuck=dbuck*Tbuck;   % [second]
%Rdiode=1.25;           % low voltage
Rdiode=0.6;             % medium voltage
%Rdiode=0.5;            % high voltage
save('Rdiode','Rdiode');
save('Cdc','Cdc');
save('Ceapmax','Ceapmax');
%%

nboost=0;
nbuck=0;

tboost=[];
tbuck=[];
Ipboost=[];
```

```
Isboost=[];

Ipbuck=[];
Isbuck=[];

Vd1(1)=Vdeap;
Vin1(1)=Vdc;
%%
while (Vdeap<(Vboost));
save('Vdc','Vdc');
nboost=nboost+1;

t1=linspace((nboost-1)*Tsw,(((nboost-1)*Tsw)+t1sw),1000);
t2=linspace((((nboost-1)*Tsw)+t1sw),((nboost)*Tsw),1000);
%%

[t1,Ion]=ode45(@swon,t1,0);
t1=rot90(t1);
Ion=Ion(:,1);
Ion=rot90(Ion);
%%
diondt=diff(Ion)./diff(t1);

off_init=[Ion(end)*0.5 -diondt(end)]; %remember here
[t2,Ioff]=ode45(@swoff,t2,off_init);

t2=rot90(t2);
Ioff=Ioff(:,1);
Ioff=rot90(Ioff);
%%
for m=1:length(Ioff)
    if Ioff(m)<=0
        Ioff(m)=0;
    end
end
for m=1:length(Ion)
    if Ion(m)<=0
        Ion(m)=0;
    end
end
%%
Vdc=Vdc-(1/Cdc)*trapz(t1,Ion);
Vin1(nboost+1)=Vdc;
%%
Vdeap=Vdeap+(1/Ceapmax)*trapz(t2,Ioff);
%Eout(n)=0.5*Ceap*Vdeap*Vdeap;
Vd1(nboost+1)=Vdeap;
tboost=[tboost t1 t2];
Ipboost=[Ipboost Ion Ioff*0];
Isboost=[Isboost Ion*0 Ioff];

end
%%

%Vdeap=(Ceapmax/Ceapmin)*Vdeap; % for real DEAP
Vd2(1)=Vdeap;
Vin2(1)=Vdc;
while (Vdeap>(Vbuck));
save('Veap','Vdeap');
```

```
nbuck=nbuck+1;

t1buck=linspace((nbuck-1)*Tbuck,(((nbuck-1)*Tbuck)+t1swbuck),1000);
t2buck=linspace((((nbuck-1)*Tbuck)+t1swbuck),((nbuck)*Tbuck),1001);
t2buck=t2buck(2:end);

[t1buck,Ion2]=ode45(@sbuckon,t1buck,0);
t1buck=rot90(t1buck);
Ion2=Ion2(:,1);
Ion2=rot90(Ion2);

%%
dion2dt=diff(Ion2)./diff(t1buck);
off2_init=[2*Ion2(end) -1*dion2dt(end)]; %remember here
[t2buck,Ioff2]=ode45(@sbuckoff,t2buck,off2_init);

t2buck=rot90(t2buck);
Ioff2=Ioff2(:,1);
Ioff2=rot90(Ioff2);
%%
for m=1:length(Ioff2)
    if Ioff2(m)<=0
        Ioff2(m)=0;
    end
end
for m=1:length(Ion2)
    if Ion2(m)<=0
        Ion2(m)=0;
    end
end

Vdc=Vdc+(1/Cdc)*trapz(t2buck,Ioff2);
Vin2(nbuck+1)=Vdc;

Vdeap=Vdeap-(1/Ceapmin)*trapz(t1buck,Ion2);
Vd2(nbuck+1)=Vdeap;

tbuck=[tbuck t1buck t2buck];
Isbuck=[Isbuck Ion2 Ioff2*0];
Ipbuck=[Ipbuck Ion2*0 Ioff2];

end
 str = ['Boost Pulses ',num2str(nboost)];
 disp(str);
 str = ['Buck Pulses ',num2str(nbuck)];
disp(str);

%%
figure
grid on
subplot(2,2,1)
plot(tboost,Ipboost)
title('Ipboost')
grid on

subplot(2,2,2)
plot(tboost,Isboost)
title('Isboost')
grid on
```

```
154
155 subplot(2,2,3)
156 plot(Vd1)
157 title('Vdeap-Boost')
158 grid on
159
160 subplot(2,2,4)
161 plot(Vin1)
162 title('Vdc-Boost')
163 grid on
164 %%
165 figure
166 subplot(2,2,1)
167 plot(tbuck,Ipbuck)
168 title('Ipbuck')
169 grid on
170
171 subplot(2,2,2)
172 plot(tbuck,Isbuck)
173 title('Isbuck')
174 grid on
175
176 subplot(2,2,3)
177 plot(Vd2)
178 title('Vdeap-Buck')
179 grid on
180
181 subplot(2,2,4)
182 plot(Vin2)
183 title('Vdc-Buck')
184 grid on
```

Listing C.2: swon

```
1  function dson=swon(t1,Ion)
2  load('Vdc');
3  Rl=0.5462;
4  Rsw=0.11;
5  Rtot=Rl+Rsw;
6  L=6.219e-3;
7
8  dson=(Vdc-Ion*Rtot)/L;
9
10 end
```

Listing C.3: swoff

```
1  function dsoff=swoff(t2,Ioff)
2  load('Rdiode');
3  load('Ceapmax');
4  Rl=3.742;
5  Rtot=Rl+Rdiode;
6  L=24.876e-3;
7
8  m1=(Rtot)/L;
9  m2=1/(L*Ceapmax);
```

```
10
11 dsoff_1=Ioff(2);
12 dsoff_2=m1*Ioff(2)+m2*Ioff(1);
13 dsoff=[dsoff_1;dsoff_2];
14 end
```

Listing C.4: sbuckon

```
1  function dson2=sbuckon(t1buck,Ion2)
2  load('Veap');
3  Rsw=0.11;
4  Rl2=3.742;
5  Rstot=Rsw+Rl2;
6  L=24.876e-3;
7
8  dson2=(Vdeap-Ion2*Rstot)/L;
9  end
```

Listing C.5: sbuckoff

```
1  function dsoff2=sbuckoff(t2buck,Ioff2)
2  load('Rdiode');
3  load('Cdc');
4  Rl=0.5462;
5  Rtotal=Rl+Rdiode;
6  L=6.219e-3;
7
8  m1=(Rtotal)/L;
9  m2=1/(L*Cdc);
10
11 dsoff2_1=Ioff2(2);
12 dsoff2_2=m1*Ioff2(2)+m2*Ioff2(1);
13 dsoff2=[dsoff2_1;dsoff2_2];
14 end
```

APPENDIX D

Microcontroller Code

Here, the microcontroller codes can be found. The program generates boost and buck pulses consecutively with 0.3 s in between operation modes i.e. boost and buck. The time between modes should be short enough, due to self discharge of the output load capacitor.

Listing D.1: DSP Code with Emulator

```
1
2
3  #include "inc/hw_memmap.h"
4  #include "inc/hw_types.h"
5  #include "driverlib/debug.h"
6  #include "driverlib/gpio.h"
7  #include "driverlib/pin_map.h"
8  #include "driverlib/pwm.h"
9  #include "driverlib/rom.h"
10 #include "driverlib/sysctl.h"
11 #include "utils/uartstdio.h"
12 #include "driverlib/interrupt.h"
13 #include "inc/hw_ints.h"
14 #include "driverlib/adc.h"
15 #include "driverlib/comp.h"
16 #include "driverlib/timer.h"
17
18
19 //*****************************************************************************
20 // Variables
21 //*****************************************************************************
22
23 unsigned short  fboost      =   3000;   //  Boost Frequency
24 unsigned short  fbuck       =   3000;   //  Buck Frequency
25 unsigned short  flag_boost  =   0;  //
26 unsigned short  flag_buck   =   0;  //
27 unsigned short  nboost      =   38;
28 unsigned short  nbuck       =   18;
29
```

```
double          dboost      =   0.265;  //  Boost Duty Cycle
double          dbuck       =   0.23;   //  Buck Duty Cycle

volatile unsigned long permm = 0;

#ifdef DEBUG
void
__error__(char *pcFilename, unsigned long ulLine)
{
}
#endif

void
PWM0IntHandler(void)
{

    PWMGenIntClear(PWM_BASE, PWM_GEN_0, PWM_INT_CNT_ZERO);
    PWMOutputInvert(PWM_BASE, PWM_OUT_0_BIT, false);
    PWMOutputState(PWM_BASE, PWM_OUT_0_BIT, true);
    flag_boost += 1;

    if (flag_boost == nboost+1)
    {
        PWMOutputState(PWM_BASE, PWM_OUT_0_BIT, false);
        PWMGenDisable(PWM_BASE, PWM_GEN_0);
        flag_boost=0;
    }
}

void
PWM5IntHandler(void)
{

    PWMGenIntClear(PWM_BASE, PWM_GEN_2, PWM_INT_CNT_ZERO);
    PWMOutputInvert(PWM_BASE, PWM_OUT_5_BIT, false);
    PWMOutputState(PWM_BASE, PWM_OUT_5_BIT, true);
    flag_buck += 1;

    if (flag_buck == nbuck+1)
    {
        PWMOutputState(PWM_BASE, PWM_OUT_5_BIT, false);
        PWMGenDisable(PWM_BASE, PWM_GEN_2);
        flag_buck = 0;
    }
}

int
main(void)
{

    volatile unsigned long say;
    //
    // Set the clocking to run directly from the mainosc .
    //
    SysCtlClockSet(SYSCTL_SYSDIV_1 | SYSCTL_USE_OSC |SYSCTL_OSC_MAIN |SYSCTL_XTAL_16MHZ);
    SysCtlPWMClockSet (SYSCTL_PWMDIV_1);

    // Enable the peripherals used by this programme.
    SysCtlPeripheralEnable(SYSCTL_PERIPH_PWM);
```

```
    SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOA);
    SysCtlPeripheralEnable(SYSCTL_PERIPH_GPIOH);

     //Set GPIO A6 and H7 as PWM pins for PWM2 and PWM5
    GPIOPinConfigure(GPIO_PA6_PWM0);
    GPIOPinConfigure(GPIO_PH7_PWM5);
    GPIOPinTypePWM(GPIO_PORTA_BASE,GPIO_PIN_6);
    GPIOPinTypePWM(GPIO_PORTH_BASE,GPIO_PIN_7);


    //GPIOPadConfigSet(GPIO_PORTA_BASE, GPIO_PIN_6, GPIO_STRENGTH_8MA, GPIO_PIN_TYPE_STD_WPU);
    //GPIOPadConfigSet(GPIO_PORTH_BASE, GPIO_PIN_7, GPIO_STRENGTH_8MA, GPIO_PIN_TYPE_STD_WPU);


    PWMGenConfigure(PWM_BASE, PWM_GEN_0, PWM_GEN_MODE_UP_DOWN | PWM_GEN_MODE_NO_SYNC);
    PWMGenConfigure(PWM_BASE, PWM_GEN_2, PWM_GEN_MODE_UP_DOWN | PWM_GEN_MODE_NO_SYNC);

    // Set the PWM periods
    PWMGenPeriodSet(PWM_BASE,PWM_GEN_0, (SysCtlClockGet() / fboost));
    PWMGenPeriodSet(PWM_BASE,PWM_GEN_2, (SysCtlClockGet() / fbuck));

    // Set the PWM duty cycles
    PWMPulseWidthSet(PWM_BASE, PWM_OUT_0, ((SysCtlClockGet() / fboost)*dboost));
    PWMPulseWidthSet(PWM_BASE, PWM_OUT_5, ((SysCtlClockGet() / fbuck)*dbuck));

    // Enable the PWM generator for outputs PWM0 & PWM1.
    PWMGenEnable(PWM_BASE, PWM_GEN_0);
    PWMGenEnable(PWM_BASE, PWM_GEN_2);

    PWMIntEnable(PWM_BASE, PWM_INT_GEN_0);
    PWMIntEnable(PWM_BASE, PWM_INT_GEN_2);

    PWMGenIntTrigEnable(PWM_BASE, PWM_GEN_0, PWM_INT_CNT_ZERO);
    PWMGenIntTrigEnable(PWM_BASE, PWM_GEN_2, PWM_INT_CNT_ZERO);
    PWMGenIntRegister (PWM_BASE, PWM_GEN_0, *PWM0IntHandler);       //Optional
    PWMGenIntRegister (PWM_BASE, PWM_GEN_2, *PWM5IntHandler);       //Optional
    IntMasterEnable();
    IntEnable(INT_PWM0);
    IntEnable(INT_PWM2);

    while(1)
    {
        if (permm == 1)
        {
        for(say = 0; say < 500000; say++)
        {
        }
        PWMGenEnable(PWM_BASE, PWM_GEN_0);          //Enable PWM_GEN_0

        for(say = 0; say < 500000; say++)
        {
        }

        PWMGenEnable(PWM_BASE, PWM_GEN_2);          //Enable PWM_GEN_1
    }
    }

}
```

APPENDIX E

Publications

Most of the work done in Chapter 2 "*Analysis of the Bi-directional Flyback Converter and Snubber*" was formed as a scientific paper and submitted for to the conference IECON 2014.

The conference is "*The 40th Annual Conference of the IEEE Industrial Electronics Society*" and it will be held in Dallas USA between October 28 - November 1, 2014. Further information can be obtained in `http://iecon2014.org/`. Notification of acceptance is on June 5th.

It should be noted that the submitted paper is a draft and small mistakes has been found. They were corrected in the relevant chapter.

An RCDD Snubber for a Bidirectional Flyback Converter

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***Abstract*—Increased utilization of renewable energy sources has boosted the demand for power electronics converters. Indeed, the DC/DC flyback converter is nowadays frequently used in applications where isolation is required, due to its low component count, simple structure and high energy efficiency. One of the major challenges faced in a flyback converter is the excess voltage stress sensed by its semiconductor devices, because of the interrupted current flow through its transformer leakage inductances. In this paper, a high-efficient bidirectional flyback converter, operating in discontinuous conduction mode, is examined with an integrated RCDD snubber. Additionally, experimental comparison where the converter runs with a typical RCD and RCDD snubber network, is done. Experimental results on an IGBT-based bidirectional flyback converter validate the applicability of the RCDD snubber demonstrating energy efficiency above 90%. Furthermore, the operation of the bidirectional converter with the employed snubber is thoroughly analysed and an appropriate mathematical analysis is conducted highlighting all the design specifications of the proposed snubber.**

I. Introduction

High voltage power supplies are encountered commonly in laser, accelerator, X-ray power generator, medical, airborne and space applications [1]–[5]. Similar to the study presented in this paper, in pulsed power applications, such as pulsed lasers, charging of high-voltage capacitors is required [1], [6]. In this paper, the employed converter was designed to boost the voltage of a Dielectric ElectroActive Polymer Generator (DEAP) from 500 V to 2 kV and buck it back to 500 V.

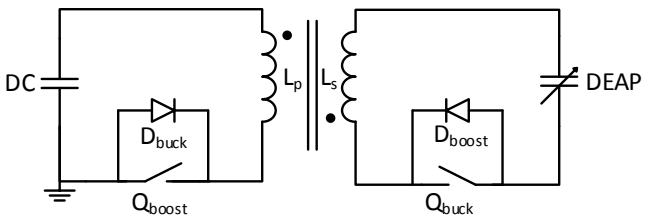


Fig. 1. Bidirectional flyback converter.

In bidirectional DC/DC converters power flow is obtained via bidirectional current flow where the polarity of the voltages at either end remains unaltered [7]. These bidirectional converters can be separated into isolated (full bridge, push-pull, flyback) and non-isolated (bidirectional buck-boost, tapped inductor, Cúk) topologies and they are mostly used in battery and super-capacitor applications. In Fig. 1 a bidirectional flyback converter is illustrated. The main advantages of this topology are its simplicity, galvanic isolation, low component count and well-known dynamic behaviour [8]. As drawbacks, low power capability and leakage inductances introduced to the circuit by the transformer can be mentioned. Correspondingly, the leakage inductance that was mentioned causes high voltage spikes therefore power switch failure. The problem arises from the high di/dt in leakage inductances and its resonance with output capacitances C_{OSS} of the power switches. In this case snubbers are used in order to suppress the overvoltage seen by the power switches to the acceptable level at turn off. These voltage snubbers are categorised as passive and active or dissipative and non-dissipative snubbers [9].

For flyback converters, the most typical dissipative passive snubbers are RC and RCD snubbers [10], [11]. While simple RC snubber networks are feasible for both rate-of-rise control of turn-off voltage and damping of parasitic resonance, RCD networks are used for either voltage clamp or rate-of-rise control [9], [12], [13].

Active clamp technique, gives the possibility to recycle the energy stored in leakage inductance of the flyback transformer and minimise the voltage spike [14], [15]. Configuration can also help both main and snubber switches to perform zero voltage switching (ZVS). Some other benefits of this snubber are, using lower voltage semiconductor compare to RCD, reduced EMI and actively resetting main transformer to third quadrant of BH curve [16].

In bidirectional flyback converter, it is possible to encounter both passive and active snubber networks. In [17] a bidirectional flyback converter was proposed for a DEAP working in actuator mode. For the low voltage side switch an RC snubber and for the high voltage side an RCD snubber was used reporting maximum efficiency of 85% in boost 80% in buck operation. In [18] a 200 W bidirectional active-clamped flyback converter prototype has been studied and efficiency of up to 90% has been achieved. Additionally, there can be encountered to bidirectional flyback converters in the field of energy storage systems such as battery backup [19] and super capacitor applied systems [20].

Talking about the consequences of previously mentioned snubber networks to this study, bidirectional flyback converter is exposed followings. RC snubber and RCD network with rate-of-rise control, absorb energy at each voltage transition across the switch hence they lower the efficiency [10]. In RCD

clamp, while energy is being stored in the flyback transformer in one side, in the other side a current path is formed by the forward-biased diode of the snubber increasing the energy loss of the converter. Besides, since the capacitive load is charged and discharged periodically and consecutively, snubber capacitors will always tend to receive predefined steady-state clamp voltage at the respective energy flow direction introducing losses. Lastly, active clamp technique will bring the necessity of two additional high-voltage switch, isolated gate driver for the clamping switch and modified control technique to achieve ZVS.

This paper deals with a bidirectional flyback converter that is designed specifically for generator mode working DEAP together with the proposed RCDD snubber given in Fig. 2. The RCDD snubber is derived from the snubber known as non-dissipative LC snubber that was examined in [21]. The snubber capacitor size is minimised by series connected damping resistor sacrificing the stored energy in leakage inductance. The configuration is offering over voltage suppression, damping and reduction of the ringing. In addition, one operation cycle of the converter together with snubber is examined by dividing it to the states supported by mathematical models and verified by experimental results.

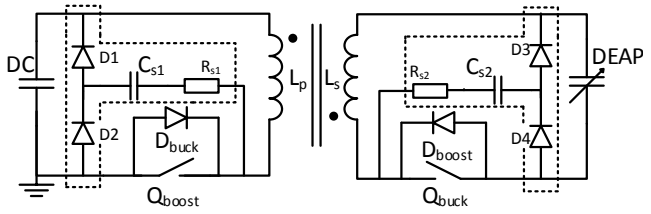


Fig. 2. Proposed bidirectional flyback converter with snubber.

The mentioned RCDD snubber that consists of a resistor R, a capacitor C and two diodes D, is given in Fig. 2 surrounded by dotted lines.

II. Principle of Operation

In this section one period of boost operation will be described in detail since operation principle is basically the same in either boost or buck mode. It should be noted that the analysis will be done considering ideal components.

In order to simplify the examination, one switching period is divided into seven time intervals i.e. from the beginning of one gate signal (G_1) to the next gate signal. In Fig. 3 ideal waveforms are depicted and they represent a random period in boost cycle since snubber capacitors are discharged at the very begining of the operation. Moreover axes of Fig. 3 are out-of-scale to accommodate the distinct interval description. It should also be noted that these waveforms are not referring to steady-state work since the converter mostly does not work in this region. This arises from the loads being a capacitor, and charged and discharged successively. However during the review of intervals the difference of steady-state work will be mentioned.

To start with, secondary side components are reflected to the primary (Fig. 4) and the DEAP variable capacitance is substituted by a fixed capacitor C_D since it can be considered constant during a boost or a buck operation. DC-link capacitor replaced with constant DC voltage source V_{DC}, names of Q_{boost} and Q_{buck} changed to Q_1 and Q_2 respectively and reflected components renamed by adding prime ($'$) to their name.

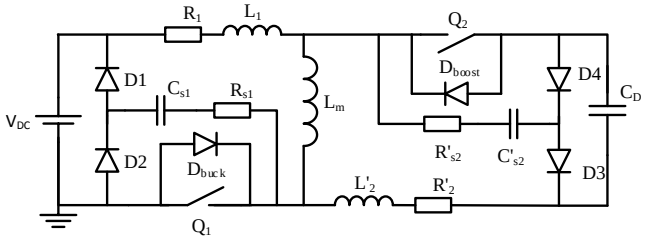


Fig. 4. Proposed bidirectional flyback converter with all the components are reflected to the primary side.

Here, in Fig. 4 denoting n for turns ratio of the transformer, reflected inductances and resistances are multiplied with n^2, while capacitances are divided by the same term.

Subsequently, in relation with the states of the switches, that is listed in Table I, current paths are demonstrated and components which no current flows in, are given in grey colour. Analysis is done by primary and secondary side leakage inductance currents $I_{L1}(t)$ and $I_{L'2}(t)$ respectively.

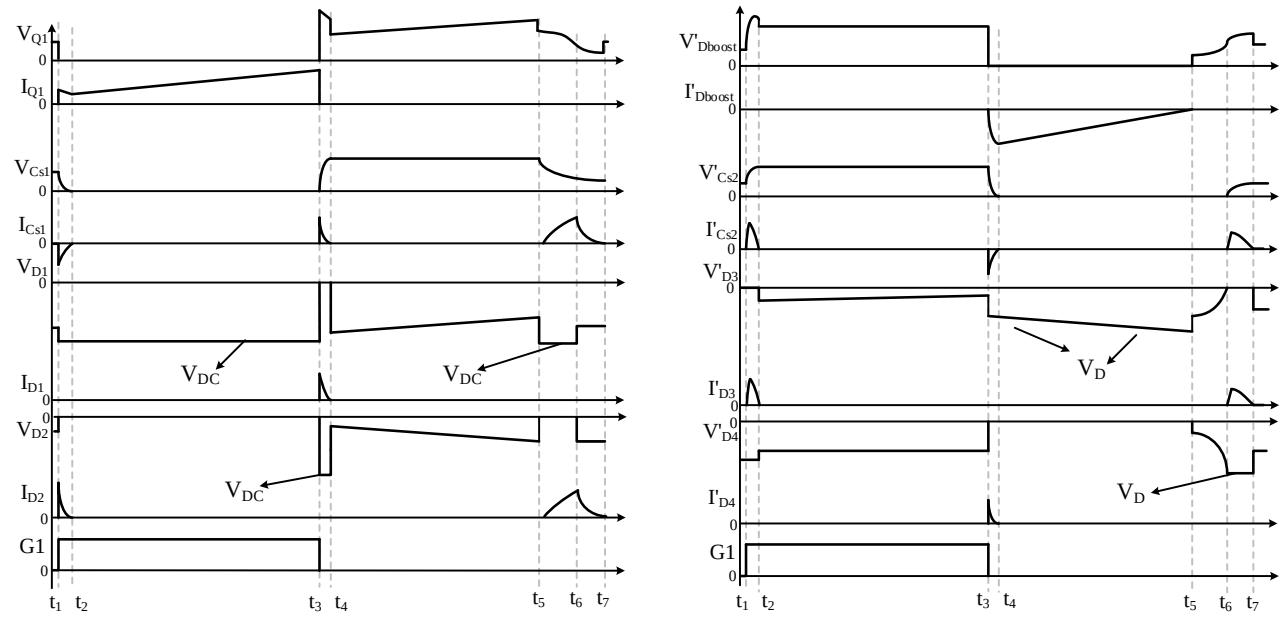
TABLE I
States of the Switches

	t_1-t_2	t_2-t_3	t_3-t_4	t_4-t_5	t_5-t_6	t_6-t_7	t_7-t_1
Q1	ON	ON	OFF	OFF	OFF	OFF	OFF
Q2	OFF	OFF	ON	ON	OFF	OFF	OFF
D1	OFF	OFF	ON	OFF	OFF	OFF	OFF
D2	ON	OFF	OFF	OFF	ON	ON	OFF
D3	ON	OFF	OFF	OFF	OFF	ON	OFF
D4	OFF	OFF	ON	OFF	OFF	OFF	OFF

A. Interval t_1-t_2

This section starts by the gate signal in Q_1. Snubber capacitor C_{s1} discharges and C'_{s2} charges, so the section ends when $I_{D2}(t)$ and $I_{L'2}(t)$ reaches to zero ampere again. States of the switches are given in Table I as well as the equivalent circuit is given in Fig. 5. Here, mesh current method is applied and equations are rearranged as in (1) and (2) which represent voltages that can be used to estimate primary and secondary side leakage inductor currents.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -L_m\frac{dI_{L2'}(t)}{dt} - R_1 I_{L1}(t) - V_{DC} \quad (1)$$



(a) Primary side waveforms

(b) Secondary side waveforms

Fig. 3. Voltage and current waveforms of one boost period.

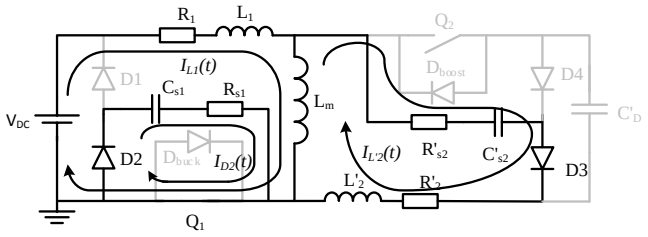


Fig. 5. State of the converter in interval t_1-t_2.

$$(L_2' + L_m)\frac{dI_{L'2}(t)}{dt} = -L_m\frac{dI_{L1}(t)}{dt} - I_{L'2}(t)(R_{s2}' + R_2') - V_{C's2}(t) \quad (2)$$

$$I_{D2}(t_{1-2}) = I_{D2}(t_1)\, e^{-t/R_{s1}C_{s1}} \quad (3)$$

To talk about the steady-state work, C_{s1} is completely discharged and C_{s2}' is charged to its final value at the end of each period and no current flows due to snubbers in this interval of t_1-t_2. Hence $I_{L'2}$ is substituted as zero value in (1) and (2) resulting $V_{C's2}$ to be constant at steady-state. Besides, before steady-state $I_{D2}(t)$ flows through Q_1 and it can be obtained by (3).

B. Interval t_2-t_3

When the converter is in this state, it means that primary side capacitor is completely discharged on Q_1 and secondary side capacitor is charged to some voltage that it does not draw current from the flyback transformer. This interval can be named as main energy storage phase to the transformer. The state ends when gate signal goes low at switch Q_1. The only current flowing in the circuit is $I_{L1}(t)$, illustrated in Fig. 6 and it can be obtained by solution of (4) for $I_{L1}(t)$.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -R_1 I_{L1}(t) - V_{DC} \quad (4)$$

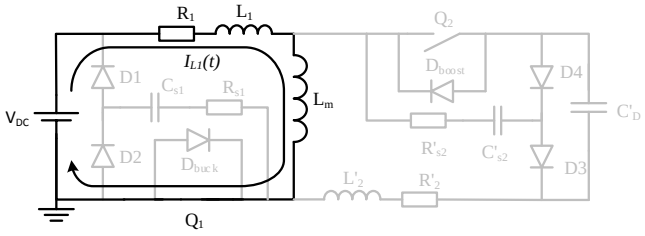


Fig. 6. State of the converter in interval t_2-t_3.

C. Interval t_3-t_4

In this interval Q_1 is no longer conducting. A high di/dt occurs at both end of the transformer, inductances L_1 and L_m changes their polarity, $I_{L1}(t)$ drops and $I_{L'2}(t)$ rises. The interval finalizes when $I_{L1}(t)$ and $I_{D4}(t)$ reach to zero ampere. The voltage spike which brings the necessity of the snubber on primary side switch, Q_1 arises at this very section. As it is illutrated in Fig. 7, primary side snubber network creates a path for the leakage inductance current I_{L1}, and the voltage spike is suppressed to acceptable level.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -L_m\frac{dI_{L'2}(t)}{dt} - I_{L1}(t)(R_1 + R_{s1}) + V_{Cs1}(t) \quad (5)$$

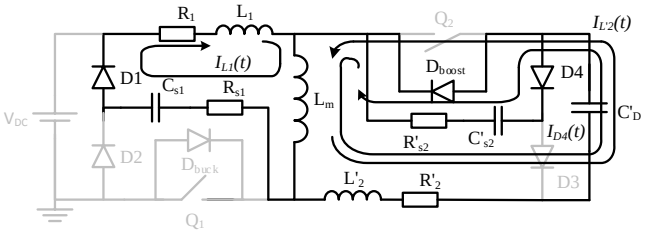


Fig. 7. State of the converter in interval t_3-t_4.

$$(L_2' + L_m)\frac{dI_{L'2}(t)}{dt} = -L_m\frac{dI_{L1}(t)}{dt} - R_2' I_{L'2}(t) + V_{C'D}(t) \quad (6)$$

Currents flowing in the converter can be obtained by solution of (5) and (6). Here, since C'_{s2} is very small compare to C_D, a simplification is made that, energy stored by itself is dissipated on R'_{s2}, R'_2 and series resistance of C'_D meaning that $I_{D4}(t)$ is not expressed.

D. Interval t_4-t_5

This period can be named as flyback period. Energy stored in the transformer is moved to the output in this interval. $I_{L'2}(t)$ is the only current flowing in the converter which is illustrated in Fig. 8 and can be calculated by solution of (7) for $I_{L'2}(t)$.

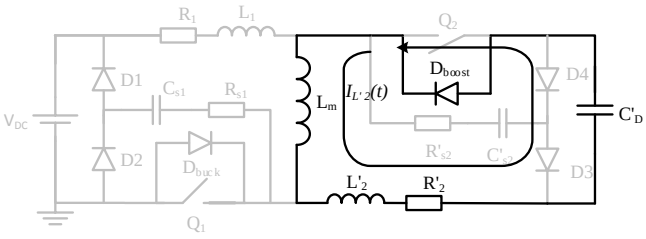


Fig. 8. State of the converter in interval t_4-t_5.

$$(L_2' + L_m)\frac{dI_{L'2}(t)}{dt} = -R_2' I_{L'2}(t) + V_{C_D'} \quad (7)$$

E. Interval t_5-t_6 and t_6-t_7

When converter steps into stage t_5-t_6, energy transfer is already done and the only current that flows in the converter is due to primary side snubber capacitor C_{s1}.

C_{s1} is at the voltage that was charged in interval t_3-t_4 and in Fig. 9 it is shown that an RLC circuit occurs, however D_2 restricts the oscillation. The current flows as follows: First $I_{L1}(t)$ builds up and at the very moment that it crosses its peak value, interval t_5-t_6 ends. So now it is interval t_6-t_7.

According to inductor voltage expression $v = Ldi/dt$, when slope of current changes its sign, i.e. di/dt changes sign, accordingly inductor changes its polarity. Then a second current $I_{L'2}(t)$ flows as in Fig. 10. In case C'_{s2} charges high enough ($\geq V_{DC}/n$) then it does not draw current in interval t_1-t_2.

Equation (8), (9) and (10) can be solved in order to calculate the currents in intervals t_5-t_6 and t_6-t_7 respectively.

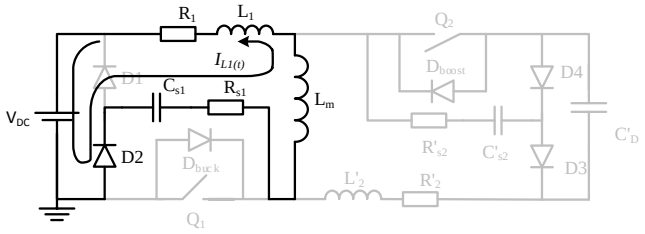


Fig. 9. State of the converter in interval t_5-t_6.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = V_{C1}(t) - I_{L1}(t)(R_1 + R_{s1}) + V_{DC} \quad (8)$$

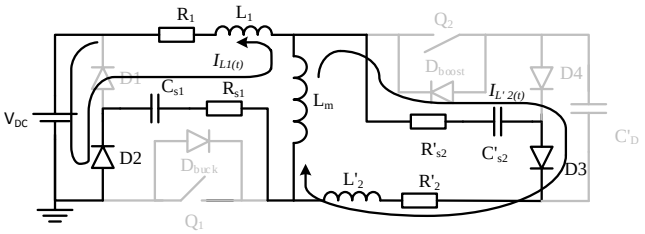


Fig. 10. State of the converter in interval t_6-t_7.

$$(L_1 + L_m)\frac{dI_{L1}(t)}{dt} = -L_m\frac{dI_{L'2}(t)}{dt} - I_{L1}(t)(R_1 + R_{s1}) - V_{DC} + V_{C1}(t) \quad (9)$$

$$(L_2' + L_m)\frac{dI_{L'2}(t)}{dt} = -L_m\frac{dI_{L1}(t)}{dt} + V_{C'2}(t) - I_{L'2}(t)(R_2 + R_{s2}) \quad (10)$$

F. Interval t_7-t_1

In this interval all the switching devices are turned-off thus there is no current flowing.

G. Snubber component selection

So far, one switching period of the converter in boost mode working has been analysed. The intervals that snubber network shows its function and influence have been observed. Converter state at interval t_3-t_4 where voltage spike is being suppressed, can be a start point to size the components.

Here, the components will be sized based on energy in leakage inductance and damping. It starts with sizing the snubber capacitances. At this point energy stored in the leakage inductances was considered. Equation (11) is derived from equalizing energy expressions of a capacitor and inductor, correspondingly writing the expression with respect to capacitance. By this, a capacitor value is found to be minimum. Measured transformer parameters and maximum

emitter-collector voltage of the IGBT to use the expression, are given in Table II.

$$C_{s1,s2} \geq \frac{L_{L1,L'2}\,\hat{I}^2_{L1,L'2}}{V^2_{Q1,Q2(\max\_CE)}} \tag{11}$$

In this case, with 15 A peak current ($\hat{\mathrm{I}}_{\mathrm{L1}}$) value on the primary side, according to (11) $\mathrm{C_{s1}}$ and $\mathrm{C_{s2}}$ are found to be 1.6 nF and 0.43 nF respectively. In practice, $\mathrm{C_{s1}}$ and $\mathrm{C_{s2}}$ are chosen to be 4.7 nF and 2.2 nF respectively. To continue with sizing the resistors, it can be done by (12). Here ζ is the damping factor and it is chosen to be $1/\sqrt{2}$ (≈ 0.707). This makes $\mathrm{R_{s1}}$ and $\mathrm{R_{s2}}$, 100 and 333 ohm respectively.

$$R_{s1,s2} = 2\zeta\sqrt{\frac{L_{L1,L2}}{C_{s1,s2}}} \tag{12}$$

Lastly, diodes on the primary side must be able to block maximum DC-link voltage, as well as the ones on the secondary side must be able to block maximum output voltage. Therefore GP02-40 diodes were used which has maximum DC blocking voltage of 4000 V and 15 A peak forward surge current.

H. Summary

In this section one period of boost operation has been examined. By division of the period to seven intervals, not just well-known flyback operation but also the proposed snubber have been analysed.

In I, it has been mentioned that snubber capacitor value is minimised. It is because not to seize the output energy in snubber part. II-A validates that secondary side snubber absorbs energy during energy storage period to the transformer and the same process arises in buck mode operation for primary side snubber as well. In intervals $\mathrm{t_1}$-$\mathrm{t_2}$ and $\mathrm{t_3}$-$\mathrm{t_4}$ this absorbed energy is dissipated. On the other hand choosing a low value snubber capacitor penalizes its ability to suppress overvoltages. So it is a trade-off between voltage spike and energy waste.

It can straightforwardly be seen in intervals $\mathrm{t_5}$-$\mathrm{t_6}$ and $\mathrm{t_6}$-$\mathrm{t_7}$ that diodes $\mathrm{D_2}$ and $\mathrm{D_4}$ create path not only to discharge of $\mathrm{C_{s1}}$ but also charge of $\mathrm{C_{s2}}$. This means that energy absorption in the secondary side during intervals $\mathrm{t_1}$-$\mathrm{t_2}$ decreases while primary side snubber becomes ready for next energy take of from leakage inductance $\mathrm{L_1}$.

Ideally, in a boost operation as long as duration of conduction of primary side switch $\mathrm{Q_1}$ remains the same, peak primary side current, accordingly energy stored in leakage inductance remains the same. It has also been observed that at the end of each period, $\mathrm{C_{s1}}$ discharges more than previous period; eventually in steady-state zero volt so that voltage overshoots ratio due to primary side components gets lower. However increasing stress caused by the load capacitance voltage, keeps the all in all voltage spike getting higher but with less increment ratio.

Lastly, current paths created by diodes D_2 and D_4 (Fig. 9 and Fig. 10) make the snubber network to involve in and lower the ringing caused by $\mathrm{C_{OSS}}$ of the switching devices and leakage inductances and so that ringing during the interval t_7-t_1 has lower amplitude and frequency.

III. Experimental Setup

To start with, firstly the design criteria then components of the converter are required to be selected. The converter is designed to work in discontinuous conduction mode boosting the voltage of DEAP generator from 500 V to 2 kV and then bucking it back to 500 V with maximum 15 A in the primary side. Considering these criteria, maximum stress on the switching devices is found by (13) and (14).

$$V_{Q_{1(max\_CE)}} = nV_{C_D} + V_{DC} \tag{13}$$

$$V_{Q_{2(max\_CE)}} = \frac{V_{DC}}{n} + V_{C_D} \tag{14}$$

IGBTs that were used, are given in Table II. According to (14) maximum voltage rating of secondary switch must be higher than maximum output voltage so that selected component fulfils the requirement.

TABLE II
Converter Component Parameters

L_1	25.86 μH	Cs1	4.7 nF
L_2	111.34 μH	Rs1	100 Ω
R_1	0.55 Ω	Cs2	2.2 nF
R_2	3.74 Ω	Rs2	333 Ω
L_m	6.22 mH	D1-D4	GP02-40 (4 kV)
n	0.5	$D_{buck,boost}$	GP02-40 (4 kV)
Q_{boost}	IXGF25N300 (3 kV)	Q_{buck}	IXGF25N300 (3 kV)
C_{DC}	53.3, 77.5, 117.5 μF	C_D	2.26 μF

Going on with the efficiency measurements, it is done by replacing the DC voltage source with a pre-charged capacitor as in Fig. 2 and estimating the energy flow in both end of the converter. Since the values of the capacitors are known, only needed parameters for the efficiency measurement are their voltages. Equation (15) is used to estimate the input and output energy of the converter during both boost and buck modes so that efficiency can be calculated by E_{out}/E_{in}.

$$\Delta E = \left|\frac{1}{2}C_{DC,D}(V^2_{\mathrm{start}} - V^2_{\mathrm{end}})\right| \tag{15}$$

In Table II three different capacitance values are given for $\mathrm{C_{DC}}$. It should be mentioned that depending on the amount of energy being transferred, different sized capacitors were used.

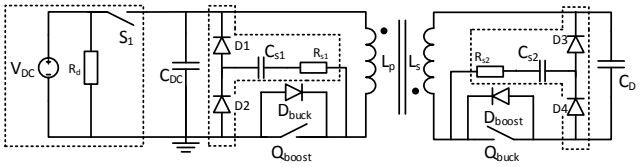


Fig. 11. Circuit diagram of the test setup.

Fig. 11 illustrates the circuit diagram of the test setup and mechanical switch S_1 is used to charge C_{DC} up to V_{start} voltage that was 400 V, and after it is opened, boost and buck operations are performed successively.

In order to operate the converter, a precise MATLAB® model was implemented and necessary duty cycle and number of pulses were obtained at desired operation current, voltage and frequency. In this way the converter was run in open-loop mode.

IV. Test Results

In this section along with the voltage waveforms of power switches, experimentally obtained converter efficiency by operating voltages at boost and buck mode working with 3 primary peak-current values (5, 10 and 15 A) are presented.

In Fig. 12 and Fig. 13 switching waveforms of IGBTs are given with RCD and RCDD snubber. For boost mode operation, last switching period of the secondary side IGBT Q_2 and accordingly for buck mode operation, first switching period of primary side IGBT Q_1 are illustrated, since the highest overshoot ratio occurs at these periods. It is clear in the figures that in spite of higher snubber capacitance in RCD snubber voltage spikes are higher. Herein series damping resistor of RCDD snubber plays a significant role. Another important point to realise in the figures, is ringing. Both frequency and amplitude of the ringing is dropped with RCDD network.

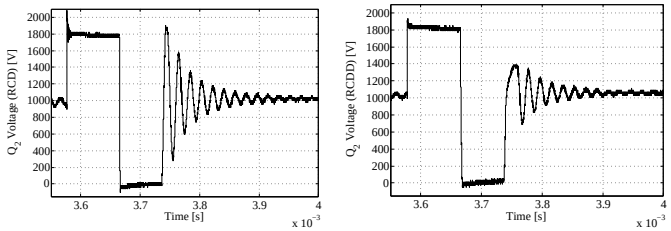


Fig. 12. Experimental voltage waveforms of the secondary side switch Q_2 with (a) RCD snubber (b) RCDD snubber at boost mode operation.

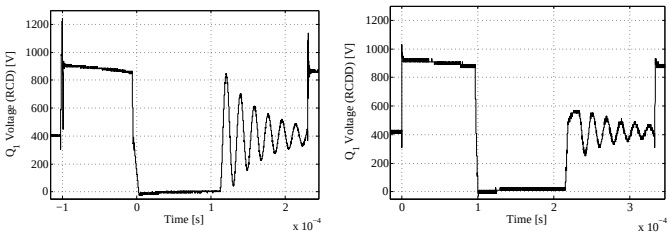


Fig. 13. Experimental collector-emitter voltage waveforms of the primary side switch Q_1 with (a) RCD snubber (b) RCDD snubber at buck mode operation.

In Fig. 14 and Fig. 15, efficiency maps of the converter with RCD and RCDD snubber, are illustrated and maximum energy conversion efficiency for the boost mode is found to be 91.34 % and 87.3 % for the buck mode (with RCDD snubber). Before the operation starts, input voltage V_{DC} and output voltage V_{C_D} were set to 400 V and 500 V respectively. After every boost operation converter working reference for buck operation was to lower the V_D voltage back to 500 V.

In the efficiency maps it can straightforwardly be noticed that at higher primary peak-current values efficiency is higher and it decreases by increasing operating voltage. This behaviour arises from decreasing number of pulses for higher current values and increasing number of pulses for higher voltage values. Switching losses of the used IGBT is remarkable.

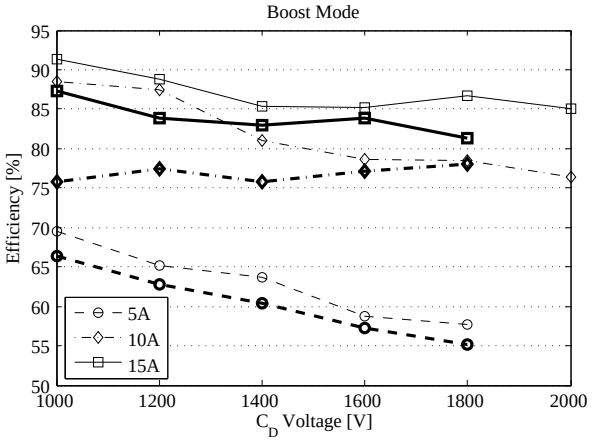


Fig. 14. Experimentally obtained energy transfer efficiency map of the converter at boost mode operation. Thick lines and markers shows RCD snubber as well as thin ones RCDD.

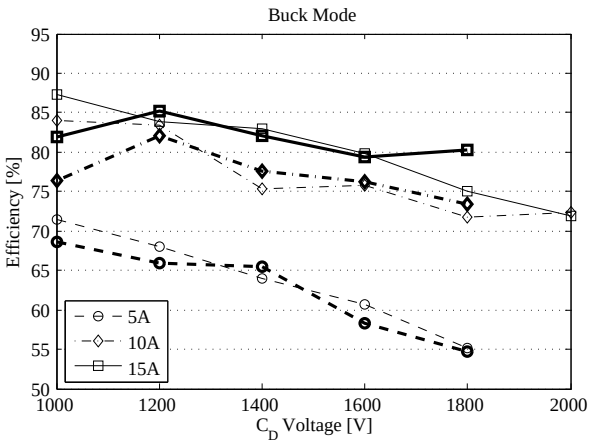


Fig. 15. Experimentally obtained energy transfer efficiency map of the converter at buck mode operation. Thick lines and markers shows RCD snubber as well as thin ones RCDD.

Lastly, RCD snubber network passive component parameters are respectively 420 kΩ and 33 nF for primary side and 1.5 MΩ and 16 nF for secondary side. The parameters are based on 50 V clamp voltage ripple, in order to minimise

energy waste by the clamp capacitor. Just as it is in interval t_1-t_2 of RCDD snubber, RCD snubber also draws energy during the energy storage period of flyback transformer. Furthermore the clamp voltage changes by the change of energy flow direction so that capacitor value is needed to be kept low. Eventually, the size of the capacitor is a trade-off between the energy loss and voltage spike.

V. Conclusion

A bidirectional flyback converter with a proposed RCDD snubber has been presented and analysed in detail. The converter has demonstrated high efficiency at specific working point promising future. Decrement in efficiency by increasing number of pulses showed that for this particular converter, performance of switching devices plays a significant role.

On the other hand, proposed RCDD snubber exhibited expected behaviour by protecting the switching devices against voltage spikes and allowing them to work safely in the designed operating area. The experimental results shows that RCDD snubber network demonstrates better over voltage protection than RCD snubber with slightly higher converter efficiency in most of the operation points.

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