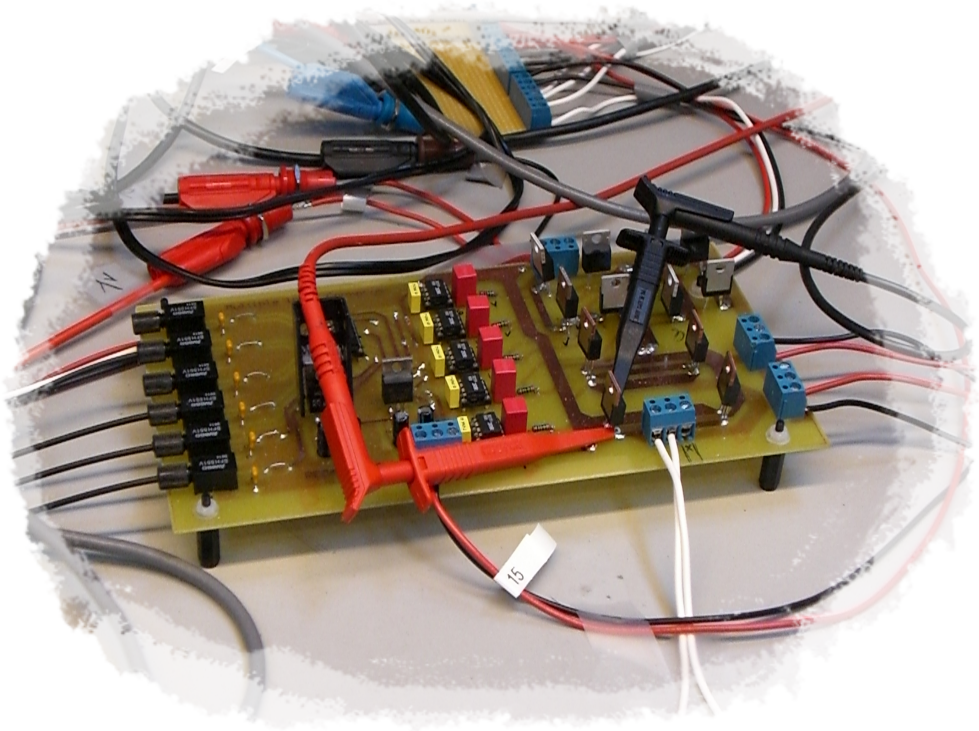
Multiple-Input-Converter for a Battery-Ultracapacitor Hybrid Electric Vehicle



Master Thesis

by

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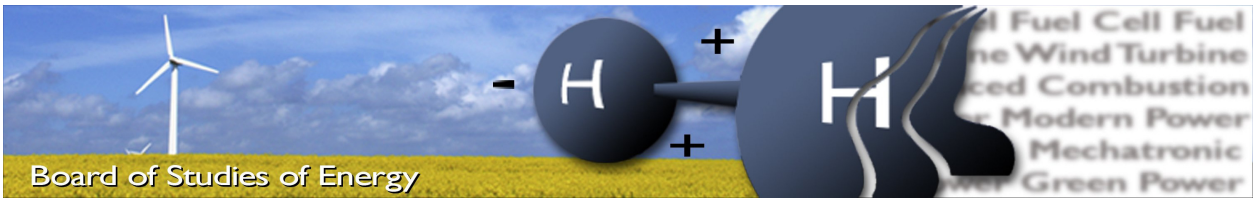
PED4-1038A - Spring Semester, 2009



Title:	Multiple-Input-Converter for a Battery-Ultracapacitor Hybrid Electric Vehicle
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Supervisor:	Erik Schaltz
Project group:	PED4-1038A

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SYNOPSIS:

The project is focused on a new DC-DC converter topology for an automotive application. The proposed converter is a multiple input DC-DC converter fed by batteries and ultracapacitors, capable of working in boost and buck mode.
The main objective is to create a simulation model of the converter, and later on, a real prototype.
The converter has been implemented in Matlab/Simulink. Then the control parameters have been modeled through Matlab/sisotool. The results confirm stable and suitable perform in close loop.
Finally a converter prototype has been built in the laboratory.

Copies:	3
Pages, total:	118
Appendix:	6
Supplements:	-

By signing this document, each member of the group confirms that all participated in the project work and thereby all members are collectively liable for the content of the report.

Preface

The present report is prepared by the Group PED4-1038A in the 4th Semester, at Power Electronics and Drives, Aalborg University. The project, with the title *Multiple-Input-Converter for a Battery-Ultracapacitor Hybrid Electric Vehicle*, was a proposal from Erick Schaltz. The main idea of the project is to build and control a bi-directional multiple-input-converter which is able to distribute the bus power between a battery and ultracapacitor in a sufficient maner.

The project is documented in a main report and appendixes. The main report can be read as a self-contained work, while the appendixes contain details about measurements or other data. In this project the chapters are consecutive numbered whereas the appendixes are labeled with letters.

Figures, equations and tables are numbered in succession within the chapters. For example, Fig. 4.2 is the second figure in chapter 4.

Bibliography is referred in brackets, using Vancouver style, for example [10]. More detailed information about the sources is given at the end of the main report in Bibliography.

Matlab/Simulink is used for all the simulations. For implementation in the real time system a DSP is used. The sofware used as an interface between the user and the DSP is the Code Composer.

A CD-ROM containing the main report and appendixes is attached to the project.

We would like to thank our supervisor, Erick Schaltz, for all his support in helping us with the problems that we confronted.

The authors

The report consists of 8 chapters. First the report begins with an introduction chapter where an introduction to the subject, the objective and problem statement are presented. In the next chapter the system description is presented. The mathematical models and simulations are discussed in Chapter 3 and Chapter 4. The control of the converter is presented in Chapter 5. Chapter 6 describes the design of the converter. In Chapter 7 the laboratory work and results are presented and analyzed. Finally in Chapter 8 the conclusions are taken.

The vision of replacing many of the cars on the road with clean commuter vehicles has caused most producers of cars to start building electric cars with as low price as possible. Electric cars use the energy stored in a battery or other type of energy storage systems for vehicle propulsion and provide a clean and safe alternative to the internal combustion engine. Nowadays in many places the governments have start limiting the use of very polluting cars, where only vehicles with very low emissions are allowed to operate. Moreover many governments have start providing financial subsidies and tax reductions to promote the use of electric vehicles (EVs). Making the society aware of a more clean and renewable transportation is a priority for many countries. Response to this governmental promotion is sure to be a major issue among automobile manufacturers around the world [7].

Chapter 3 presents the battery and ultracapacitor. With multiple-input converters the advantages of different sources with different voltage and current characteristics can be combined for an optimal energy use. The integration of different power sources with distinct energy and power density enables the coordination of the advantages of each source and overcome the limitations they may have and the reliability and flexibility of renewable sources are improved.

In Chapter 4 is described the model of the converter. First, the buck converter is presented. The mathematical development is made. Afterwards, the implementation in Matlab/Simulink is done and finally, the results are shown. The same is made for the boost converter. The chapter is concluded with the combination of the buck and boost converter. The new two power direction converter is presented without any control, wich is presented in the Chapter5 of the report. The main task of the Chapter 5 is to analyze and implement closed loop control of the converter. Regulation of the duty cycle value ensures the stable operation of the converter, and keeps the output voltage to the desired voltage. This control is made up of an inner current closed loop, which regulates the inductor current, and an outer close loop necessary for regulating the output voltage.

The theoretical analysis shown in the previous chapters, enables developing the converter that would meet the design demands. The main concern is the selection of the switches together with the gate drivers for them.

After the converter, together with the control board, was designed and successfully built, its performance should be evaluated through laboratory tests. This chapter summarizes the obtained results. The tests were conducted in such a manor to be able to examine operation of each part separetely. Final test compromised the whole system linked together to check if it can operate together. Therefore in the next sections are presented the measurementes and observations made for separate to the separate components and for the whole setup.

Contents

List of Figures

1 Introduction

1.1 Task background

The vision of replacing many of the cars on the road with clean commuter vehicles has caused most producers of cars to start building electric cars with as low price as possible. Electric cars use the energy stored in a battery or other type of energy storage systems for vehicle propulsion and provide a clean and safe alternative to the internal combustion engine. Nowadays in many places the governments have start limiting the use of very polluting cars, where only vehicles with very low emissions are allowed to operate. Moreover many governments have start providing financial subsidies and tax reductions to promote the use of electric vehicles (EVs). Making the society aware of a more clean and renewable transportation is a priority for many countries. Response to this governmental promotion is sure to be a major issue among automobile manufacturers around the world [7].

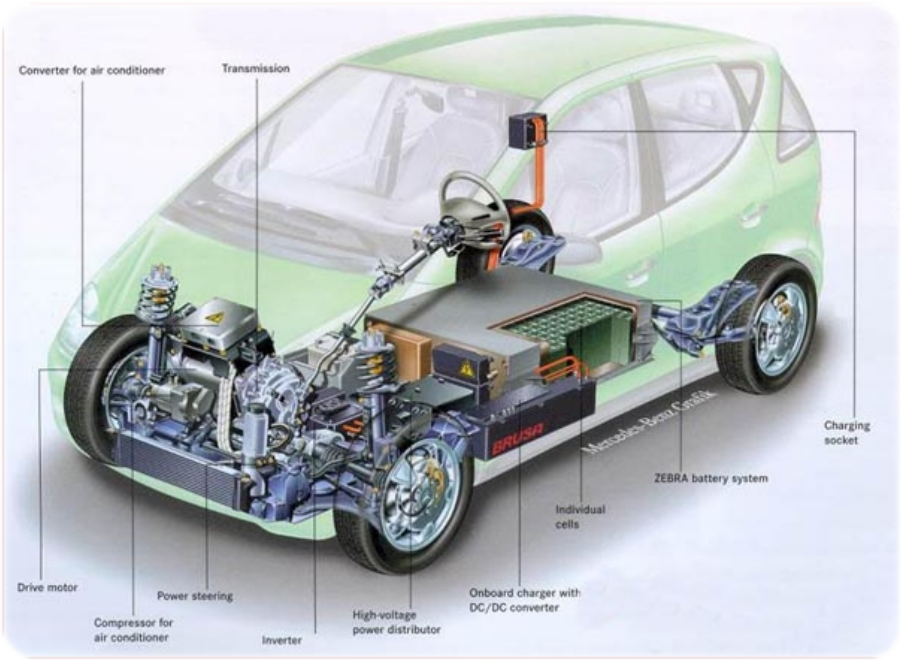


Figure 1.1: *Example of a comercial electric car.*

There are three types of electric cars [6]:

- The battery EV (BEV) uses batteries as an energy source, and electric motors as the propulsion device. The BEVs have not been commercially available under mass production yet, mainly because of their high limitations for long distance routes, as they have a driving range of about 100 km per charge.

- The hybrid EV (HEV) is composed by a common combustion engine as well as by an electric motor propulsion device. It uses a gasoline or diesel fuel as the main propulsion source, and makes use of batteries as a secondary energy source. Hybrid cars can drive ranges as diesel or gasoline cars while produces much lower emissions. This HEV has start been commercially under mass production.

- The fuel cell EV (FCEV) adopts fuel cells as the main energy source, and the electric motor as the propulsion device. Being fueled by hydrogen or methanol, the FCEV can provide a driving range comparable with a typical gasoline car but due to the high costs, this FCEV is not yet commercially available, see Fig.1.2.

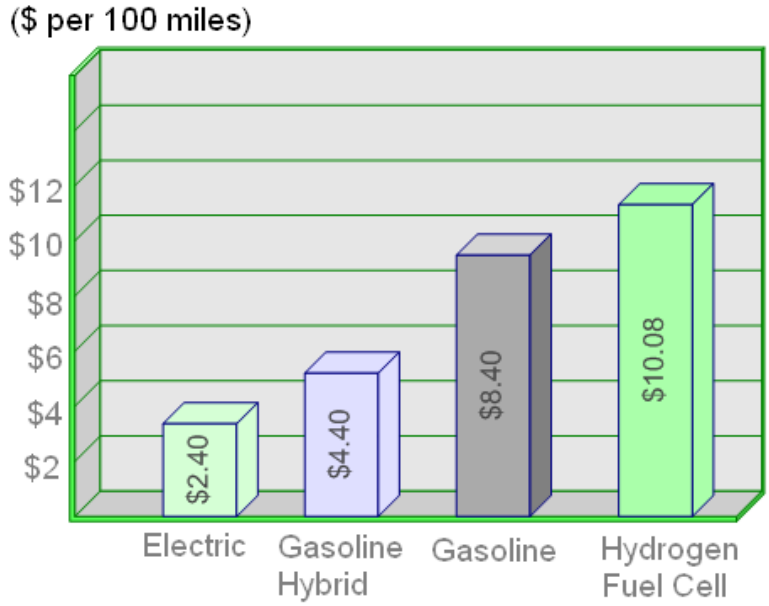


Figure 1.2: *Equivalent costs per distance of different vehicles. [10]*

Figure 1.2 shows the money costs for different types of cars, per 100 miles route. I.e. for a 100 miles route with a gasoline car, it is necessary an equivalent money of 8.40 dollar, while a hybrid electric car can coverthe double of the distance with the same amount of money. Furthermore, a pure electric car, can make between 3 and 4 times the distance made by the gasoline car (with the same amount of money). However, even if the manufacture and the energy costs of an electric car could be cheaper than a normal car, they will certainly not be cheaper until their sales will be as higher as a diesel or gasoline car.

Until an electric car manufacturer achieves high enough sales to approach a gasoline car manufacturer's volume efficiencies, electric cars will need to compete on other grounds besides price where the advantages are evident as summarized below [6]:

- EVs offer high energy efficiency. In general, the overall energy conversion efficiencies from crude oil to vehicle motion are about 9-18%. While EVs, can perform efficient braking

by converting the kinetic energy back to electricity with an efficiency of nearly25%.(Including the efficiency of the electrical energy generation process). The overall process is presented in the next Fig.1.3

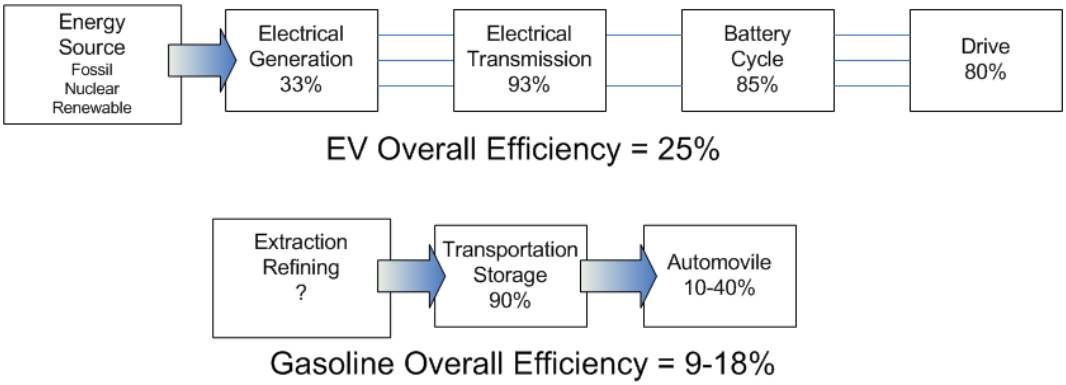


Figure 1.3: *Energy conversion efficiency.*

- Electricity can be generated not only from coal fired or nuclear power stations, but also from hydro-power, wind power, geothermal power, nuclear power, wave power, solar power...etc.

- By recharging EVs at night, non peak consumtions are produced and non-stockable energy is caused and so, the power generation facilities can be effectively utilized, contributing to energy saving and stabilization of power cost.

- Even globally, the emissions due to the generation of electricity for EVs are very low compare to the emissions caused by each of the gasoline or diesel vehicles all over the word.

- EVs operate quietly and almost do not vibrate. Thus, EVs are welcomed by drivers and appreciated by local residents. Electric motors provide a clean and safe alternative to the internal combustion engine.

Besides the obvious emissions advantage, there is another way that an electric car can be better than a gasoline car – in a word, torque. A gasoline engine has very little torque at low rpm's and only delivers reasonable horsepower in a narrow rpm range. On the other hand, an electric motor has high torque at zero rpm. It is quite easy to build an electric car that is both highly efficient and also very quick. The electric car accelerates at least as well as the best sports cars, but is six times as efficient and produces one-tenth the pollution [7].

The main inconvenient of the electric cars is their too short driving range, of about 100 km, while a typical gasoline car can go more than 400 km with a full tank. Moreover there are not any recharging stations along the highways, and since it takes time to charge batteries it would not be possible to make long trips. From this perspective, an electric car could only be suitable for urban use [7].

Hybrid-electric vehicles require an advanced, compact, high energy-density electrical storage system to provide both high power and high energy.

The Ragone Diagram, shown in Fig. 1.4, compares the performance of energy storage in terms of power and energy density.

In a near future, utilization of renewable sources will be of particular interest. Customer demands for good acceleration and performance in pure EVs and the requirements in hybrid

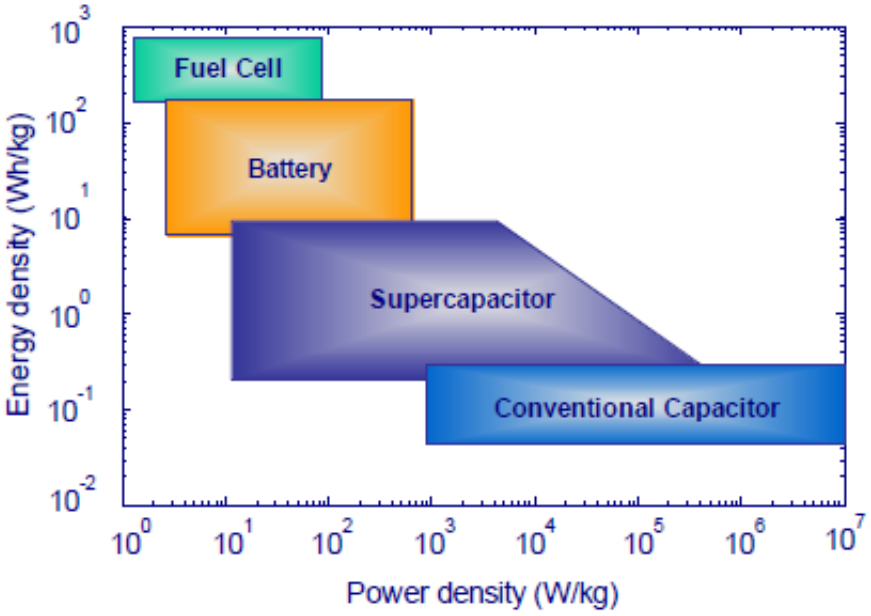


Figure 1.4: *Ragone diagram: energy and power density. [11]*

cars to reduce the emissions will be of great challenge for vehicle companies when combining different energy storage systems and propulsion. The electrical vehicles field, integrates electrical engineering where the interfacing of different energy sources will be required. In most cases, one source may be preferential to others, and should satisfy differentdemands, like fast charging and discharging capabilities, long life components, low cost and low maintenance.

1.2 Problem analysis

This project is based on the investigation of a multiple input power converter. In other words, the project is focused on the device which is capable of managing the energy flow between the electric motor and the storage devices.

Because batteries have a high energy density, but limited power density, are capable of supplying the main power to drive the motor; however is not able to supply peaks of power in short time periods. Moreover, ultracapacitors have a low energy density but high power density. Therefore; by combining these two devices an efficient, light, and high-performance vehicle can be obtained.[8]. By means of this combination, it is possible to use a smaller battery with less peak-output power capability.

1.3 Project goal

In this project the goal is to analyze, simulate and control a bi-directional multiple-input-converter which is able to distribute the bus power between a battery and ultracapacitor in a sufficient manner. Therefore, simulation and verification of a battery and ultracapacitor is also necessary for a proper modeling. The proposed converter is directly applicable to dc–dc systems and is derived from the buck-boost converter [9]. The multiple-input bi-directional topology has been introduced in this report can operate in buck, boost, modes.

The control strategies for the appropriate power distribution are implemented in a DSP for its real application analysis.

1.4 Constraints and limitations of the report

The project deals with the creation of a multiple-input-bidirectional dc/dc converter. Some constraints and limitations were applied during the development of the project in order to reach the objective.

- The switches are considered ideal. No losses are taken into account
- The converter works in Continuous Conduction Mode (CCM)

1.5 Report structure

The report consists of 8 chapters. First the report begins with an introduction chapter where an introduction to the subject, the objective and problem statement are presented. In the next chapter the system description is presented. The mathematical models and simulations are discussed in Chapter 3 and Chapter 4. The control of the converter is presented in Chapter 5. Chapter 6 describes the design of the converter. In Chapter 7 the laboratory work and results are presented and analyzed. Finally in Chapter 8 the conclusions are taken.

2
System Description

As mentioned in the previous Chapter 1, with multiple-input converters the advantages of different sources with different voltage and current characteristics can be combined for an optimal energy use. The integration of different power sources with distinct energy and power density (see Fig. 1.4) enables the coordination of the advantages of each source and overcome the limitations they may have and the reliability and flexibility of renewable sources are improved.

In Fig. 2.1(a) it is showed the height of a random track (m). It can be seen that there are some positive slopes, also as negative. The track lenght is about 3660 (m) and the variation of height is approximately 6 (m). The energy consumed by an electric car during a track is not always the same. It depends on the slope of the track, the requested speed of the vehicle or on possible accelerations. Therefore, in the same Fig.2.1(b), it is plotted the requested power (W) by a small mass car to maintain a constant speed along the track (constant speed of 30 km/h).

Bidirectional power flow

Taking a look to Fig.2.1(b) it can be seen that in most of the time, the energy is positive. It means that the motor is consuming energy. However, in a short time of period, the energy is negative. During this time, the energy is not consumed. It means that the motor is actuating as a generator. This way of working mode is known as regenerative brake. The energy obtained from braking the vehicle can be used to recharge the battery or the ultracapacitor. Usually, when the converter is supplying energy from the sources to the motor, is working in boost mode. It means that the output voltage of the converter is higher than the input. In the other case, when the system is working in the regeneration mode, the converter is stepping down the voltage. The output voltage is smaller than the input. This corresponds to the buck converter topology.

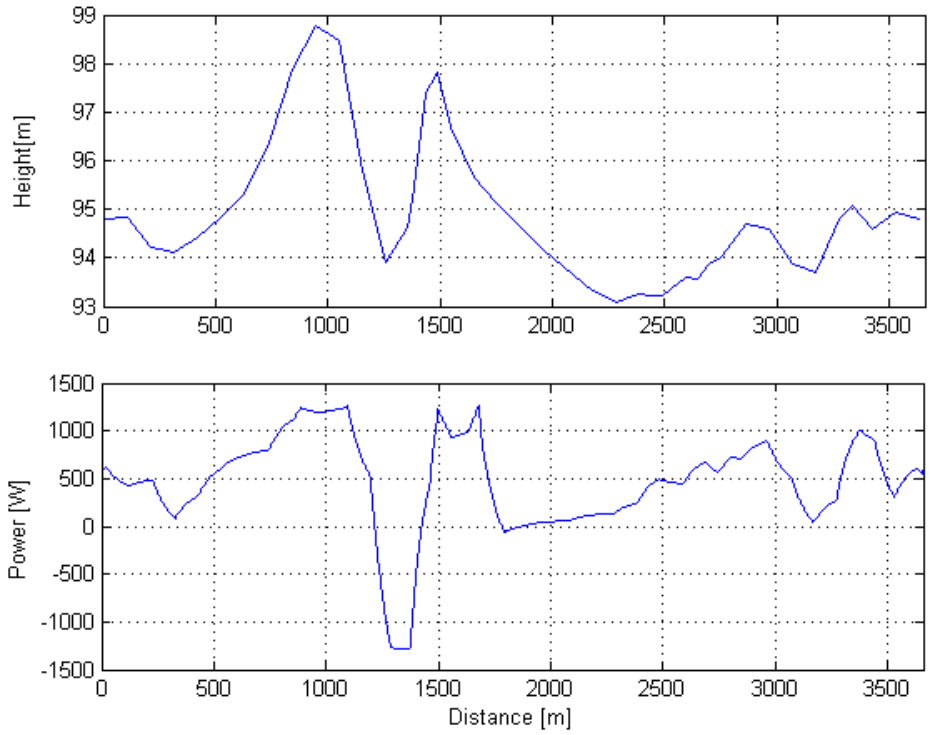


Figure 2.1: *(a)Height of a random track. (b) Power needed by an EV to maintain the speed in a random track*

Multiple input

In the same Fig. 2.1(b), if it is payed attention to the positive parts of the power (converter is working in boost mode), it can be seen that there are several peaks of power. As mentioned before, the combination of batteries and ultra-capacitors prolongs the lifetime of the battery because is the ultracapacitor the one who provides the power peaks.

System description

Next Fig. 2.2 presents the proposed electrical system of an EV. There are two input sources, a DC/DC converter, a dc bus, an inverter, an finally the motor. The project is focused on the DC/DC converter. It is important to mention that the parameters of the converter do not correspond to a real one used for this kind of application. The prototipe is scaled down in order to simplify the laboratory implementation. The rated power of the prototype is 2000 kW, around 10 times lower than a real application. Therefore, the parameters of the system are taken from a prototype placed in Aalborg University. It uses a battery bank of 4 components wich gives an output voltage of 48 V and several ultra-capacitors wich give 64 V in the output. The inverter Dc bus is rated to a voltage value of 136 V. With this data, the parameters of the converter are calculated in the Appendix A.

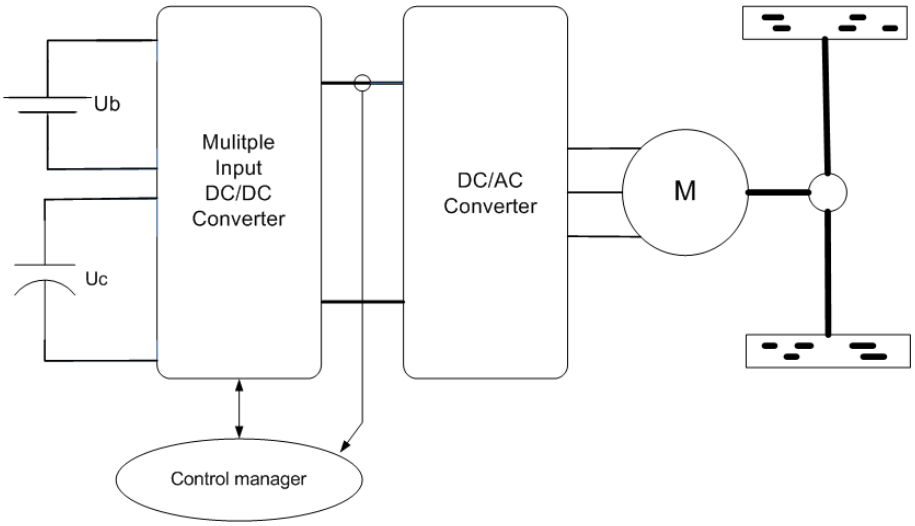


Figure 2.2: *Proposed multiple input topology.*

***

Once the system is described and the parameters are fixed, it is possible to implement the different Matlab/Simulink models of the energy sources and the converter. These models are presented in the following Chapter 3 and Chapter 4.

3
Model of the energy sources

This chapter is focused on the model analysis of the dc sources on the previous presented EV. First the battery bank is analyzed and afterwards, the ultracapacitors. The Matlab/Simulink models are implemented and to conclude the chapter simulation results are presented.

The performance and life-cycle costs of electric vehicles (EV) and hybrid electric vehicles (HEV) depend inherently on energy storage systems such as batteries. Battery pack performance directly affects the all-electric range, power for acceleration, economy, and charge acceptance during energy recovery from regenerative braking. Because the battery pack cost, durability, and life also affect the cost and reliability of the vehicle, any parameter that affects the battery pack must be considered [16].

3.1 Lead-acid battery pack

The batteries used in this project are lead-acid batteries. The model is presented in the Fig. 3.1

Their low cost of manufacture, their simplicity of design, reliability and they fact that they are considered quite safety when compared to other electrochemical systems make these type of the batteries one of the most spread electrochemical solutions used to store electrical energy. Other advantages of a lead acid battery are [16]:

- Robust.
- Tolerant to overcharging.
- Low internal impedance.
- Can deliver very high currents.
- Can be left on float charge for prolonged periods.
- Recycled product.

However, lead-acid batteries have many aspects to be improving for a better integration in automation and be competitive in the market. Their weigh and the fact that are very bulky is a big disadvantage for integrating them in a vehicle. Another factor to beat is their low charging time and the low cycle life. For their application in transport, the necessity of a

Figure 3.1: *Lead acid battery [18]*

fast charging is essential while their life should not be affected on each charge and discharge cycle. Other fact to be improved should be[5]:

- Prevention for overheating during charging;
- Sulphation may occur if a battery is stored for prolonged periods in a completely discharged state;
- Completely discharging the battery may cause irreparable damage;
- Contain toxic chemicals;
- Lower temperature limit.

Batteries can usually ensure a proper operation beyond a -3 C to + 35 C temperature environments. Battery life in a hybrid-electric vehicle is usually defined by the number of 100% charge/discharge cycles. Reducing the depth of discharge, increases the number of cycles in a battery's life [17].

Model Analysis of the Battery

The battery used in this project is a 12 (V) Lead-acid provided by Sonnenschein. The battery parameters are presented in Table 3.1[18].

Parameter	**Symbol**	**Value**
Nominal Voltage	V_n	12 $[V]$
Internal Resistance	R_s	0.0116[Ω]
Nominal Capacity (C_{20})	Q_n	40[Ah]
Discharge current	I	5[A]

Table 3.1: *Battery parameters.*

For modelling a battery there are many factors that affect the battery performance. The most important are:

- State of charge (SOC)
- Battery storage capacity
- Rate of charge/discharge
- Temperature
- Age

Model assumptions

In order to simplify the battery model, some assumptions are made:

- The internal resistance is supposed constant during the charge and the discharge cycles and does not vary with the amplitude of the current.
- The parameters of the model are deduced from discharge characteristics and assumed to be the same for charging.
- The capacity of the battery doesn't change with the amplitude of current.
- The model does not take the temperature into account nor the age.

The model of a lead acid battery has been implemented in Matlab/simulink. The model is based in a build-in model of the SimPowerSystems blockset.

The equivalent circuit of the battery is shown in Fig 3.2:

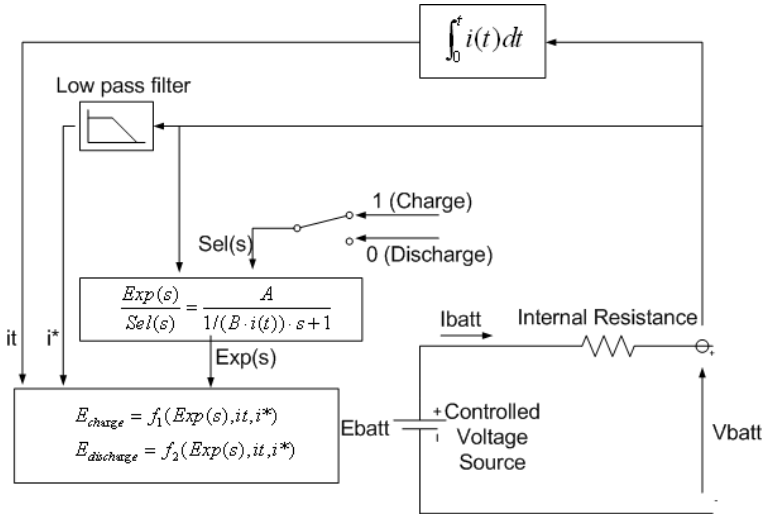


Figure 3.2: *Equivalent circuit of a battery.*

The control is made by measuring the current trough the internal resistance. This current is filtered to obtain an average current dynamic. The capacity extracted by the battery, is calculated by integrating the measured current. So as to make the control, the obtained variables are inserted in two different dynamic equations that controls the battery terminal voltage. A switch is the responsible for selecting the necessary equation for battery operating mode for charging or discharging it.

Dynamic equations for a Lead-Acid model

In the following are presented the dynamics equations used for modelling the battery:
In discharging mode the filtered current is considered positive (i*> 0), and the implemented equation is:

$$f_1(it, i*, i(t)) = E_0 - K \cdot \frac{Q}{Q - it} \cdot i* - K \cdot \frac{Q}{Q - it} \cdot it \tag{3.1}$$

On the other hand, when the battery is charging the low frequency current is negative (i* < 0):

$$f_2(it, i*, i(t)) = E_0 - K \cdot \frac{Q}{Q \cdot 0.1 + it} \cdot i* - K \cdot \frac{Q}{Q - it} \cdot it + \mathcal{L}^{-1}(\frac{A}{1/(B \cdot i(t))s + 1}.\frac{1}{s}) \tag{3.2}$$

The equation must be totally in time domain therefore:

$$1/(B \cdot i(t)) = C \tag{3.3}$$

$$\mathcal{L}^{-1}(\frac{A}{1/(B \cdot i(t))s + 1}.\frac{1}{s}) = \mathcal{L}^{-1}(A \cdot \frac{1}{Cs + 1}.\frac{1}{s}) = \frac{A}{C} \cdot \mathcal{L}^{-1}(\frac{1}{s + \frac{1}{C}}.\frac{1}{s}) \tag{3.4}$$

aplaying the Laplace tranformation

$$\frac{1}{s(s + a)} = \frac{1}{a}(1 - e^{-at}) \tag{3.5}$$

the discharging equation is expressed as follows

$$f_2(it, i*, i(t)) = E_0 - K \cdot \frac{Q}{Q \cdot 0.1 + it} \cdot i* - K \cdot \frac{Q}{Q - it} \cdot it + A(1 - e^{-B \cdot it}) \tag{3.6}$$

where,
E_0= Constant voltage (V);
K= Polarization resistance (Ohms);
Q= Maximum battery capacity (Ah);
$i(t)$= Battery current (A);
$i*$= Low frequency current (A);
it= Extracted capacity (Ah);
A= Exponential voltage (V);
B= Exponential capacity (Ah^{-1}).

State Of Charge

Knowing the amount of energy left in a battery compared with the energy it had when it was full gives the user an indication of how much longer a battery continues working before it needs to recharge. Thus, the state of charge of the battery (SOC) represents the difference between the amounts of energy left in the battery compared to the energy it has when it is full. For a good maintenance of the battery this value should not be less than 75% if possible.

The SOC for a fully charged battery is 100% and for an empty battery is 0%. The SOC is defined as the available capacity expressed as a percentage of some reference, sometimes its rated capacity but more likely its current.

To calculate the state of charge, Equ. 3.7 is used. The integral is approximated at each time step by a simple cumulative sum.

The SOC is calculated as:

$$SOC = 100\left(1 - \frac{\int_0^t i(t)dt}{Q}\right) \tag{3.7}$$

where,
$i(t)$=battery current,
Q= battery nominal capacity.

Matlab/Simulink model of the Battery

As different style of connection is used in SimPower, the equations have been implemented in Matlab-Simulink by using standard Simulink blocks.

The configuration of the battery is depicted in Fig. 3.3.

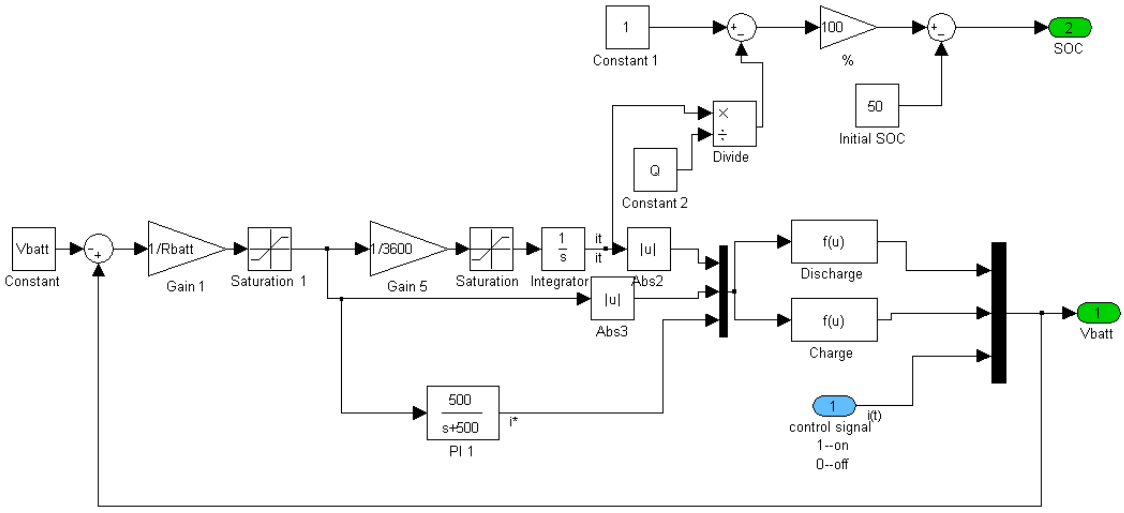


Figure 3.3: *Battery model*

The equation for the discharge mode of the battery is implemented inside the Fcn *'Discharge'* block . This block applies the specified mathematical expression to its input made up by the user. The charge mode is made the same way by introducing the dynamic equations inside the Fcn *'Charge'* block. For choosing the battery operation mode a control signal is necessary.

Simulation results

The discharge and charge voltages are despicted in Figure 3.4, which shows the exponential zone of the battery. As it can be seen this area is very small, typical for lead acid batteries. After this period the battery voltage is maintained near the nominal. In the case it is discharging, the voltage decreases very slowly near the nominal voltage until the battery energy is totally discharge.

When the battery is charging, the voltage is maintained to the supplied voltage, this case 12.5 voltage. A big advantage of Lead-Acid batteries is that they can last much time in float charge without overcharging them.

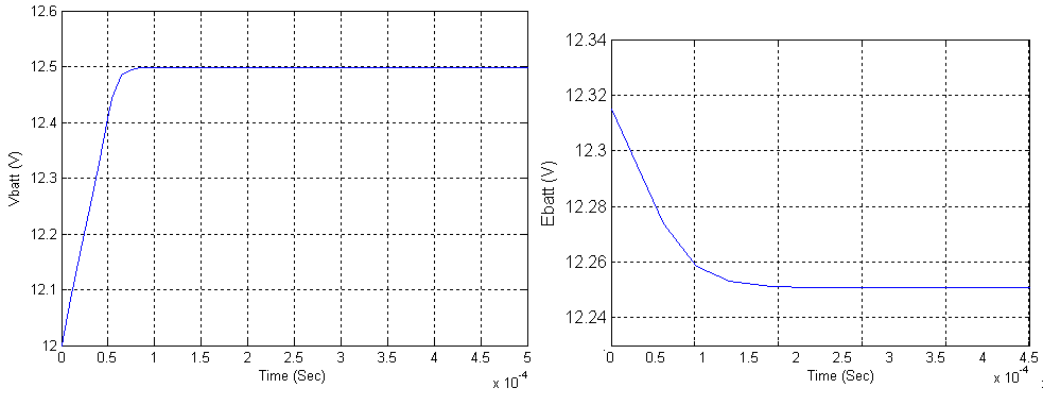


Figure 3.4: *Battery discharge and charge graphs.*

As it is mentioned before, batteries are responsible for supplying energy to the vehicles. A battery with 24 Ah can provide 24 amperes during one hour before is totally discharged. As it is shown in Fig. 3.5 for 10 seconds range the battery SOC decrease only 0.0012 %. This supposes 2.30 hours before is totally discharge if the battery would be totally charged.

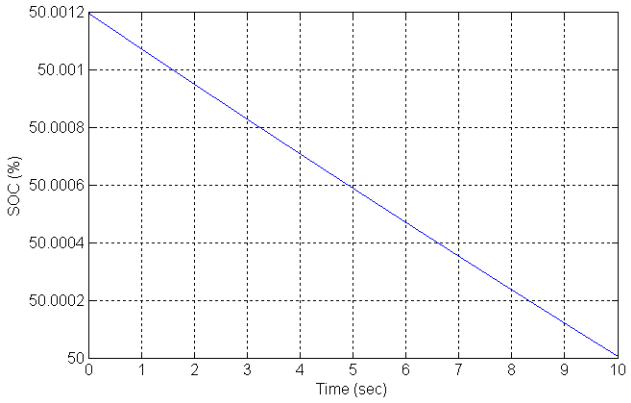


Figure 3.5: *State Of Charge*

3.2 Ultracapacitors

Capacitors are known to accept high power levels and store energy very quickly —much more quickly than the batteries and fuel cells already being used in electric and hybrid-electric cars. Unfortunately, typical capacitors have been able to store only tiny amounts of charge, making them useless for driving the high power engines these cars use. Not so ultracapacitors. Ultracapacitors are high power, low energy devices with high power density and cycle life, but cannot store the energy needed for long term or extended range all-electric operation. Ultracapacitor packs offer the storage and delivery of hundreds of kilowatts at efficiencies greater than 84%(depending on the power level). They have a greater than 500,000 charge/discharge cycle life and a -35 C to +65 C operating temperature environment. In hybrid vehicle applications ultracapacitor packs are projected to have a 10 to 12 year life [7]. While they still cannot store as much total energy as a fuel cell or a battery, ultracapacitors can supply the amount of energy needed to accelerate up a hill or around another car on the highway.

Model Analysis of the Ultra-Capacitor

The ultracapacitor used in this project is a 16 (V) module provided by Maxwell. The UC parameters are presented in Table 3.2[19]

Parameter	Symbol	Value
Operating Voltage	V_c	$16.2[V]$
Capacitance	C_{UC}	$250\ [F]$
Series Resistance	$R_{s_{UC}}$	$0.0075[\Omega]$

Table 3.2: *Ultracapacitor parameters*

The equivalent circuit used for conventional capacitors can also be applied to ultracapacitors. The circuit schematic in Fig.3.6 represents the first-order model for an ultracapacitor.

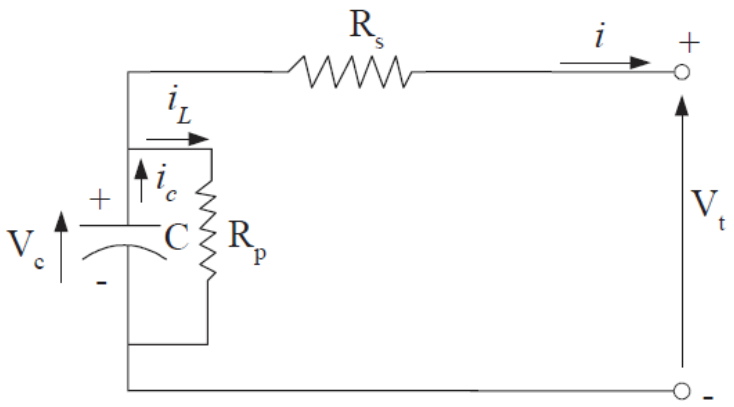


Figure 3.6: *Equivalent circuit of an ultracapacitor.*

It is comprised of four ideal circuit elements: a capacitance C, a series resistor Rs, and a parallel resistor Rp. Rs is called the equivalent series resistance (ESR) and contributes to energy loss during capacitor charging and discharging. Rp simulates energy loss due to capacitor self-discharge, and is often referred to as the leakage current resistance. Inductor L results primarily from the physical construction of the capacitor and is usually small. Therefore this value has been neglected.

Resistor Rp is always much higher than Rs in practical capacitors. Thus, it can often be neglected, particularly in high-power applications.

$$\begin{cases} V_t = V_c - R_s \cdot i \\ V_c = V_c^0 - \frac{1}{C}\int_0^t i_c dt \\ i_L = \frac{V_c}{R_p} \\ i_c = i + i_L \end{cases} \tag{3.8}$$

Many system applications require that capacitors be connected together, in series and/or parallel combinations, to form a "bank" with a specific voltage and capacitance rating. Because sustained overvoltage can cause an ultracapacitor to fail, the voltage across each cell in series stack must not exceed the maximum continuous working voltage rating of individual cells in the stack.

Matlab/Simulink model of the Ultra-Capacitor

The model for the ultracapacitor in simulink toolbox is shown in Fig. 3.7.

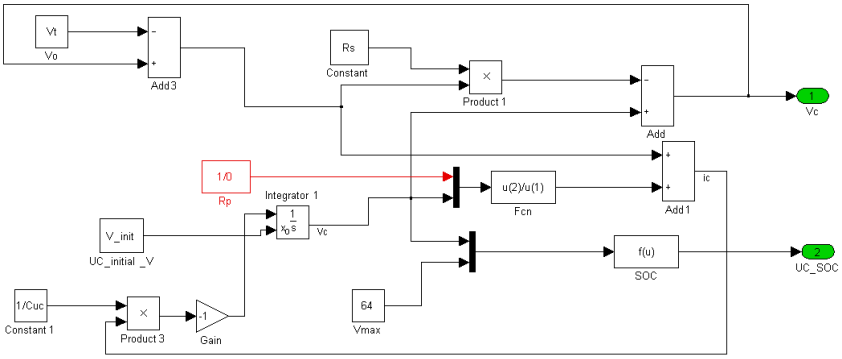


Figure 3.7: *UC equivalent circuit in Simulink*

Simulation results

Figures 3.8 and 3.9 show the capacitor charging and discharging modes.

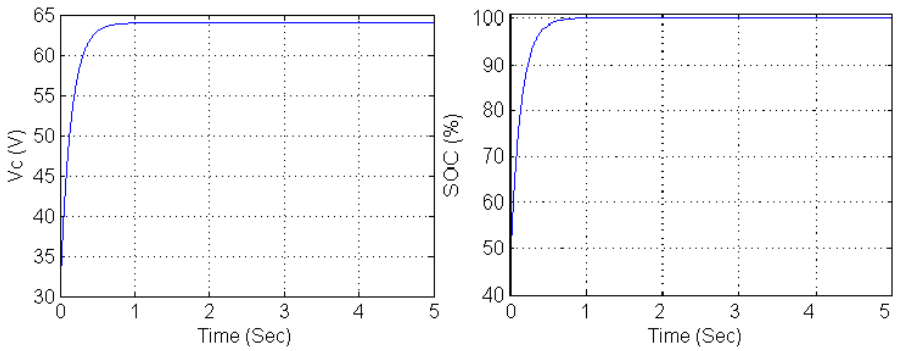


Figure 3.8: *UC charge characteristics*

The previous pictures show the UC charge period which has been charged to the nominal voltage. The capacitors have an initial voltage of 30 V. For this voltage the capacitors are charge to 40 % of their total energy capacitance. The voltage charge rapidly to 64 V as well as the SOC.
In the next Fig.3.9 are presented the voltage and the SOC of an ultracapacitor during the discharge period.
The discharge simulations are also obtained. As the previous Fig.3.9 the voltage goes from

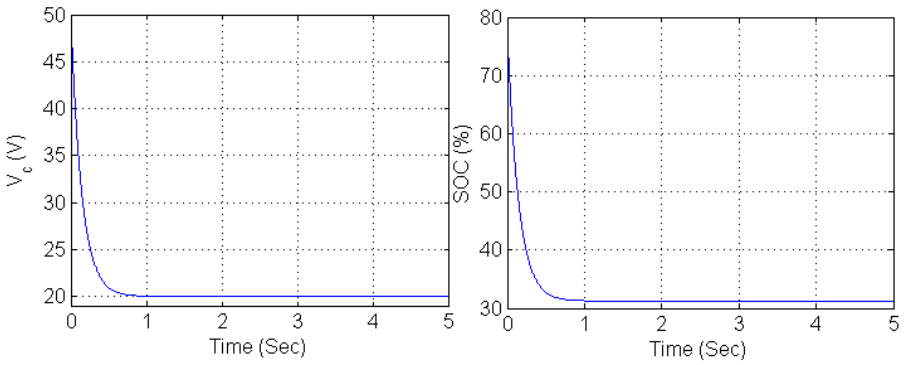


Figure 3.9: *UC discharge characteristics.*

45 V to 20 V . The SOC also follos the same shape as the voltage.

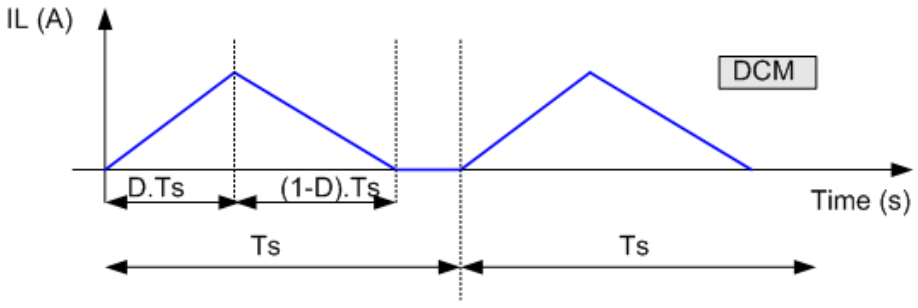
***

In the presented Chapter, two different energy sources were presented, batteries and ultracapacitor. After the model analysis of each one, Matlab/Simulink models were implemented. Each model was tested and the simulation results show that can be used as inputs for the converter model, wich is presented in the next Chapter 4. It is important to mention that even if the models are working properly, changes in the parameters have to be done to adapt the dynamic behaviour to the length of the Matlab/Simulink simulations (3.5 sec)

4
Model of the converter

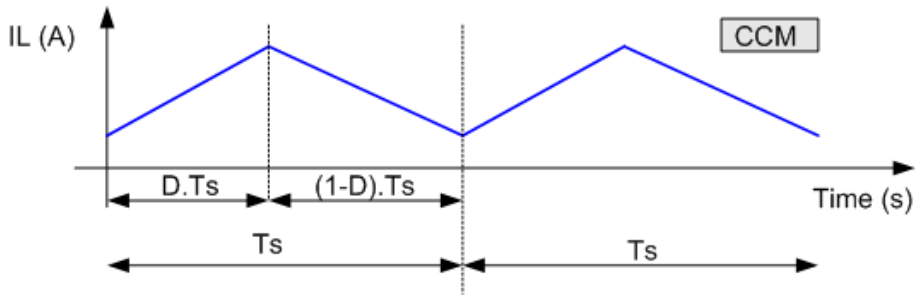
In this chapter the model of the converter is described. First, the buck converter is presented. The mathematical development is made. Afterwards, the implementation in Matlab/Simulink is done and finally, the results are shown. The same is made for the boost converter. The chapter is concluded with the combination of the buck and boost converter. The new two power direction converter is presented without any control, wich is presented in Chapter 5 of the report.

As mentioned before, the objetive of this report is to study a multiple input and bidireccional dc/dc converter. In the following are explained the different operations modes of the converter. This operations modes are first described separately, and then combined, to obtain the final converter.
Usually, a power converter has two main parts, the control stage and the power stage. The control stage is where the small signals for controlling the switches are. The power stage manages the big output voltages and currents. A power stage can operate in continuous or discontinuous inductor current mode. Continuous inductor current mode (CCM) is characterized by current flowing continuously in the inductor during the entire switching cycle in steady state operation. Discontinuous inductor current mode is characterized by the inductor current being zero for a portion of the switching cycle. A graphical representation of both conduction modes is presented in Fig.4.1.[3]



(a)

It is very desirable for a power stage to stay in only one mode, because behaviour changes significantly between the two modes of operation. Due to the complexity of making a control



(b)

Figure 4.1: *Different working modes of the DC/DC converters. (a)Discontinuous Conduction Mode, DCM. (b) Continuous conduction mode, CCM*

for continuous and discontinuos mode, this report is focused only in the continuous mode, the most common.
The following sections describe the model analysis of the boost and buck converter power stages and its implementation in Matlab/Simulink working in CCM.

4.1 Model Analysis of the DC/DC Boost Converter

The energy storage devices usually give an output voltage value lower than the required dc bus of the inverter. Therefore, the voltage level has to be increased when giving energy to the motor. The converter has to work in the boost mode. In the following is described the steady state operation of the boost power stage in continous conduction mode. Fig. 4.2 shows a simplified schematic of the boost converter. In this figure the power flow is from left to right. The main components of the converter are the inductor, L, the ouput capacitor, C and the swicth, Q1.

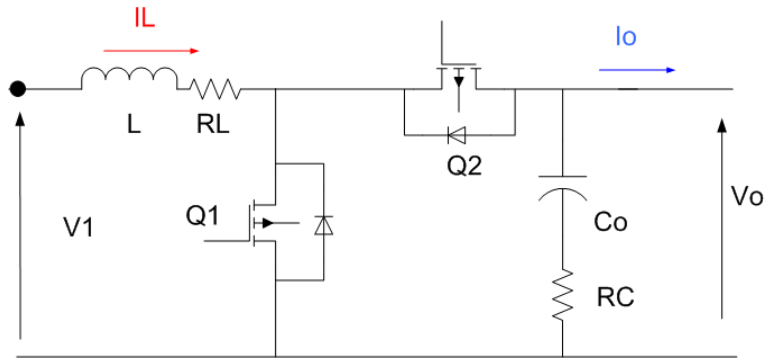


Figure 4.2: *Multiple input boost converter power stage*

Where,

V_1 is the *input dc source*,
Q_1 is the *switch*,
D_1 is a *diode*,
R_L is the *parasitic resistance of the inductance*,
L is the *inductance*,
R_C is the *parasitic resistance of the capacitor*,
C_O is the *capacitor*,
V_O is the *output voltage of the converter* and
R_O is the *resistive load*.

The capacitor ESR, RC, and the inductor DC resistance, RL, are included in the model. The resistor, R_O, represents the load seen by the power stage output.
The boost power stage assumes two states per switching cycle. Each stage corresponds to one position of the switch Q1.

In the next Fig.4.3 are presented the main signals of a boost converter. The PWM signal corresponds to the control stage and the current and voltage in the inductance to the power stage.

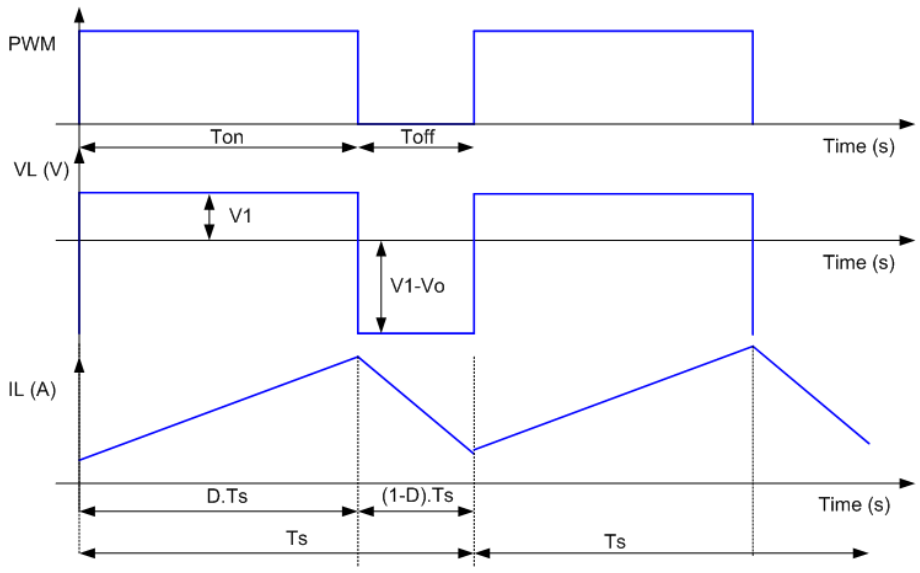


Figure 4.3: *Main singal in the boost converter*

The period of the signal is T_s. By means of a ratio D (duty time), this period is divided in two parts, T_{on} and T_{off}. T_{on} is obtained by multiplying $D \cdot T_s$ and T_{off} is the rest of the period or $(1 - D) \cdot T_s$ During T_{on}, the coil is supporting the input voltage, so the current increases. At the same time, the capacitor is giving energy to the load. During T_{off}, the coil is supporting $V_1 - V_O$. In this period, the capacitor is being charged and also power is delibered to the output load.

Mathematical model of the boost converter

It can be very easily found in the literature ([3],[4]) a complete mathematical anaylisis of the boost converter, therefore, in this section are only presented the most relevant formulas.

Current through the inductor:

$$i_L = \frac{1}{L} \cdot \int_{t_1}^{t_2} v_L \cdot dt \tag{4.1}$$

where v_L equals to v_1 during T_{on} and v_L equals to $v_1 - v_o$ during T_off.

Voltage in the capacitor:

$$v_c = \frac{1}{C} \cdot \int_{t_1}^{t_2} i_c \cdot dt \tag{4.2}$$

where i_c can be obtained from the relation between i_L and i_o.

$$i_o = i_L + i_c \tag{4.3}$$

The voltage conversion relationship in CCM:

$$v_o = v_1 \cdot \frac{1}{1-D} \cdot \frac{1}{1 + \frac{R_L}{R_O \cdot (1-D)^2}} \tag{4.4}$$

wich can be simplified to:

$$v_o = v_1 \cdot \frac{1}{(1-D)} \tag{4.5}$$

The relation between the average inductor current and the output current in CCM:

$$i_{Lavg} = \frac{i_o}{(1-D)} \tag{4.6}$$

and between output current and input current:

$$i_O = i_1 \cdot (1-D) \tag{4.7}$$

4.2 Matlab/Simulink model of the DC/DC Boost Converter

Once the analysis of the boost converter is done, it can be implemented in the Matlab/Simulink. This section presents the different blocks and the signals of the converter.
The boost converter can be implemented in one main block, wich is shown in Fig.4.4.

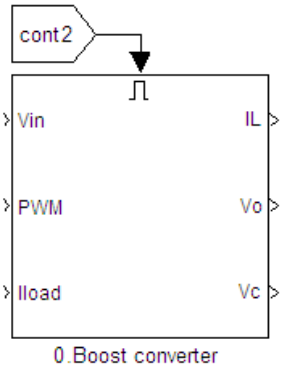


Figure 4.4: *Boost-type dc/dc switching converter Matlab/Simulink model. Main block*

The inputs to the system are input voltage, V_{in}, the modulated signal from the control stage, PWM, and the feedback of the current, I_{load}. The outputs of the block are output voltage, V_O, the voltage in the filter capacitor, V_c, and the inductor current, I_L. There is also a control signal (cont2) wich enables or disables the complete block.
Inside the block are build the two main equations of the converter. The current flowing throught the inductance and also the capacitor voltage. Furthermore, an ideal switch is build. In Fig.4.5 it can be seen how the equations are implemented in the model. [5]

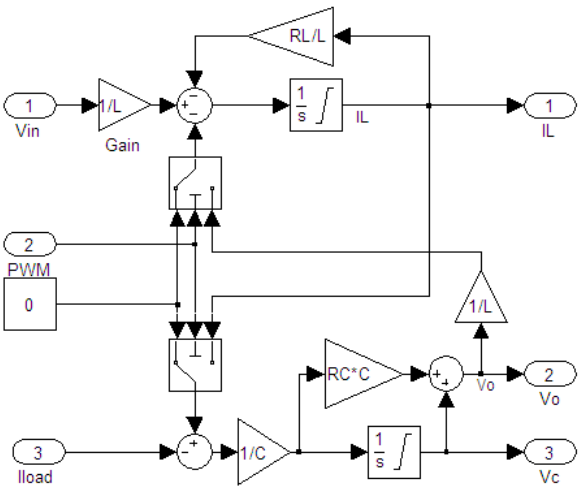


Figure 4.5: *Boost-type dc/dc switching converter Matlab/Simulink model. Inside block*

The input voltage V_{in} is always applied to one side of the inductor, but, in the other side, the voltage is depending on the position of the switch. When the switch is on, the voltage is 0, and when the switch is off, the voltage in the other terminal of the inductor is V_O. Therefore, the current is changing. The upper integrator represents the inductor current, Eq.4.2 and the lower integrator of the figure corresponds to the capacitors voltage, Eq.4.4. Limits in the integrator are used to avoid the negative current flow throught the inductor. At the same time that the switch connects the output voltage to the terminal of the inductor, it also connects the inductor current to the input of the capacitor. The switch can be compared to two different switches, one for the current and another for the voltage. The parasitic resistance of the inductance and the output capacitor are included in the model. They are modeled using the gains wich appear in parallel with the integrators.

4.3 Model Analysis of the DC/DC Buck Converter

When the motor is working as a generator and the system is producing energy, the converter has to reduce the voltage from the dc bus to charge the batteries or the ultracapacitors. Therefore, the choosen topology has to work in buck mode. In order to be able to build the model of the BUCK converter it is necessary to analyze the circuit topology. A general overview of the device is presented in Fig.4.6. In this figure, the power flow is from left to right.

The inductor, L, and capacitor, C, make up the output filter. The capacitor ESR, R_C (equivalent series resistance) and inductor DC resistance, R_L, are included in the analysis. The resistance, R_O, represents the load. [2]

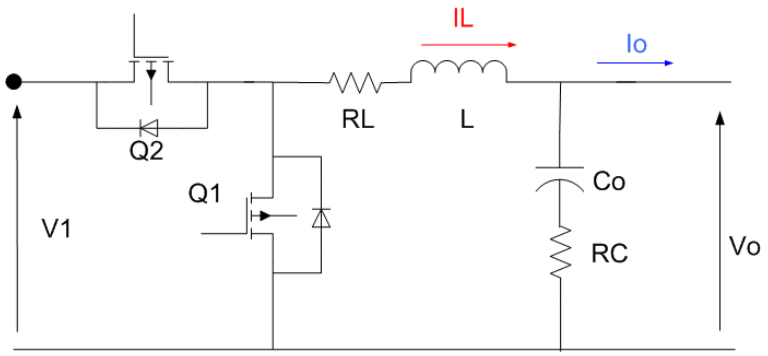


Figure 4.6: *Buck-type dc/dc switching converter*

Where,

V_1 is the *input dc source*,
Q_1 is the *switch*,
D_1 is a *diode*,
R_L is the *parasitic resistance of the inductance*,
L is the *inductance*,
R_C is the *parasitic resistance of the capacitor*,
C_O is the *capacitor*,
V_O is the *output voltage of the converter* and
R_O is the *resistive load*.

In CCM the power stage can be described with two different circuits depending on the position of the switch Q1. In Fig.4.7 are presentd the waveforms for the continous-conduction operation mode.

As it is explained in the previous subsection of the boost converter, the period T_s is divided in T_{on} and T_{off}. When the switch is on, it conducts the inductor current and the diode is reverse polarized. This results in a positive voltage across the inductance, V_L=V_1-V_O. This voltage causes an increase in the inductor current. When the switch is turned off, because of the inductive energy storage, I_L continues to flow. This current now flows through the

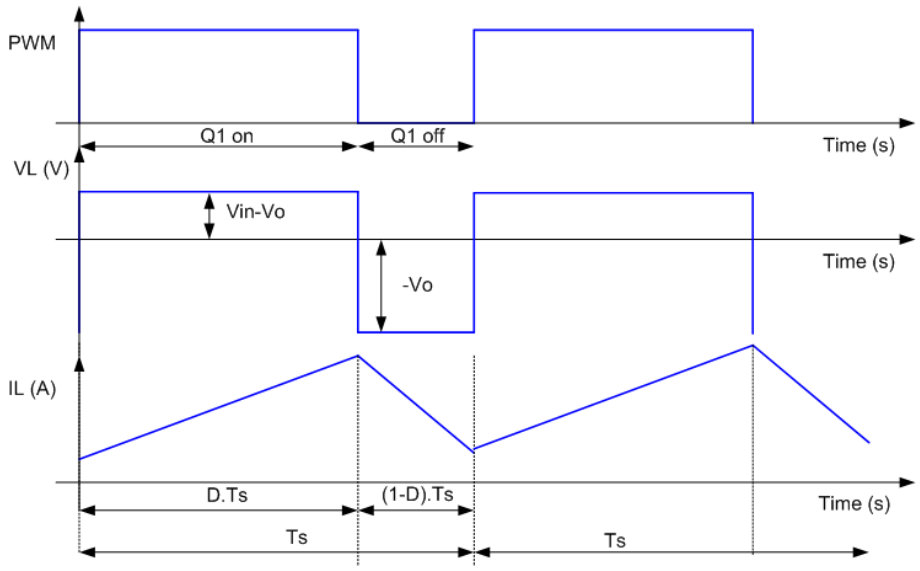


Figure 4.7: *Main signals of the buck converter*

diode, and V_L=-V_O.[4]

Mathematical model of the buck converter

As mentioned in the previous sections, only a brief description of the mathematical formulas is presented because very deep studies can be easily found in the literature.[4][2]

Current through the inductor:

$$i_L = \frac{1}{L} \cdot \int_{t_1}^{t_2} v_L \cdot dt \tag{4.8}$$

where v_L equals to $v_1 - v_O$ during T_{on} and v_L equals to $-v_O$ during T_off.

Voltage in the capacitor:

$$v_c = \frac{1}{C} \cdot \int_{t_1}^{t_2} i_c \cdot dt \tag{4.9}$$

where i_c can be obtained from the relation between i_L and i_O.

$$i_O = i_L + i_c \tag{4.10}$$

The voltage conversion relationship in CCM:

$$v_o = v_1 \cdot D \tag{4.11}$$

The relation between the average inductor current and the output current in CCM:

$$i_{Lavg} = i_o \tag{4.12}$$

and between output current and input current:

$$i_o = \frac{i_1}{D} \tag{4.13}$$

4.4 Matlab/Simulink model of the DC/DC Buck Converter

Once the analysis of the buck converter is done, it can be implemented in the Matlab/Simulink. This section presents the different blocks and the signals of the converter.
As it is done with the boost converter, the buck converter is implemented in one main block, wich is shown in Fig. 4.8.

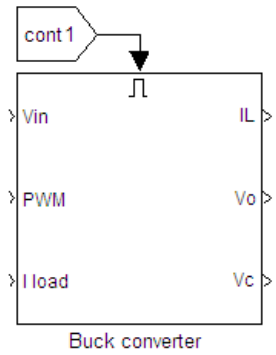


Figure 4.8: *Buck-type dc/dc switching converter Matlab/Simulink model. Main block*

The inputs to the system are input voltage, V_{in}, the modulated signal from the control stage, PWM, and the feedback of the current, I_{load}. The outputs of the block are output voltage, V_{out}, the voltage in the filter capacitor, V_c, and the inductor current, I_L. There is also a control signal (cont1) wich enables or disables the complete block.
Inside the block are build the two main equations of the converter. The current flowing throught the inductance and also the capacitor voltage. In Fig. 4.9 it can be seen how the equations are implemented in the model. [5]

The main purpose of the switch Q1 is to create a square voltage wave wich is applied to the inductor. The upper integrator represents current in the inductance and the lower integrator of the figure corresponds to the capacitors voltage. The voltage at the output V_o is the voltage after Q1 but filtered. The parasitic resistance of the inductance and the

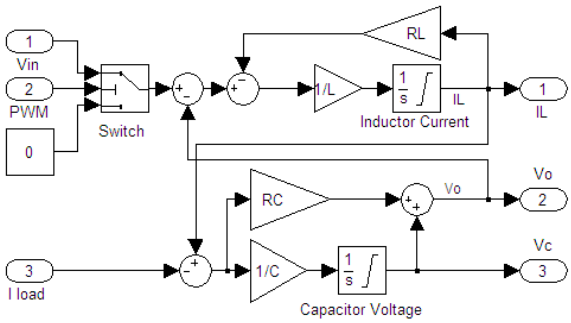


Figure 4.9: *Buck-type dc/dc switching converter Matlab/Simulink model. Inside block*

output capacitor are included in the model. They are modeled using the gains wich appear in parallel with the integrators.

Proposed bidirectional DC/DC converter

As it is mentioned in Chapter 1, due to the requirements of the system, the proposed converter has to be able to work in two different modes, buck and boost, but also, the power flow direction has to be the opposite for each working mode. In the following is presented how to combine the two previous models to obtain the desired converter. The main purpose is to build the converter with the fewer amount of components.
In the next Fig. 4.10 it is presented the proposed topology of the converter. When the power is flowing from left to right, the converter has to work in boost mode. In the opposite direction, from right to left, the converter has to work in buck mode. As Fig. 4.10 shows,

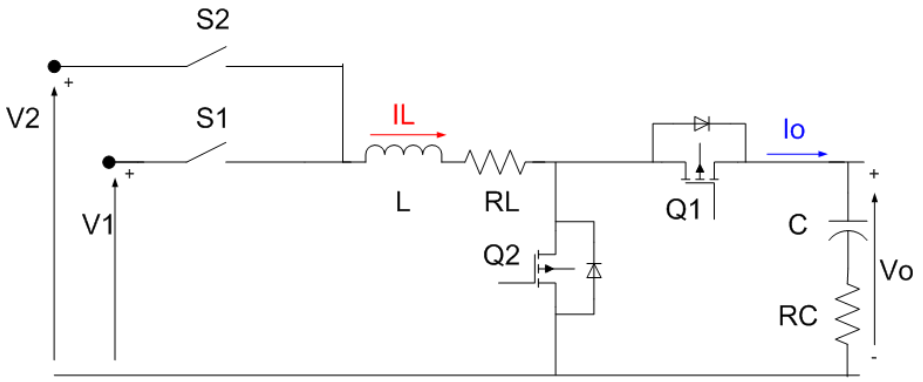


Figure 4.10: *Proposed bidireccional multiple input dc/dc converter*

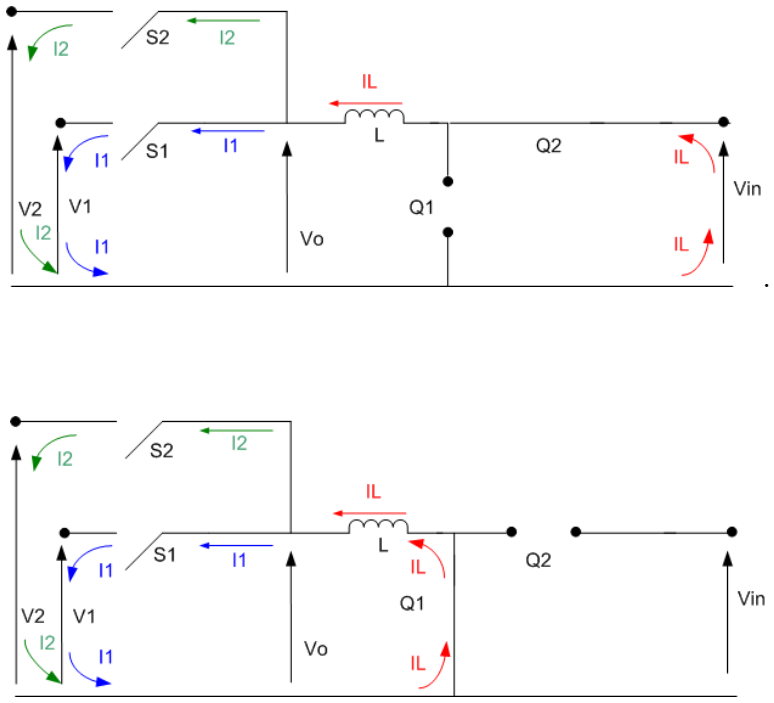
the multiple input bidireccional converter can be made with only four main switches (S1, S2, Q1 and Q2), one inductance (L) and three capacitors (C1, C2 and C3). In this section, only a very basic scheme of the switches S1 and S2 is presented. In Chapter 5 a deeper study of both switches is made.

In the next subsections it is explained the switching sequence for the boost operation mode and for the buck mode. In order to make simpler the graphics, the parasitic resistances (R_L and R_C), the same as the capacitors C1 and C2 are neglected. Furthermore, in order to make clear how does the converter works, currents and voltages are represented for each state.

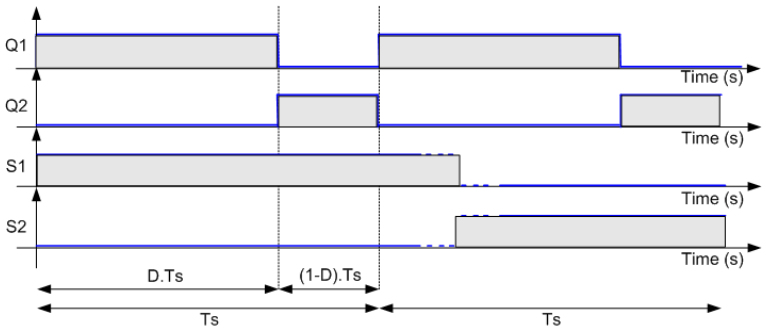
Buck mode

The first explained mode is the buck mode. This is when power, in Fig.4.10, is flowing from the right to the left.

As it is mentioned before, the power stage of the buck converter has two possible states in each period. The first of the states is presented in Fig. 4.11(a). In this case the switch Q2 is closed and Q1 is open. Depending on wich output is choosen, the current can go through S1 or S2. The control signals for the switches can be seen in Fig.4.11(b). The part of the period $D \cdot Ts$ correspond to Fig.4.11(a). In this state, all the currents of the circuit are the same (I_L=I_1 or I_L=I_2). The voltage in the terminals of the inductance is V_{in}-V_O. This is a positive voltage, therefore, the current is increasing. In the second state, Fig. 4.11(a) both, S1 and S2 switches are in the same position but Q2 is open and Q1 is closed. This state is presented in Fig. 4.11(b) during the period $(1-D) \cdot Ts$. Now, the input voltage is insolated from the output voltage. The voltage in the terminals of the inductance is -V_O. This is a negative voltage, so during this state, the current decreases. The output current is the same as the inductance current, but the input current of the converter is cero.
It is important to mention that in this mode the switches S1 and S2 can not be closed at the same time, or during the same PWM period. The working mode is to give an output voltage to charge a battery or an ultracapacitor, therefore, the output voltage can only be suitable for one, not for both.



(a)



(b)

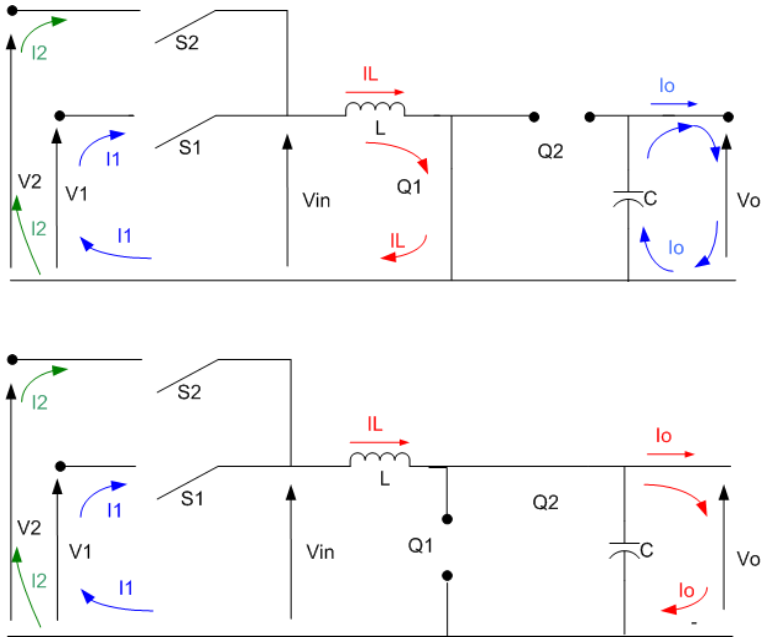
Figure 4.11: *Switching squence in buck mode*

Boost mode

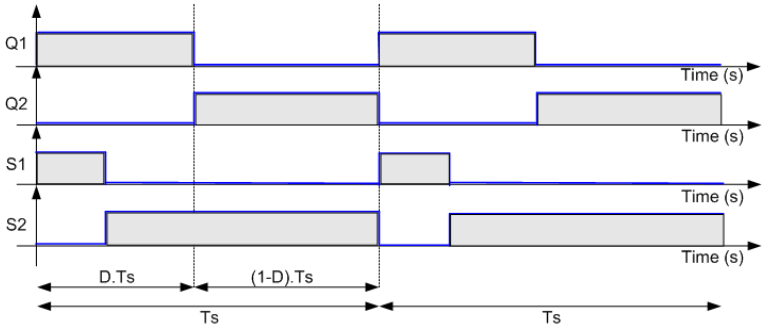
The other working mode of the converter is the boost mode. Based on Fig.4.10, the boost mode occurs when the power is flowing from left to right. The input voltage from $V1$ and $V2$ is stepped up to be V_O. As mentioned for the buck mode, the power stage of a single input boost converter has two states. When using the multiple input topology, more different states can be obtained. The number of different states depends on the number of multiple inputs. In this case, only two inputs are considered, therefore, four different states can be observed during the steady state operation mode. However, because of the control technique, only three states are used in this mode.

The first of the states is presented in Fig. 4.12(a) where the switch Q1 is closed and Q2 is open. Taking a look to Fig. 4.12(b), it can be seen that this period last for $D{\cdot}Ts$. In this state, the voltage V_L across the inductance is V_{in}, but, depending on the switches S1 and S2, V_{in} can be two different values. Therefore, the period $D{\cdot}Ts$ can be split in two subperiods, where the voltages V1 and V2 are supplied to the inductance in order to generate the current. The switching between S1 and S2 is presented in Fig. 4.12(b) during the period $D{\cdot}Ts$. During this period, the output current to the load comes from the filter capacitor.

The last of the states is when $Q1$ is open and $Q2$ is closed. In Fig.4.12(a) are presented the currents in the converter and in Fig.4.12(b) the switching state. During this period, $(1-D){\cdot}Ts$, only one input voltage is used. This is why the presented converter only has three states instead of four. This simplification makes easier the control. The voltage V_L applied to the inductance is $Vin - Vo$, this voltage is opposite to the one applied during the period $D{\cdot}Ts$, therefore, the current decreses. As Fig.4.12(b)shows that the current through the inductance, the input current and output current are the same.



(a)



(b)

Figure 4.12: *Switching squence in boost mode*

It is important to mention that the output voltage depends on the duty cycles S1 and S2. The relation between input voltage and output voltage is deduced in the following:

$$\int_o^{Ts} v_L dt = v_1 \cdot S1_{on} \cdot Ts + v_2 \cdot (D - S1_{on}) \cdot Ts + (v_2 - vo) \cdot (1 - D) \cdot Ts = 0 \tag{4.14}$$

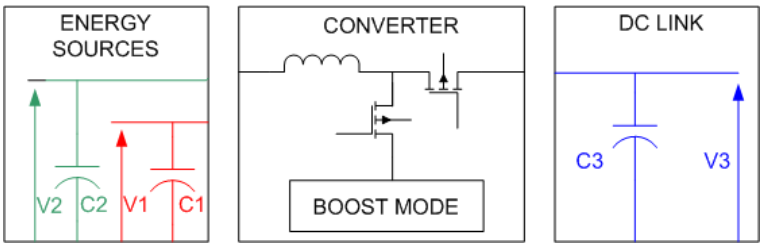
$$v_1 \cdot S1_{on} + V2 \cdot (1 - S1_{on}) - v_o \cdot (1 - D) = 0 \tag{4.15}$$

$$\frac{v_1 \cdot S1_{on} + v_2 \cdot (1 - S1_{on})}{1 - D} = v_o \tag{4.16}$$

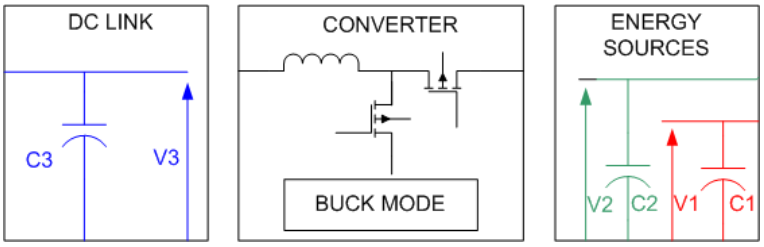
Matlab/Simulink model of the proposed DC/DC converter

The multiple input bidirectional converter is implemented in Matlab/Simulink. As it is mentioned before, in order to simulate the current in the inductor and the voltage in the capacitor, two integrators are used. The voltage in the capacitors is always positive. The current throught the inductance, can be positive or negative, depending on the working mode of the converter. The problem comes when implementing the bidirectional sources and loads.

In Fig. 4.13(a) the converter is working in boost mode. The input energy to the system



(a)



(b)

Figure 4.13: *Explanation of the simulink model*

comes from two energy sources, and the output energy goes to the dc link. The energy sources can be a very simple model, as for example constant voltage, or the whole model of a battery or a ultracapacitor, but non of the models can work in bidirectional mode. The main idea is to use a control signal to enable and disable the different blocks, and also, use this signal to change the connections of the different voltages and currents. A very basic example of how does the system work is presented in Fig. 4.13(a) and (b), where the converter is working in boost and buck mode.

To run the bidirectional converter, it is necessary to change the input capacitor, output capacitor, load, and input voltage for every working mode. When the capacitors are exchanged, it is possible to initialize the input capacitor voltage with the previous output capacitor voltage. For example, if the converter is working in boost mode, as is presented in Fig. 4.13(a), the output capacitor is C3 (blue color), and together with a resistance are actuating as a load. If the working mode is changed to buck mode,Fig. 4.13(b), this capacitor and now,

instead of a resistance, and energy source (blue color), become the input to the system. As in real life, the voltage in the capacitor can not change in a fast way, therefore, everytime it is made a change in the working mode, the previous output and input voltage, have to be stored in order to initialize the new input and output voltages.
It is not necessary to do the same with the current through the inductance because when the working mode is changed, the current through the coil is cero.

In the Fig.4.14 (next page) the model in Matlab/Simulink of the bidirectional multiple-input converter is presented. The inputs to the system (light blue) are the inductance, resistances and capacitors values (5, 6, 7, 8, 10 and 11), the control signals, PWM1, PWM2, CONTROL (3, 4 and 9), the input voltage (2), the feedback of the output current (1) and finally, the initial conditions for the capacitors (12 and 13). The outputs of the model (green) are the inductor current (1), the output voltage (2) and the voltage in the capacitor (3).
In the model it can be seen two different switches, Q1 and Q2, this is why two different PWM signals are needed. It is also very clear to see the equation of the current through the inductance, wich is reminded here,

$$i_L = \frac{1}{L} \cdot \int_{t_1}^{t_2} v_L \cdot dt \tag{4.17}$$

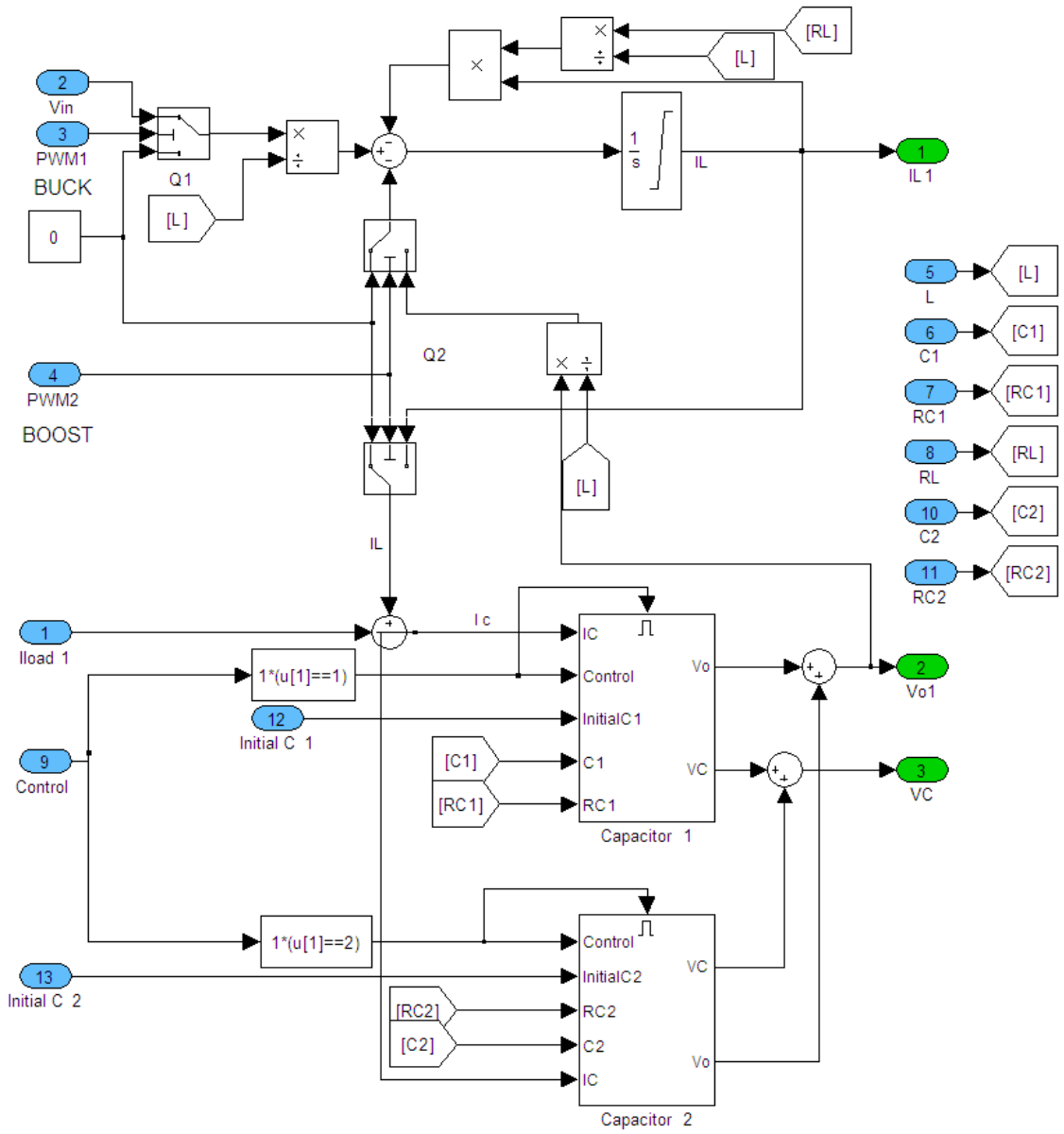


Figure 4.14: *Main block of the multiple input bidireccional dc/dc converter*

There are also two sublocks, wich contain the equations of two different output capacitors. With the control signal it is possible to choose between the capacitors and furthermore, initialize their voltage to the desired value. The next Fig.4.15 shows how the capacitors are implemented. In this case the integrators are able to be reset and initialized. The equation of the capacitor voltage is also reminded,

$$v_c = \frac{1}{C} \cdot \int_{t_1}^{t_2} i_c \cdot dt \tag{4.18}$$

Not only the output capacitor has to be changed, also the output resistance needs to be

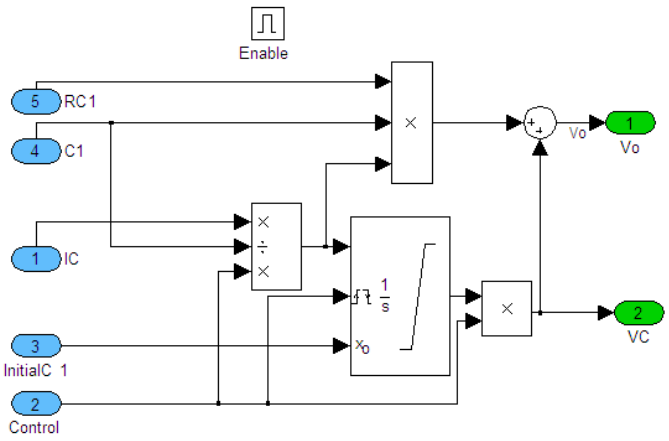


Figure 4.15: *Block of the capacitor*

changed.

Moreover, the input voltage to the converter is not the same when is working in boost mode and in buck mode. In the Fig. 4.16 it is presented the Matlab/Simulink block wich changes the input voltage to the system depending on the control signal. The input voltage for the buck mode comes from de dclink, and the input voltage for the boost mode, comes from the batteries and ultracacitors model.

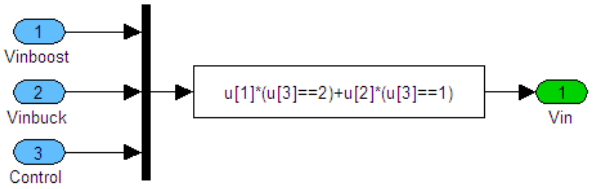


Figure 4.16: *Input voltage depending on the control signal*

Therefore, in the Fig. 4.17 the model wich makes the multiple input is presented. When the system is working in boost mode, dependig on the PWM signals S1 and S2, the input voltage for the converter in boost mode is the voltage of the batteries or the ultracapacitors. Once the main blocks of the converter are explained, simulation results are presented in the

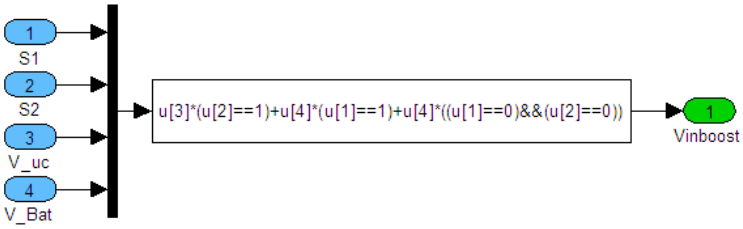


Figure 4.17: *Main block of the multiple input bidireccional dc/dc converter*

next section. It is important to mention that this simulation results are done without any control and they are just to check that the model of the converter is working in both of the modes.

4.5 Simulation Results

This section contains the simulation results of the proposed converter. First, the converter is tested in the boost mode and afterwards, in the buck mode. The most important parameters used for running the simulations are presented in Table 4.1 and the initialization file is included in the AppendixA. This parameters are calculated in the AppendixB. In order to do these calculations, are used the system specifications described in Chapter3. It is important to mention that this parameters do not correspond to a real system, they are scaled down to build a prototype of lower power.

Parameter	**Symbol**	**Value**
Switching frequency	fs	15000 Hz
Battery voltage	$Vbat$	48 V
Ultra capacitor voltage	Vuc	64 V
Dc bus voltage	$Vbus$	136 V
Inductance	L	$218\mu H$
Battery capacitor	$Cbatt$	$149\mu F$
Ultra capacitor capacitor	Cuc	$4.7\mu F$
Load resistance	Ro	9.25Ω

Table 4.1: *Parameters for simulation*

The simulations are done with the converter in open loop. No control is included and the duty cycles, S1, S2, PWMbuck and PWMboost are fixed, S1=0.25, S2=0.25, PWMboost=0.5 and PWMbuck=0.5 . The commutation squence is the same as presented in Fig.4.12(b). In the next Fig.4.18 is presented the output voltage of the converter. The average voltage is 92 V and it has a ripple of 5.5 V. The voltage drops are caused because of the parasitic resistances of the inductance and the capacitor. Considering that the input voltages are V1=64 V and V2=48 V, the obtained output, according to Eq.4.16 shows that the model of the converter works with accuracy in the boost mode.

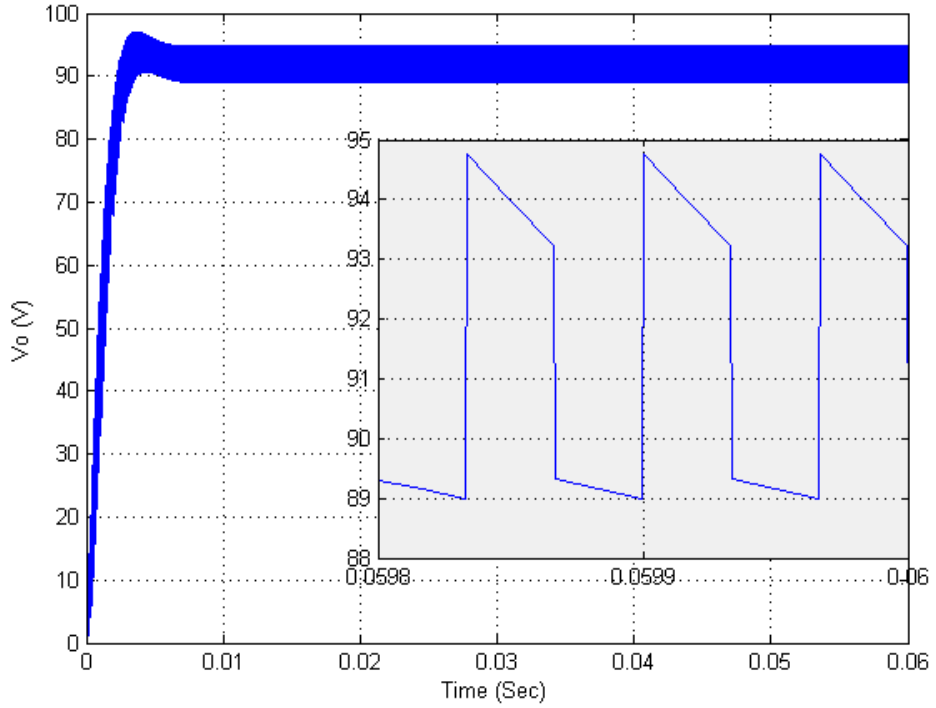


Figure 4.18: *Output voltage of the multiple input boost converter in openloop*

The Fig.4.19 shows the current through the inductor. It can be seen the two different slopes when the current is increasing. This is because of the multiple input applied voltage. The average current is 20 A and it has got a ripple of 8 A.
At the beginning of the simulation, in the voltage graph and in the inductor current graph,

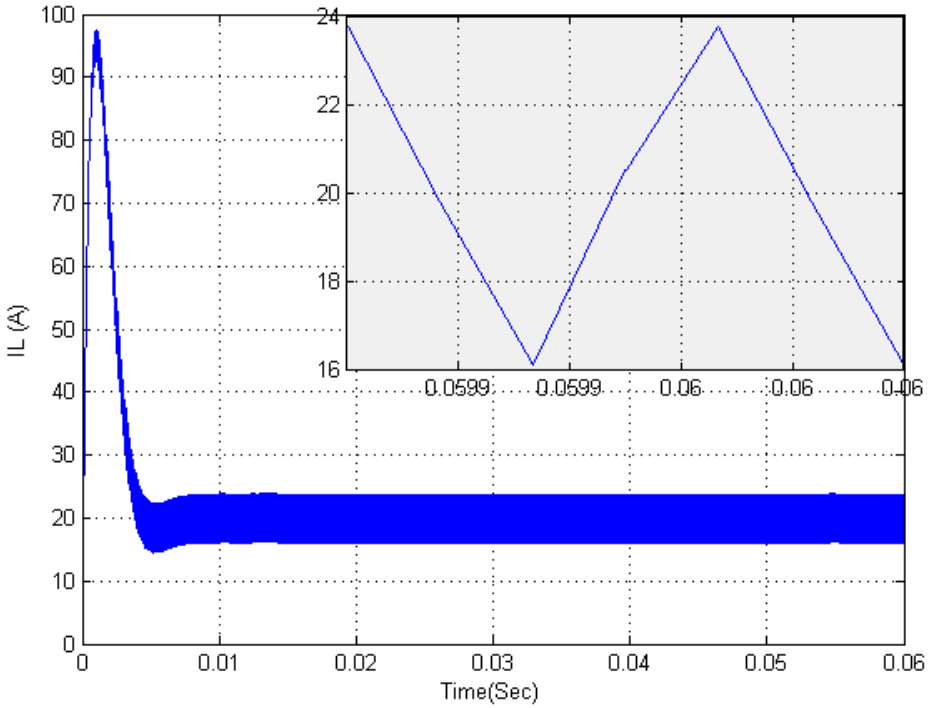


Figure 4.19: *Inductor current of the multiple input boost converter in openloop*

it can be seen a peak. This peak is due to there is no control implemented, and the output capacitors are dischargued. Therefore, when the simulation stars, there is a big voltage drop between Vin and Vo, causing the fast increase of current, and therefore, the increase of voltage.
The load used for running the simulation is a pure resistive load, therefore, the shape of the output current is the same as the output voltage but divided by 9.25 (resistive load).

The converter is also run in the buck mode. The input voltage is 136 V and the used load is a resistance of 9.25 Ω. In Fig. 4.20 is presented the output voltage. It takes around 0.02 seconds to reach the steady state. The average output voltage value is approximately 68 V and it has a ripple of 0.6 V. Basing in Eq.4.11, the output voltage confirms that the model of the converter is working properly. As it is mention for the boost mode, the ouput current is not presented because it has the same shape as the voltage, but divided by 9.25 (resistive load).

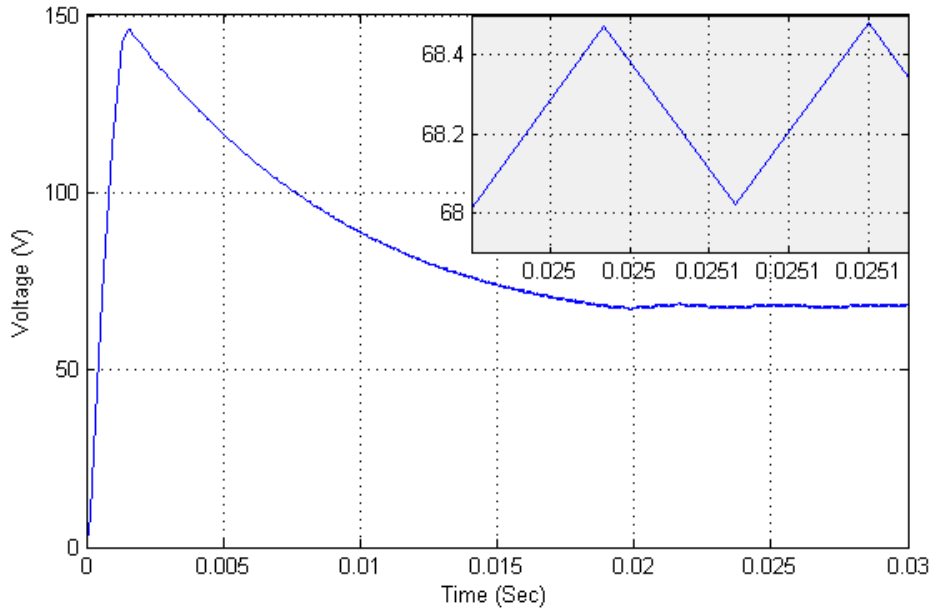


Figure 4.20: *Output voltage of the multiple input converter working in buck mode in open loop*

The following Fig. 4.21 presents the current through the inductor. It reachs the steady state at the time 0.02 sec as the voltage does. The average inductor current is around 7 A with a ripple of 10 A.

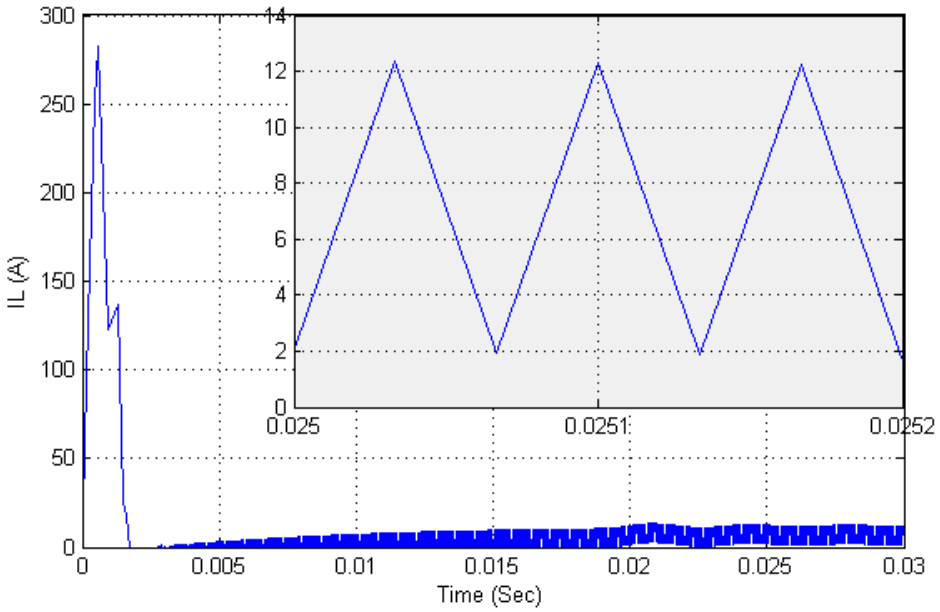


Figure 4.21: *Inductor current of the multiple input converter working in buck mode in open loop*

Also in the buck mode, it appear a peak of current at the beginning of the simulation. The reason is the same as in the boost mode. When de simulation start, the output capacitor is discharged causing a voltage drop through the inductor.

***

In this chapter the model of the multiple-input bidirectional converter is presented. Simulations in openloop are done and it is verified that the model can be used as a base for tunning the controls of both working modes. The control analysis is done in the next Chapter 5.

5 Control of the converter

The main task of this chapter is to analyze and implement closed loop control of the converter. Regulation of the duty cycle value ensures the stable operation of the converter, and keeps the output voltage to the desired voltage. This control is made up of an inner current closed loop, which regulates the inductor current, and an outer close loop necessary for regulating the output voltage. The values for the control are calculated with the sisotool application (Matlab) and tested in the Matlab/Simulink models presented in the previous Chapter.

The calculation of the control values are divided in two sections. First the values for the buck mode are analyzed. Then, the analysis is focused on the boost mode control parameters. For the control parameters design it has not been considered the multi input topology. The calculation has been made for different input voltages to ensure the good response at any voltage level. Finally the control for the multiple input topology is described. This chapter describes the control topology for the energy management for the batteries and UCs sources.

5.1 Buck and boost control system

The converter control diagram is presented in Fig. 5.1.

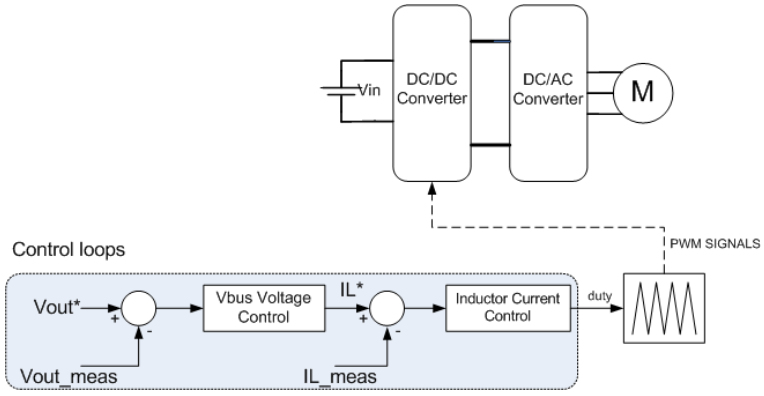


Figure 5.1: *Main control diagram.*

The DC/DC converter is connected to the inverter and must maintain the input voltage for the inverter to the desired voltage. The control implements a fast inner current loop and a slower outer loop for setting the DC voltage. Standard PI controllers are implemented

for all the control block, resulting the overall control structure described in Fig.5.5. The system is controlling DC voltage by sending references to an outer voltage control loop that generates an inductor current reference, which generates a duty cycle value, for PWM signal generation.

This regulation topology is used for the boost mode such as for the buck mode.

Inner control loop design for buck mode

In this mode the output source V_o delivers power to the input source V_1. The inductor current is controlled by switching the switch Q_2. When the Q_2 is not conducting, the diode D_1 is active. The input is modeled as a resistive load R_1. The circuit can be therefore depicted as in Fig. 5.2. To simplify the equations, the output capacitor resistor and the inductance resistor has been neglected.

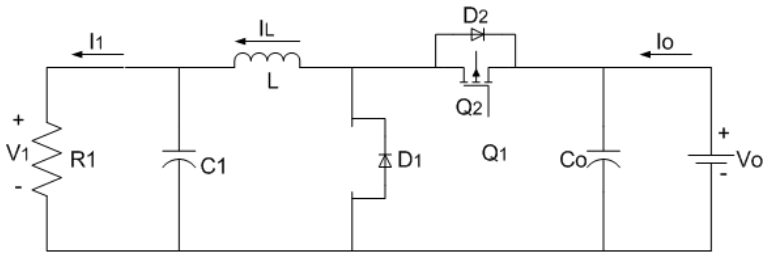


Figure 5.2: *Multi input power converter in buck mode.*

In order to design the controller it is needed the transfer function of the converter. However, to obtain this transfer function, some assumpitons are made:

- the switches are ideal.
- the time delays of the switching are not considered.
- the losses in inductor and the capacitor are negligible.

Duty cycle to inductor current transfer function with resistive load (G_1)

$$Interval\ D_{Q_2}T_s \begin{cases} L\frac{di_L}{dt} = v_o - v_1 \\ C_1\frac{dv_1}{dt} = i_L - \frac{v_1}{R_1} \\ C_o\frac{dv_o}{dt} = i_o - i_L \end{cases} ;\ Interval\ (1 - D_{Q_2})T_s \begin{cases} L\frac{di_L}{dt} = -v_1 \\ C_1\frac{dv_1}{dt} = i_L - \frac{v_1}{R_1} \\ C_o\frac{dv_o}{dt} = i_o \end{cases} \tag{5.1}$$

Average State-Equations

$$L\frac{di_L}{dt} = (v_o - v_1)d_{Q_2} - (v_1)(1 - d_{Q_2}) = v_o d_{Q_2} - v_1 \tag{5.2}$$

$$C_1\frac{dv_1}{dt} = (i_L - \frac{v_1}{R_1})d_{Q_2} + (i_L - \frac{v_1}{R_1})(1 - d_{Q_2}) = i_L - \frac{v_1}{R_1} \tag{5.3}$$

$$C_o\frac{dv_o}{dt} = (i_o - i_L)d_{Q_2} + i_o(1 - d_{Q_2}) = i_o - i_L d_{Q_2} \tag{5.4}$$

Perturbation

$$L\frac{d(I_L + \tilde{i}_L)}{dt} = (V_o + \tilde{v}_o)(D_{Q_2} + \tilde{d}_{Q_2}) - (V_1 + \tilde{v}_1) \tag{5.5}$$

$$C_1\frac{d(V_1 + \tilde{v}_1)}{dt} = (I_L + \tilde{i}_L) - \frac{(V_1 + \tilde{v}_1)}{R_1} \tag{5.6}$$

$$C_o\frac{d(V_o + \tilde{v}_o)}{dt} = (I_o + \tilde{i}_o) - (I_L + \tilde{i}_L)(D_{Q_2} + \tilde{d}_{Q_2}) \tag{5.7}$$

Perturbation

$$L\frac{d(I_L + \tilde{i}_L)}{dt} = (V_o + \tilde{v}_o)(D_{Q_2} + \tilde{d}_{Q_2}) - (V_1 + \tilde{v}_1) \tag{5.8}$$

$$C_1\frac{d(V_1 + \tilde{v}_1)}{dt} = (I_L + \tilde{i}_L) - \frac{(V_1 + \tilde{v}_1)}{R_1} \tag{5.9}$$

$$C_o\frac{d(V_o + \tilde{v}_o)}{dt} = (I_o + \tilde{i}_o) - (I_L + \tilde{i}_L)(D_{Q_2} + \tilde{d}_{Q_2}) \tag{5.10}$$

Small-Signal Model

$$L\frac{d\tilde{i}_L}{dt} = V_o\tilde{d}_{Q_2} + D_{Q_2}\tilde{v}_o - \tilde{v}_1 \tag{5.11}$$

$$C_1\frac{d\tilde{v}_1}{dt} = \tilde{i}_L - \frac{\tilde{v}_1}{R_1} \tag{5.12}$$

$$C_o\frac{d\tilde{v}_o}{dt} = \tilde{i}_o - I_L\tilde{d}_{Q_2} + \tilde{i}_L D_{Q_2} \tag{5.13}$$

Transfer functions

$$LsI_L(s) = V_o D_{Q_2}(s) + D_{Q_2}V_o(s) - V_1(s) \tag{5.14}$$

$$V_1(s) = \frac{R_1}{R_1C_1s + 1}I_L(s) \tag{5.15}$$

$$V_o(s) = \frac{1}{C_o s}I_o(s) - \frac{I_L}{C_o s}D_{Q_2}(s) - \frac{D_{Q_2}}{C_o s}I_L(s) \tag{5.16}$$

For $V_o(s) = 0$ the relationship between the inductor current and the duty ratio of switch Q_2 is given by

$$LsI_L(s) = V_o D_{Q_2}(s) - \frac{R_1}{R_1C_1s + 1}I_L(s) \tag{5.17}$$

$$I_L(s)\left(Ls + \frac{R_1}{R_1C_1s+1}\right) = V_oD_{Q_2}(s) \tag{5.18}$$

$$G_1 = \frac{I_L(s)}{D_{Q_2}(s)} = V_o\frac{R_1C_1s+1}{R_1C_1Ls^2 + Ls + R_1} \tag{5.19}$$

After obtaining the transfer function for the inner loop, the values for the current PI (C_2) are calculated. As it was mention before, this is made trough sisotool. The current control loop is represented in Fig. 5.3 where,

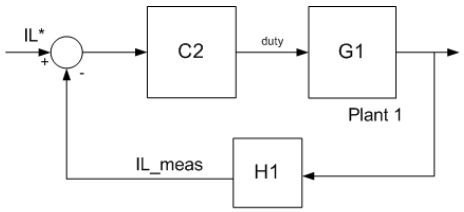


Figure 5.3: *Current control loop.*

$$C_2 = K_p(\frac{k_is+1}{s}) \tag{5.20}$$

For a better current measurement, the feedback current has been filtered to 6 kHz.

$$H_1 = \frac{6000}{s+6000} \tag{5.21}$$

Current control verification

The step response of the close loop transfer function for the inner loop in Fig.5.4 shows that the PI controller introduced in the closed loop transfer function provides certainty the value of the step input. For dimensioning the PI parameters Matlab sisotool different values for the regulator has been tested. The values for the control have been calculated to have as fast step and stable response as possible. As it is shown in figure a) the control is quite fast as current reaches the steady state value in approximately 0.07 seconds. However, to achieve a fast response, some initial disturbances are assumed. It can be observed that the simulink results are very close to the step response obtained with the sisotool. In both graphs, the steady state is obtain at the same time.

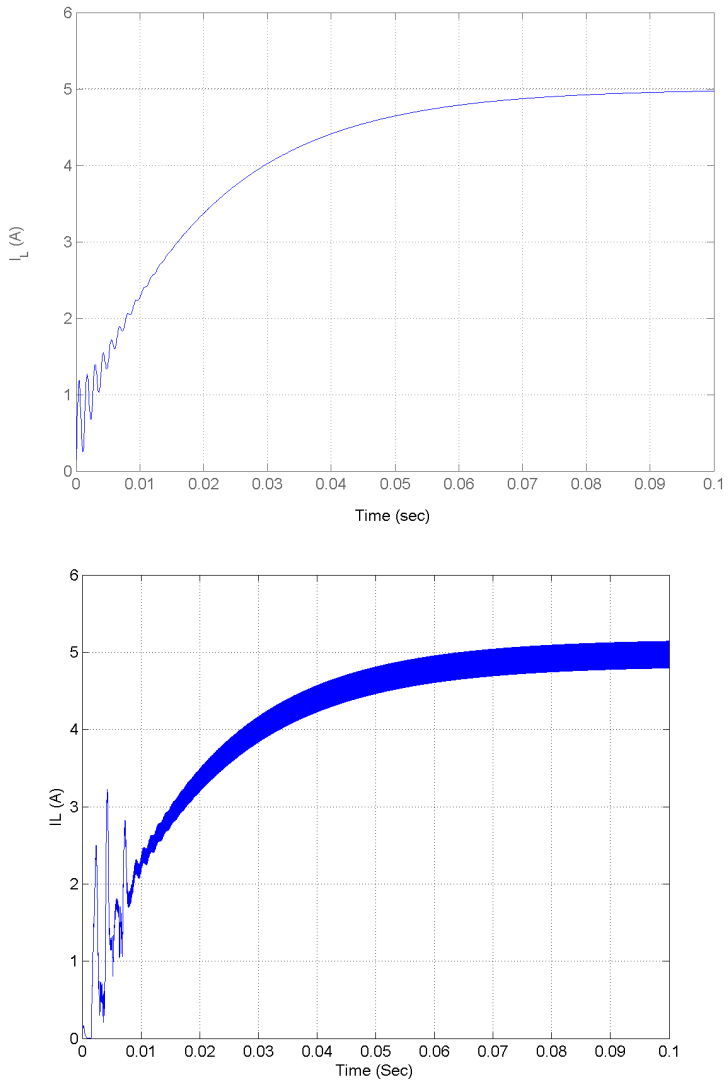


Figure 5.4: *a) Step response from the sisotool. b) Step response from the simulink model.*

Outer control loop design for buck mode

Inductor current to output voltage transfer function with resistive load (G_2)

The transfer function for the outer control loop is

$$G_2 = \frac{V_1}{I_L(s)} = \frac{R_1}{R_1 C_1 s + 1} \tag{5.22}$$

With the values for the inner control loop calculated, the voltage PI parameters can be find. The closed loop used in sisotool for parameterization of C_1 is shown in Fig.5.5.

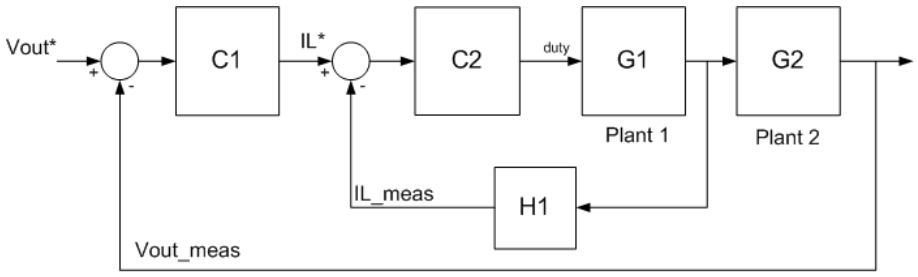


Figure 5.5: *Inner and outer control loops.*

Voltage control verification

The same as for the current control, the values has been obtained for the voltage regulator by means of the sisotool. As it can be observed in Fig.5.6 the step response for the simulink model is very similar to the sisotool response. In both graphs, the steady state is approximately at 0.35 seconds. Clearly shows that the controller is stabilizing after a step input and that the system is stable as expected.

Fig. 5.7 shows the entire system close diagram and the root locus graph. It can be appreciate that all the poles and zeros of the system are in the left side of the abscissa. It can be observed that 2 poles are closed to the abscissa and if the gain values are increased too much the poles may cross the axis. Therefore, the gain values of the PIs cannot be increased too much so as to ensure the stable mode.

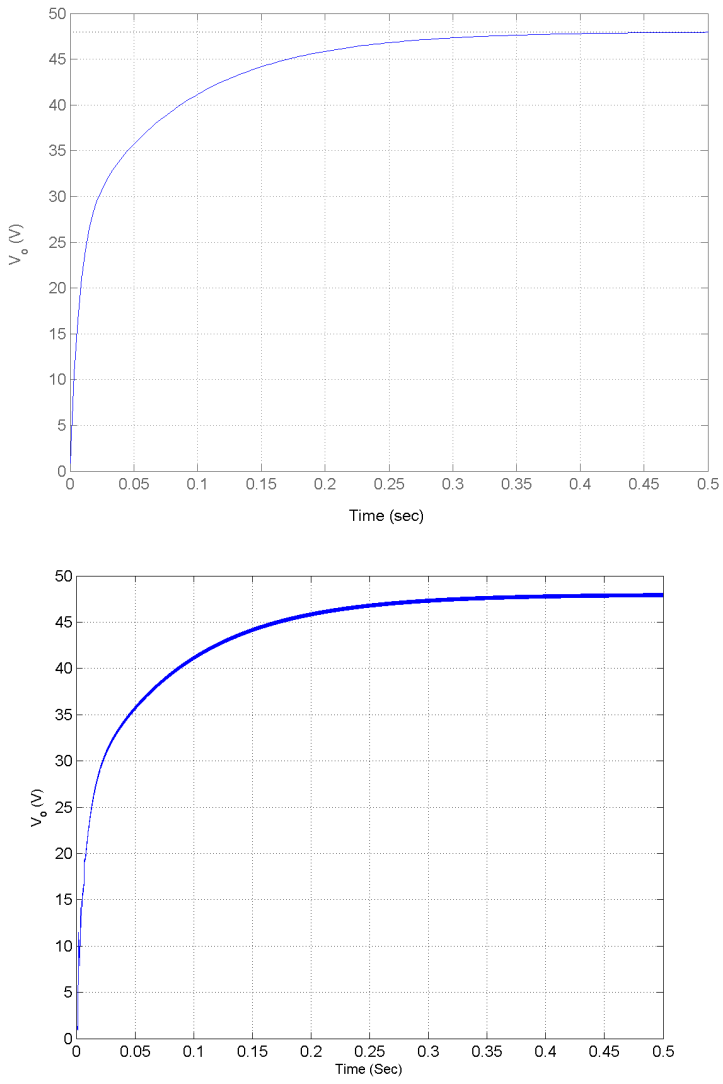


Figure 5.6: *Voltage step response for sisotool and simulink.*

Inner control loop design for boost mode

In this mode, the energy sources deliver power to the electric motor. The input voltages are lower than the output, thus they must be stepped up to have the required output voltage through a controlled boost circuit. The energy source V_1 delivers power to the output voltage V_o. For boost operation, the switching action only happens with Q_1. While Q_2 is always the oppositeof Q_1. In other words, when the switch Q_2 is 'on', the switch 'Q_1' is 'off', and when Q_2 is turned off, Q_1 is 'off'.

The control loops for the boost are identical, but with different transfer function. Controlling the inductor current and the output voltage, similar results are obtained for designing PI controllers. As well as in buck mode, the inductor resistor and the output capacitance resistor have not been taken into account.

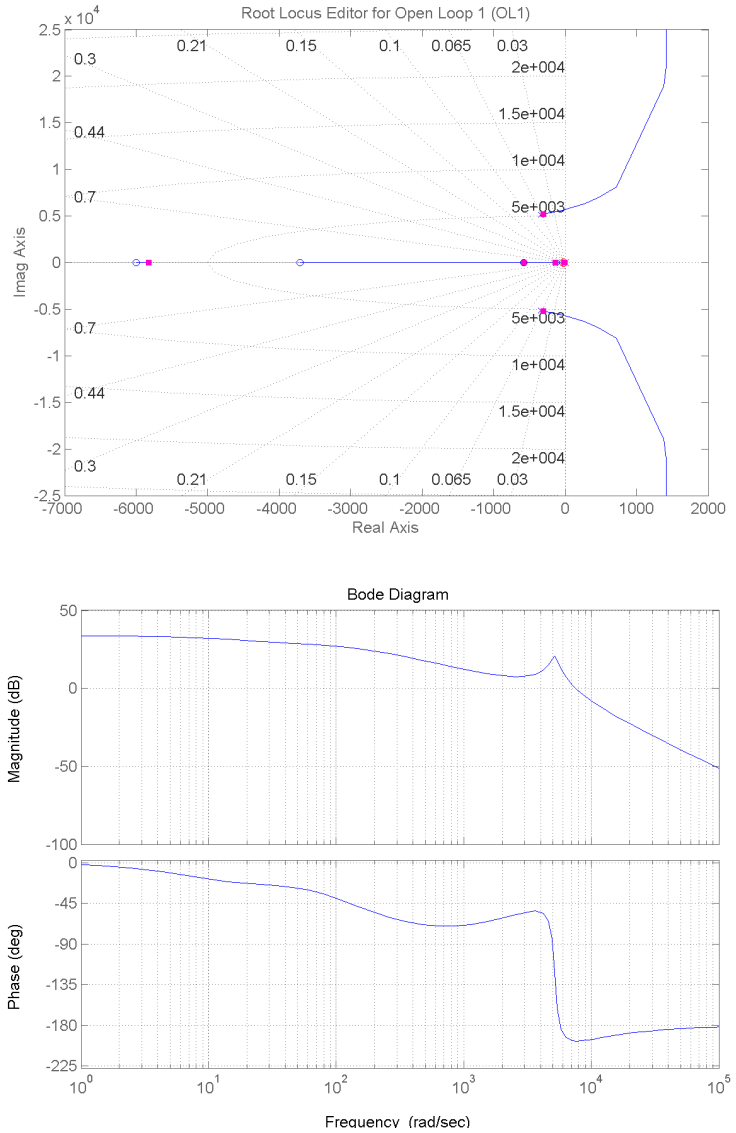


Figure 5.7: *Root locus and system closeloop bode.*

Duty cycle to inductor current transfer function with resistive load (G_1)

State Equations

$$Interval\ D_{Q_1}T_s \begin{cases} L\frac{di_L}{dt} = v_1 \\ C_1\frac{dv_1}{dt} = i_1 - i_L \\ C_o\frac{dv_o}{dt} = -\frac{v_o}{R_o} \end{cases} \quad ; \quad Interval\ (1-D_{Q_1})T_s \begin{cases} L\frac{di_L}{dt} = v_1 - v_o \\ C_1\frac{dv_1}{dt} = i_1 - i_L \\ C_o\frac{dv_o}{dt} = i_L - \frac{v_o}{R_o} \end{cases} \tag{5.23}$$

Average State-Equations

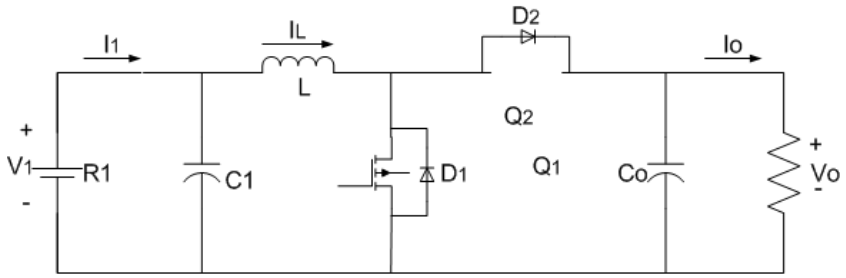


Figure 5.8: *Multi input power converter in boost mode.*

$$L\frac{di_L}{dt} = v_1 d_{Q_1} + (v_1 - v_o)(1 - d_{Q_1}) = v_1 - v_o(1 - d_{Q_1}) \tag{5.24}$$

$$C_1\frac{dv_1}{dt} = (i_1 - i_L)d_{Q_1} + (i_1 - i_L)(1 - d_{Q_1}) = i_1 - i_L \tag{5.25}$$

$$C_o\frac{dv_o}{dt} = -\frac{v_o}{R_o}d_{Q_1} + (i_L - \frac{v_o}{R_o})(1 - d_{Q_1}) = i_L(1 - d_{Q_1}) - \frac{v_o}{R_o} \tag{5.26}$$

Perturbation

$$L\frac{d(I_L + \tilde{i}_L)}{dt} = (V_1 + \tilde{v}_1) - (V_o + \tilde{v}_o)(1 - (D_{Q_1} + \tilde{d}_{Q_1}) \tag{5.27}$$

$$C_1\frac{d(V_1 + \tilde{v}_1)}{dt} = (I_1 + \tilde{i}_1) - (I_L + \tilde{i}_L) \tag{5.28}$$

$$C_o\frac{d(V_o + \tilde{v}_o)}{dt} = (I_L + \tilde{i}_L)(1 - (D_{Q_1} + \tilde{d}_{Q_1}) - \frac{(V_o + \tilde{v}_o)}{R_o} \tag{5.29}$$

Small-Signal Model

$$L\frac{d\tilde{i}_L}{dt} = \tilde{v}_1 + V_o\tilde{d}_{Q_1} - (1 - D_{Q_1})\tilde{v}_o \tag{5.30}$$

$$C_1\frac{\tilde{v}_1}{dt} = \tilde{i}_1 - \tilde{i}_L \tag{5.31}$$

$$C_o\frac{\tilde{v}_o}{dt} = I_L\tilde{d}_{Q_1} - (1 - D_{Q_1})\tilde{i}_L - \frac{\tilde{v}_o}{R_o} \tag{5.32}$$

Transfer functions

$$LsI_L(s) = V_1(s) + V_o D_{Q_1}(s) - (1 - D_{Q_1})V_o(s) \tag{5.33}$$

$$V_1(s) = \frac{1}{C_1 s}I_1(s) - \frac{I_L}{C_1 s} \tag{5.34}$$

$$V_o(s) = \frac{R_o(1 - D_{Q_1})}{R_o C_o s + 1} I_L(s) - \frac{R_o I_L}{R_o C_o s + 1} D_{Q_1}(s) \tag{5.35}$$

For $V_1(s) = 0$ relationship between the inductor current and the duty cycle of switch $Q_2$is given by

$$LsI_L(s) = V_o D_{Q_1}(s) - (1 - D_{Q_1}) V_o(s)$$

$$= V_o D_{Q_1}(s) - (1 - D_{Q_1}) \left(\frac{R_o(1 - D_{Q_1})}{R_o C_o s + 1} I_L(s) - \frac{R_o I_L}{R_o C_o s + 1} D_{Q_1}(s) \right) \tag{5.36}$$

$$\frac{I_L(s)}{D_{Q_1}(s)} = \frac{V_o R_o C_o s + V_o + (1 - D_{Q_1}) R_o I_L}{C_0 L R_o s^2 + Ls + R_o(1 - D_{Q_1})^2} \tag{5.37}$$

$$I_L = \frac{V_o}{R_o} \cdot \frac{1}{(1 - D_{Q_1})} \tag{5.38}$$

$$G_1 = \frac{I_L(s)}{D_{Q_1}(s)} = V_o \frac{2 + C_0 R_o s}{C_0 L R_o s^2 + Ls + R_o(1 - D_{Q_1})^2} \tag{5.39}$$

Current control verification

As well as for the buck mode, the values for the boost regulator have been calculated. As it can be seen in Fig.5.9 the step response for the simulink model is very similar to the sisotool response. Due to the initial values in the simulink program, the step response for the initial seconds is not totally equal to sisotool response, however the setting time for both graphs is obtained at around 0.06 seconds.

Voltage control verification

As it can be observed in Fig. 5.10, the step response for the simulink model is close to the sisotool response. In both graphs, the steady state is approximately at 0.14 seconds. However, due to the initial values of the system, the reponse in simulink model is not totally equal to the sisotool response.

Fig. 5.11 shows the root locus graph and the entire system close bode in boost operation. The root locus shows that the system is stable for the regulator values that have been chosen. All the poles are situated in the negative part of the ordinate axe. A big increment of the PIs values could make the system unstable if the poles cross the abscissa axe.

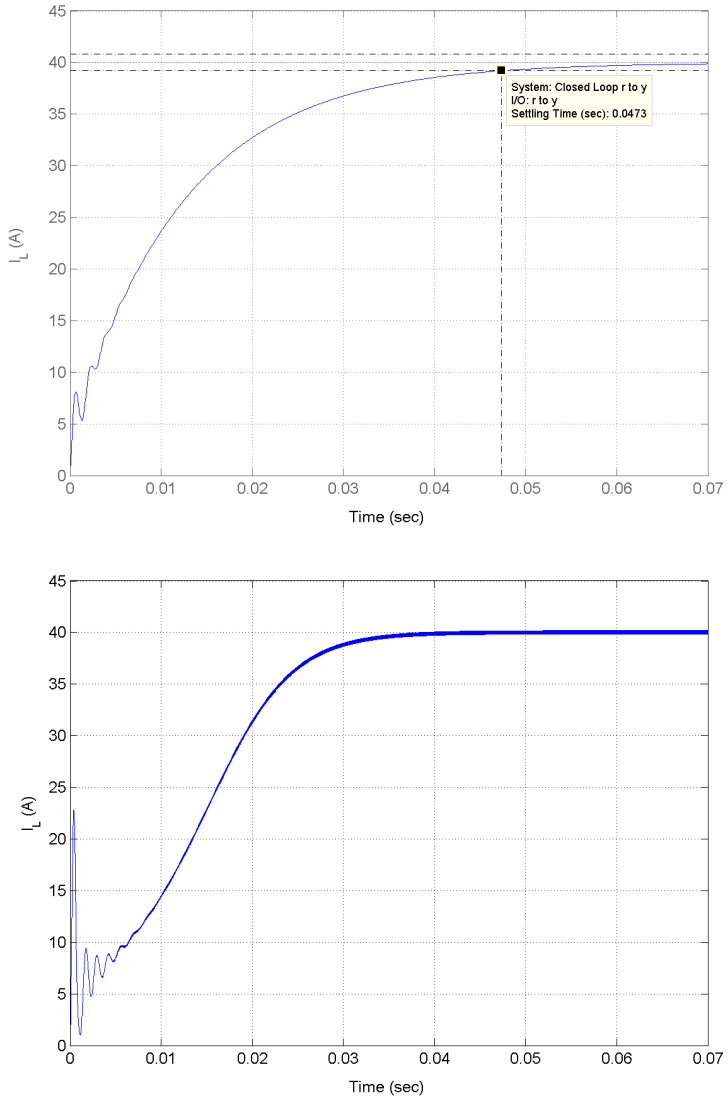


Figure 5.9: *Inner loop step response for boost mode in sisotool and simulink*

Outer control loop design for boost mode

The transfer function for the outer control loop is

$$\frac{V_o}{I_L(s)} = \frac{R_1}{R_1 C_1 s + 1} \cdot \frac{1}{D_{Q_2}} \tag{5.40}$$

5.2 Multiple input control topology and analysis

The general circuit topology for bidirectional multiple-input converter is shown in Fig. 5.12. The main advantage of this topology is that the inputs share a common inductance, an

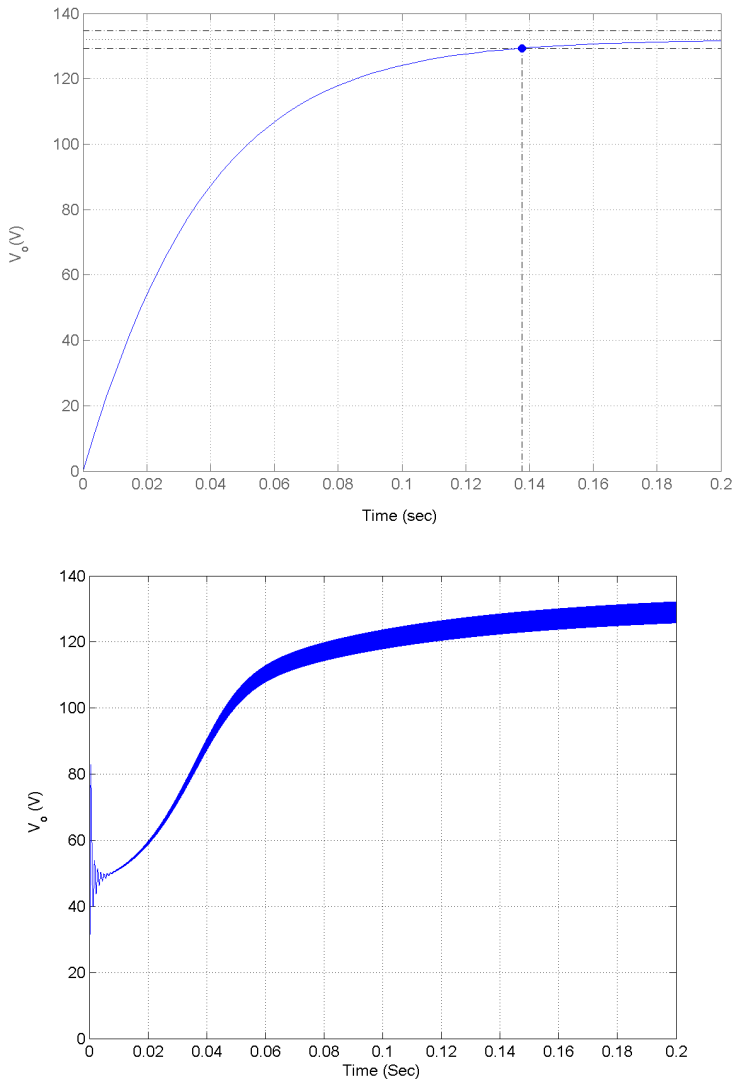


Figure 5.10: *Voltage step response for sisotool and simulink.*

output capacitance, as well as the switches. That way, by sampling the inductor current and the bus voltage, the current and bus voltage can be controlled through the gate signals. In this project, 2 input voltages are interfaced (V1 and V2), and 2 input currents respectively.

Boost operating mode

Depending on the power required from the load, different energy sources must be working at a time. The circuit for the boost operation can be reduced to Fig. 5.13.

The power distribution of the inputs is controlled through S_{1A} and S_{2A} switches. In other words, depending on the power required from the load, different energy sources would provide power to the motor, and this is made by controlling S_{1A} and S_{2A}. This topology can only transfer energy into the load with one input at a time. Thus, when the switch S_{1A} is 'on', the switch S_{2A} must be 'off' and vice versa. Switches S_{1B} and S_{2B} are 'off' for all boost operation mode.

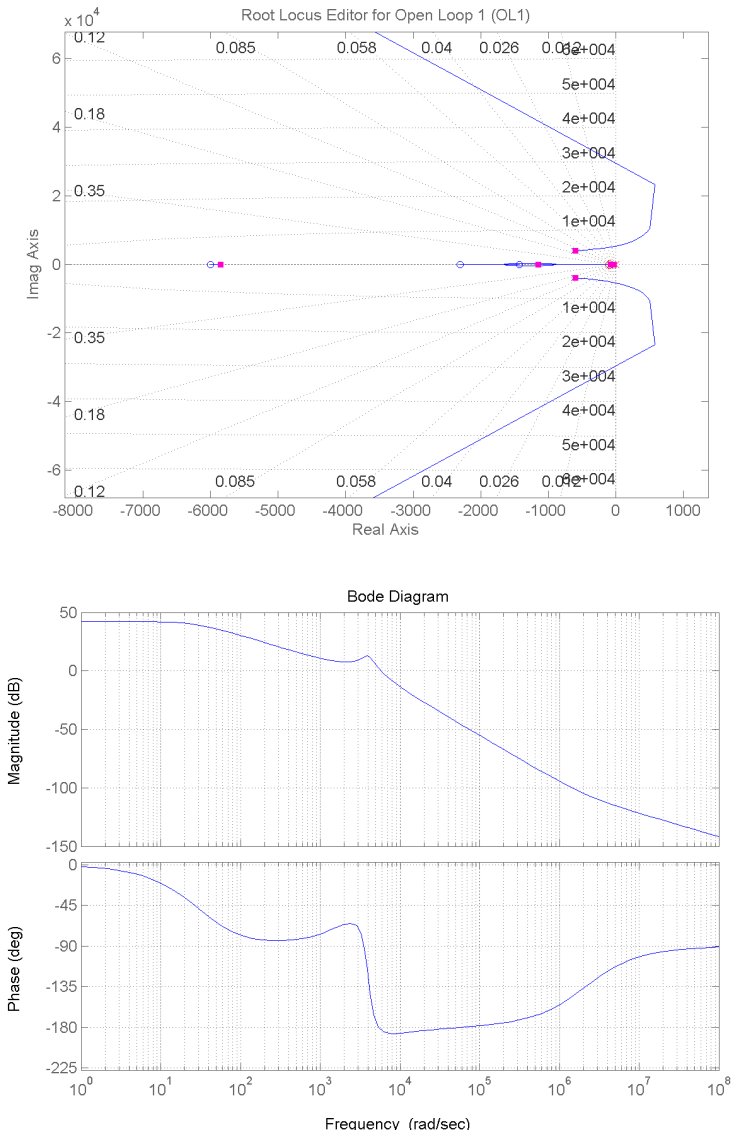


Figure 5.11: *Root locus and close bode for boost mode.*

The switching frequency for S_{1A} and S_{2A} is calculated as in Fig.5.14:

The measured inductor current is filtered to two different frequencies. The first filter (LPF_1) is a very strong filter used to obtain IL_1, which is filtered to 10 Hz. At the same time, the inductor current is also filtered to 1500 Hz with LPF_2 low pass filter, the resultant current is designated IL_2. After, the IL_1 is compared with IL_2 to calculate the current peaks (see Fig.5.15). In other words, if the inductor current suffers small variations, the difference between IL_2 and IL_1 is very small. On the other hand, if the electric car accelerates strongly, a big peak of current is required. In that moment, the comparison between IL_1 and IL_2, is very high and a current peak is measured.

This difference between both currents is named *ratio*, which has a value between 1 and 0. If the difference between IL_1 and IL_2 is high the *ratio* value is near to 1, however, if the difference between both currents is low the value is near 0. This value is multiplied with the

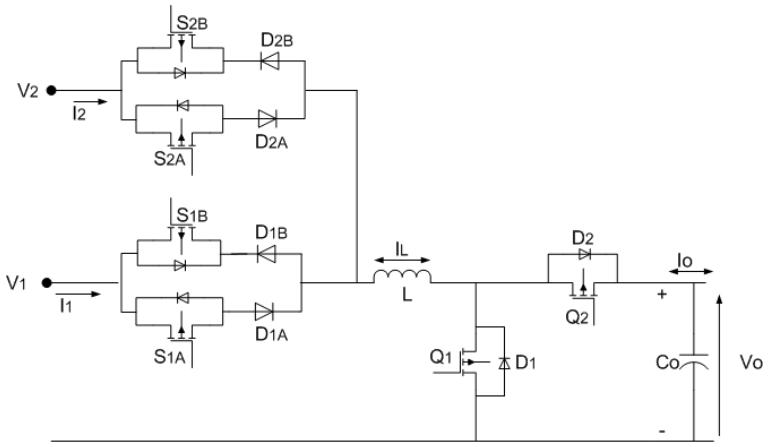


Figure 5.12: *Proposed multi-input DC/DC converter*

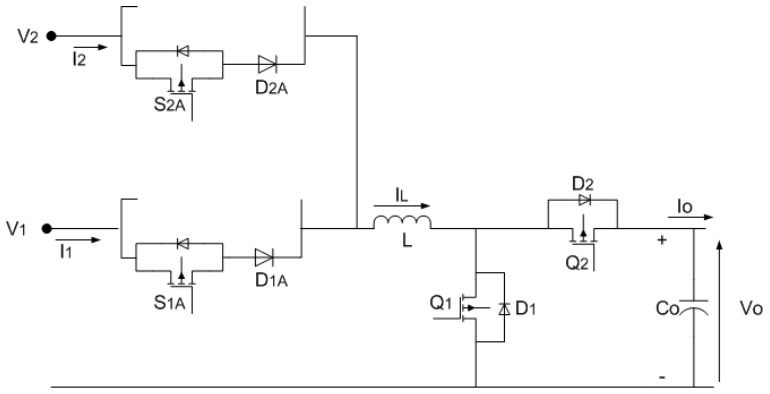


Figure 5.13: *Multi input converter in boost mode.*

duty cycle of the $DQ_1$to obtain the duty for the S_{2A}. Therefore, the bigger the *ratio* value is, the longer the S_{2A} is opened and the capacitors provide more current to the load. The difference between D_{Q1} and D_{2A}, is the duty for battery switch. When the Q_1 is off, only the battery provides current to the load, (see Fig.5.16).

In the real application, the duty ratios for both S_{1A} and S_{2A} should be calculated considering the SOC of the energy sources. However, for the simulation this factor has been neglected.

Considering that the output voltage is almost constant, the inductor voltage is

$$V_L = [V_1 - V_{out}]S_{1A} + [V_2 - V_{out}]S_{2A} + (V_1 - V_{out})(1 - [S_{1A} + S_{2A}]) \tag{5.41}$$

Thus, as it is mention in the previous Chapter, Vout is calculated as

$$V_o = \frac{V_1 Deff_{S2A} + V_2(1 - Deff_{S2A})}{1 - D_{Q1}} \tag{5.42}$$

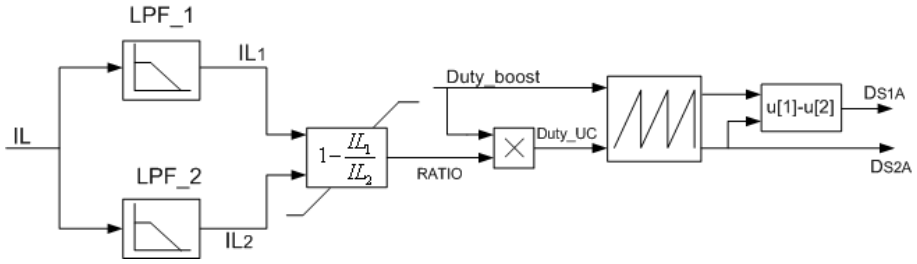


Figure 5.14: *Duty ratio calculation for S_{1A} and S_{2B}.*

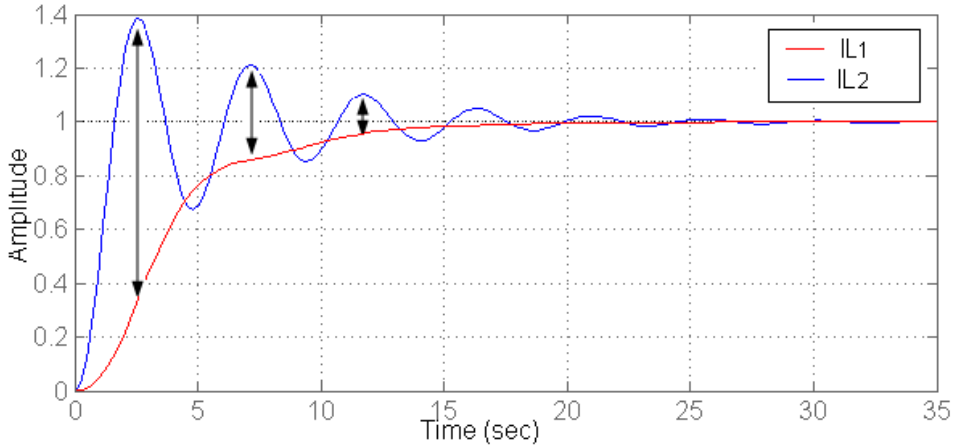


Figure 5.15: *Ratio calculation.*

where $Deff$ is the effective duty cycle of each switch.

Buck operating mode

In this mode, the power flows from the output voltage to charge the energy sources. The current is produced from an output source (Vo) such as during regenerative braking from an hybrid electric vehicle application. This topology can only charge one of the input sources at time. In this mode the current goes 'left way' and is considered as negative. The circuit for the buck operation can be reduced to Fig.5.17 .

In this mode the switching action is between Q_2 and D_1. Q_1 is always the inverse of Q_2. For this mode, the energy distribution is made in a different way than in boost mode. The control has been made considering the SOC of the UCs. First the ultracapacitor is charged and once it is fully charged, the battery start charging. As the ultracapacitor is much faster in charging operation than the batteries, they are charged before. This way, when the electric car starts consuming power, is ensure that the UCs are totally charged to provide big peak of currents on acceleration times.

In relation with these type of topologies where batteries and UCs are combined as electric vehicles energy sources, many different methods has been studied for the power distribution. One of the methods that can be considered is explained in reference[20]. In this paper, the UC and battery are charge considering different SOCs of both energy sources.

Another interesting paper is in reference to [21]. This paper not only takes in consid-

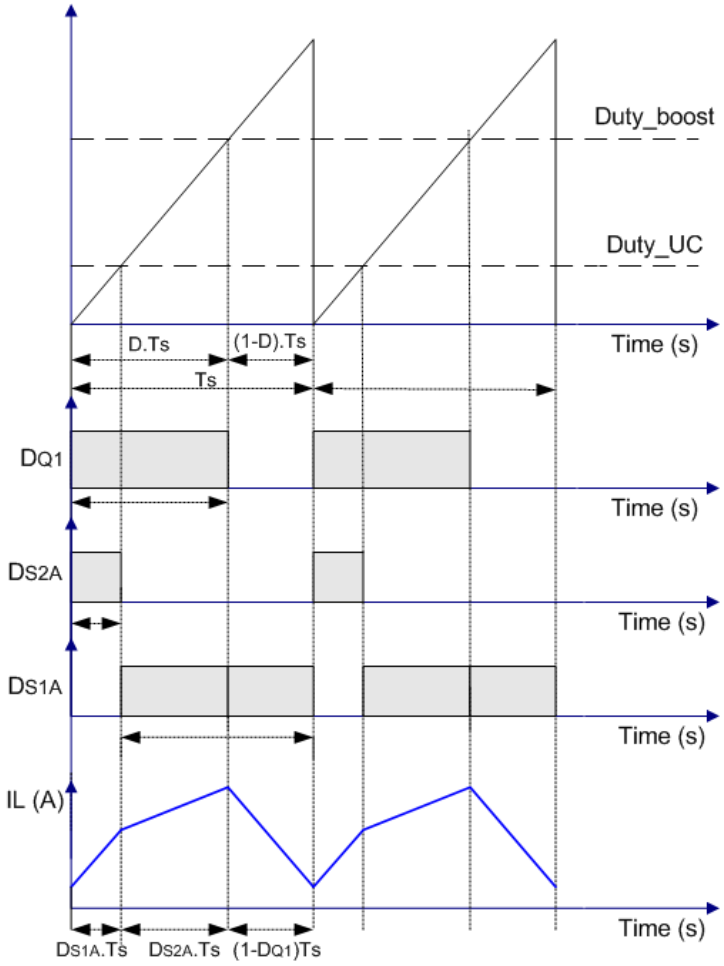


Figure 5.16: *Duty cycles for boost mode.*

eration the SOC of the battery and UC, but also takes in consideration the electric vehicle speed to estimate the braking kinetic energy when braking.

The previous PI controller are included in the Appendix G.

5.3 Simulations Results

In Fig.5.18 is presented the graph used for the test. The figure shows the electric car power consumption. During the simulation the car has different power levels that have been input random. When the power has a positive value the motor is consuming power, therefore the converter works as boost mode. In case the power is negative, the car is generating power and so, the converter works as buck mode. Considering the maximum power of the car settle to 2 kW, the power is always between 2000 kW and -2000 kW.

To test that the converter operates correctly, first the D_{Q1} and D_{Q2} switching has been checked. As it was mention previously, D_{Q1} is the responsible for the boost operation control, while D_{Q2} make the control for buck mode. Fig. 5.19 represents the output power of the

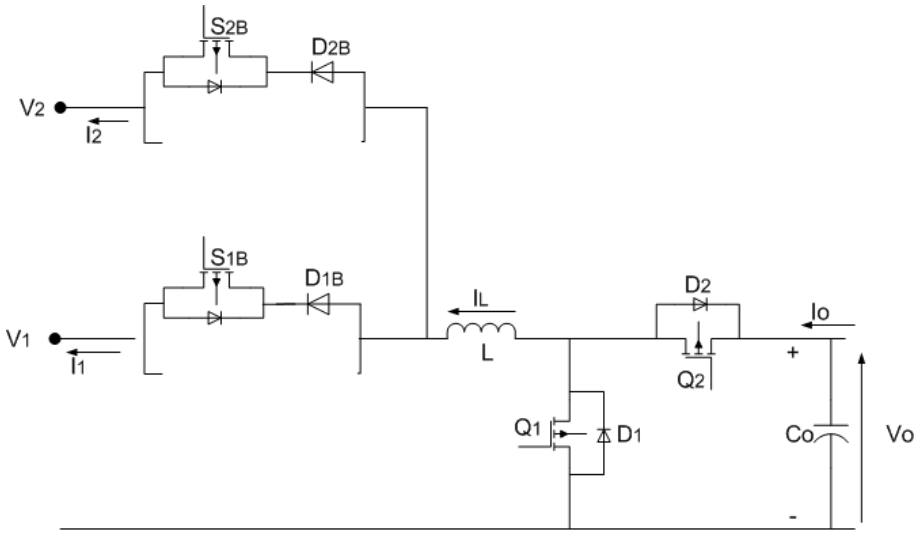


Figure 5.17: *Multi input converter in buck mode.*

electric car together with the PWM for Q_1, S_{1A} and S_{2A} switches of the converter. It can be seen that when the car is consuming power, the D_{Q1} is activated, thus, the energy sources are the responsible for delivering power to the motor, and the converter is working as boost topology. Meanwhile, D_{Q2} is set to 1. In the real application the D_{Q2} should be set to zero. Nevertheless for the correct operation of the simulation this must be 1.

On the other hand, when the car is generating power, D_{Q2} is commuting, which makes possible the buck operating mode. As it is shown in the figure this happens between 0.9 and 2.1 seconds, and 3.5 and 3.8 seconds interval. In buck mode, the switch D_{Q1} is set to 0.

After verifying that the converter control switches work properly another simulation has been performed in order to verify that the voltages are the desired values. In Fig.5.20 the output and input voltages are described when the car for all the simulation range.

It can be seen that for any output power value, the voltage is always near to the rated, set to 132 V. In the second 0.9 it can be observed that the voltage drops for a small period to 0. At this moment, the converter start working as buck mode and due to the initial values of the output capacitor a voltage drop happens.

In the same graph it can be seen the input voltage of the converter. It can be appreciated easily that the capacitors and batteries delivered power to the motor. Having a look to the figure it can be seen that when the car is accelerating both energy sources are feeding the converter. Thus, the multiple input topology is acting.

On the other hand, when the car is decelerating the input voltage is almost constant.

The multiple input action is made trough the ratio value obtained from filtering the inductor current. The values for the ratio variable is detailed in Fig. 5.21. The ratio variable represents the amplitude for the peak inductor currents in a range of 0 and 1 value. When the inductor current is increasing, the ratio value increase and so the duty cycle D_{S2A}, allowing the UC switch (S_{2A})to start commuting. This ratio is calculated for all the

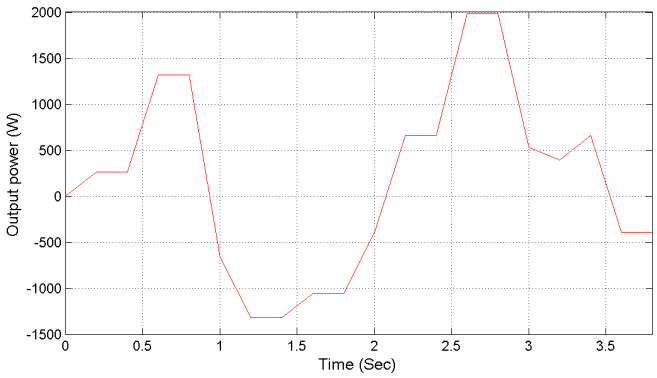


Figure 5.18: *Electric car output power .*

simulation; however, in buck operation mode is not used, as a different energy management control is used.

Fig. 5.22 shows the PWMs generated to control S_{1A} and S_{2A} switching. As it is shown, when the electric car is requiring more power, both D_{S1A} and D_{S2A} switch on, and energy is supplied from both sources. As was mention before, the energy sources cannot deliver power both at the same time. However, in so long simulation period, they seem to be commuting both together. As the switching frequency is 15 kHz, is impossible to appreciate the PWM periods for the switches.

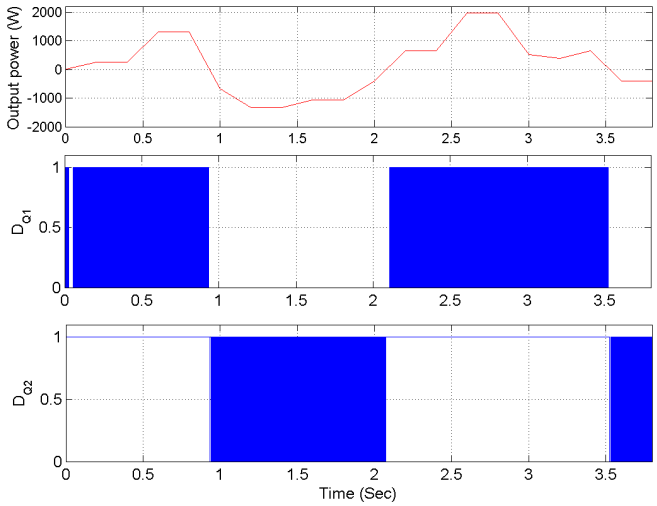


Figure 5.19: *D_{Q1} and D_{Q2} switching intervals.*

In order to see more in detail the PWMs, Fig.5.23 shows the values for a very short step time.

In Fig.5.23 can be seen the PWM for all the switches that operate in boost mode. The figure confirms that the PWMs for multiple input switching do not happen at the same time to prevent short circuits. In a period where the Q_1 is 'on', a small part S_{1A} is activated and for the rest of the period where $Q_1$is 'on', S_{2A} is activated.

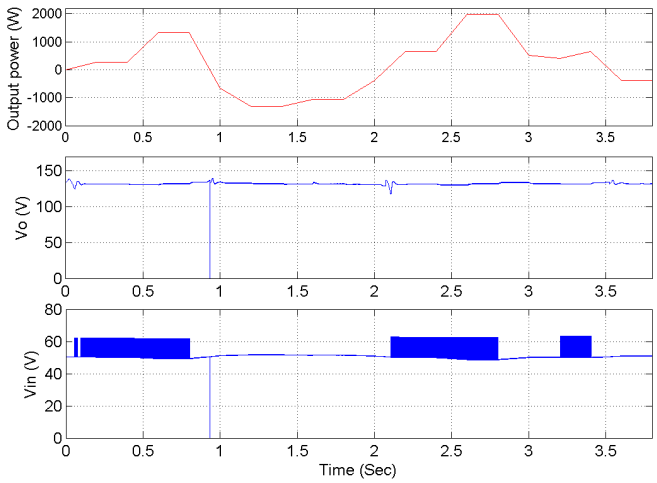


Figure 5.20: *Output and input converter voltages.5.20*

In Fig.5.24 the inductor current when the converter is working with multi input sources is shown. The use of the capacitors, provide bigger peaks of current when necessary. The figure shows that the inductor current suffers a small change on the slope when both energy sources are actuating together. On the first period where the coil is charging, D_{S2A} is switching. It can be observed that the current slope is higher, however, in the second half, D_{S1A} is activated instead of D_{S2A}. In this moment, the slope decrease a little bit.

Fig. 5.25 represents the batteries and UCs SOCs level. In boost mode, both energy sources discharge. However, as both are delivering current and due to the high capacity of the capacitors, the discharge of the capacitors is almost impossible to notice. However the battery state of charge change considerably depending on the input current.

According to the buck energy management control implemented, in regenerative mode the UC must be charge completely before the batteries start to charge. Therefore, in buck mode the UC charge while the battery SOCs keeps constant. As all the generated current goes to the capacitors, the UCs charge much more than discharge.

***

In this Chapter the transfer functions needed for the duty-cycle control are described from small signal equations of the converter. The duty cycle control has been calculated with the MATLAB/sisotool and afterwards, tested in Matlab/Simulink. The response achieved in the sisotool, corresponds to the values obtained with the Matlab/Simulink models. The control for the mulitiple input is described and several simulations were made to check the proper control of the system. Different converter parameters were analyzed with satisfactory results. Once the models are working with the control in the simulation, it is time to implement the prototype in the laboratory. Design of the converter is presented in the next Chapter.
Simulation results

To test the correct operation of the converter, several simulations have been run. Next the results of the simulation are presented. All the values have been obtained from the same simulation to have the same parameters and initial conditions. The analysis is made for

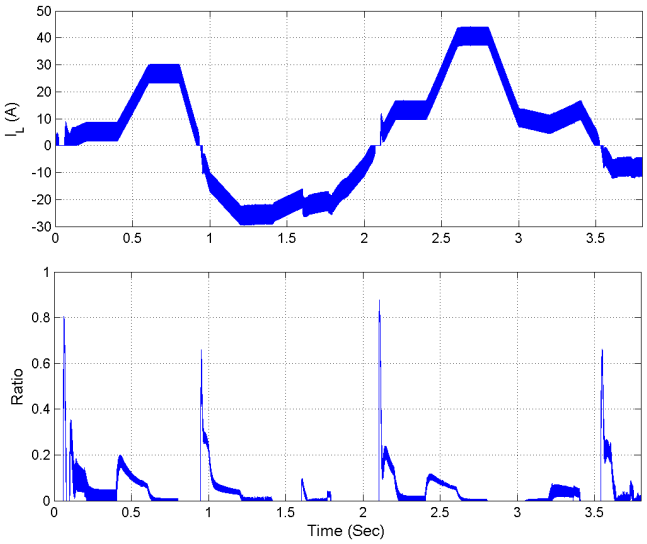


Figure 5.21: *Inductor current and ratio value.*

different power compsumtion of the car, thus the car operates as motor and generator modes. The analysis is made for 3.8 seconds simulation.

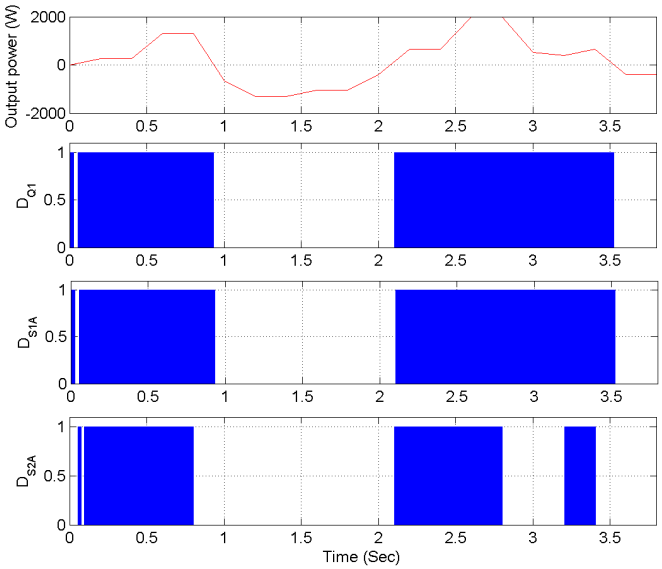


Figure 5.22: *Multy input control.*

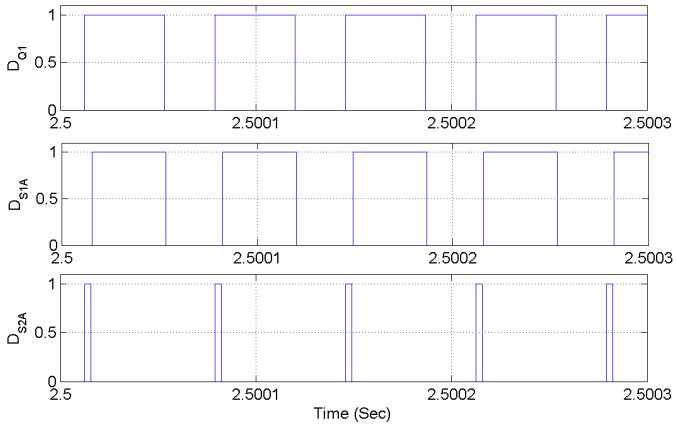


Figure 5.23: *Boost operating mode PWMs.*

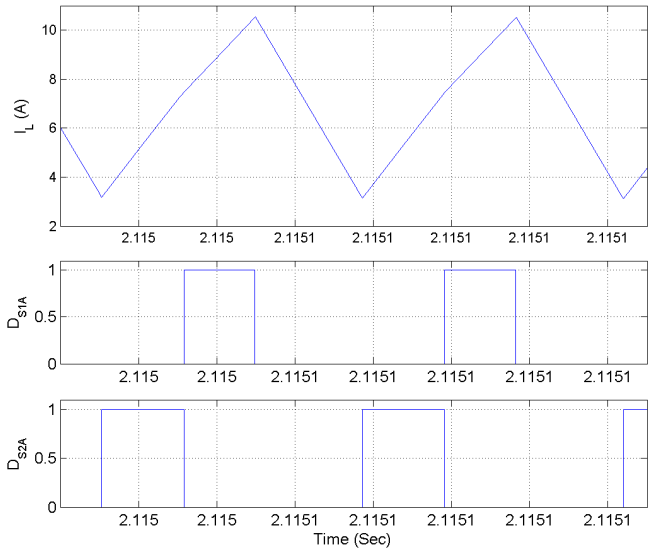


Figure 5.24: *Inductor current for multiple input converter.*

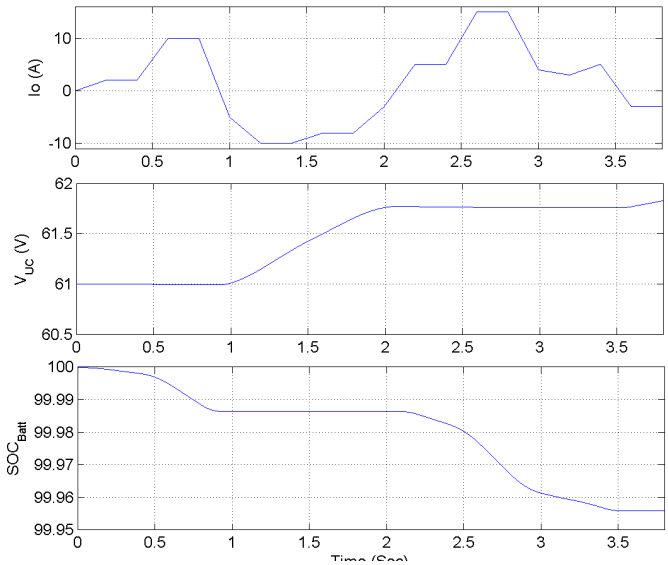


Figure 5.25: *Battery and UCs voltages.*

6
Design of the converter

The theoretical analysis shown in the previous chapters, enables developing the converter that would meet the design demands. The main concern is the selection of the switches together with the gate drivers for them.

As it is mentioned in the previous chapters, it is not the objetive of this report to build a real converter. Therefore, a scaled down prototipe was build. Furthermore, due to time limitations, only the boost mode was implemented in the laboratory.

6.1 Design of the power circuit

In the following sections are presented: the selection of the mosfets, the gate drivers and the diodes. In the last section miscellaneuos elements necessary for the power stage completion are introduced. It is also designed the pcb board where all the components are placed. The Altium files are included in the Appendix F

Selection of the mosfets

In Chapter 4 are presented the specifications for the birectional multiple-input dc/dc converter. The dc sources have a rated voltage of 48 V and 64 V (input voltage in boost mode) and the dc link 136 V (output voltage in boost mode). The converter is rated to a power of 2000 W, therefore, if it is working in boost mode, there is an output current of 14.7 A. In order to remind where the mosfets in the converter are placed, the topology is presented in the next Fig. 6.1. For the boost mode, only are used S1A, S2A, Q1 and Q2.

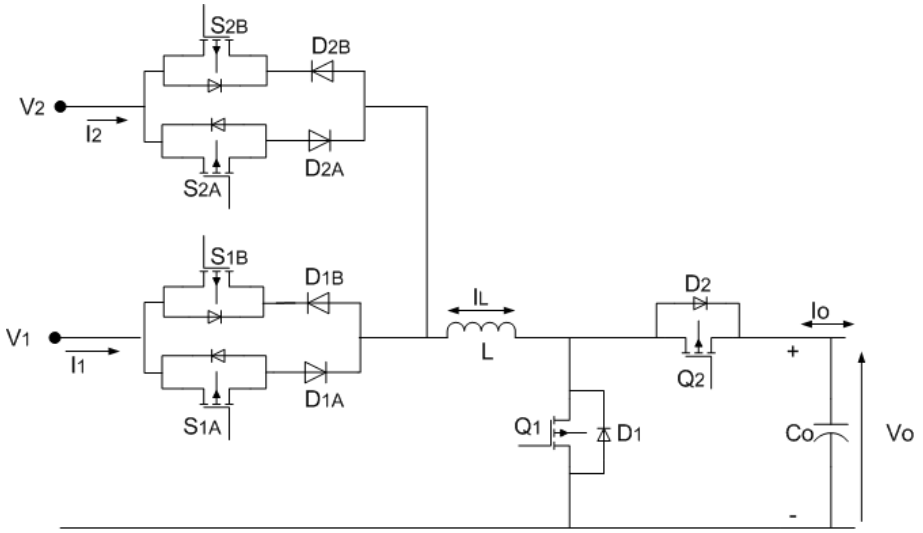


Figure 6.1: *Topology of the multiple input converter, mosfets and diodes selection*

S1A and S2A have to support the input currents to the system. The input currents in the boost mode are bigger than the output currents. Furthermore, in some cases, only one of the switches (S1A and S2A) takes care of the input current (the system is working just with one input source), therefore they have to support at least:

$$V_O = \frac{V_{in}}{(1-D)} \tag{6.1}$$

The extreme case is when just using the smaller voltage source, in this case 48 V. The maximun duty cycle is:

$$D = -\frac{V_{in}}{V_o} + 1 = -\frac{48}{136} + 1 = 0.64 \tag{6.2}$$

If the maximun output current is 15 A, it can be obtained the maximun input current,

$$I_{in} = \frac{I_o}{(1-D)} = 15 \cdot (1 - 0.64) = 42.5A \tag{6.3}$$

The mosfets placed in S1A and S2A have to support at least 64 V and 43 A. The choosen devices are RFP40N10. To implement Q1 and Q2 are used the 20N60S5 mosfets, but in this case two of them are installed in parallel to support the current.

Selection of the diodes

It is necessary to install two diodes to make the converter work in boost mode. The diodes are D1A and D2A. As mentioned in the previous section, these diosdes have to support the input currents of the system, therefore, the specifications are the same as for the mosfets. The choosen device is B10100.

Selection of the gate drivers

The gate drivers are the devices responsible of switching the mosfets. They change the control signals (5 V) to higher voltage signals (15 V). Some of them can drive the mosfets when their source is not refered to ground. As Fig.6.2 shows, the gates of the mosfets S1A, S2A and Q2 are not connected to ground, therefore it is necessary to supply +15 V between every gate and source.

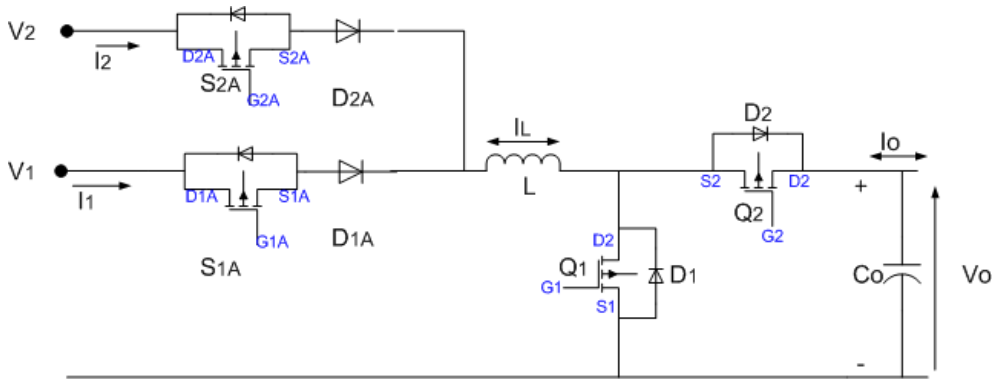


Figure 6.2: *Inverter topology, applied voltage between gate and source for each mosfet.*

Furthermore, if it is taken a look to switching squence in Fig.4.12, it can be seen that the mosfets Q1 and Q2 always take the opposite position. This can be considered as an advantage. Some of the driver can generate two opposite output signals with an included hardware dead-time. Example of this kind of devices is the integrated circuit IR 2103.

In the next Fig.6.3 is presented a diagram of how are done the connections in the power board using this device. Using this driver, the converter can be made synchronous. Instead

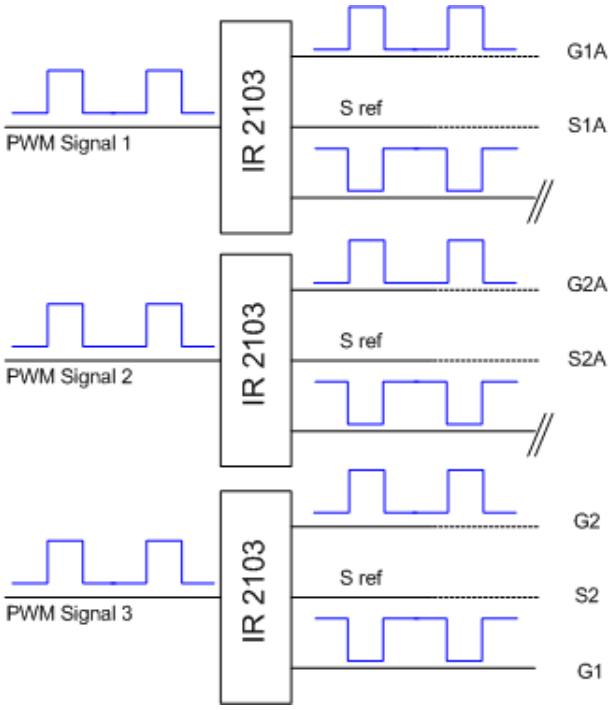


Figure 6.3: *Diagram of how are the mosfet driven in the power board of the converter*

of making the current flow throught diodes, the switches Q1 or Q2 are closed and they take the current. Therefore, because of their low conduction resistance, the losses are smaller. A last remark about choosing the drivers is that it is necessary to instal a small resistance between the output of the driver and the gate of each mosfet to limit the current.

Miscellaneus components

Once the main components of the power board are selected, some other components have to be installed to make the whole system work. First, the optical signals from the control have to be transformed to electrical signals. To do this task, the recievers SFH551V are used. In order to supply the system are installed two voltage regulator to obtain +5V and + 15V. Finally, the inductance and the filter capacitor are connected to the board but they are not placed there.

Once the power board is designed, a control board to create the PWM signals is needed.

6.2 Design of the control circuit

In this section is presented a brief introduction to the digital signal proccesor and later on, the components used in the control circuit.

Digital Signal Proccesor - DSP

For the presented application, the TMS320C28335 DSP is chosen. It consist on a logic integrated circuit mounted in an auxiliary board ($F28335_eZdsp$)[13]. This device provides the necessary supply connections for the TMS320c28335 to be run and programmed. The DSP clock is of 150 Mhz and needs to be supplied with 3,3 V. It is able to do hardware PWM signals and includes several AD converters. For further information, see [12]. The DSP is programmed in C code, and it is used the Code Composer Studio compiler.
Using this programmable divece to control the converter assures enough computation speed and it also has the advantage that it can operate with floating point, therefore, operations are very easily done.

Control board

The used control board is designed by the Aalborg University. It provides the necessary circuitery to adapt the readings given by the sensors and also is able to transmit optical PWM signals. It is possible to connect four sensors and to transmit six PWM signals. The Altium files are included in the Appendix F. The choosen sensors are three lv-25 P for reading the two input voltages and the output voltage, and a current sensor to measure the inductor current. The implemented code to create the PWM signals and to read the sensor is shown in the Appendix E.

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Once the control board and the power board are designed and built, they have to be tested in the laboratory, together with the implemented software. In the next Chapter 7 are presented the laboratory setup and the obtained results.

7 Laboratory Results

After the converter, together with the control board, was designed and successfully built, its performance should be evaluated through laboratory tests. This chapter summarizes the obtained results. The tests were conducted in such a manor to be able to examine operation of each part separetely. Final test compromised the whole system linked together to check if it can operate together. Therefore in the next sections are presented the measurementes and observations made for separate to the separate components and for the whole setup. Finally, test plans for the future are introduced.

7.1 Separate components test results

First priority was to show that the control board is operative and capable to create the proper PWM signals. Main goal of the test was achieved as it can be seen in Fig. 7.1.

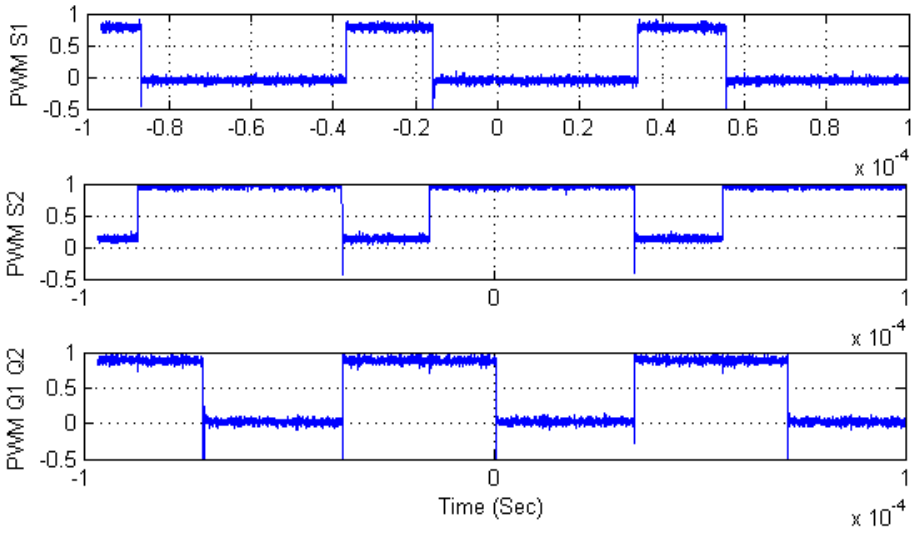


Figure 7.1: *PWM signal measured in the output of the control board*

The preivous Fig.7.1 shows the PWM signal applied to the converter. The upper graph presents control signal given to the mosfet S1. Input source V1 delivers power to the converter while this signal is in on state. The graph in the middle reprents the switching state of the mosfet S2. When this switch is on is V2 the source that supplys energy to the system. The lower graph represents the gate signal given to the mosfet Q1.
As it is mentioned before, it is necessary to apply at least 15 V between the gate and the source of a mosfet to make it conduct. The signal presented in the next Fig. 7.2 shows the mosgets driver response. It is plotted in blue the control signal given by the DSP and in black color the switching signal created by the driver.

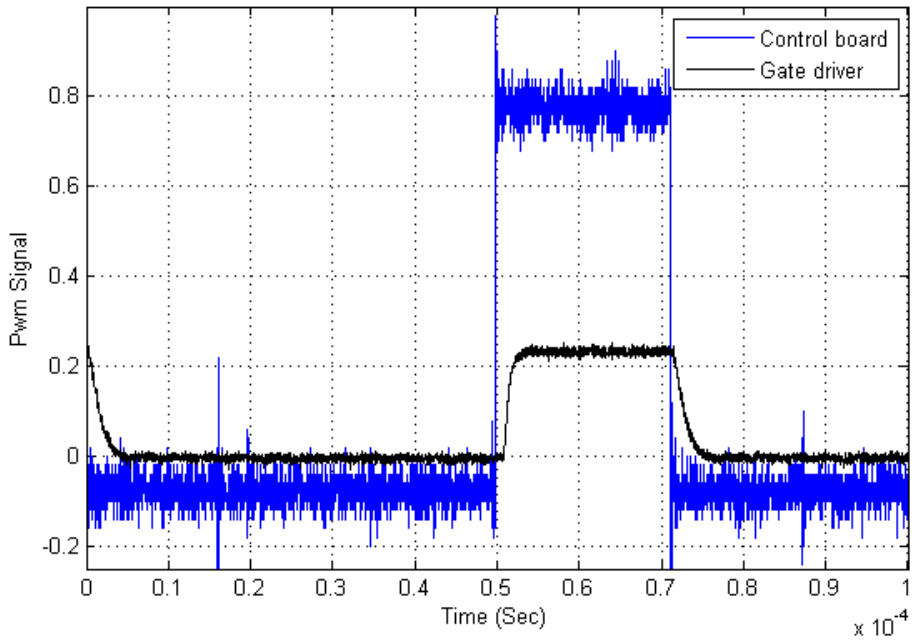


Figure 7.2: *PWM signal measured in the output of the control board (blue) and same PWM signal measured between G2 and S2*

It is visible between the two signal a small delay, introduced by the driver. This delay does not represent a big problem, because is the same for all the mosfets and it can be also compesated by software. This Fig. 7.2 also shows that the driver response is not fast enough. A possible answer to this phenomenon is that the resistor installed between the driver and the mosfet (resistor to limit the currents) was calculated for just one mosfet, and in the board are installed two in parallel.

7.2 System test results

Once it is proved that the control signals work properly, it is decided to apply power to the system. In order to realize the test, the choosen setup is presented in the next Fig.7.3

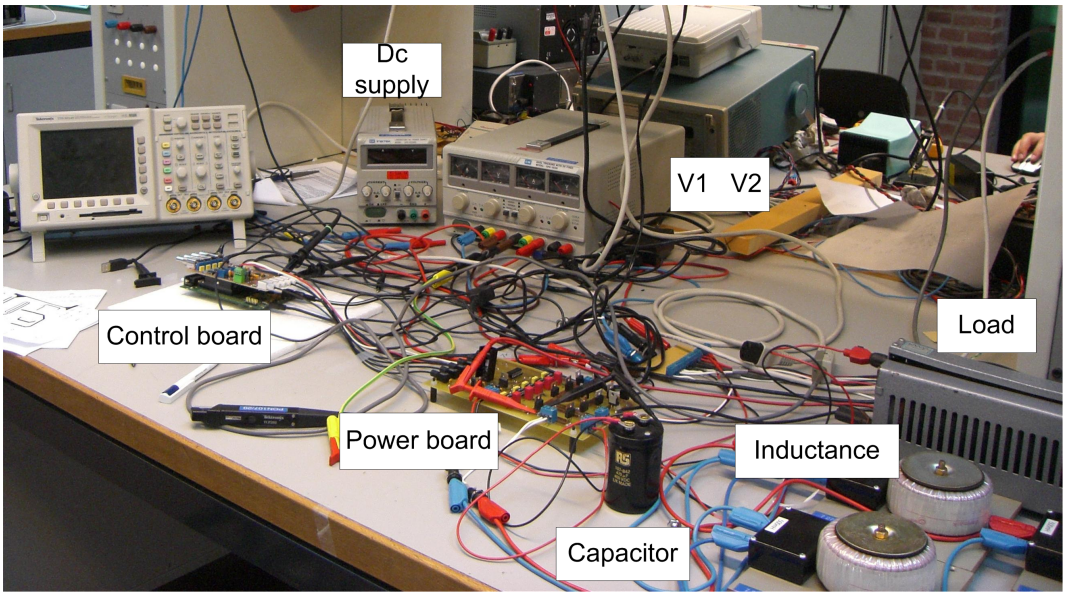


Figure 7.3: *Laboratory test setup*

To perfom the whole test setup it was choosen and inductance of 166 μ H, an output capacitor of 470 μ F, V1 was set to 13 V and V2 to 18 V. The switching frequency was decreased to 150 Hz to increase the changing in the slope of the inductor current. Results are shown in Fig.7.4

In the previous Fig.7.4 are presented from up to down, inductor current, IL, output voltage, Vo, input current from source V2 and Q1 duty cycle. In the inductor current plot it can be seen that when V1 is applied the slope in the current is smaller that when V2 is the input source. V1 should be higher than V2, but the dc source used for the test could not give more power. This figure also shows that the source 2 gives current to the system during Q1 T_{off} and also during the half of T_{on}.
This results confirm that the proposed converter works properly and the next step, implement the control can be realized.

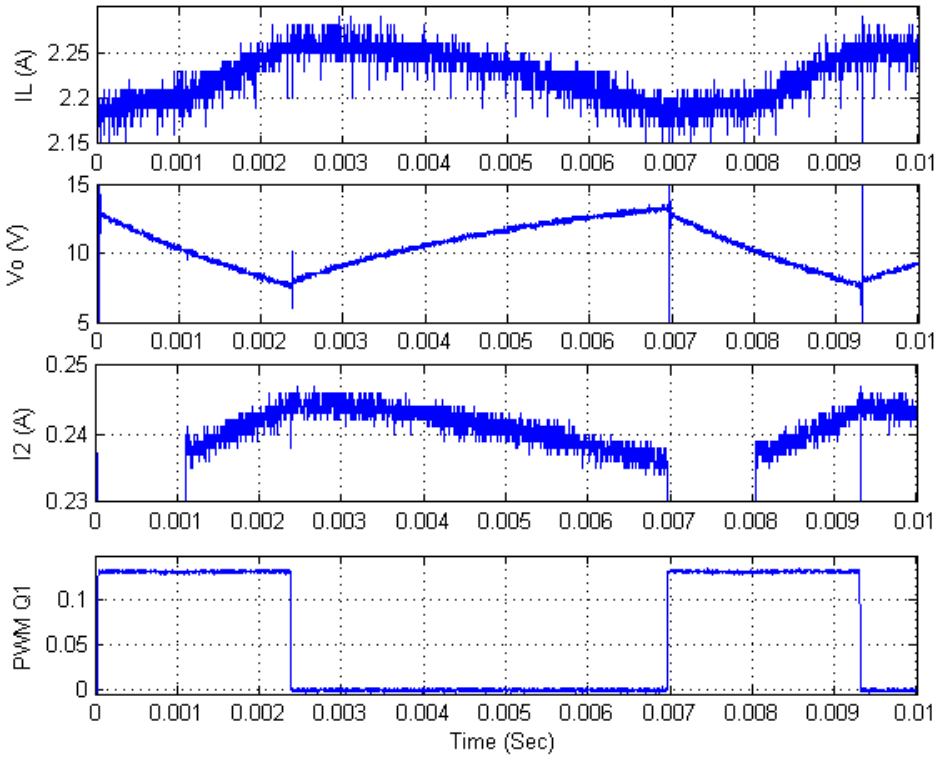


Figure 7.4: *Signals measured in the converter in boost mode operation. Starting from the upper one: Inductor current, IL, output voltage, V_o, input current from V2, I2 and PWM control signal for the mosfet Q1*

7.3 Future test plans

Due to the time limitation, the control loops for current and voltage were not managed to be tested. However, the code is prepared for the implementation of the control. The sensors are read correctly.
To fully complete the projects objective, the whole designed converter should be able to work in boost and buck mode. Such can be easily performed by changing the gate mosfets drivers. With the actual ones, it is not possible to maintain switches S1 and S2 closed for more than one period.

***

Despite the fact that not all the intended test were conduct, shown results are enough to prove that the built converter is capable of stepping up both input voltages. The sources of the errors were located and can be easily removed.

8

Conclusions and Future Work

8.1 Conclusions

The main goal of this project was to design, build and control a multiple input dc/dc converter for an automotive application. It was stated that a stable output voltage was desired on the DC link for any electric vehicle power output, and also a high efficiency design was required. So as to improve the efficiency, a converter feed by batteries and ultracapacitors which share the same inductance and switches has been implemented. In other words, a multiple input DC/DC converter. The combination of these energy sources can provide a light and high-performance vehicle.

Therefore, to reach the objective of the project, the power circuit has been simulated in Matlab/Simulink. First, the model has been analyzed in open loop by fixing a duty ratio for the switching of the transistors. This way, the correct design of the converter, in buck and boost mode has been checked. Afterwards, the control has been designed and test. The controllers have been tunned through the Matlab/sisotool, to obtain a fast and stable response.

Then the close loops control have been implemented in Matlab/Simulink. For concluding the simulation section, the multiple input was added to the model. Satisfactory results were obtained controlling the converter in both modes.

Once the simulations were working properly, it was decided to build the prototype in the laboratory. A DSP was used to control the power board. Due to time constraints, the implementation of the control was not possible.

The converter was tested in the laboratory using fixed duty cycles. Obtained results were as expected. Unfortunately, because of the hardware configuration, only boost mode could be run.

The analysis has been made for a new DC/DC converter topology. The converter is able to support multiple inputs and shows that could be a future application for power energy diversification of different energy sources.

8.2 Future work

Due to the time limitation not all of the intended objectives were managed to be accomplished. The future work of this project may include:

- A more detailed energy sources. The main objective of this project was to simulate and control the converter. Therefore less attention has been paid to the ultra-capacitor and battery model.

- Implementation of a buck mode energy management. On this project, the multiple input management has been focus mainly on the boost topology living apart the control for the buck mode. Two references were mention in Chapter 4 with two control topologies for the control. To study and implement one of these controls could be of particular interest.

- Implement and test the control system on the DSP board. For future work the DSP should be programmed with the close loop control, measuring the current and voltage from the converter and testing it in the lab.

- Build a more powerful converter for automotive application. The converter has been modelled for low power so as to simplify the converter design.

Bibliography

[1] Direct Torque Control, Technical Guide No.1, ABB

[2] Understanding Buck Power Stages in Switchmode Power Supplies, Application Report,SLVA057

[3] Understanding Boost Power Stages in Switchmode Power Supplies, Application Report, SLVA061.

[4] Power Electronics, Mohan&Undeland,

[5] Juing-Huei Su, Jiann-Jong Chen, Dong-Shiuh Wu, Learning Feedback Controller Design of Switching Converters Via Matlab/Simulink, IEE Transactions on educantion, Vol.45,No.4, November 2002.

[6] K.T. Chau and Zheng Wang. *Overview of power electronics drives.* Department of Electrical and Electronic Engineering - Hong Kong university [cited June 2005]

[7] Martin Eberhard and Marc Tarpenning. *The 21st Century Electric Car.* Tesla Motors Inc. [cited July 2006]

[8] Alireza Khaligh. *A Multiple-Input Dc-Dc Positive Buck-Boost Converter Topology.* IEEE, Electric Power and Power Electronics Center - Illinois Institute of Technology

[9] Bryan G. Dobbs and Patrick L. Chapman. *A Multiple-Input DC-DC Converter Topology.* IEEE, [cited March 2003]

[10] Dr. Ray Ridley. *The future of the electric car.* Switching Power Magazine. Available from: www.ridleyengineering.com

[11] Andr A. Ferreira, Leonardo de A. Silva and Jos A. Pomilio. *DC-DC Converter Solutions For Modern Electric Vehicle Power Supply Systems.* State University of Campinas-Brazil.

[12] TMS320F28xxx, Digital Signal Controllers (DSCs), Data Manual,SPRS439C

[13] eZdspTM F28335, DSP Development Systems Reference Technical,510195-0001 Rev. C

[14] Zhihao Li, Omer Onar, Alireza Khaligh and Erik Schaltz*Design and Control of a Multiple Input DC/DC Converter for Battery/Ultra-capacitor Based Electric Vehicle Power System*Department of Energy Technology, Aalborg University, Aalborg, Denmark.

[15] Orestes Anastasia, Nancy Checklick, Vivianne Couts, Julie Doherty, Jette Findsen, Laura Gehlin, and Josh Radoff . *Battery-Powered Electric and Hybrid Electric Vehicle Projects to Reduce Greenhouse Gas Emissions.* Science Applications International Corporation (SAIC)-Climate Change Services.

[16] Electropedia. *Battery and Energy Technologies.* Available from: http://www.mpoweruk.com/leadacid.htm.

[17] Tom Bartley ISE Corporation.*Ultracapacitors and Batteries for Energy Storage in Heavy-Duty Hybrid- Electric Vehicles.* The 22nd International Battery Seminar & Exhibit-Cited [March 14 - 17, 2005].

[18] Sonnenschein A512/40 A* datasheet

[19] MC BMOD Energy Series 16v BOOSTCAP Ultracapacitor Modules

[20] Andrew C. Baisden, Student Member, IEEE and Ali Emadi. ADVISOR-Based Model of a Battery and an Ultra-Capacitor Energy Source for Hybrid Electric Vehicles.

[21] Leon C. Rosario, Patrick C.K.Luk.IMPLEMENTATION OF A MODULAR POWER AND ENERGY MANAGEMENT STRUCTURE FOR BATTERY - ULTRACAPACITOR POWERED ELECTRIC VEHICLES. Cranfield University -Defence College of Management and Technology

A
Appendix A

Parameters calculation for the converter

The parameters are calculated for the boost mode and the buck mode. Between both cases, are choosen the more restrictive. The prototype is rated to a power of 20 Kw. The voltage of the batteries and the ultra-capacitor are taken from the prototype used in Aalborg university.

Boost mode parameters

The maximum output current can be calculated from next Equ. A.1:

$$I_{load_{max}}(A) = \frac{P_{out_{max}}(W)}{V_{out}(V)} = \frac{2000}{136} = 14.7A \tag{A.1}$$

In order to run the simulations and for laboratory test, the proper resistive load is calculated:

$$R_L(\Omega) = \frac{Vo^2(V)}{P_{out}(W)} = \frac{136^2}{2000} = 9.25\Omega \tag{A.2}$$

The duty cycles for the steady state in this working mode are:

$$D_{uc} = 1 - \frac{V_{uc}}{Vo} = 1 - \frac{64}{136} = 0.52 \tag{A.3}$$

$$D_{batt} = 1 - \frac{V_{batt}}{Vo} = 1 - \frac{48}{136} = 0.64 \tag{A.4}$$

$$\Delta Vo = 5\% = 6.8V. \tag{A.5}$$

When the converter is working in boost mode, to calculate the inductance, is has to be used the duty cycle obtained when the input source are the ultra-capacitors.

$$L = \frac{Ts \cdot Vo \cdot D_{uc} \cdot (1 - D_{uc})^2}{2 \cdot Io} = \frac{\frac{1}{15000} \cdot 136 \cdot 0.52(1 - 0.52)^2}{2 \cdot 15} = 36\mu H \tag{A.6}$$

To calculate the capacitor, the one obtained when the input source for the converter is the battery.

$$C_{out} = \frac{Io \cdot D_{batt} \cdot Ts}{\Delta Vo} = \frac{15 \cdot 0.64\frac{1}{15000}}{0.8} = 94\mu F \tag{A.7}$$

Buck mode parameters

In this mode of operation, the parameters of the components are calculated when the output voltage is the required for charging the battery.
The duty cycle in the steady state for this working conditions is:

$$D = \frac{57}{136} = 0.42 \tag{A.8}$$

For charging the battery, it is required a low ripple, as for example 1%:

$$\Delta Vo = 1\% = 0.57V. \tag{A.9}$$

Therefore, the inductance and capacitor value can be calculated:

$$L = \frac{D \cdot Ts \cdot (Vin - Vo)}{2 \cdot Io} = \frac{0.42 \cdot \frac{1}{15000} \cdot (136 - 57)}{2 \cdot 5} = 218\mu H \tag{A.10}$$

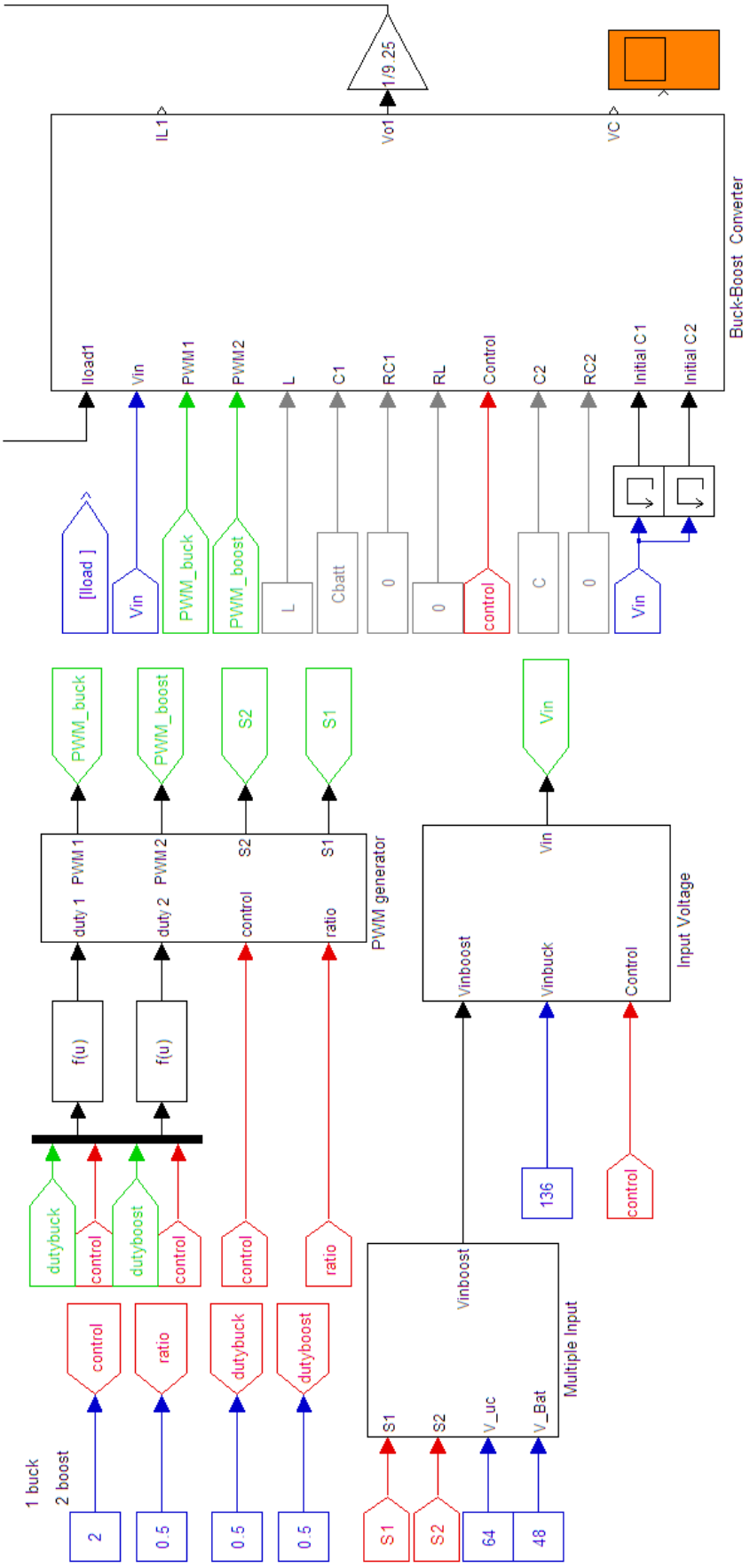
$$C_{batt} = \frac{Ts \cdot Vo \cdot (1 - D) \cdot Ts}{8 \cdot \Delta Vo \cdot L} = \frac{\frac{1}{15000}^2 \cdot 57 \cdot (1 - 0.42)}{8 \cdot 0.57 \cdot 218 \cdot 10^{-6}} = 149\mu F \tag{A.11}$$

The choosen values are L=218μ H, output capacitor in buck mode, C_{obuck}=149 μ F and output capacitor in boost mode, C_{oboost}=94 μ F.
This parameters assure the CCM of the converter.

B
Appendix B

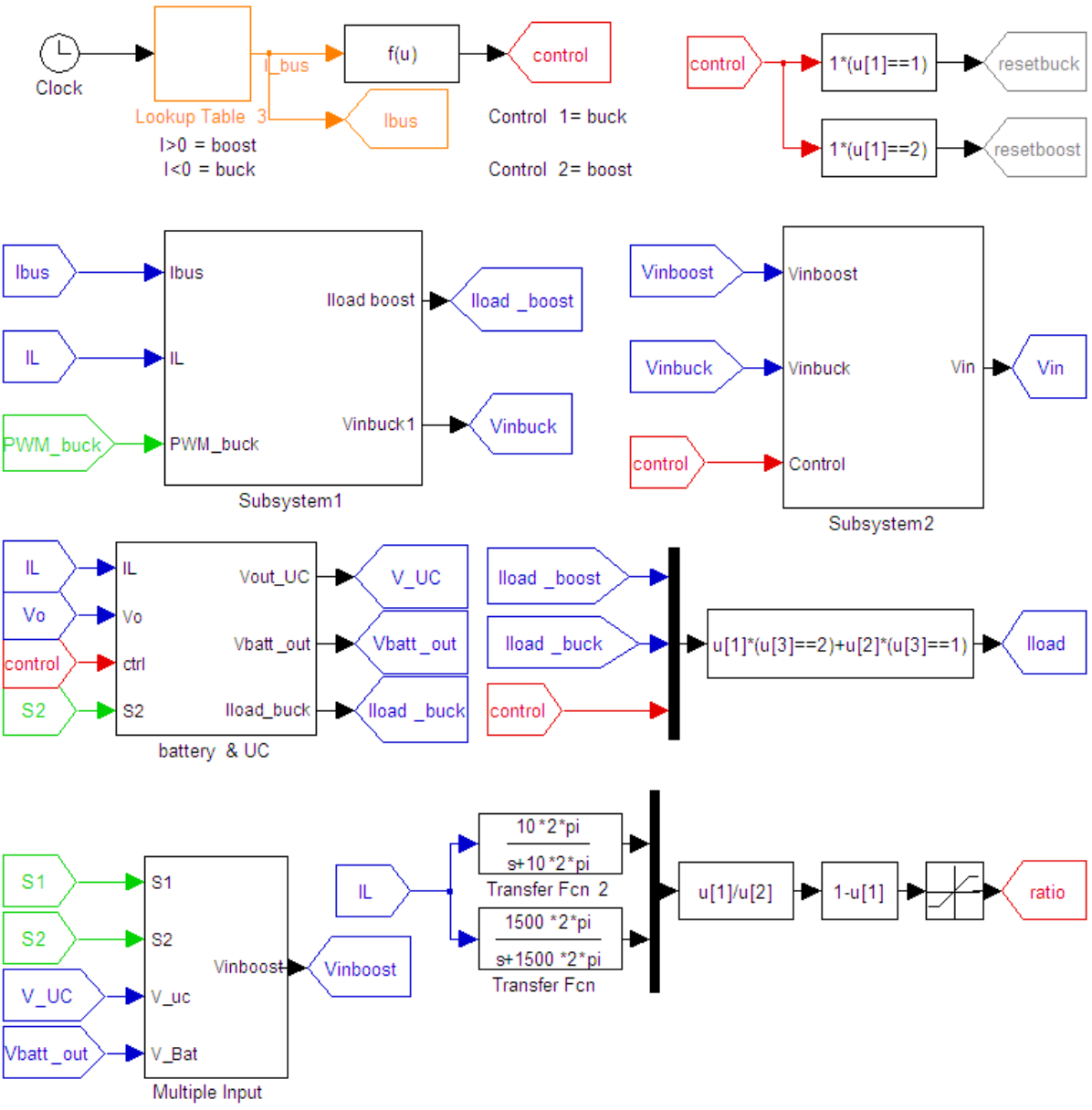
```
%Initialization file for the  simulation:  Multipe-Input-Converter  for  a
%Battery-Ultracapacitor Hybrid Electric Vehicle
%Group PED4-1038A                                    Supervisor: Erik Schaltz
clear all;
clc;

duty=0.5;
fs=15000;           %switching frequency
Ts=1/fs;
Vbus=136;           %Dc bus voltage
Vuc=64              %[V] output voltage of the ultracapacitors
ruc=17e-3           %[Ohms] internal resistance of the ultracapacitors
Cuc=145e-3          %[F]    Capacitor in parallel with the ultracapacitors
Cin_uc=4.7-4        %[F]
Vbatt=48;           %[V] output voltage fo the batteries
Rbatt=4*11e-3;      %[Ohms] internal resistance of the batteries
Cbatt=149e-5;       %[F]  capacitor in parallel with the batteries
L=218e-6;           %[H]  inductance of the converter
rl=0.25             %[Ohms] parasitic resistance of the inductance
C=94e-5             %[F]  Output boost capacitor
rc=0.25             %[Ohms] parasitic resistance of the output capacitor
Ro=9.25;            %[Ohms] Output resistance openlood simulation
%Inductor Current Filter
numfilter=[6000]
denfilter= [1 6000]
filter=tf(numfilter,denfilter)
%Battery control
K=0.0014;
Q=1;
A=0.111;
B=2.3;
```

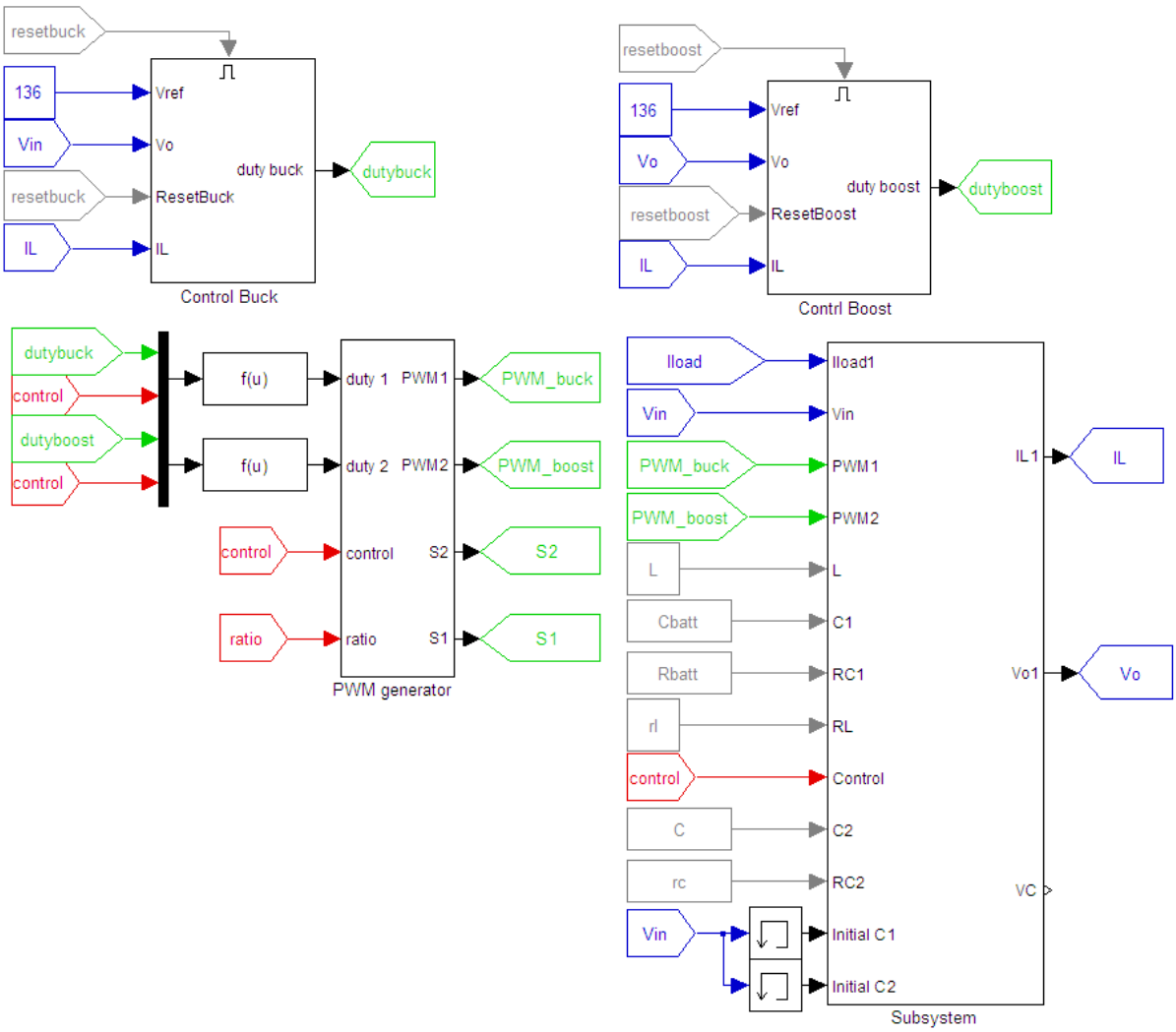
C
Appendix C


1/9.25
IL1
Vo1
VC
Buck-Boost Converter
Iload1
Vin
PWM1
PWM2
L
C1
RC1
RL
Control
C2
RC2
Initial C1
Initial C2
[Iload]
PWM_buck
PWM_boost
Cbatt
0
C
PWM generator
duty 1
duty 2
control
ratio
f(u)
dutybuck
dutyboost
Input Voltage
Vinboost
Vinbuck
136
Multiple Input
S1
S2
V_uc
V_Bat
64
48
1 buck
2 boost
2
0.5

D

Appendix D


Clock
Lookup Table 3
I>0 = boost
I<0 = buck
I_bus
Ibus
f(u)
control
Control 1= buck
Control 2= boost
control
1*(u[1]==1)
resetbuck
1*(u[1]==2)
resetboost
Ibus
IL
PWM_buck
Ibus
IL
PWM_buck
Iload boost
Vinbuck1
Iload _boost
Vinbuck
Subsystem1
Vinboost
Vinbuck
control
Vinboost
Vinbuck
Control
Vin
Vin
Subsystem2
IL
Vo
control
S2
IL
Vo
ctrl
S2
Vout_UC
Vbatt _out
Iload_buck
V_UC
Vbatt _out
Iload _buck
battery & UC
Iload _boost
Iload _buck
control
u[1]*(u[3]==2)+u[2]*(u[3]==1)
Iload
S1
S2
V_UC
Vbatt _out
S1
S2
V_uc
V_Bat
Vinboost
Vinboost
Multiple Input
IL
10*2*pi
s+10*2*pi
Transfer Fcn 2
1500 *2*pi
s+1500 *2*pi
Transfer Fcn
u[1]/u[2]
1-u[1]
ratio


resetbuck
136
Vin
resetbuck
IL
Vref
Vo
duty buck
ResetBuck
IL
dutybuck
Control Buck
resetboost
136
Vo
resetboost
IL
Vref
Vo
duty boost
ResetBoost
IL
dutyboost
Contrl Boost
dutybuck
control
dutyboost
control
f(u)
f(u)
control
ratio
duty 1
duty 2
control
ratio
PWM1
PWM2
S2
S1
PWM_buck
PWM_boost
S2
S1
PWM generator
Iload
Vin
PWM_buck
PWM_boost
L
Cbatt
Rbatt
rl
control
C
rc
Vin
Iload1
Vin
PWM1
PWM2
L
C1
RC1
RL
Control
C2
RC2
Initial C1
Initial C2
IL1
Vo1
VC
IL
Vo
Subsystem

Appendix E

```
//MULTIPLE-INPUT-CONVERTER FOR A BATTERY-ULTRACAPACITOR HYBRID ELECTRIC VEHICLE

//GROUP PED4-1038A  Supervisor: Erick Schaltz
//                                        date:30/05/2009



//                                !!!ATENTION!!!
//This program  is  made  to  run  the  version  of the  converter V.1 and it has
//NO CONTROL implemented, therfore, some external device must be used to limit
// the currents and the voltages.



//  Used variables:

//  PWM variables:
// period
//  duty1a
//  duty1b
//  duty2a
//  duty2b
//  duty3a
//  duty3b

//  Analog to Digital conversions:
// SampleTable1[20]
//  SampleTable2[20]
//  SampleTable3[20]
//  SampleTable4[20]

#include "DSP28x_Project.h"     // Device Headerfile and Examples Include File

// Prototype statements for functions found within this file.
```

```
void InitEPwm1Example(void);
void InitEPwm2Example(void);
void InitEPwm3Example(void);
interrupt void epwm1_isr(void);
interrupt void epwm2_isr(void);
interrupt void epwm3_isr(void);

void do_adc(void);
// ADC start parameters
#if (CPU_FRQ_150MHZ)     // Default - 150 MHz SYSCLKOUT
  #define ADC_MODCLK 0x3 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2=150/(2*3)=25.0 MHz
#endif
#if (CPU_FRQ_100MHZ)
  #define ADC_MODCLK 0x2 // HSPCLK = SYSCLKOUT/2*ADC_MODCLK2=100/(2*2)=25.0 MHz
#endif
#define ADC_CKPS   0x0   // ADC module clock = HSPCLK/1  = 25.5MHz/(1)=25.0 MHz
#define ADC_SHCLK  0x1   // S/H width in ADC module periods       = 2 ADC cycle
#define AVG        1000  // Average sample limit
#define ZOFFSET    0x00  // Average Zero offset
#define BUF_SIZE   20  // Sample buffer size

// Global variables used
Uint16 interrupt1;
Uint16 duty1a;
Uint16 duty1b;
Uint16 duty2a;
Uint16 duty2b;
Uint16 duty3a;
Uint16 duty3b;

Uint16 period;
Uint16 array_index1;
Uint16 i;
// Global variable
float32 SampleTable1[BUF_SIZE];
float32 SampleTable2[BUF_SIZE];
float32 SampleTable3[BUF_SIZE];
float32 SampleTable4[BUF_SIZE];


void main(void)
{
// Step 1. Initialize System Control:
// PLL, WatchDog, enable Peripheral Clocks
// This example function is found in the DSP2833x_SysCtrl.c file.
```

```
   InitSysCtrl();
// Specific clock setting for this example:
  // EALLOW;
  // SysCtrlRegs.HISPCP.all = ADC_MODCLK; // HSPCLK = SYSCLKOUT/ADC_MODCLK
  // EDIS;
// Step 2. Initalize GPIO:
// This example function is found in the DSP2833x_Gpio.c file and
// illustrates how to set the GPIO to it's default state.
// InitGpio();  // Skipped for this example

// For this case just init GPIO pins for ePWM1, ePWM2, ePWM3
// These functions are in the DSP2833x_EPwm.c file
   InitEPwm1Gpio();
   InitEPwm2Gpio();
   InitEPwm3Gpio();

// Step 3. Clear all interrupts and initialize PIE vector table:
// Disable CPU interrupts
   DINT;

// Initialize the PIE control registers to their default state.
// The default state is all PIE interrupts disabled and flags
// are cleared.
// This function is found in the DSP2833x_PieCtrl.c file.
   InitPieCtrl();

// Disable CPU interrupts and clear all CPU interrupt flags:
   IER = 0x0000;
   IFR = 0x0000;

// Initialize the PIE vector table with pointers to the shell Interrupt
// Service Routines (ISR).
// This will populate the entire table, even if the interrupt
// is not used in this example.  This is useful for debug purposes.
// The shell ISR routines are found in DSP2833x_DefaultIsr.c.
// This function is found in DSP2833x_PieVect.c.
   InitPieVectTable();

// Interrupts that are used in this example are re-mapped to
// ISR functions found within this file.
   EALLOW;  // This is needed to write to EALLOW protected registers
   PieVectTable.EPWM1_INT = &epwm1_isr;
   PieVectTable.EPWM2_INT = &epwm2_isr;
   PieVectTable.EPWM3_INT = &epwm3_isr;
   EDIS;    // This is needed to disable write to EALLOW protected registers
```

```
// Step 4. Initialize all the Device Peripherals:
// This function is found in DSP2833x_InitPeripherals.c
// InitPeripherals();  // Not required for this example

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 0;
   EDIS;

   InitEPwm1Example();
   InitEPwm2Example();
   InitEPwm3Example();

   EALLOW;
   SysCtrlRegs.PCLKCR0.bit.TBCLKSYNC = 1;
   EDIS;

// Step 5. User specific code, enable interrupts

// Enable CPU INT3 which is connected to EPWM1-3 INT:
   IER |= M_INT3;

// Enable EPWM INTn in the PIE: Group 3 interrupt 1-3
   PieCtrlRegs.PIEIER3.bit.INTx1 = 1;
   PieCtrlRegs.PIEIER3.bit.INTx2 = 1;
   PieCtrlRegs.PIEIER3.bit.INTx3 = 1;

   InitAdc();         // For this example, init the ADC

// Specific ADC setup for this example:
   AdcRegs.ADCTRL1.bit.ACQ_PS = ADC_SHCLK;// Sequential mode: Sample rate=
//         = 1/[(2+ACQ_PS)*ADC clock in ns]
//         = 1/(3*40ns) =8.3MHz (for 150 MHz SYSCLKOUT)
//         = 1/(3*80ns) =4.17MHz (for 100 MHz SYSC
//If Simultaneous mode enabled: Sample rate=1/[(3+ACQ_PS)*ADC clock in ns]
   AdcRegs.ADCTRL3.bit.ADCCLKPS = ADC_CKPS;
   AdcRegs.ADCTRL3.bit.SMODE_SEL = 0x1;// Setup simultaneous sampling mode
   AdcRegs.ADCTRL1.bit.SEQ_CASC = 1;   // 1  Cascaded mode
  // AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x0;
   AdcRegs.ADCTRL1.bit.CONT_RUN = 1;  // Setup continuous run
   AdcRegs.ADCTRL1.bit.SEQ_OVRD = 0;  // Enable Sequencer override feature

   AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0x2; // Setup conv from ADCINA2
   AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 0x3; // Setup conv from ADCINA3
   AdcRegs.ADCCHSELSEQ1.bit.CONV02 = 0x4; // Setup conv from ADCINA4
```

```
   AdcRegs.ADCCHSELSEQ1.bit.CONV03 = 0x5; // Setup conv from ADCINA5

AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 0x15;
//convert and store in 15 results registers

// Enable global Interrupts and higher priority real-time debug events:
   EINT;   // Enable Global interrupt INTM
   ERTM;   // Enable Global realtime interrupt DBGM

 for (i=0; i<BUF_SIZE; i++)
   {
     SampleTable1[i] = 0;
 SampleTable2[i] = 0;
 SampleTable3[i] = 0;
 SampleTable4[i] = 0;
   }

// Start SEQ1
 AdcRegs.ADCTRL2.all = 0x2000;

array_index1=2;
interrupt1=2;
//period=6666;   //15 khz frequency
//OPEN LOOP FIXED DUTYS

duty1a=0;
duty1b=15000;
duty2a=15050;
duty2b=65000;
duty3a=32000;
duty3b=0;

// Step 6. IDLE loop. Just sit and loop forever (optional):
   for(;;)
   {
//PLACE FOR THE CONTROLS//
       EPwm1Regs.CMPA.half.CMPA = duty1a;
  EPwm1Regs.CMPB = duty1b;

  EPwm2Regs.CMPA.half.CMPA = duty2a;
       EPwm2Regs.CMPB = duty2b;

  EPwm3Regs.CMPA.half.CMPA = duty3a;
       EPwm3Regs.CMPB = duty3b;
```

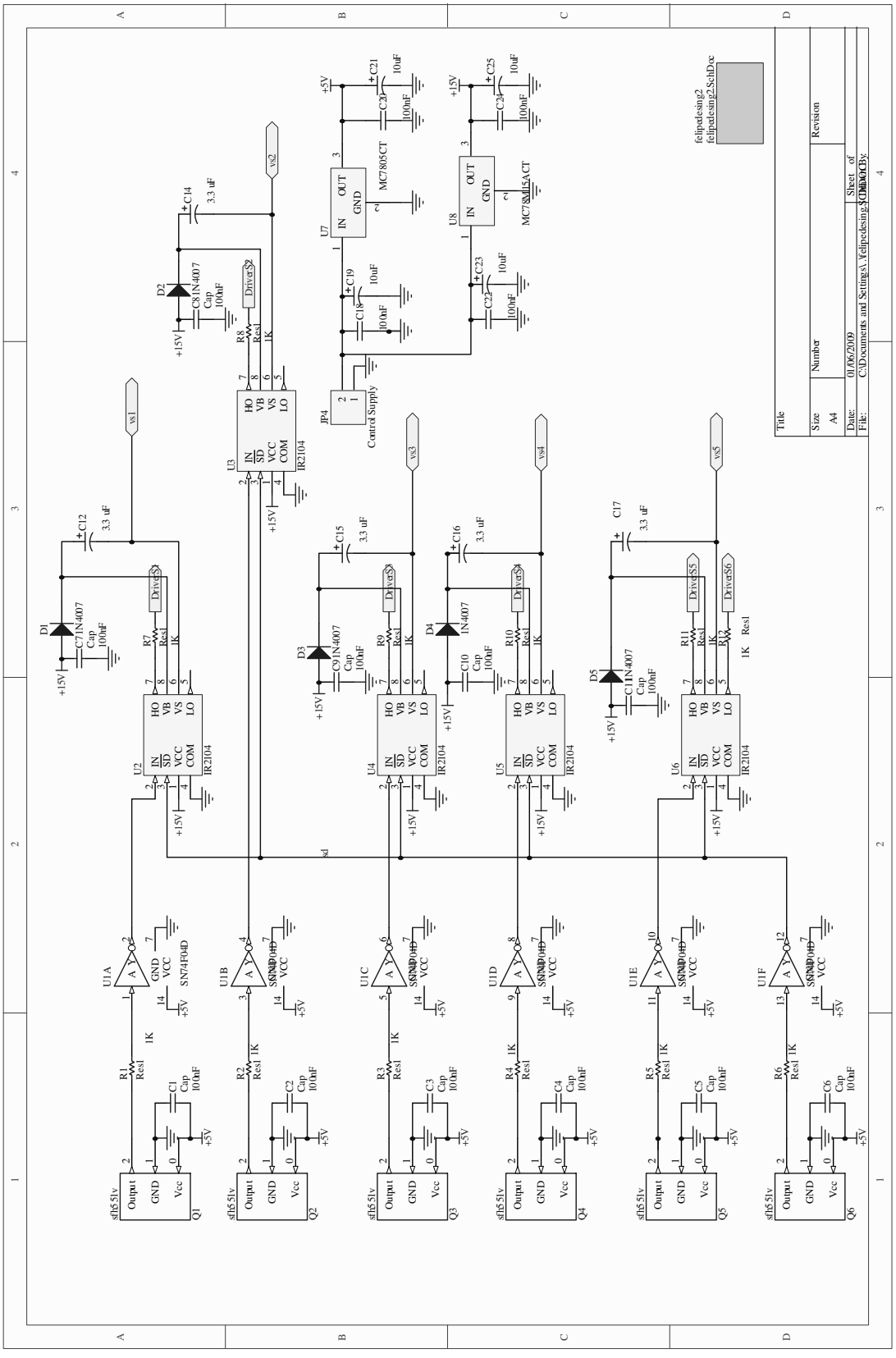
```
       asm("          NOP");
   }

}

interrupt void epwm1_isr(void)
{
interrupt1++;
do_adc();
   // Clear INT flag for this timer
   EPwm1Regs.ETCLR.bit.INT = 1;
   // Acknowledge this interrupt to receive more interrupts from group 3
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;

}
interrupt void epwm2_isr(void)
{
do_adc();
   // Clear INT flag for this timer
   EPwm2Regs.ETCLR.bit.INT = 1;
   // Acknowledge this interrupt to receive more interrupts from group 3
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}

interrupt void epwm3_isr(void)
{
do_adc();
   // Clear INT flag for this timer
   EPwm3Regs.ETCLR.bit.INT = 1;
   // Acknowledge this interrupt to receive more interrupts from group 3
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP3;
}
void InitEPwm1Example()
{
EPwm1Regs.TBPRD =65000;
EPwm1Regs.CMPA.half.CMPA =duty1a; // Compare A = 350 TBCLK counts
EPwm1Regs.CMPB = duty1b; // Compare B = 200 TBCLK counts
EPwm1Regs.TBPHS.half.TBPHS = 0; // Set Phase register to zero
EPwm1Regs.TBCTR = 0; // clear TB counter
EPwm1Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
EPwm1Regs.TBCTL.bit.PHSEN = TB_DISABLE; // Phase loading disabled
EPwm1Regs.TBCTL.bit.PRDLD = TB_SHADOW;
EPwm1Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
EPwm1Regs.TBCTL.bit.HSPCLKDIV = TB_DIV4; // TBCLK = SYSCLKOUT
EPwm1Regs.TBCTL.bit.CLKDIV = TB_DIV4;
```

```
EPwm1Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
EPwm1Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO; // load on TBCTR = Zero
EPwm1Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO; // load on TBCTR = Zero
EPwm1Regs.AQCTLA.bit.CBU = AQ_CLEAR;
EPwm1Regs.AQCTLA.bit.CAU = AQ_SET;
EPwm1Regs.AQCTLB.bit.CBU = AQ_SET;
EPwm1Regs.AQCTLB.bit.CAU = AQ_CLEAR;


EPwm1Regs.ETSEL.bit.INTSEL = ET_CTR_ZERO;     // Select INT on Zero event
EPwm1Regs.ETSEL.bit.INTEN = 1;  // Enable INT
EPwm1Regs.ETPS.bit.INTPRD = ET_1ST;           // Generate INT on 1st event

EPwm1Regs.ETSEL.bit.SOCASEL = 2; // ADCSOCA on TBCTR=TBPRD
EPwm1Regs.ETPS.bit.SOCAPRD = 1; // Generate SOCA on 1st event
EPwm1Regs.ETSEL.bit.SOCAEN = 1; // Enable SOCA generation

}
void InitEPwm2Example()
{
   EPwm2Regs.TBPRD = 65000;
   EPwm2Regs.CMPA.half.CMPA = duty2a;
   EPwm2Regs.CMPB = duty2b;
   EPwm2Regs.TBPHS.half.TBPHS = 0x0000;           // Phase is 0
   EPwm2Regs.TBCTR = 0x0000;                      // Clear counter
   EPwm2Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
   EPwm2Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable phase loading
   EPwm2Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
   EPwm2Regs.TBCTL.bit.HSPCLKDIV = TB_DIV4;       // Clock ratio to SYSCLKOUT
   EPwm2Regs.TBCTL.bit.CLKDIV = TB_DIV4;
   EPwm2Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;    // Load registers every ZERO
   EPwm2Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
   EPwm2Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
   EPwm2Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
   // Set actions
EPwm2Regs.AQCTLA.bit.CBU = AQ_CLEAR;
EPwm2Regs.AQCTLA.bit.CAU = AQ_SET;
EPwm2Regs.AQCTLB.bit.CBU = AQ_SET;
EPwm2Regs.AQCTLB.bit.CAU = AQ_CLEAR;
}
void InitEPwm3Example()
{
   EPwm3Regs.TBPRD = 65000;
   EPwm3Regs.CMPA.half.CMPA = duty3a;
```

```
   EPwm3Regs.CMPB = duty3b;
   EPwm3Regs.TBPHS.half.TBPHS = 0x0000;           // Phase is 0
   EPwm3Regs.TBCTR = 0x0000;                      // Clear counter
   EPwm3Regs.TBCTL.bit.CTRMODE = TB_COUNT_UP;
   EPwm3Regs.TBCTL.bit.PHSEN = TB_DISABLE;        // Disable phase loading
   EPwm3Regs.TBCTL.bit.SYNCOSEL = TB_SYNC_DISABLE;
   EPwm3Regs.TBCTL.bit.HSPCLKDIV = TB_DIV4;       // Clock ratio to SYSCLKOUT
   EPwm3Regs.TBCTL.bit.CLKDIV = TB_DIV4;
   EPwm3Regs.CMPCTL.bit.SHDWAMODE = CC_SHADOW;    // Load registers every ZERO
   EPwm3Regs.CMPCTL.bit.SHDWBMODE = CC_SHADOW;
   EPwm3Regs.CMPCTL.bit.LOADAMODE = CC_CTR_ZERO;
   EPwm3Regs.CMPCTL.bit.LOADBMODE = CC_CTR_ZERO;
   // Set actions
EPwm3Regs.AQCTLA.bit.CBU = AQ_CLEAR;
EPwm3Regs.AQCTLA.bit.CAU = AQ_SET;
EPwm3Regs.AQCTLB.bit.CBU = AQ_SET;
EPwm3Regs.AQCTLB.bit.CAU = AQ_CLEAR;
}
void do_adc()
{
     SampleTable1[0]= (float)( AdcRegs.ADCRESULT0>>4)/1365;//4096 divided by 3
     SampleTable2[0]= (float)( AdcRegs.ADCRESULT2>>4)/1365;
     SampleTable3[0]= (float)( AdcRegs.ADCRESULT4>>4)/1365;
     SampleTable4[0]= (float)( AdcRegs.ADCRESULT6>>4)/1365;
  array_index1++;
  for(i=0;i<BUF_SIZE;i++)
  {
SampleTable1[i+1]=SampleTable1[i];
SampleTable2[i+1]=SampleTable2[i];
SampleTable3[i+1]=SampleTable3[i];
SampleTable4[i+1]=SampleTable4[i];

  }

}

//===========================================================================
// END
//===========================================================================
```

Appendix F

Power board Schematics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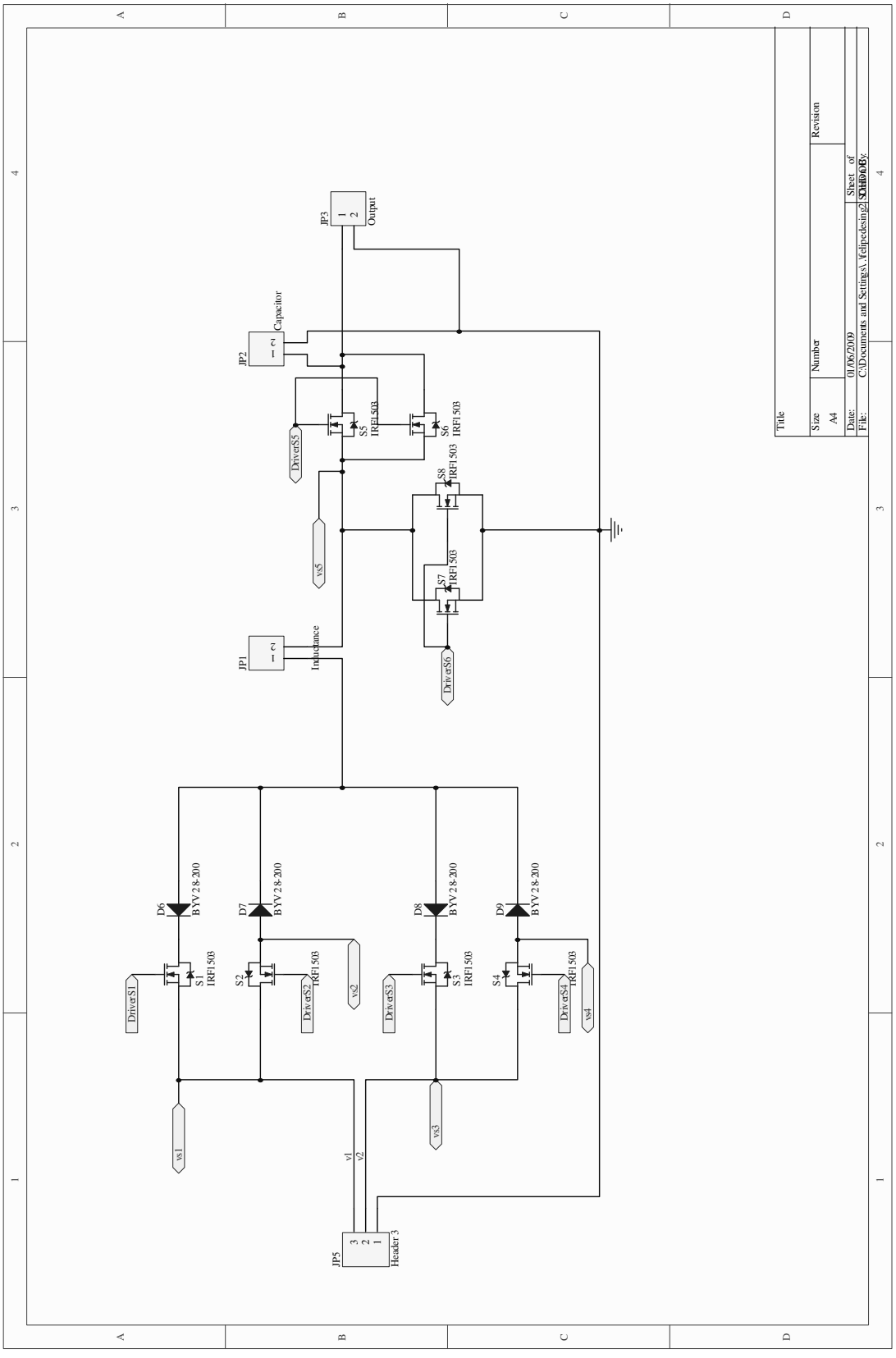
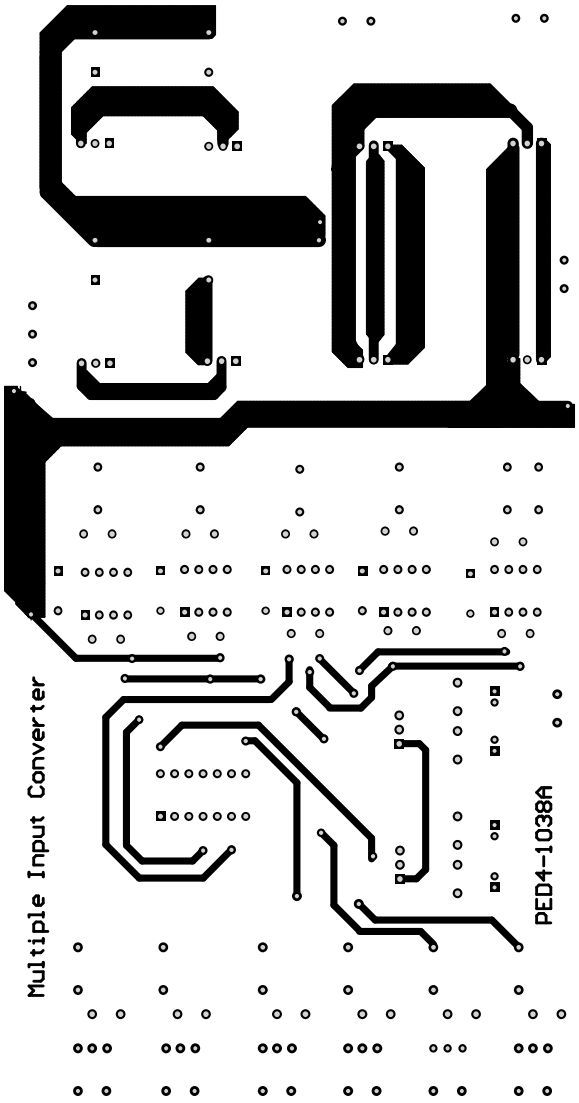
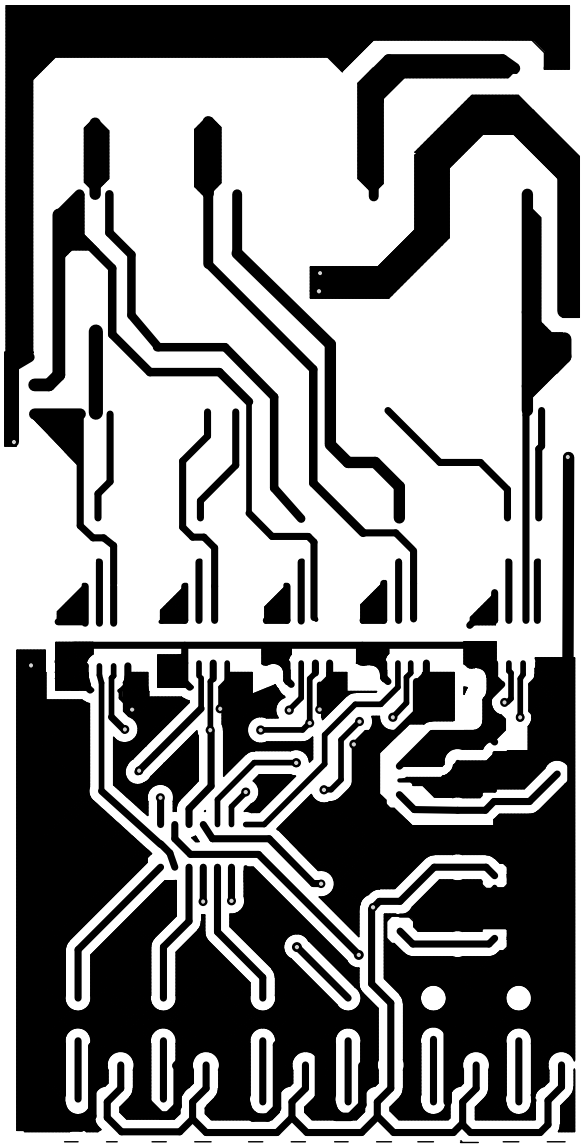
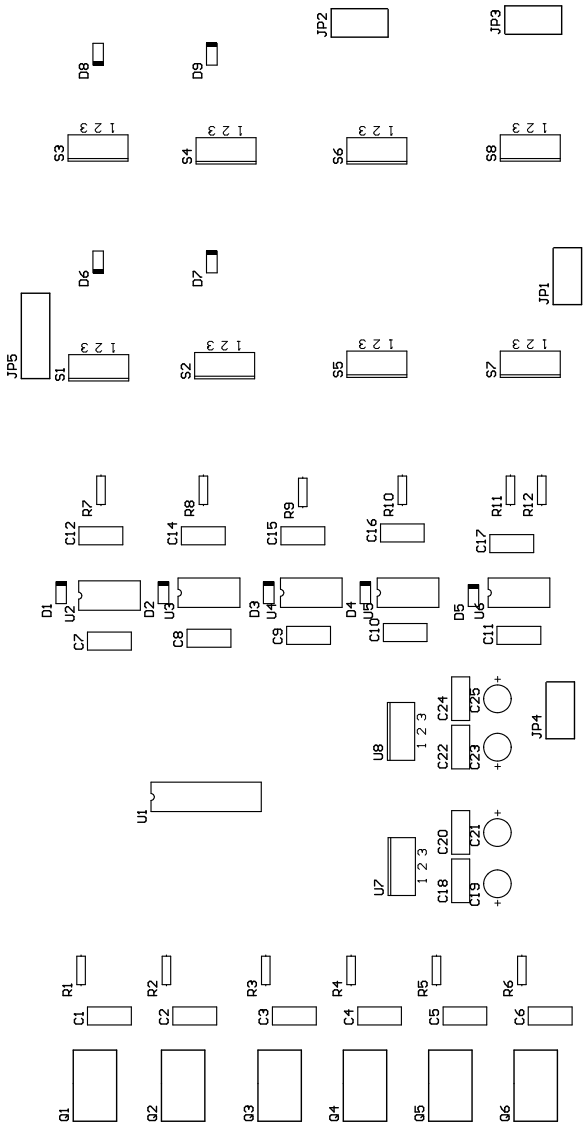
Size A4
Number
Revision
Date: 01/06/2009
File: C:\Documents and Settings\...\felipedesing2.SchDoc
Sheet of
felipedesing2
felipedesing2.SchDoc
Control Supply
IR2104
SN74F04D
MC7805CT
MC7815ACT
1N4007
Res1
Cap
1K
10uF
100nF
3.3 uF
+15V
+5V


JP3
Output
JP2
Capacitor
JP1
Inductance
JP5
Header 3
S1
S2
S3
S4
S5
S6
S7
S8
IRFI 503
D6
D7
D8
D9
BYV 28-200
DriverS1
DriverS2
DriverS3
DriverS4
DriverS5
DriverS6
vs1
vs2
vs3
vs4
vs5
v1
v2
Title
Size
A4
Number
Revision
Date:
01/06/2009
Sheet of
File:
C:\Documents and Settings\ Velipcdesing2\

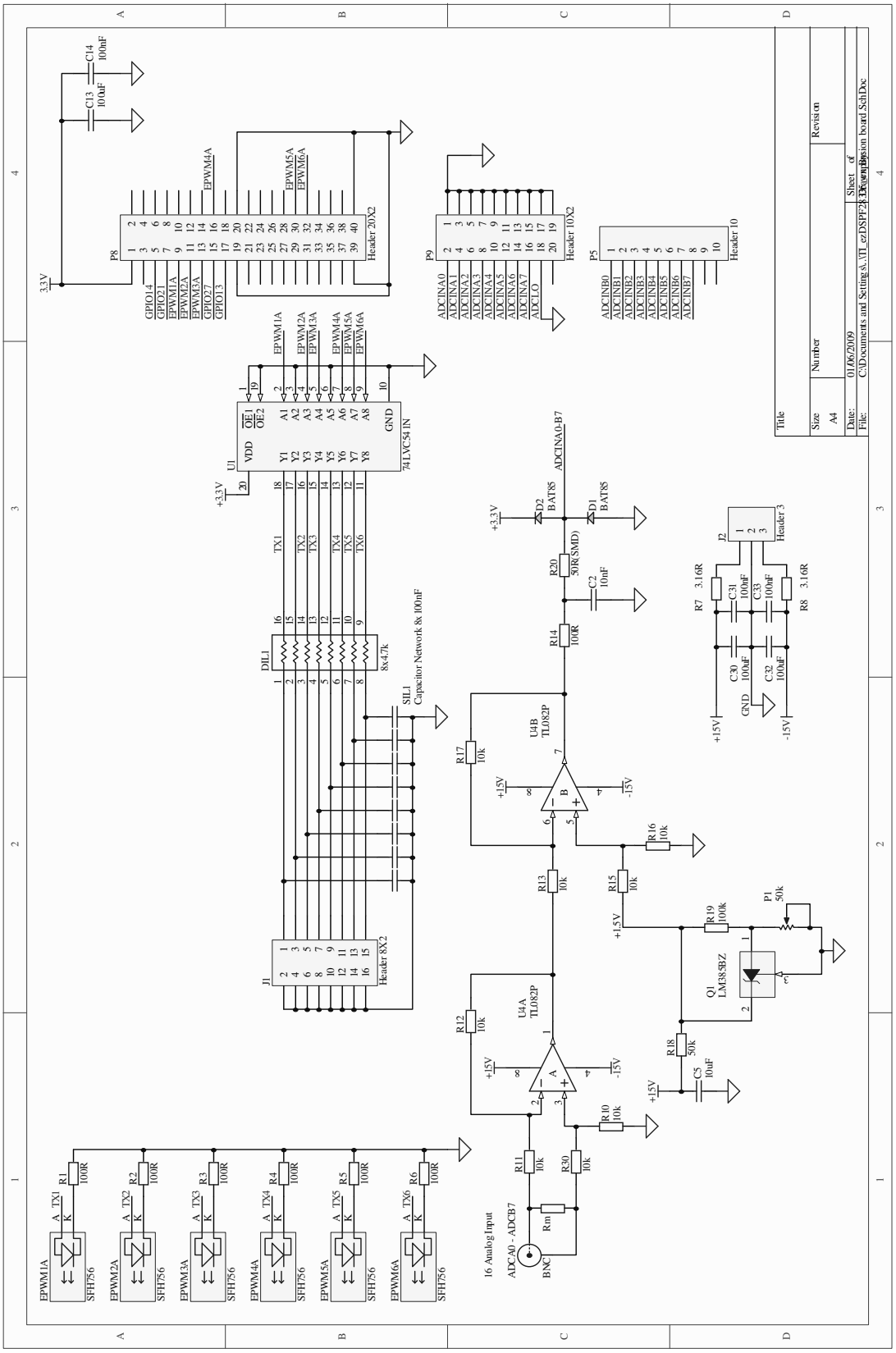
Power board Designs


Multiple Input Converter
PED4-1038A




JP2
JP3
D8
D9
S3
S4
S6
S8
D6
D7
JP1
JP5
S1
S2
S5
S7
R7
R8
R9
R10
R11
R12
C12
C14
C15
C16
C17
D1
D2
D3
D4
D5
U2
U3
U4
U5
U6
C7
C8
C9
C10
C11
U8
C24
C25
JP4
C22
C23
U1
U7
C20
C21
C18
C19
R1
R2
R3
R4
R5
R6
C1
C2
C3
C4
C5
C6
Q1
Q2
Q3
Q4
Q5
Q6

Control Board Schematics


C14 100nF
C13 100uF
3.3V
P8
Header 20X2
EPWM4A
EPWM5A
EPWM6A
GPIO14
GPIO21
EPWM1A
EPWM2A
EPWM3A
GPIO27
GPIO13
P9
Header 10X2
ADCINA0
ADCINA1
ADCINA2
ADCINA3
ADCINA4
ADCINA5
ADCINA6
ADCINA7
ADCLO
P5
Header 10
ADCINB0
ADCINB1
ADCINB2
ADCINB3
ADCINB4
ADCINB5
ADCINB6
ADCINB7
U1
74LVC541N
VDD
GND
TX1
TX2
TX3
TX4
TX5
TX6
+3.3V
ADCINA0-B7
D2 BAT85
D1 BAT85
R20 50R(SMD)
C2 10nF
R14 10R
DIL1
8x4.7k
SIL1
Capacitor Network 8x 100nF
J1
Header 8X2
J2
Header 3
R7 3.16R
R8 3.16R
C31 100nF
C33 100nF
C30 100nF
C32 100nF
+15V
GND
-15V
U4B
TL082P
R17 10k
R16 10k
R13 10k
R15 10k
P1 50k
+1.5V
R19 100k
Q1
LM385BZ
U4A
TL082P
R12 10k
R18 50k
C5 10uF
R10 10k
R11 10k
R30 10k
Rm
16 Analog Input
ADCA0 - ADCB7
BNC
EPWM1A
EPWM2A
EPWM3A
EPWM4A
EPWM5A
EPWM6A
A TX1 K
R1 100R
R2 100R
R3 100R
R4 100R
R5 100R
R6 100R
SFH756
Title
Size
A4
Number
Revision
Date:
01/06/2009
Sheet of
File:
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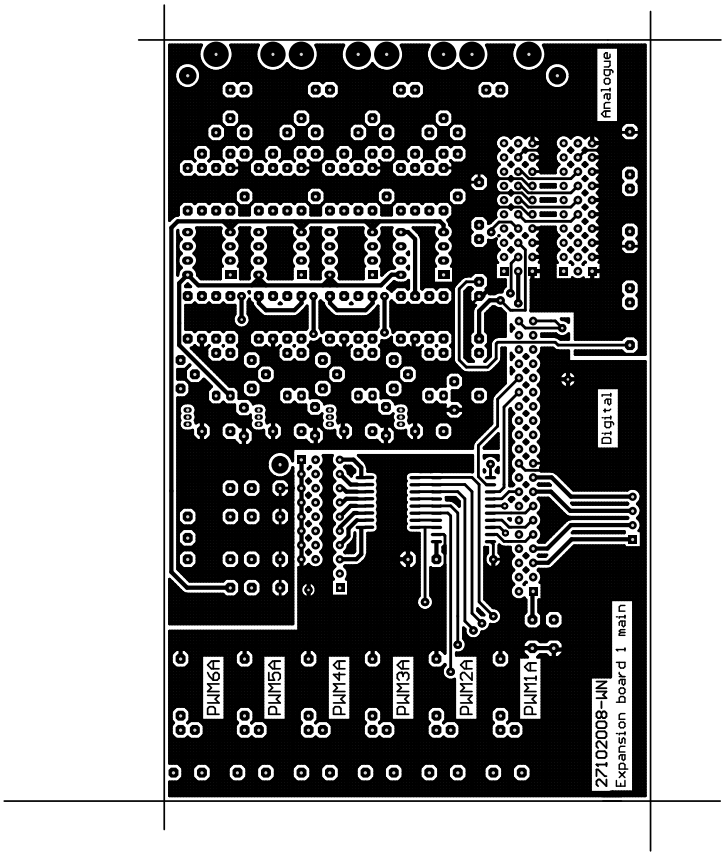
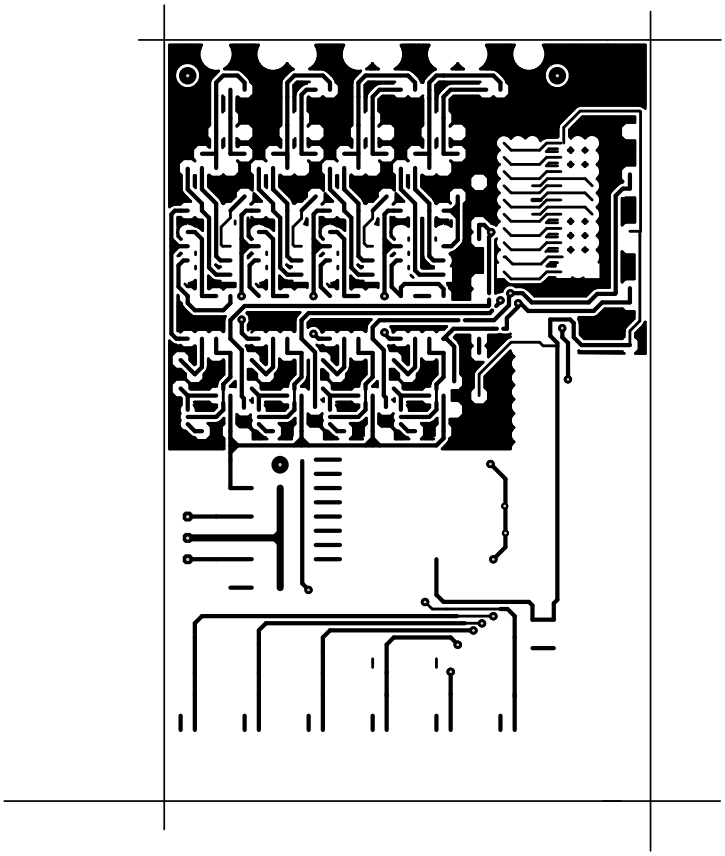
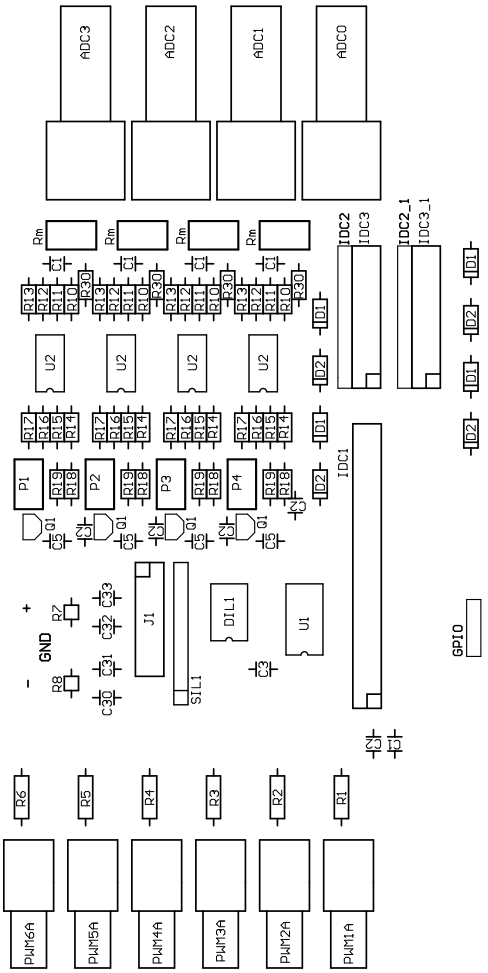
Drawn By:

Control Board Designs


Analogue
Digital
PWM6A
PWM5A
PWM4A
PWM3A
PWM2A
PWM1A
27102008-WN
Expansion board 1 main




ADC3
ADC2
ADC1
ADC0
Rm
C1
R13
R12
R11
R10
R30
U2
R17
R16
R15
R14
P1
P2
P3
P4
R19
R18
Q1
C5
C4
D1
D2
IDC2
IDC3
IDC2_1
IDC3_1
IDC1
J1
SIL1
DIL1
U1
C3
C30
C31
C32
C33
R7
R8
GND
+
-
GPIO
PWM6A
PWM5A
PWM4A
PWM3A
PWM2A
PWM1A
R6
R5
R4
R3
R2
R1

Appendix G

PI parameters for the buck converter mode

$$C = K_p(\frac{K_i s + 1}{s}) \tag{G.1}$$

A.1 Inner loop controller

- $Kp_2 = 3.4$
- $Ki_2 = 0.0042$

A.2 Outer loop controller

- $Kp_1 = 66.66$
- $Ki_1 = 0.015$

PI parameters for the boost converter mode

A.3 Inner control loop

- $Kp_3 = 8$
- $Ki_3 = 0.005$

A.4 Outer control loop

- $Kp_4 = 79.2$
- $Ki_4 = 0.01$