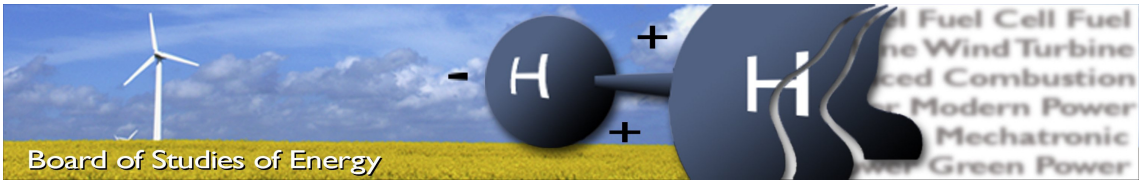
AALBORG UNIVERSITET

INSTITUTE OF ENERGY TECHNOLOGY

A THREE-LEVEL SPACE VECTOR MODULATION STRATEGY FOR TWO-LEVEL PARALLEL INVERTERS

CONDUCTED BY GROUP PED4 1034
SPRING SEMESTER, 2009



Title:	Control of parallel inverters
Semester:	10th semseter - Spring 2008
Semester theme:	Master Thesis
Project period:	04.02.09 to 03.06.09
ECTS:	30
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SYNOPSIS:

This master thesis presents a three-level Space Vector Modulation (SVM) for two parallel connected two-level inverters having the dc supply connected through a dc-link. The proposed three-level strategy is compared to two other exsisting modulation strategies for parallel converters; synchronized pulses and interleaved pulses, and to a three-level SVM for the Neutral Point Clamped (NPC) inverter. A down scaled converter setup is realized in the laboratory. Test results from the setup is compared with simulation results and discussed in the report.

Copies:	5
Pages, total:	99
Appendix:	21
Supplements:	CD-ROM

By signing this document, both members of the group confirms that they participated in the project work and thereby both members are collectively liable for the content of the report.

SUMMARY

This project is continuation of 9th semester project "Control of parallel inverters". In 9th semester project the laboratory test setup has been built, and basic issues connected with system of parallel inverters has been studied.

The main focus of 10th semester project "A THREE-LEVEL SPACE VECTOR MODULATION STRATEGY FOR TWO-LEVEL PARALLEL INVERTERS"is put in different kinds of modulation (pulses synchronized, interleaved pulses and proposed three-level SVM) for the system of parallel connected inverters. The project is divided into five chapter. First - Analytical Study presents the mathematical model of the system together with two-level space vector modulation, three-level space vector modulation and three-level space vector modulation for system of two parallel connected inverters. In this chapter the descripton of three-level NPC inverter is also presented. In next chapter - Simulations, the Matlab/Simulink-PLECS models of the system and NPC inverter are presented. Several measurements have been taken like phase, line-to-line voltages; individual and load currents; dc-link voltage and current. To verify simulation results, the same measurements have been taken in the laboratory. The test setup has been built during 9th semester, and it has been upgraded with new protections (software and hardware) during 10th semester. The DSP program for proposed method has been developed. All the laboratory work is presented in chapter Laboratory experiments. The last chapter - Conclusion contain summary of all gathered data from simulations and laboratory experiments.

The simulation results shows very good performance of proposed modulation method. The Total Harmonic Distortion (THD) of the load current has the smallest value compared to other modulation techniques. Furthermore the voltages are created from the highest number of levels for the proposed method. The laboratory results confirm simulations result only regarding to voltage levels. The THD is the highest value among all methods. This phenomenon can be refered to problem in implementation and hardware.

Preface

This Master thesis is conducted at The Institute of Energy Technology. It is written by group PED4-1034 during the period from 2^{st} of February to 03^{th} of June 2009. The thesis is a continued 9th semester project, which had the title *Control of parallel inverters*.

The purpose of the Master thesis is *to contribute to studentś documentation of his/her obtained skills and the level at which he/she is able to exploit these skills in solving a specified task*.

Reading Instructions

The bibliography is on page 99. Figures are numbered continuously in their respective chapters. For example Fig.2.3 is the third figure in chapter 2. Equations are numbered in the same way as figures - but they are shown in brackets. Appendices, source codes and documents are attached on a CD-ROM. The contents of the CD-ROM is shown in Appendix H.
This report has been written using the LaTeX typesetting system.

Acknowledgements

We would like to thank our supervisor Stig Munk-Nielsen, Associate professor at AAU, and co-supervisor Paul Bach Thøgersen, Manager R&D at KK-Electronics, for their cooperation, kindness, patience and time spent with us. We greatly appreciate their help in guiding us in the right direction for continuing the 9th semester project. We would like to thank our fellow students for the time we have spent together in the University. A special thanks goes out to Anca Julean, who started the project with us in 9th semester. Finally we would like send our greatest thanks to our families for their support and patience with us in this very busy period.

The report is conducted by:

Miłosz Miśkiewicz

Arnstein Johannesen

Contents

List of Figures

LIST OF FIGURES

1 Introduction

This chapter serves as an introduction to the report. The background for the project is explained along with the motivation and constraints for the report. The overall system is presented and the different chapters of the report are described.

1.1 Background

The last decades growth in the production of electric energy from renewable energy sources has led to an increased focus on power electronics. Renewable energy sources like photovoltaic, wind and wave energy are relying on power converters in order to exchange power with the grid. Anyone who wants to produce power for the grid has to make sure that their facilities are complying with national grid codes. The grid codes has strict regulations when it comes to the voltage quality, including limits for rapid voltage variations, flicker and harmonic distortion[1]. Rapid voltage variations and flicker are matters of control of the inverter system, but harmonic distortion is created by the pulse width modulated switching of the converter. Different filters topologies can be used in order to reduce the harmonics generated by the switching action in the converter. However, filters for high power converters can be of substantial size and weight and therefore also of great cost since they are made of several expensive metals. Therefore, a lot of effort is made in order to improve the converter system so that the filter can be reduced while the crid codes and system specifications are still met. There are mainly two ways of reducing the harmonic distortion. One way is to optimize the switching sequence, with harmonics as the most important constraint. Another way is to use several levels to build the fundamental voltage i.e. converters with three levels or more. An example of a multilevel inverter is the Neutral Point Clamped (NPC) inverter. Some of the most favorable benefits from using more levels to build the voltage is: lower du/dt and harmonic distortion, lower common mode voltage and lower switching frequency [2]. Some of the drawbacks of adding more levels to the inverter are increased complexity and the need to balance the voltage in the neutral point of the inverter (NPC). It is important to remember that optimizing for harmonics might very well influence other parameters for the converter, such as switching losses and switching frequency in a negative way. It is always a drawback/benefit issue when optimization is performed on a system.

The current limit for high power IGBT switches is today around 2400A. Demands for inverters with higher current capability and also higher reliability has given interest in parallel converters[3]. The benefit of paralleling inverters are not only increased current and reliability, it also gives the designer the possibility to use interaction between the parallel inverters for reducing the Total Harmonic Distortion (THD). An example of this is interleaving as mentioned in [4][5]. A drawback of having converters connected in

parallel is that the interactions between the converters creates circulating currents[6][7][8] if the dc-link is shared between the inverters. Other drawbacks are: the need for a more advanced control system with additional drive circuits, paralleled converters will have a larger volume than one single converter with the same power rating and must have sharing reactors between the inverters. However, in [4] it is reported that the total inductor volume can be decreased when interleaving is used. Unlike for the NPC inverter there is no need to balance the voltage in the neutral point in the parallel inverters, since this point is not used for two-level inverters. However, there is the need to balance the current in each inverter.

1.2 Project motivation

Fig. 1.1 shows the electrical scheme for a wind turbine power plant, which is the system considered in this project. The power level of the system is 1 to 6 MW. KK-electronics is a company manufacturing power electronics and filters needed for wind power plants. As one of few manufacturers, they are using parallel inverters in the AC-AC converter. Four to six inverters are used in parallel operation. The inverters are mounted next to each other, in contrast to other systems where the distance between the inverters can be several hundred meters, e.g. PV power plants. Usually, all wind turbines over 500 KW have their own transformer, and are connected together by a cable grid. This provides an effective filter against common mode voltages, so only switching frequencies have to be delt with in the LC filter. On the generator side, a du/dt filter is applied. At startup for the generator, the windings have to be magnetized. This is done by supplying the generator from the grid via the inverter. The du/dt filter protects the windings against the PWM voltages from the inverter.

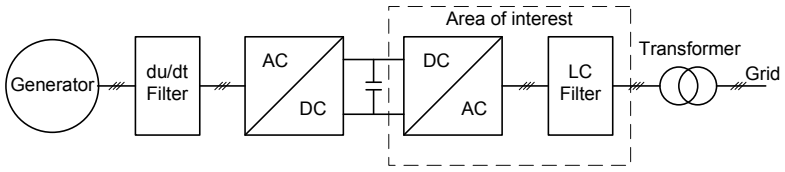
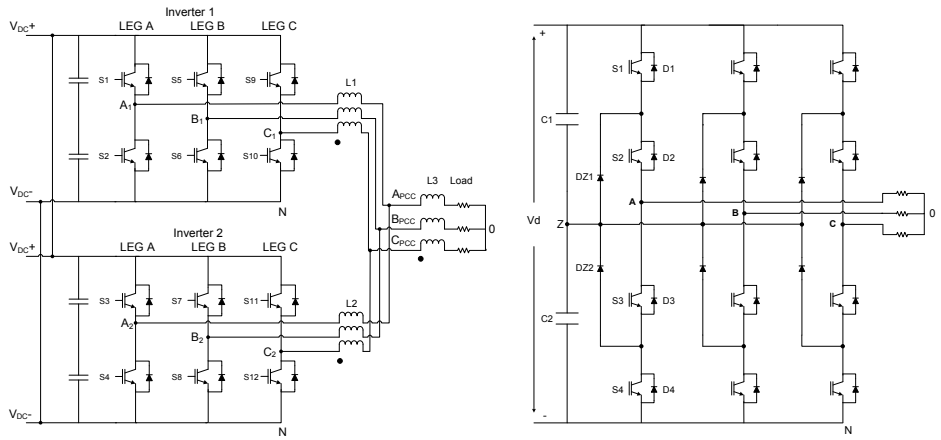


Figure 1.1: *A Wind Power system with area of interest marked.*

Two inverter topologies will be studied in this report, namely parallel connected two-level inverters with shared dc-link and the Neutral Point Clamped inverter (NPC). The first topology will be the main focus, and the NPC will serve as comparison for some simulations and measurements.

The two inverter topologies can be seen in Fig.1.2(a) and Fig.1.2(b).



(a) Two parallel connected two-level inverters with shared dc-link.

(b) Neutral Point Clamped inverter.

Figure 1.2: *The two different topologies*

The NPC depicted is a three-level inverter. This report will investegate the possibility to treat the parallel connected two-level inverters as one three-level inverter.

1.3 Project limitation

In Fig.1.1 the area of interest is marked. Only the inverter (DC-AC) and part of the filter will be dealt with, and the grid will be simplified by a load. The project will not deal with the problems of grid connection. The aim of the project is on the comparison of the produced harmonics from the different inverter topologies. The same filter will be used for all experiments, in order to make a valid comparison. Therefore the filter will not be optimal for some of the inverter topologies, but this will help in distiguishing the different performance of the modulation strategies.

It was not possible to work at the mega watt power level for this project, therefore the project has been downscaled to two 2.2 KW inverters with all the simplifications that this implies. The inverters used in the project have a full bridge diode rectifier to create the DC voltage and a three leg two level IGBT inverter for generating the AC voltage. This means that the power flow can only go in one direction, in contrast to back-to-back inverters which are used in a real size system.

The current in the dc-link between the parallel connected inverters will be measured, but not the current in the capacitors for each inverter or the current in the dc supply for each inverter. This is because the inverters from Danfoss gives no possibility to measure the two latter, since the connections for the capacitors and the dc supply are enclosed in the casing and cannot be accessed without dissasembling the inverter.

This report will only deal with Space Vector Pulse Width Modulation (SVPWM) as modulation strategy. There will be no comparison between sine-triangle based modulation strategy or sine-triangle modulation with third harmonic injection strategy. If the reader is interested in the mentioned comparison, an article written by Mr. Fei Wang is recommended [9]. The SVPWM is chosen because of its benefits regarding control, graphical representation of voltage vectors, and the authors previous experience in digital implementation of this strategy.

All models presented and used in this report are discretised. This is done either with setting the sample time for source blocks equal to the period time for the carrier wave or by using the zero-order-hold block. Using discrete models gives a better simulation of the real system which is implemented on a DSP based setup.

1.4 Problem formulation

The problem definition for this master thesis is to study the parallel two-level inverter system and to realize a three level modulation strategy for this system. The realized modulation strategy will be compared to two-level SVM with synchronized pulses, with two-level interleaved SVM and to a three level Neutral Point Clamped (NPC) inverter.

To achieve this, the following goals are stated:

- Study the parallel two level system.
- Modify the three-level Space Vector Modulation strategy so it fits to the parallel two level system.
- Implement the strategy on a DSP in a laboratory setup.
- Compare the proposed system with a three-level NPC inverter in simulation.
- Compare the proposed system with synchronized pulses modulation strategy and interleaved modulation strategy in experiments in the laboratory.

1.5 Overview

The report contains 5 main chapters. It begins with an introduction chapter which describes the background for the project as well as the motivation, formulation and limitations. Chapter 2 presents a review of the two-level inverter and then proceeds with a study of the parallel inverter topology. Two-level and three-level space vector modulation will be derived. The NPC inverter will also be briefly explained together with the drawbacks and benefits of this inverter. In chapter 3 the simulation for the different modulation strategies will be explained and the results from the different strategies will be

compared to each other. Chapter 4 contains a description of the setup in the laboratory and the comparison for the measurements taken in the laboratory for the different strategies. The conclusion for the report can be found in chapter 5 together with the suggestions for future work. The report ends with Appendix, A to H.

Analytical study

2

This chapter begins with a quick review of the three phase two-level inverter, before explaining a system of two parallel two-level inverters. Interleaving of the two inverters and a three-level modulation strategy is explained. The two-level and three-level Space Vector Modulation (SVM) is derived together with the switching sequences and the calculation of the dwell times. The Neutral Point Clamped (NPC) inverter is presented with its benefits and drawbacks for comparison with the proposed parallel system. The chapter is ended with a conclusion.

2.1 Two-level inverter

The diagram of a three-phase two-level voltage source inverter is depicted in Fig.2.1.

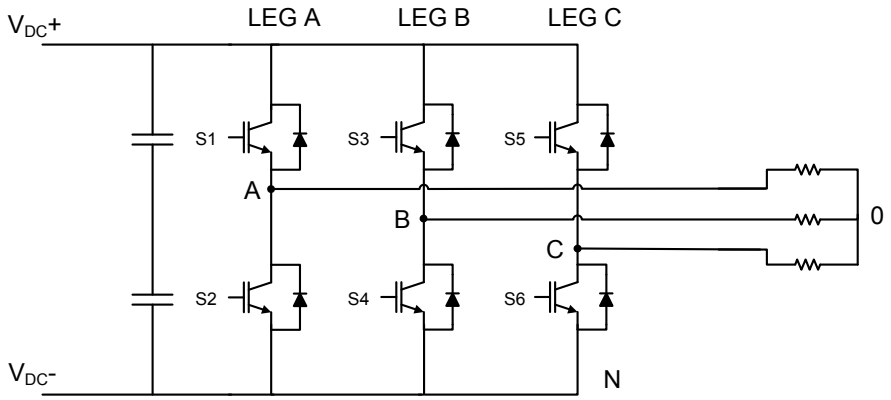


Figure 2.1: *Two-level inverter*

The switches in each inverter leg can have two different states P and O, where P is the upper switch turned on and O is the lower switch turned on. The same state syntax is also used in [10]. The different states for each leg can be seen in table 2.1, and in table 2.2 a more graphical representation of the states is shown.

	Leg A		**Leg B**		**Leg C**	
State	S1	S2	S3	S4	S5	S6
P	1	0	1	0	1	0
O	0	1	0	1	0	1

Table 2.1: *Switching states for a three-phase two-level inverter*

The output of each leg, v_{AN} v_{BN} v_{CN}, depends only on V_{DC} and the switch status. The switches are assumed ideal, meaning that blanking time (also called dead-time) which

States	P			O		
	Leg A	Leg B	Leg C	Leg A	Leg B	Leg C
Upper Switch	1	1	1	0	0	0
Lower Switch	0	0	0	1	1	1

Table 2.2: *State P and O representation*

is implemented in practical circuits is neglected. This leads to the conclusion that the output voltage is independent of the load current since one of the switches in one leg is always on. [11] Assuming balanced operation, the instantaneous line-to-line voltages can be expressed as in equation 2.1.

$$\begin{aligned} v_{AB} &= v_{AN} - v_{BN} \\ v_{BC} &= v_{BN} - v_{CN} \\ v_{CA} &= v_{CN} - v_{AN} \end{aligned} \tag{2.1}$$

where N is the negative dc bus.

Fig.2.2 shows a graphical view of equation 2.1. It can be observed that v_{AN} and v_{AB} will only have two levels, V_{DC} or 0, but the line-to-line voltage, v_{AB} will have three levels, $+V_{DC}$, $-V_{DC}$ and 0.

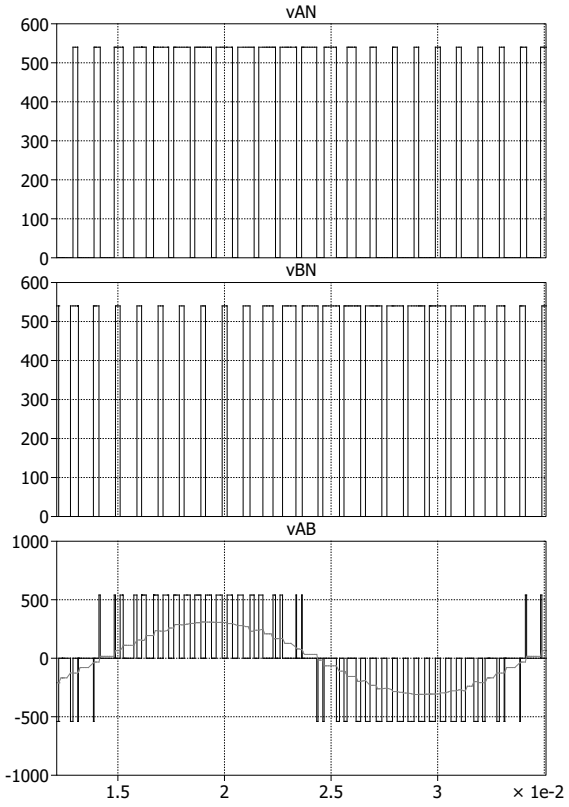


Figure 2.2: *Waveforms from two-level inverter.* f_{SW}*=1000Hz* V_{DC}*=540V* V_{ref}*=180V*

In Fig.2.2 the average value is plotted together with the voltage v_{AB}.

Still assuming balanced operation, the inverter phase output voltages can be expressed as in equation 2.2.

$$\begin{aligned} v_{A0} &= v_{AN} - v_{0N} \\ v_{B0} &= v_{BN} - v_{0N} \\ v_{C0} &= v_{CN} - v_{0N} \end{aligned} \tag{2.2}$$

Where 0 is the star point of the load.

In Fig.2.3 the relationship between v_{AN}, v_{0N} and v_{A0} in Eq.2.2 is presented. It can be observed that the phase voltage v_{A0} will have a maximum amplitude of 2/3 V_{DC}. Looking at v_{A0} it can be seen that there will be 5 different levels present on the phase voltage, namely $\pm$2/3V_{DC}, $\pm$1/3V_{DC} and zero.

In a three phase, three wire system

$$i_A + i_B + i_C = 0 \tag{2.3}$$

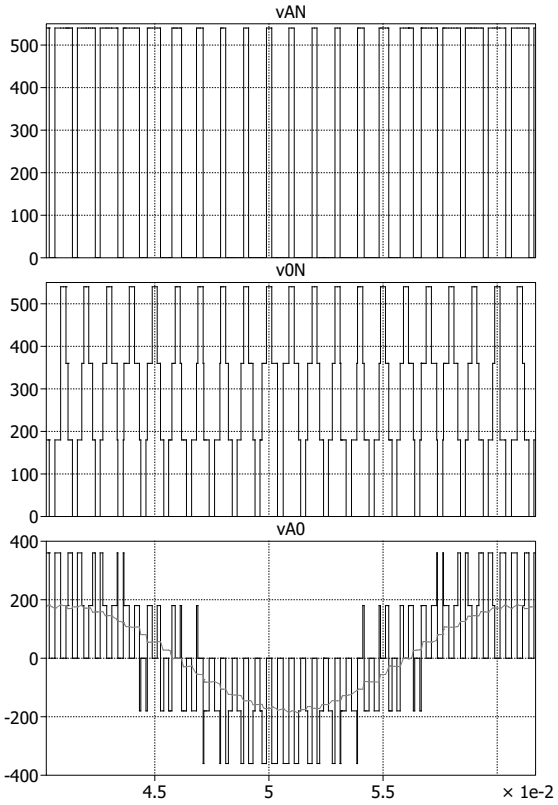


Figure 2.3: *Waveforms from two-level inverter.* f_{SW}*=1000Hz* V_{DC}*=540V* V_{ref}*=180V*

and

$$v_{A0} + v_{B0} + v_{C0} = 0 \tag{2.4}$$

Eq.2.4 is presented in Fig.2.4.

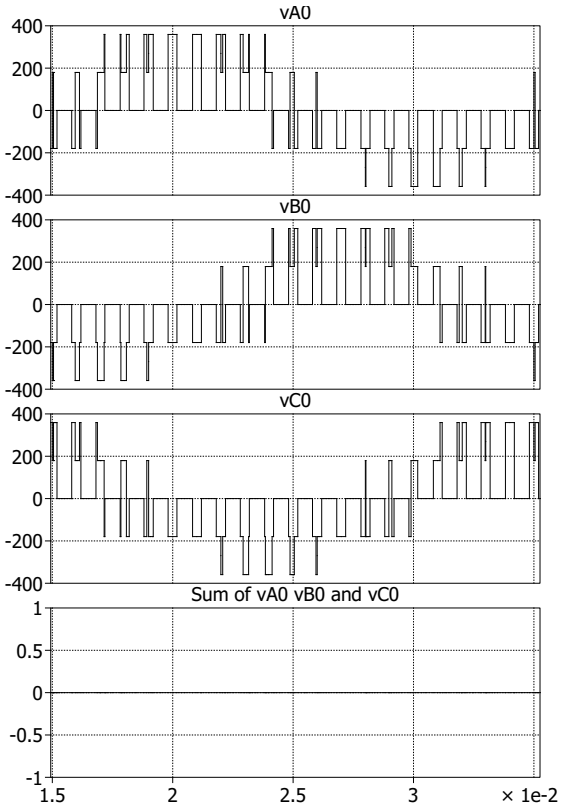


Figure 2.4: *Waveforms from two-level inverter.* f_{SW}*=1000Hz* V_{DC}*=540V* V_{ref}*=180V*

Using Eq.2.2 in Eq.2.4 gives

$$(v_{AN} - v_{0N}) + (v_{BN} - v_{0N}) + (v_{CN} - v_{0N}) = 0 \tag{2.5}$$

This can be simplified to

$$v_{0N} = \frac{v_{AN} + v_{BN} + v_{CN}}{3} \tag{2.6}$$

v_{0N} is generally refered to as the common-mode voltage, and is the voltage that is "common"in all three phases at the specific time.

If Eq.2.6 is used in Eq.2.2 it will give Eq.2.7, an expression of the phase voltage for phase A. Similar equations can be found for phase B and C.

$$v_{A0} = \frac{2}{3}v_{AN} - \frac{1}{3}(v_{BN} + v_{CN}) \tag{2.7}$$

Two-level three-phase inverters are commonly used in applications such as ac motor drives and uninterruptible ac power supplies [11]. However, at high power levels (MW) power quality is an important factor, because the ac filter needed to reduce harmonics will

be of substantial size and therefore a big part of the cost for the whole inverter system. If the harmonics can be reduced by using a different inverter topology, then the filter can also be reduced. Therefore a lot of effort is being made on multilevel inverters that has three or more levels such as the three level Neutral Point Clamped (NPC) inverter. The level count refers to the levels present on v_{xN} where x = A,B and C. By increasing the levels on v_{xN} it is possible to build a fundamental voltage that contains less harmonics.

2.1.1 Space Vector Modulation for two-level Inverter

The parallel converter system contains two two-levels inverters. This allows the use of two-level Space Vector Modulation strategy to each of them. Taking into consideration one of the inverters, the voltage between phase to neutral can have two levels: $P = V_{DC}$, and $O = 0$.

A property of the Space Vector Modulation (SVM) is the fact that it makes sure that the pulses for all three phases are always centered. In other words, the middle point of the pulses for all three phases are the same for one switching period.

Stationary Space Vectors

There are eight different possibilities for switching states, because of the three phase system, Fig. 2.5. The vector representation of the voltages created by switching states is depicted on the Fig. 2.6

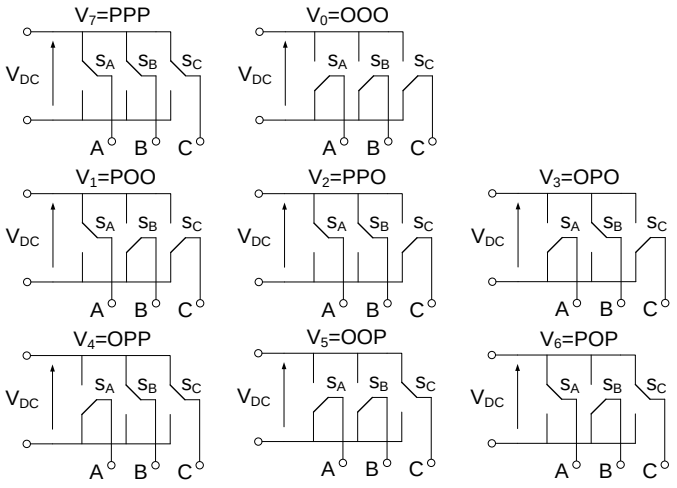


Figure 2.5: *Different switching states of two level inverter.*

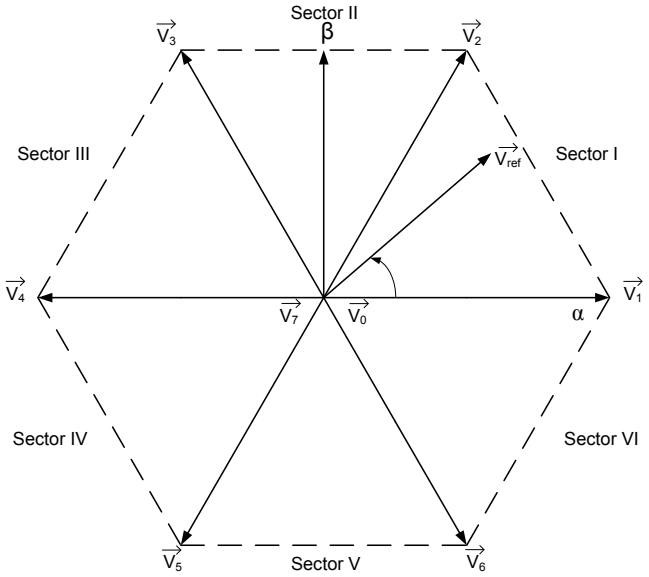


Figure 2.6: *Space vector diagram of two level SVM.*

As it can be observed on the Fig. 2.5 and 2.6 there are six active vectors $\vec{V_1} - \vec{V_6}$ and two zero vectors $\vec{V_0}$ and $\vec{V_7}$ (phase voltage and line-to-line will be zero during their activity[12]).

Space Vector	Switching State	Vector Classification	Vector Magnitude
$\vec{V_0}$	[OOO]	Zero Vector	0
$\vec{V_1}$	[POO]	Active Vectors	$\frac{2}{3}V_{DC}$
$\vec{V_2}$	[PPO]		
$\vec{V_3}$	[OPO]		
$\vec{V_4}$	[OPP]		
$\vec{V_5}$	[OOP]		
$\vec{V_6}$	[POP]		
$\vec{V_7}$	[PPP]	Zero Vector	0

Table 2.3: *Voltage vectors created from different combination of the switches*

The active vectors divides the plane into six sectors. The combination of vectors which should be used to synthetize $\vec{V_{ref}}$ is based on position of $\vec{V_{ref}}$.

Dwell Times

The dwell times are the times for which each of the state space vectors is utilized.

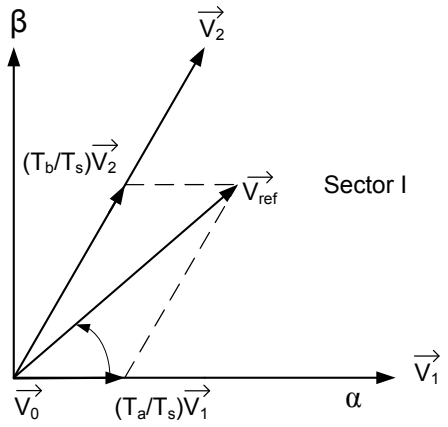


Figure 2.7: $\vec{V_{ref}}$ *representation in sector I.*

The dwell times calculation is based on 'the volt-second balancing' principle[10][12], which says that the product of the reference vector and sampling period is equal to the sum of the three nearest space vectors, each multiplied by the period of their extend. E.g: $\vec{V_1}$, $\vec{V_2}$ and $\vec{V_0}$ are used when $\vec{V_{ref}}$ is in sector I:

$$\vec{V_1}T_a + \vec{V_2}T_b + \vec{V_0}T_0 = \vec{V_{ref}}T_s \tag{2.8}$$

where:

$$\vec{V_1} = \frac{2}{3}V_{DC}; \qquad \vec{V_2} = \frac{2}{3}V_{DC}e^{j\frac{\pi}{3}}; \qquad \vec{V_0} = 0 \tag{2.9}$$

Using 2.9 in 2.8 and splitting into real and imaginary parts:

- Real

$$\frac{2}{3}T_a + \frac{1}{3}T_b = \frac{V_{ref}}{V_{DC}}cos(\theta)T_s \tag{2.10}$$

- Imaginary

$$\frac{1}{\sqrt{3}}T_b = \frac{V_{ref}}{V_{DC}}sin(\theta)T_s \tag{2.11}$$

Together with:

$$T_a + T_b + T_0 = T_s \tag{2.12}$$

set of equations (2.10, 2.11 and 2.12) can be created to calculate dwell times: T_a, T_b, T_0:

$$T_a = \frac{\sqrt{3}T_s V_{ref}}{V_{DC}} sin(\frac{\pi}{3} - \theta) \tag{2.13}$$

$$T_b = \frac{\sqrt{3}T_s V_{ref}}{V_{DC}} sin(\theta) \tag{2.14}$$

$$T_0 = T_s - T_a - T_b \tag{2.15}$$

Switching Sequence

By choosing the three nearest vectors to create $\vec{V_{ref}}$ it is possible to minimize the harmonic content of the switched waveforms . The main problem is how to put them in collation during switching period to minimize switching transitions and optimize the harmonic profile of the output voltage[13][14]. For two and three level inverters, Space Vector Modulation with seven-segment switching sequence is widely used. There are two main requirements when designing switching sequence according to [15][10][12]:

- Zero or minimum changes in switching are desirable when the reference vector $\vec{V_{ref}}$ is passing from one sector to another.
- Only two switches in the same leg are involved when passing from one switching state to another in order to reduce device switching frequency.

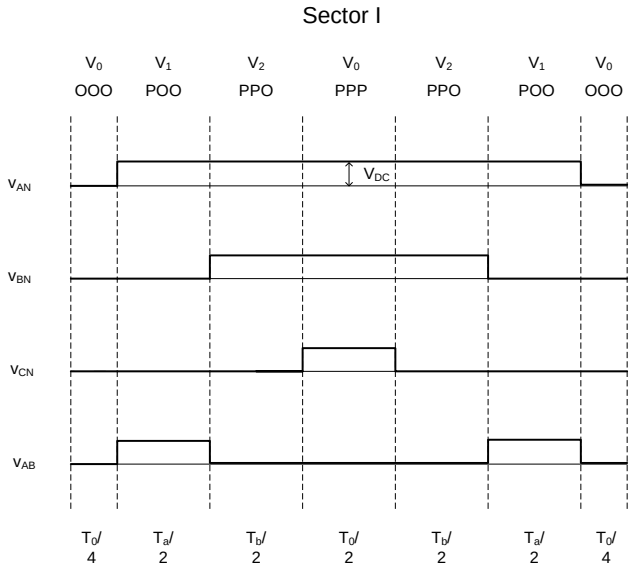


Figure 2.8: *Switching pattern when $\vec{V_{ref}}$ is placed in sector I.*

2.2 Two-level inverters in parallel

The demand for inverters with high current capability and also high reliability has given interest in parallel inverters[3]. Two two-level inverters connected in parallel can be represented as in Fig.2.9. If the two inverters together with L1 and L2 are concidered ideal and are recieving identical PWM signals containing only O and P state then

$$v_{A1N} = v_{A2N}, \qquad v_{B1N} = v_{B2N}, \qquad v_{C1N} = v_{C2N} \tag{2.16}$$

Thus

$$v_{A10} = v_{A20}, \qquad v_{B10} = v_{B20}, \qquad v_{C10} = v_{C20} \tag{2.17}$$

Eq.2.1 and Eq.2.2 are still valid since they will be the same as if only one inverter were used, and can be represented as in Eq.2.18 and Eq.2.19. With the introduction of an inverter in parallel, there are now three reference points: 1, 2 and pcc. The topology for parallel inverters with reference points used in Eq.2.18 and Eq.2.19 is shown in Fig.2.9.

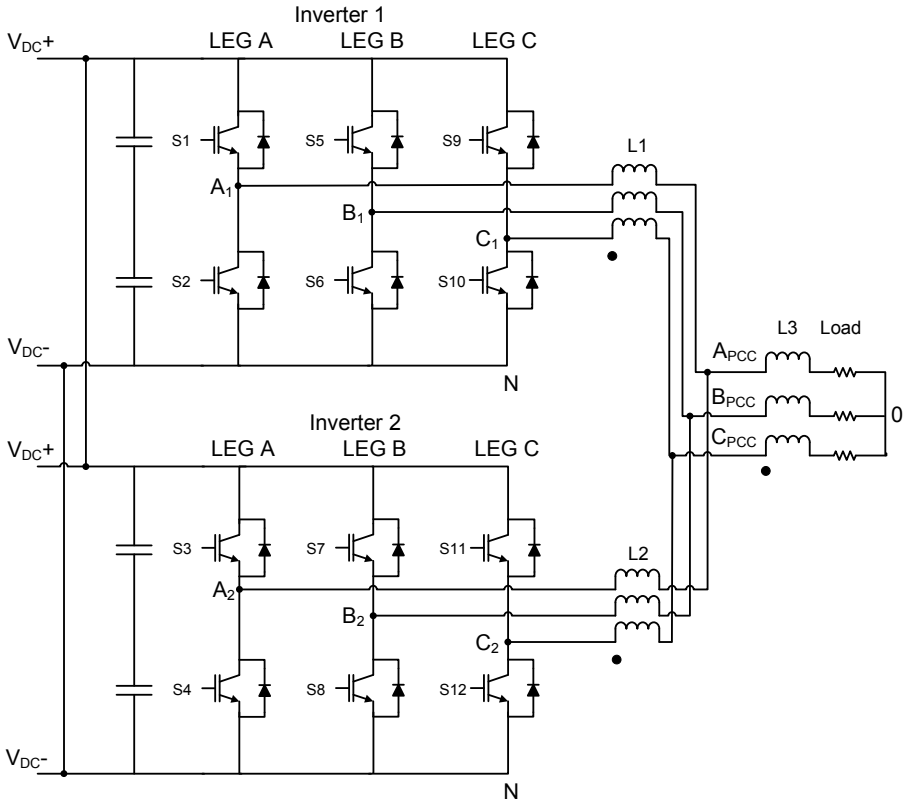


Figure 2.9: *Two-level inverters in parallel operation*

$$
\begin{aligned}
v_{AkB} &= v_{AkN} - v_{BkN} \\
v_{BkC} &= v_{BkN} - v_{CkN} \\
v_{CkA} &= v_{CkN} - v_{AkN}
\end{aligned}
\tag{2.18}
$$

$$
\begin{aligned}
v_{Ak0} &= v_{AkN} - v_{0N} \\
v_{Bk0} &= v_{BkN} - v_{0N} \\
v_{Ck0} &= v_{CkN} - v_{0N}
\end{aligned}
\tag{2.19}
$$

$$(k = 1, 2, pcc)$$

If the two inverters are recieving synchronized (identical) PWM signals, the current capability for the system is increased compared to one inverter. However, the harmonics and current ripple are the same as having one inverter with the same current capability as the parallel system.

A drawback of paralleling inverters is the interaction that will occur between the inverters and create a current that will circulate from one inverter to the other through the dc-link [4]. The circulating current is also called zero-sequence current [7] since it occurs because of the opposite zero vectors used (V_0 and V_7) in the switching sequence. In theory one can say that if the impedance for both inverter branches are equal and the duty cycles for both inverters were identical, there would be no interactions between the inverters and thus no circulating currents. However, there will always be a slight difference in the impedance, and if the inverters have separate current controllers the duty cycles can have a small difference. This will allow a current to circulate in the circuit. For high power applications the impedance in the circuit is very low, since the current can reach several thousand amps and any impedance will result in losses in the circuit as a function of the current. Thus a difference in impedance or in pulse width for a high power system will give a bigger circulating current than a system for low power applications.

The low frequency component of the circulating current can be eliminated by a controller located on the zero-axis, as proposed by several articles [6][7][8]. However, it is not possible to reduce the high frequency component of the circulating current with a current controller since the frequency is given by the switching frequency[4]. Since the high frequency component will increase the peak value of the current in each inverter, it will reduce the maximum output current for the parallel inverter system and therefore it will reduce the systems total efficiency. In order to reduce the high frequency component, the impedance between the two inverters is increased by inserting inductors before the inverter‘s output are connected together. The inductors can be seen in Fig.2.9 as L1 and L2.

The case with circulating currents is only true if the dc-link is shared between the inverters. If the dc-link is not shared, no circulating currents will flow in the system. Having the dc supply separate for each inverter module will eliminate the circulating currents, but then a reduction of ripple in the dc current and in the capacitor will not be possible. So by having the dc-link shared, one must accept a high frequency cirulating current in the system, but the dc capacitor can be reduced and will experience lower stresses[4].

The parasitic resistance of an inductor will be constant for all frequencies, but the reactance will increase with increasing frequency. This means that the impedance of the inductor will be higher for higher frequencies. The equation for reactance in an inductor is shown in equation 2.20.

$$X_L = \omega \cdot L = 2 \cdot \pi \cdot f \cdot L \tag{2.20}$$

It can be observed in Eq.2.20 that the reactance X_L changes according to the change of f. This makes an inductor suited for reducing the high frequency components in the current but allow low frequency components to pass.

The parallel inverter system inherits the possibility for achieving better performance for the system trough different modulation strategies. This is done solely in the software for the controller and no hardware changes are required from the initial parallel setup shown in Fig.2.9. An interleaved modulation strategy is described in subsection 2.2.1, and a three-level strategy is explained in subsection 2.2.2

2.2.1 Two interleaved two-level inverters

Interleaving inverters has shown that line inductors can be reduced with up to 60% compared to a single two-level inverter, and if the topology is used for reactive power compensation the dc-capacitor can be reduced by 25% [4]. It should be noted that the interleaved inverters will have one three-phase inductor each, while the single two-level inverter circuit will use only one three-phase inductor. Therefore it should be calculated for each case if it is economically viable to use interleaved inverters with respect to cost for the inductors. In [4] it is reported that the total weight and size for two inductors of 3% rated 300 Amps is less than the weight and size for one inductor of 5% rated 600 Amps. In the same article it is also reported that the use of common-mode coils shows promising results with respect to reducing the common-mode signals. Interleaving of inverters is also refered to as pulse shifting or phase shifted gate signals.

When the term of percentage value is used for a inductor, it refers to the percent of voltage drop the inductor will experience compared to the rated voltage when the rated current is passed through the component. For an inverter rated 10 Amps and 230 phase voltage, an inductor of 10mH will give:

$$X_L = \omega \cdot L = 2\pi f \cdot L = 2\pi \cdot 50Hz \cdot 10mH = 3.14\Omega \tag{2.21}$$

The voltage drop

$$V_{DROP} = X_L \cdot I_{RATED} \cdot 100 = 3.14\Omega \cdot 10A \cdot 100 = 31.4V \tag{2.22}$$

This means that the inductor will have a percentage value of:

$$\frac{V_{DROP}}{V_{RATED}} = \frac{31.4V}{230V} = 13.7\% \tag{2.23}$$

By using the percentage value it is easier to relate the size of the inductor to different power levels.

As mentioned in subsection 2.2 the main drawback of paralleling inverters, and especially if they are interleaved, is the problem with circulating currents. When the inverters are interleaved, a conduction path is purposely formed from the output of both inverters through the dc-link.

The general idea of interleaved inverters, is to have the ripple in the current from inverter 2 shifted 180 degrees from the ripple in the current from inverter 1. Since the current on the output is formed by the current from both inverters, the two ripple currents will cancel each other out to a certain amount giving a reduction in the output current ripple. This is shown in Fig.2.10. In [5] it is reported that the cancellation will only be total when the duty cycle is 50%. If the duty cycle has a different value, the ripple will remain in the output current but with a reduced amplitude. Another benefit from interleaving is that the switching frequency seen from the output of the parallel system appears as twice the switching frequency of each inverter. This gives a reduction in the harmonics. On the other side, interleaving will give an increase in the peak current for each inverter and thus lower the total output current. It is therefore a desicion to make between system efficiency and harmonics.

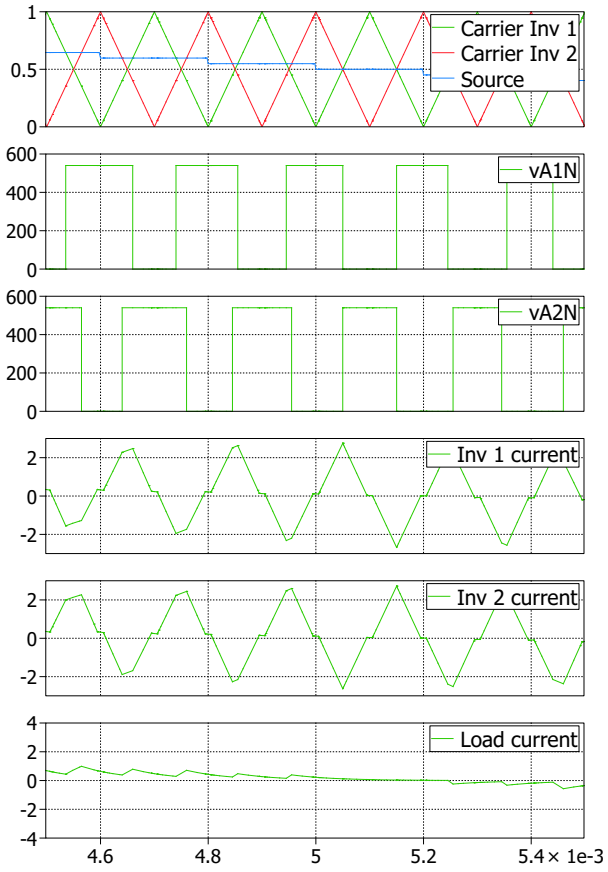


Figure 2.10: *Pulses shifted* $180°$ *by shifting carrier waves (Discretised model).*

The inverters can be interleaved by simply shifting the carrier waves for the PWM for each inverter, so that inverter 2 has carrier waves that are $180°$ shifted compared to the carrier waves for inverter 1. The source signal for both PWM can be the same or it can come from seperate controllers giving an almost identical source signal. As seen in Fig.2.10, the source signal is sampled during the on time for the gate signal for inverter 1. This will lead to a smaller pulse width for inverter 1 than for inverter 2 when the source signal is descending, and opposite when the source signal is ascending. The sampling can be done in a different time or with a different frequency, but there will always be a difference in the pulses for inverter 1 compared to inverter 2 during one carrier period if the source signal is varying. For one period of the source signal this pulse difference will be equalized if the source signal is a uniform signal (identical half waves but with different polarity).

When the pulses to inverter 1 and inverter 2 are not identical, the voltages can be expressed as:

$$v_{ApccN} = \frac{v_{A1N} + v_{A2N}}{2} \tag{2.24}$$

And

$$v_{ApccBpcc} = v_{ApccN} - v_{BpccN} \tag{2.25}$$

Combining Eq.2.24 with Eq.2.25 gives Eq.2.26, which is an expression for $v_{ApccBpcc}$ by the use of $vA1N, vA2N, vB1N$ and $vB2N$.

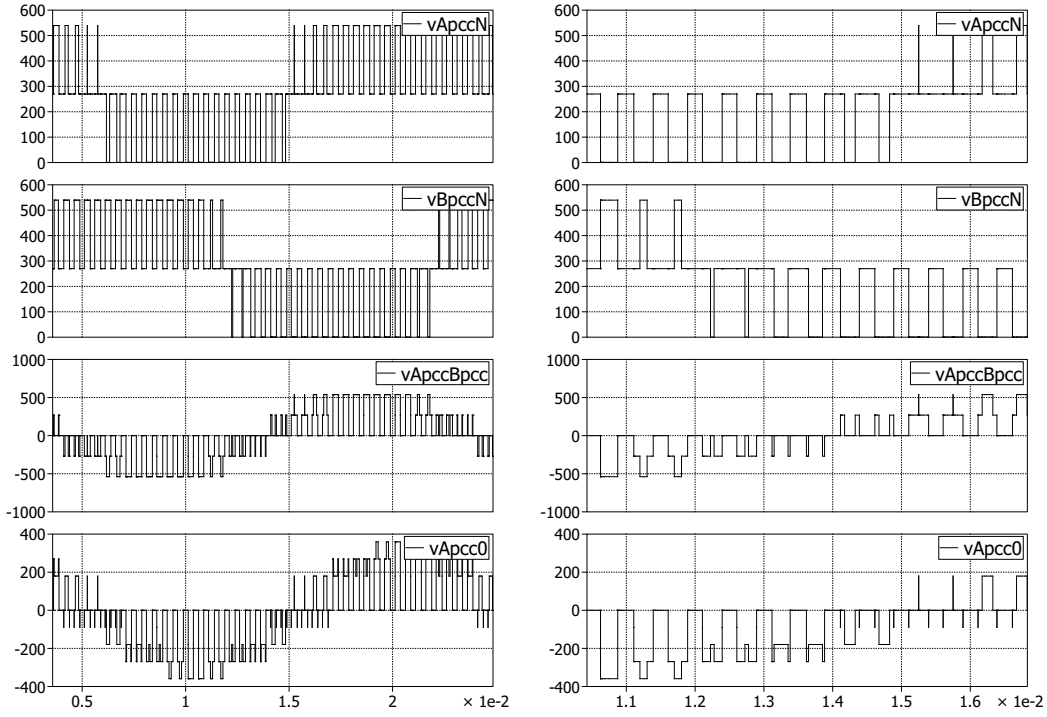
$$v_{ApccBpcc} = (\frac{v_{A1N} + v_{A2N}}{2}) - (\frac{v_{B1N} + v_{B2N}}{2}) \tag{2.26}$$

Since v_{A1N} and v_{A2N} can only have the value V_{DC} or 0, there are three possible results from Eq.2.24: V_{DC}, $1/2V_{DC}$ and 0. This proves that there will be three levels on the phase voltages v_{ApccN} v_{BpccN} v_{CpccN}, which is also confirmed in Fig.2.11

The interleaved modulation strategy gives 5 levels on the line-to-line voltage $v_{ApccBpcc}$ and 8 levels on the phase voltage $v_{Apcc}0$. This gives a better representation of the fundamental voltage, but as it can be seen in Fig.2.11 all levels reach zero at half the switching frequency and can therefore not be seen as "real"levels. Since the inverters are interleaved, the frequency of the pulses in the voltages after pcc is twice of the individual invertes switching frequency. The "real"levels generated from the three-level modulation strategy used in the proposed three-level strategy for parallel inverters and in the NPC inverter are presented in the next sections in this chapter.

For it to be easy to distinguish the different levels all inductance in the circuit in Fig.2.9 have been removed and replaced with only resistors. This is solely done for explanation purposes for the different voltage levels, and will not represent the system later in the report or in the laboratory.

The reason for the levels in the line-to-line or phase voltage reaching zero is because of the nature of the interleaved strategy. Having Eq.2.25 in mind, it can be seen in Fig.2.11 that the voltages v_{ApccN} and v_{BpccN} will have the same value two times every switching period. This will lead to $v_{ApccBpcc}$ beeing zero. This means that the load will experience the highest du/dt stresses when the voltage is at its peak value. Using the interleaved strategy it is not possible to raise or lower the middle value of the voltage, like it is in a three-level inverter.



(a) v_{ApccN}, v_{BpccN} and $v_{ApccBpcc}$. (b) Zoom of 2.11(a)

Figure 2.11: *f_{SW}=1000Hz V_{DC}=540V V_{ref}=180V*

The effect interleaving has on the circulating current and on the THD will be investegated in simulations and in experiments in the laboratory.

2.2.2 Two parallel two-level inverters used as one three-level inverter

When two inverters are paralleled, it is possible to increase the number of states for each phase leg. A phase leg consists of all the paralleled legs for one phase. In fact, it is possible to represent the paralleled two level inverters as one three-level inverter if pcc is used as reference point. A three-level representation of Fig.2.9 is depicted in Fig.2.12. Notice that no connections has been changed, only the way the circuit is drawn. Taking the phase leg A as an example, one can observe that the legs individually can only have two states, O and P. By combining these two states it is possible to get a third state H. However, the third state H will only appear at pcc and not on the individual legs of the inverter. This phenomenon is also observable for the interleaved modulation strategy in section 2.2.1, but not actively utilized. Tab.2.4 presents the different states and how they are created for phase leg A. The procedure is the same for phase leg B and C. H is created by using different states on inverter 1 and 2, therefore there will be two ways of creating H. The deciding factors when chosing which one of H1 or H2 to use to represent H, are switching loss reduction and equal load sharing of the switches.

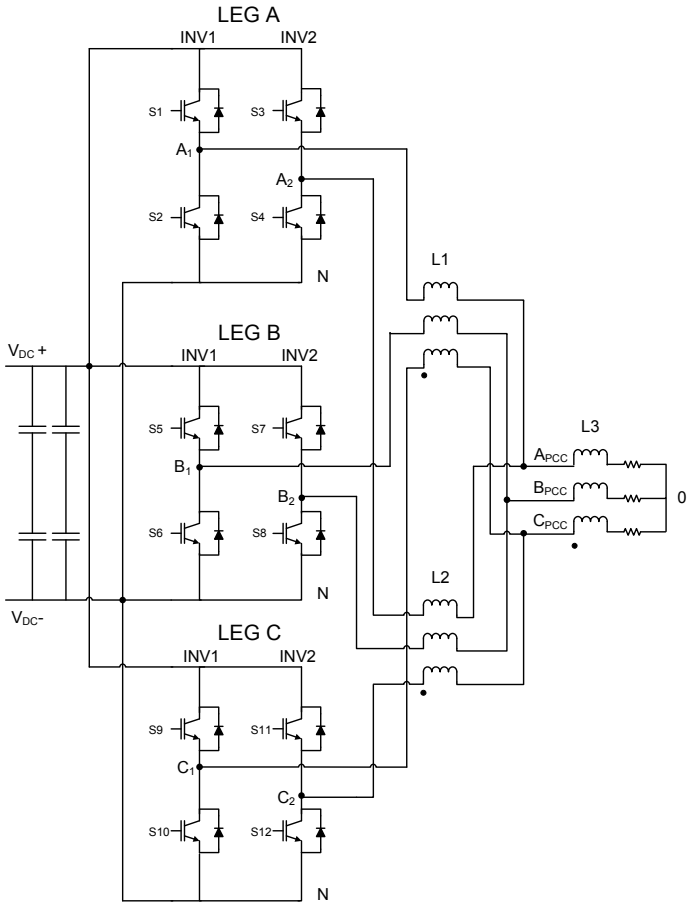


Figure 2.12: *Three-level representation of two parallel two-level inverters*

	Switching States			
Leg A	**O**	**H1**	**H2**	**P**
S1	0	1	0	1
S2	1	0	1	0
S3	0	0	1	1
S4	1	1	0	0

Table 2.4: *Switchingstates for Leg A*

When the state H is used, a current path from one phase of V_{DC}, through leg A on both inverters and back to the opposite phase of V_{DC} is created. This is also the case for leg B and leg C. The current path for H1 is drawn in Fig.2.13. It can be seen in Fig.2.13 that the inductors will act as a voltage dividers in the H state. This explains why there will be three levels when looking at v_{ApccN}, and only two levels when looking at v_{A1N} or v_{A2N}. It should be noted that the inductors in Fig.2.12 and in Fig.2.13 are the same, three-phase inductors with common core, but for explanation purposes the drawing is simplified in Fig.2.13.

States	O		H1		H2		P	
	Leg A1	Leg A2	Leg A1	Leg A2	Leg A1	Leg A2	Leg A1	Leg A2
Upper switch	0	0	1	0	0	1	1	1
Lower switch	1	1	0	1	1	0	0	0

Table 2.5: *Representation of the different states for phase leg A*

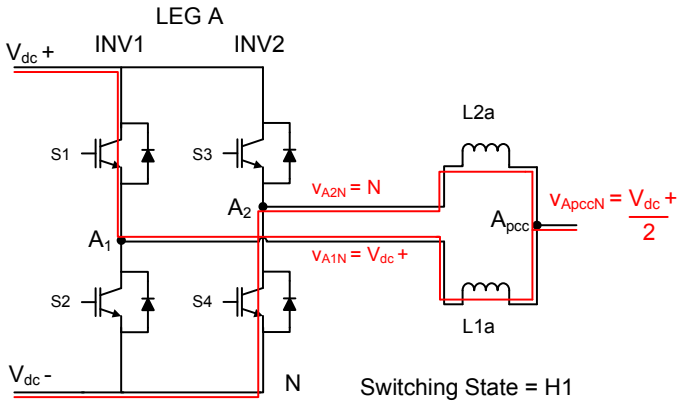


Figure 2.13: *Phase leg A for state H1*

Looking at the line-to-line voltage $v_{ApccBpcc}$, it can be observed that there will be three levels on v_{ApccN} and three levels on v_{BpccN}. Combining 3 by 3 levels gives a total of nine possible combinations. This is shown in Tab.2.6.

	Levels for $v_{ApccBpcc}$		
State	v_{ApccN}	v_{BpccN}	$v_{ApccBpcc}$
OO	0	0	0
OH	0	1/2	-1/2
OP	0	1	-1
HO	1/2	0	1/2
HH	1	1	0
HP	1	1/2	1/2
PO	1	0	1
PH	1	1/2	1/2
PP	1	1	0

Table 2.6: *Possible levels for two parallel two-level inverters on the line-to-line voltage*

Even if there are nine combinations for the states for phase leg A and B, there are only five combinations that will give different levels, thus there will be five levels on the line-to-line voltage. See Eq.2.25 for the calculation of $v_{ApccBpcc}$. In comparison, a two-level inverter has two levels on phase voltage and three levels on line-to-line voltage.

2.2.3 Space Vector Modulation for 3 level Inverter

One of the features of two parallel connected inverters is the ability to obtain three levels of voltage (phase to neutral) $P = V_{DC}$, $H = \frac{1}{2}V_{DC}$ and $O = 0$. Describing system in the

meaning of three voltage levels provides similarity to Three-Level Neutral Point Clamped Inverter. This similarity allows to approach Space Vector Modulation in the same way like for Neutral Point Clamped Inverter [10].

Stationary Space Vectors

There are twenty seven different possibilities for switching states, because of the three phase system. Additionaly, the H-state can be created in two ways. The nineteen vectors can be obtained from this switching states which are presented in Table 2.7 and depicted in the Fig. [2.17]

Space Vector	Switching State	Vector Classification	Vector Magnitude
$\vec{V_0}$	[OOO], [HHH], [PPP]	Zero Vector	0
$\vec{V_1}$	[HOO] and [PHH]	Small Vector	$\frac{1}{3}V_{DC}$
$\vec{V_2}$	[HHO] and [PPH]		
$\vec{V_3}$	[OHO] and [HPH]		
$\vec{V_4}$	[OHH] and [HPP]		
$\vec{V_5}$	[OOH] and [HHP]		
$\vec{V_6}$	[HOH] and [PHP]		
$\vec{V_7}$	[PHO]	Medium Vector	$\frac{\sqrt{3}}{3}V_{DC}$
$\vec{V_8}$	[HPO]		
$\vec{V_9}$	[OPH]		
$\vec{V_{10}}$	[OHP]		
$\vec{V_{11}}$	[HOP]		
$\vec{V_{12}}$	[POH]		
$\vec{V_{13}}$	[POO]	Large Vector	$\frac{2}{3}V_{DC}$
$\vec{V_{14}}$	[PPO]		
$\vec{V_{15}}$	[OPO]		
$\vec{V_{16}}$	[OPP]		
$\vec{V_{17}}$	[OOP]		
$\vec{V_{18}}$	[POP]		

Table 2.7: *Voltage vectors created from different combination of the switches*

Taking into consideration the length of these vectors four different kinds can be distinguished:

- Zero vector

  The zero vector is created by three different switching states [OOO], [HHH] and [PPP]. The amplitude of V_0 is equal to 0.

- Small vectors

  Their amplitude is equal to $\frac{1}{3}V_{DC}$. Each of them can be created in two ways, f.e. $\vec{V_1}$ is made by [HOO] and [PHH] switching states.

$$\begin{aligned}\vec{V_1}(HOO) &= \frac{2}{3}(V_{AN}e^{j0} + V_{BN}e^{j\frac{2\pi}{3}} + V_{CN}e^{j\frac{4\pi}{3}}) \\ &= \frac{2}{3}(\frac{V_{DC}}{2}e^{j0}) = \frac{V_{DC}}{3}\end{aligned} \tag{2.27}$$

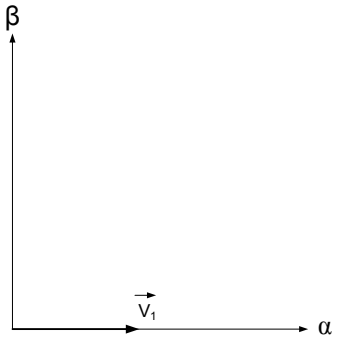


Figure 2.14: *Small vector $\vec{V_1}(HOO)$ representation in $\alpha\beta$ plane.*

- Medium vectors

  Their amplitude is equal to $\frac{\sqrt{3}}{3}V_{DC}$.

$$\begin{aligned}\vec{V_8}(HPO) &= \frac{2}{3}(V_{AN}e^{j0} + V_{BN}e^{j\frac{2\pi}{3}} + V_{CN}e^{j\frac{4\pi}{3}}) \\ &= \frac{2}{3}(\frac{V_{DC}}{2}e^{j0} + V_{DC}e^{j\frac{2\pi}{3}}) = j\frac{\sqrt{3}}{3}V_{DC}\end{aligned} \tag{2.28}$$

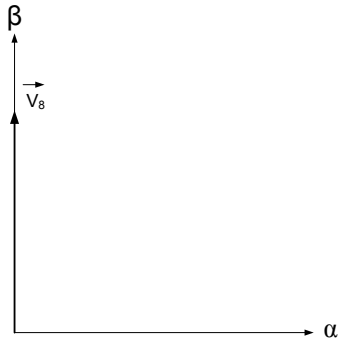


Figure 2.15: *Medium vector $\vec{V_8}(HPO)$ representation in $\alpha\beta$ plane.*

- Large vectors

  Their amplitude is equal to $\frac{2}{3}V_{DC}$.

$$\begin{aligned} \vec{V_{13}}(POO) &= \frac{2}{3}(V_{AN}e^{j0} + V_{BN}e^{j\frac{2\pi}{3}} + V_{CN}e^{j\frac{4\pi}{3}}) \\ &= \frac{2}{3}(V_{DC}e^{j0}) = \frac{2}{3}V_{DC} \end{aligned} \tag{2.29}$$

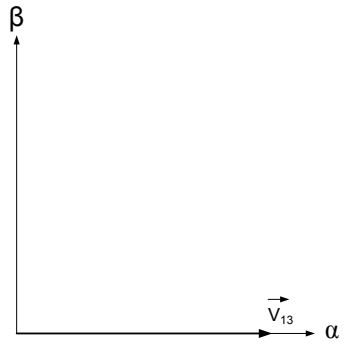


Figure 2.16: *Large vector $\vec{V_{13}}(POO)$ representation in $\alpha\beta$ plane.*

The large vectors divides the plane into six sectors. Each of these sectors can be split into four regions as it is depicted in Fig.2.17. Combination of vectors which should be used to synthetize $\vec{V_{ref}}$ is based on its position. For example, when $\vec{V_{ref}}$ is in region four of sector I, $\vec{V_2}$, $\vec{V_7}$ and $\vec{V_{14}}$ are used.

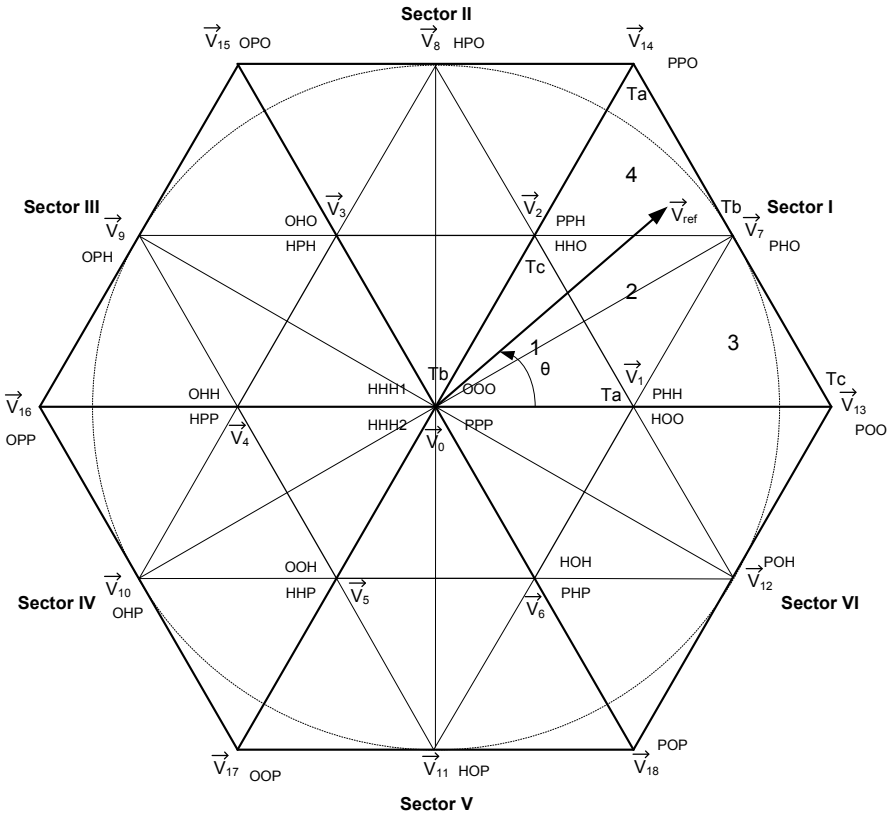


Figure 2.17: *Space Vector Diagram.*

Dwell Times

The following Figure presents reference vector transition from sector I to sector II:

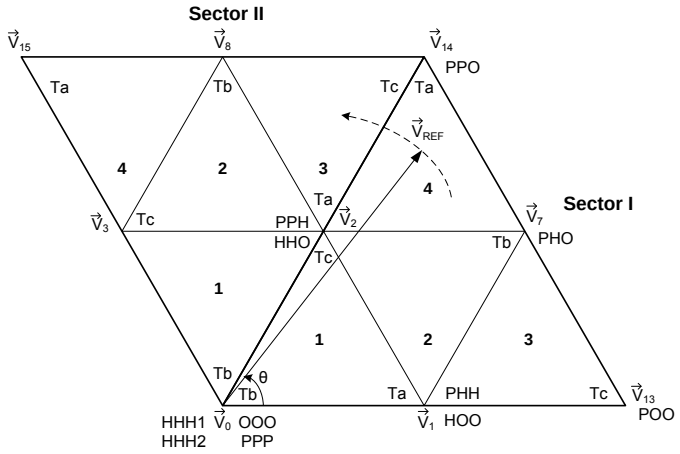


Figure 2.18: $\vec{V_{ref}}$ *transition between two sectors.*

The dwell times calculation for three level SVM is similar to two level SVM. Vectors: $\vec{V_2}$, $\vec{V_7}$ and $\vec{V_{14}}$ are used when $\vec{V_{ref}}$ is in region four of sector I:

$$\vec{V_{14}}T_a + \vec{V_7}T_b + \vec{V_2}T_c = \vec{V_{ref}}T_s \tag{2.30}$$

where:

$$\vec{V_{14}} = \frac{2}{3}V_{DC}e^{j\frac{\pi}{3}}; \qquad \vec{V_7} = \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}}; \qquad \vec{V_2} = \frac{1}{3}V_{DC}e^{j\frac{\pi}{3}}$$

Solving Eq.2.31:

$$\begin{aligned}\frac{2}{3}[cos(\frac{\pi}{3}) + jsin(\frac{\pi}{3})]T_a \quad &+\tfrac{\sqrt{3}}{3}[cos(\tfrac{\pi}{6}) + jsin(\tfrac{\pi}{6})]T_b \quad +\frac{1}{3}[cos(\frac{\pi}{6}) + jsin(\frac{\pi}{6})]T_c \\ &= \tfrac{V_{ref}}{V_{DC}}[cos(\theta) + jsin(\theta)]T_s\end{aligned} \tag{2.31}$$

And splitting into real and imaginary part:

- Real

$$\frac{1}{3}T_a + \frac{1}{2}T_b + \frac{1}{6}T_c = \frac{V_{ref}}{V_{DC}}cos(\theta)T_s \tag{2.32}$$

- Imaginary

$$\frac{\sqrt{3}}{3}T_a + \frac{\sqrt{3}}{6}T_b + \frac{\sqrt{3}}{6}T_c = \frac{V_{ref}}{V_{DC}}sin(\theta)T_s \tag{2.33}$$

Together with:

$$T_a + T_b + T_c = T_s \tag{2.34}$$

a set of equations (2.32, 2.33 and 2.34) can be created to calculate dwell times: T_a, T_b, T_c.

The dwell times for every region in sector I are presented in Tab.2.8:

Region	T_a		T_b		T_c	
1	$\vec{V_1}$	$T_s[2m_asin(\frac{\Pi}{3} - \theta)]$	$\vec{V_0}$	$T_s[1 - 2m_asin(\frac{\Pi}{3} + \theta)]$	$\vec{V_2}$	$T_s[2m_asin(\theta)]$
2	$\vec{V_1}$	$T_s[1 - 2m_asin(\theta)]$	$\vec{V_7}$	$T_s[2m_asin(\frac{\Pi}{3} + \theta) - 1]$	$\vec{V_2}$	$T_s[1 - 2m_asin(\frac{\Pi}{3} - \theta)]$
3	$\vec{V_1}$	$T_s[2 - 2m_asin(\frac{\Pi}{3} + \theta)]$	$\vec{V_7}$	$T_s[2m_asin(\theta)]$	$\vec{V_{13}}$	$T_s[2m_asin(\frac{\Pi}{3} - \theta) - 1]$
4	$\vec{V_{14}}$	$T_s[2m_asin(\theta) - 1]$	$\vec{V_7}$	$T_s[2m_asin(\frac{\Pi}{3} - \theta)]$	$\vec{V_2}$	$T_s[2 - 2m_asin(\frac{\Pi}{3} + \theta)]$

Table 2.8: *Dwell times for sector I*

, where $m_a = \frac{\sqrt{3}V_{ref}}{V_{DC}}$ is modulation index.

The dwell times for the other sectors (II to VI) are calculated by subtracting a multiple of $\frac{\pi}{3}$ from the angular displacement θ. By doing this the modified angle falls into sector I and the calculations presented in Tab.2.8 can be used.

Switching Pattern

The requirements for choosing switching pattern are the same like for two-level SVM.

- Zero or minimum changes in switching are desirable when the reference vector $\vec{V_{ref}}$ is passing from one sector (region) to another.
- Only two switches in the same leg are involved when passing from one switching state to another in order to reduce device switching frequency.

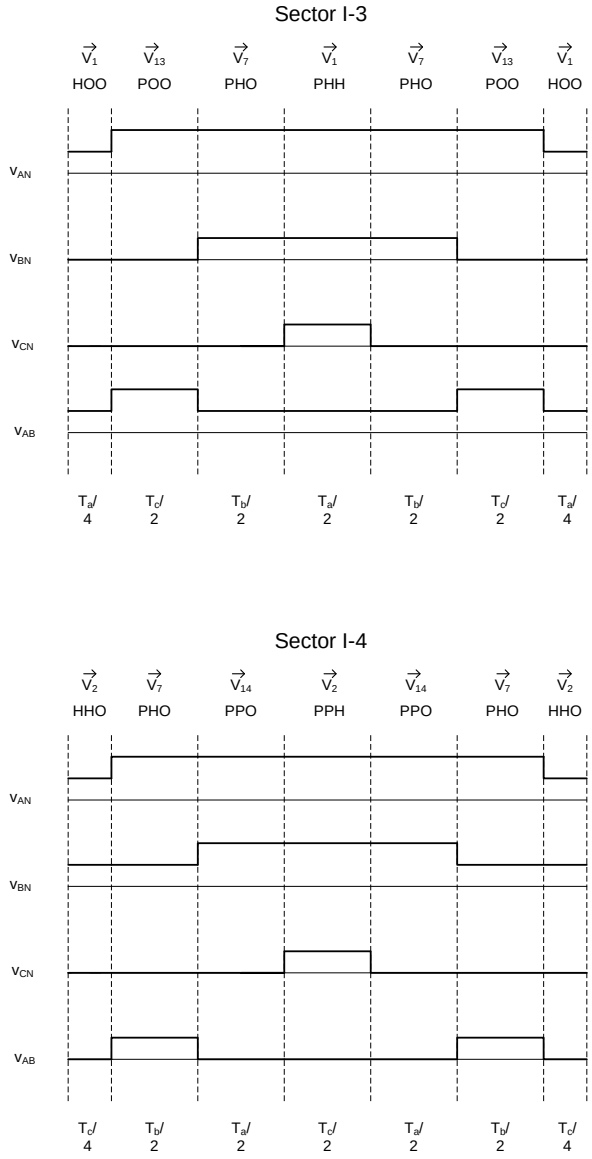


Figure 2.19: *Switching pattern when $\vec{V_{ref}}$ is placed in sector I region three and four.*

Tab.2.9 and Tab.2.10 presents the switching sequence for $\vec{V_{ref}}$ positioned in sector I and II. The transition of $\vec{V_{ref}}$ between two successive sectors is done excluding change in switching state. Also transition between two regions is realized with minimum number of switches changes. Reference vector in region three can be synthetized by three nearest stationary vectors: $\vec{V_1}$, $\vec{V_7}$ and $\vec{V_{13}}$. It can be observed at Fig.2.19, that transition between two states includes change only between O and H state, or H and P. The switching patterns for all sectors are presented in Appendix C. The switching sequence presented on the Fig.2.19 has been designed for three level NPC inverter and spread in order to implement

SECTOR I								
Segment	**1**		**2**		**3**		**4**	
1st	$\vec{V}_0$	[OOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]
2nd	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{13}$	[POO]	$\vec{V}_7$	[PHO]
3rd	$\vec{V}_{2O}$	[HHO]	$\vec{V}_7$	[PHO]	$\vec{V}_7$	[PHO]	$\vec{V}_{14}$	[PPO]
4th	$\vec{V}_0$	[HHH]	$\vec{V}_{1P}$	[PHH]	$\vec{V}_{1P}$	[PHH]	$\vec{V}_{2P}$	[PPH]
5th	$\vec{V}_{2O}$	[HHO]	$\vec{V}_7$	[PHO]	$\vec{V}_7$	[PHO]	$\vec{V}_{14}$	[PPO]
6th	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{13}$	[POO]	$\vec{V}_7$	[PHO]
7th	$\vec{V}_0$	[OOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]

Table 2.9: *Switching pattern for sector I*

SECTOR II								
Segment	**1**		**2**		**3**		**4**	
1	$\vec{V}_0$	[OOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3O}$	[OHO]
2	$\vec{V}_{3O}$	[OHO]	$\vec{V}_8$	[HPO]	$\vec{V}_8$	[HPO]	$\vec{V}_{15}$	[OPO]
3	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3P}$	[HPH]	$\vec{V}_{14}$	[PPO]	$\vec{V}_8$	[HPO]
4	$\vec{V}_0$	[HHH]	$\vec{V}_{2P}$	[PPH]	$\vec{V}_{2P}$	[PPH]	$\vec{V}_{3P}$	[HPH]
5	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3P}$	[HPH]	$\vec{V}_{14}$	[PPO]	$\vec{V}_8$	[HPO]
6	$\vec{V}_{3O}$	[OHO]	$\vec{V}_8$	[HPO]	$\vec{V}_8$	[HPO]	$\vec{V}_{15}$	[OPO]
7	$\vec{V}_0$	[OOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3O}$	[OHO]

Table 2.10: *Switching pattern for sector II*

in system of parallel connected inverters. As it can be observed on the Fig.2.20 twelve new signals (six for H1 state utilization and six for H2 state utilization) has been created in order to control every leg of the system. The new switching pattern contains continous states (P or 0) for whole sampling period.
From this pattern it is possible to calculate duty cycles, which will be compared with triangular in order to create switching signals. Following example presents calculation of duty cycle, which has been made for phase B of inverter one when the reference vector is passing through region three of sector one.

$$D_{B1} = \frac{0 \cdot \frac{T_a}{4} + 1 \cdot \frac{T_c}{2} + 1 \cdot \frac{T_b}{2} + 1 \cdot \frac{T_a}{4}}{\frac{T_s}{2}} \tag{2.35}$$

Following Eq.2.35 the duty cycles of each phase can be calculated likewise for every sector in hexagon depicted on the Fig.2.17.

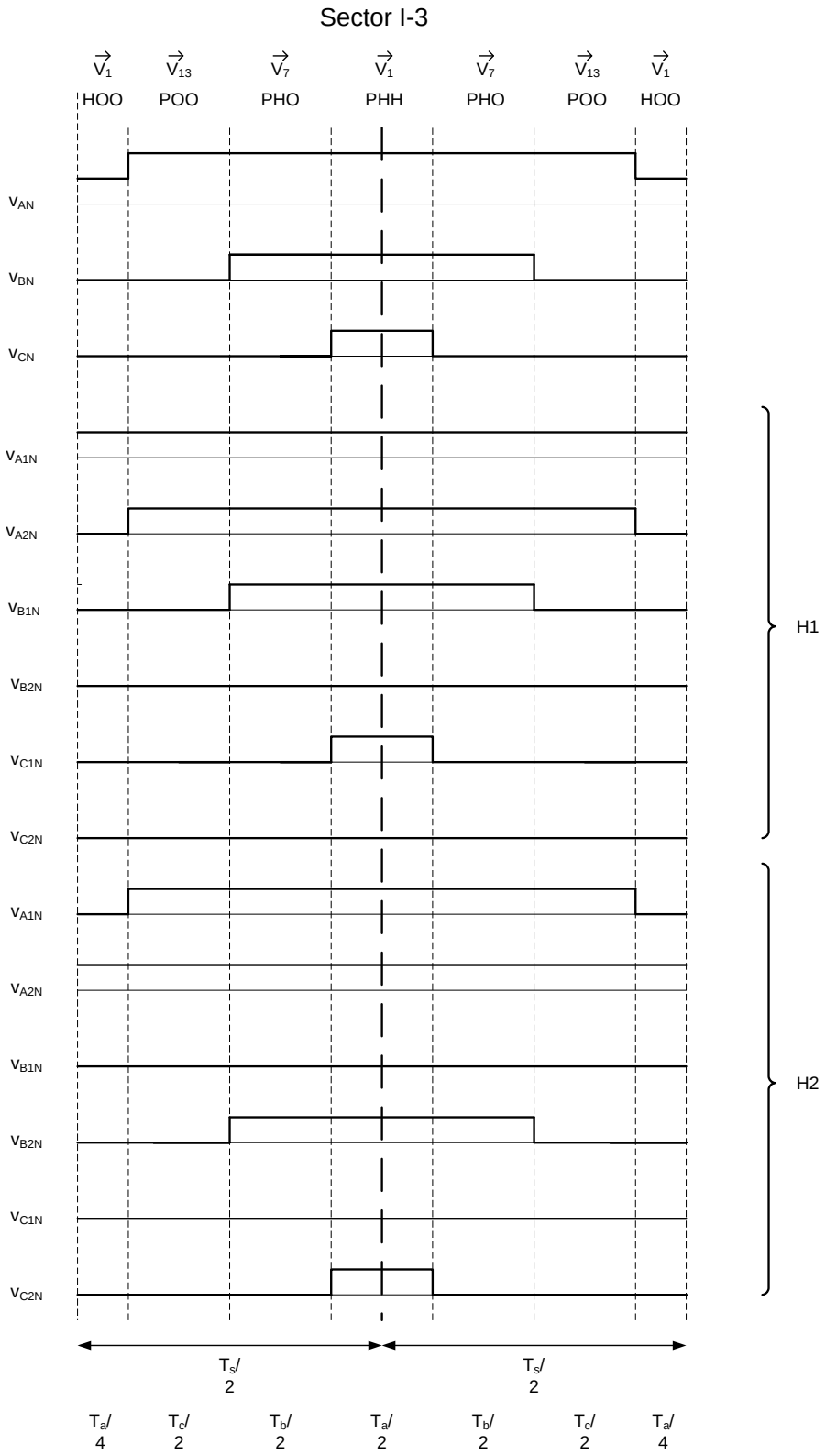


Figure 2.20: *Switching pattern separated for implementation in system of parallel connected inverters when $\vec{V_{ref}}$ is placed in sector I region three and four.*

The Fig.2.21 presents the duty cycle (D_B) of phase B for NPC inverter, which is decomposed for duty cycles (D_{B1} and D_{B2}) for parallel connected inverters system.

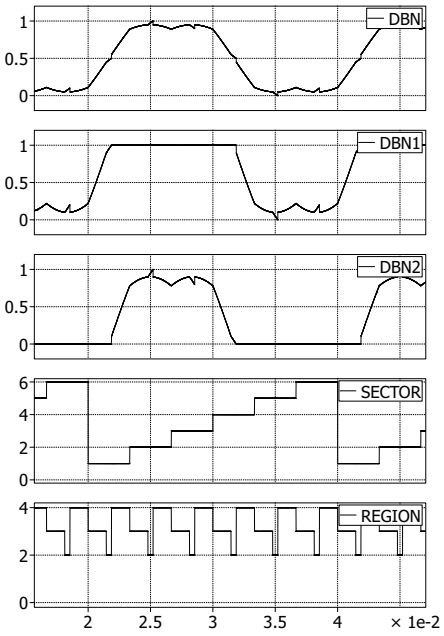


Figure 2.21: *Duty cycles (D_{B1} and D_{B2}) for system of parallel inverters obtained from duty cycle (D_B) for NPC inverter .*

From Fig.2.21 it can be seen that the waveform of the duty cycles contains small spikes on lower and upper part of the waveform. The spikes occur in region two. The reason for this is the chosen switching sequence. The same three-level switching sequence is used for the proposed three-level SVM for parallel inverters and for the NPC inverter. Therefore the two methods will still be comparable.

As it can be observed the duty cycles D_{B1} and D_{B2} contains continuos states, which could be referred to switching pattern depicted on the Fig.2.20. Especially this phenomenon is visible in sector I - region three, where D_{B2} has value zero, which was shown in the switching pattern.

2.3 Three-level Neutral Point Clamped inverter

The most commonly used three-level inverter is the NPC inverter depicted in Fig.2.22 [10]. The main application area for the NPC is within MV drives. There are also other types of three-level inverters such as the Cascaded H-Bridge inverter and the capacitor-clamped (flying capacitor) inverter [10][2], but as mentioned before, the NPC is the most commonly used and therefore most suited for comparison with the parallel two-level inverter.

The NPC has three states that creates three levels on v_{xN}. The states and switch combinations can be seen in Tab.2.11.

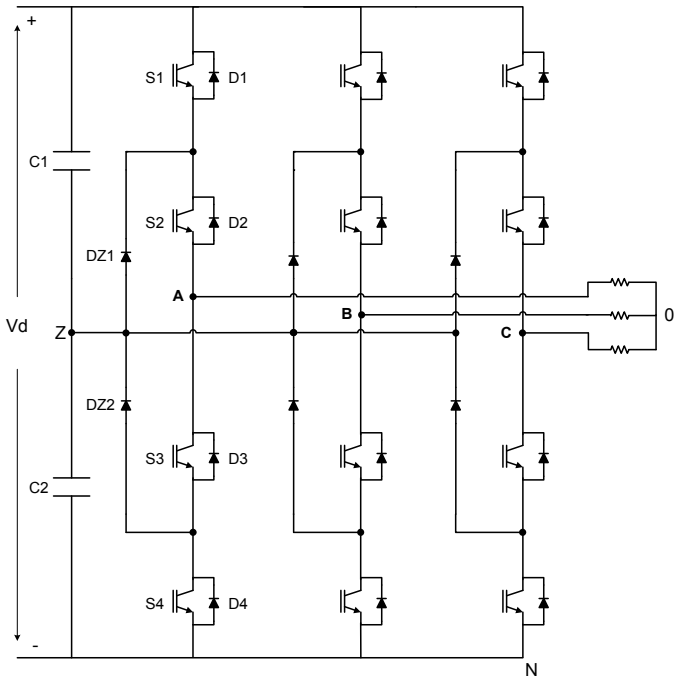


Figure 2.22: *Three-phase NPC inverter*

In the H state, when switches S2 or S3 are on, the neutral point is clamped to the output through DZ1 or DZ2 and v_{AN}=1/2 v_{dc}. For the other two states, P and 0, the diodes are not conducting giving v_{AN} equal to v_{dc} and 0 respectively.

State	**Leg A**				**v_{AN}**
	S1	S2	S3	S4	
P	1	1	0	0	v_{dc}
H	0	1	1	0	1/2v_{dc}
O	0	0	1	1	0

Table 2.11: *Switching states for a three-phase three-level NPC inverter*

Tab.2.12 presents a different view of how the levels are created in the NPC inverter.

State	**O**	**H**	**P**
Top switch	0	0	1
Upper middle switch	0	1	1
Lower middle switch	1	1	0
Bottom switch	1	0	0

Table 2.12: *Representation of the different states for leg A*

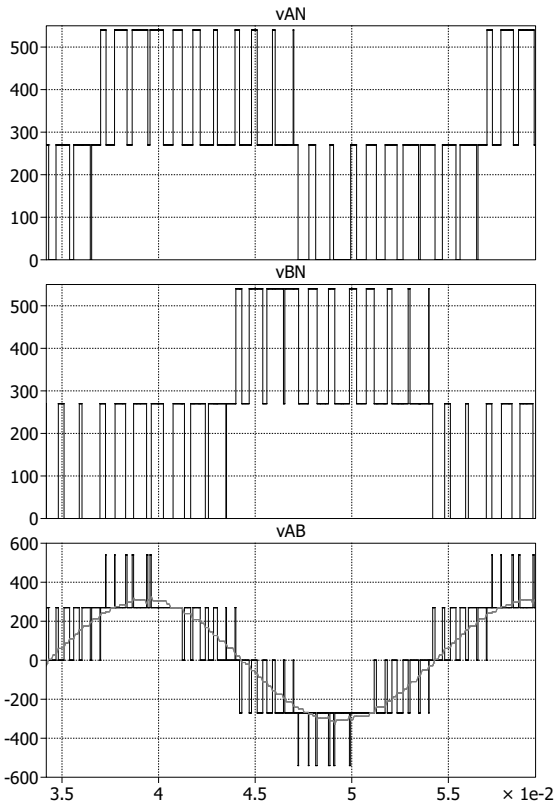


Figure 2.23: *Waveforms of the NPC inverter.* f_{SW}*=1000Hz* V_{DC}*=540V* V_{ref}*=180V*

Benefits of the NPC:

- Low du/dt and harmonics. The line-to-line voltage will have five levels, which will give lower du/dt and harmonics compared to the two-level inverter which will have three level line-to-line voltage[2][10][13]. This will reduce switching stresses for the windings in a motor or a transformer.
- Because of the topology of the NPC, the switches withstand only half of the dc bus voltage during commutation from P to H, H to 0 and vica versa. Switching between P and 0 is not allowed[10].
- The input current will have very low distortion[2].

Drawbacks of the NPC:

- Increased complexity for control and modulation strategy.[10]
- Unequal load distribution on the switches. S2 is always on in P state and S3 always on in the 0 state. S1 and S4 is not used in the H state so S2 and S3 are used more than S1 and S4. This has been corrected in the Active Neutral Point Clamped (ANPC), where the clamping diodes have been replaced with switches[16].

- Additional clamping diodes (NPC), or additional switches (ANPC) compared to a two-level inverter. This increases the inverter cost and also the losses in the inverter.
- Neutral point balancing problems. The neutral point may deviate during operation because of minor component difference in the capacitors[10].

2.4 Conclusion

The relation between two parallel connected two-level inverters and a three-level inverter has been shown. The two-level and the three-level Space Vector Modulation strategy has been derived and will be used in simulations and experiments.

The three-level NPC gives better performance when it comes to harmonics on the ac side and also regarding ripple in the dc current, but the complexity of control together with the increased number of components makes it more expensive compared to the single two level inverter. The proposed system of two parallel connected two-level inverters has the ability to create the voltage levels much like in the NPC inverter. For the parallel inverters, the number of switches are the same as for the NPC, but the NPC will have six extra diodes. On the other hand the parallel inverters need sharing inductors on the output of each inverter and the two inverter currents must be balanced. It must be noted that the sharing inductors will only need to take half of the load current.

The three-level NPC inverter experience unequeal load distribution on the switches and neutral point balancing problems, where in the parallel system the switches can be loaded equally and will not have problems with balancing the neutral voltage since this point is not used at all in the inverter. The unequal loading of the switches in the NPC inverter comes from the fact that the states will only change between P and H and between H and 0. Therefore the state H will be used more than P and 0, leading to more use of the switches representing H. However, in the parallel system of two-level inverters, H can be represented in two ways giving a chance to distribute the load more evenly on the switches.

In theory it is possible to use the same three-level SVM strategy for the NPC and the parallel two-level inverter. The only difference is how the states P, H and 0 are represented by the switches and how the triangle modulation is realized.

The proposed system of two parallel connected two-level inverters will be tested in simulations and experiments and its performance will be compared when using identical two-level SVPWM, pulse shifted two-level SVPWM and three-level SVPWM. The comparison with the three level NPC inverter using three-level SVPWM will be done only in simulation due to laboratory contraints.

3 Simulations

This chapter deals with different simulations for the system of two parallel connected two-level inverters. Two-level SVM with synchronized pulses, two-level SVM with pulses shifted and three level SVM are implemented in open loop condition to study behaviour of the system. The simulation of Three-Level NPC Inverter is also presented in this chapter in order to compare with the system of parallel connected inverters. All the simulations have been made in Matlab/Simulink environment with the use of PLECS toolbox. Each modulation strategy will be briefly discussed before the results are compared.

3.1 Simulation constraints and parameters

The simulation for the different modulation strategies are carried out in open loop, since the purpose is to make a comparison between the performance of the system with synchronized pulses, shifted pulses and the proposed system using three-level SVM. In addition, simulation results of the NPC inverter will be briefly discussed. By running the system in open loop it can be observed what amount of THD and which harmonics the different strategies will generate. This makes the comparison as fair as possible. A current controller will be able to reduce and possibly eliminate the low order harmonics. Therefore a modulation strategy having mainly low order harmonics can be improved more by a current controller than a modulation strategy with higher order harmonics.

It should also be noted than only an L-L filter is used, so there is no capacitor to short circuit the high frequency components in the voltage. Therefore there will be a high ripple in the current, and there will be a lot of harmonics in the voltage. However, this will make it easier to distinguish any difference in performance between the different systems.

Simulation Parameters:

- Power for each inverter = 2.2kW
- V_{DC} = 540V
- Carrier frequency $f_{carrier}$ = 5000Hz
- Modulation index m_a = 0.9 (Vref = 280V)
- Three-phase inductor L1 and L2 = 8mH 0.2Ω
- Three-phase load inductor = 7.2mH
- Load resistor = 40Ω

The simulation parameters represent the values for the components that is used in the lab. This ensures the best comparison between the simulation results and the laboratory results.

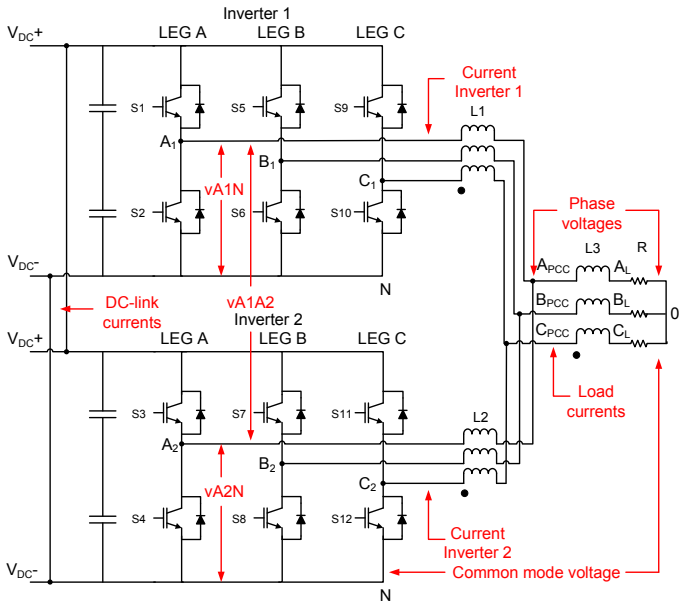


Figure 3.1: *Specification of measurements for the parallel inverter system.*

Fig.3.1 shows where the different measurements are taken. This is valid for all measurements taken on the parallel inverter system. The measurements taken for the NPC inverter will be specified in the relevant section.

3.2 Simulation models

3.2.1 Two-level SVM

The idea behind two-level SVM has been explained in the previous chapter. The model of two-level SVM contains sector selection, dwell time calculation, duty cycle calculation and triangle modulator. The created switching signals are input to the inverter switches. A block diagram of the simulation model is depicted in Fig.3.2.

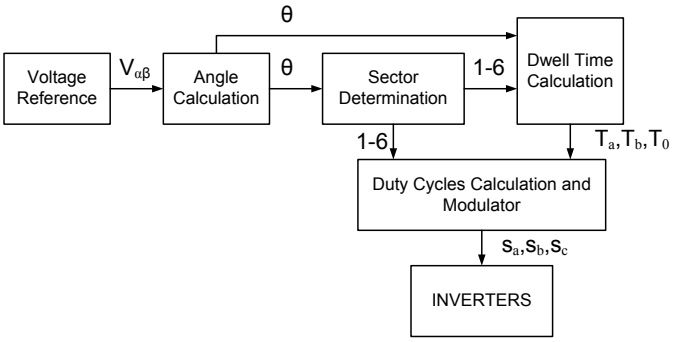


Figure 3.2: *Block diagram of two-level SVM.*

3.2.2 Parallel inverters with synchronized pulses

In Matlab/Simulink with Plecs all wires are ideal and equal components have the exact same value. This means that the case explained in 2.2 where components are ideal and the duty cycles are synchronized (identical) will be true for the simulation.

The two inverters use the same SVM to calculate the duty cycle from the voltage reference. This ensures that the duty cycles are identical for inverter 1 and inverter 2. The duty cycle is compared to a synchronized PWM module for each inverter.

3.2.3 Parallel inverters with interleaved pulses

The simulation model for parallel inverters with interleaved pulses is the same model as the one used for synchronized pulses, with exception for the PWM modules. In the PWM module the carrier wave for Inverter 2 is shifted with $180°$ compared to inverter 1.

3.2.4 Proposed three-level SVM for system of parallel connected inverters.

The analytical explanation of the three-level SVM has been presented in section 2.2.3. The simulation model is similar to two-level SVM. Additional part is region determination in which reference vector appears.

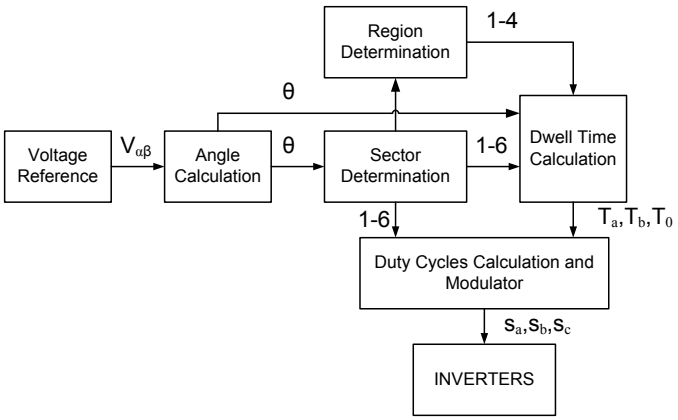
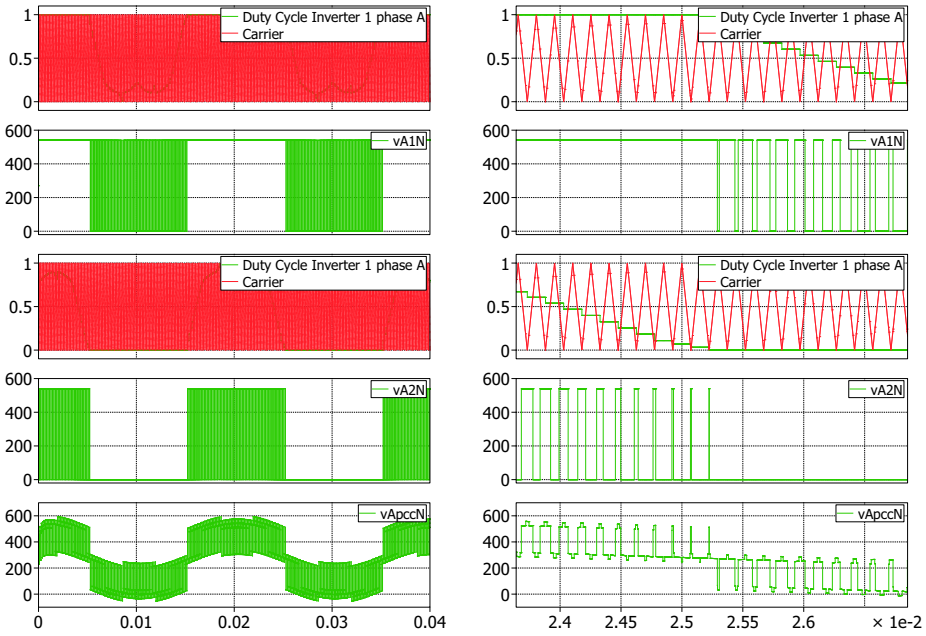


Figure 3.3: *Block diagram of three-level SVM.*

Because of the possibility to realize state $H = 0.5V_{DC}$ in two ways (H1 and H2), three different ways of realization of three-level SVM has been designed. In first case the modulation has been realized, when H1 state is only used. The next modulation strategies have been designed in case when state H1 and H2 are swapping each other every sampling period or every second sampling period. The modulator of the first strategy is presented on the Fig.3.4(a) and 3.4(b). v_{A1N} and v_{A2N} contain continous states P and 0 for every $t = 0.01$. The voltage v_{ApccN} is created from three levels.



(a) $v_{A1N}, v_{A2N}, v_{ApccN}$ waveforms.

(b) Zoom of v_{A1N}, v_{A2N}, v_{ApccN} waveforms.

Figure 3.4: *Three-level SVM using only H1 state.*

The Fig.3.5 presents the individual currents of inverters of phase A, when state H is realized in one way (H1 or H2). As it can be observed the big dc-offset is introduced in these currents with mean value around $380[A]$. Even if the current on the load will have smooth sinusoidal waveform, this modulation technique can not be use in real system due to danger of destroying inverters.

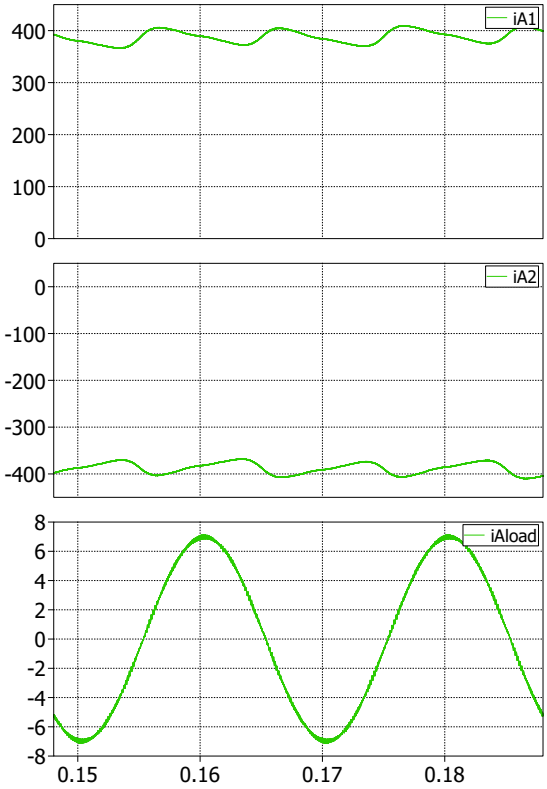
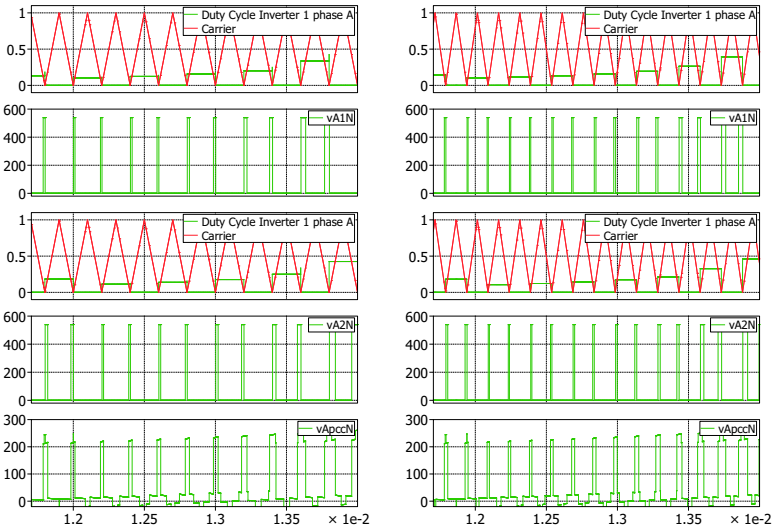


Figure 3.5: *Individual inerters and load A-phase current.*

The next modulation strategy has been designed in case when state H1 and H2 are swapping each other every sampling period. This strategy introduce less stresses on the single power module. It can be observed from the Fig.3.6(a) and 3.6(b) that to realize state H two different pairs of the switches are used. The duty cycles are compared to two traingular carriers with different frequencies. Using $f_{carrier} = 5[kHz]$ the number of switching signals sent to single leg of individual inverter was equal $N_{switch} = 77$ during $t = 0.02[s]$ which gives avarage switching frequency equal $f_{switching} = 3.85[kHz]$. By increasing carrier frequency to $f_{carrier} = 6.7[kHz]$ it was possible to obtain $f_{switching} = 5[kHz]$.

$$f_{switching} = \frac{N_{switch}}{t} = \frac{77}{0.02} = 3850[Hz] \tag{3.1}$$

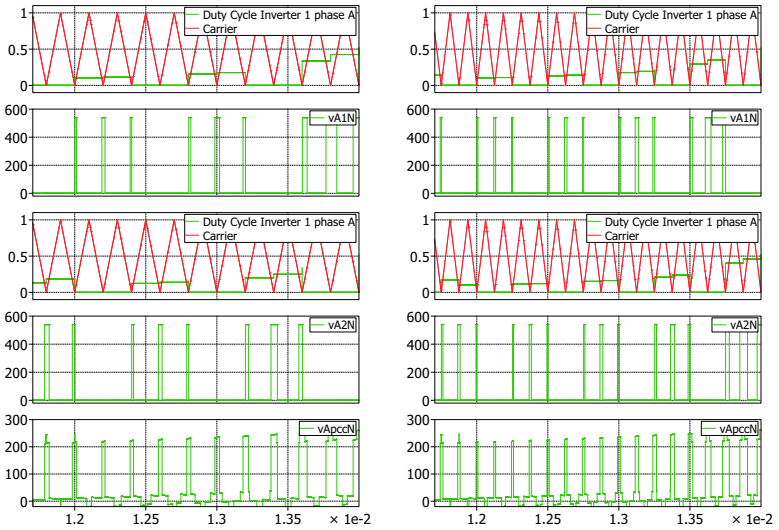


(a) Inverter 1: v_{A1N}, v_{A2N}, v_{ApccN} waveforms.

(b) Inverter 2: v_{A1N}, v_{A2N}, v_{ApccN} waveforms.

Figure 3.6: *Three-level SVM with H1 and H2 swapping each other every sampling period; a)* $f_{carrier} = 5[kHz]$*, b)* $f_{carrier} = 6.7[kHz]$.

The modulation method for the system when H1, H2 are swapping each other every sampling period could be optimized by swapping this two states every two sampling periods. Following the same rule like for previous modulation, where H1 and H2 were changing every sampling period, it was possible to obtain switching frequency $f_{switching} = 5[kHz]$ by increasing carrier frequency to $f_{carrier} = 8[kHz]$. For this $f_{carrier}$ the number of switching signals sent to one leg of individual inverter was counted to $N_{switch} = 100$, during $t = 0.02[s]$.

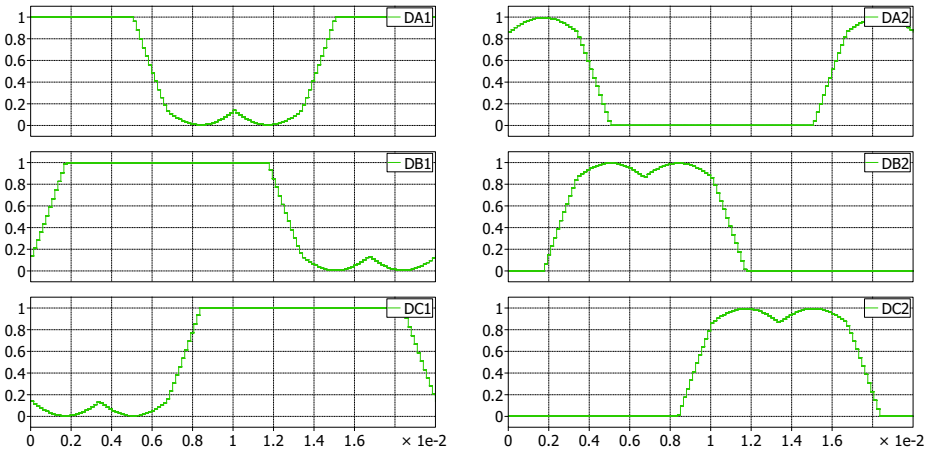


(a) Inverter 1: v_{A1N}, v_{A2N}, v_{ApccN} waveforms.

(b) Inverter 2: v_{A1N}, v_{A2N}, v_{ApccN} waveforms.

Figure 3.7: *Three-level SVM with H1 and H2 swapping each other every two sampling periods; a)* $f_{carrier} = 5[kHz]$*, b)* $f_{carrier} = 8[kHz]$.

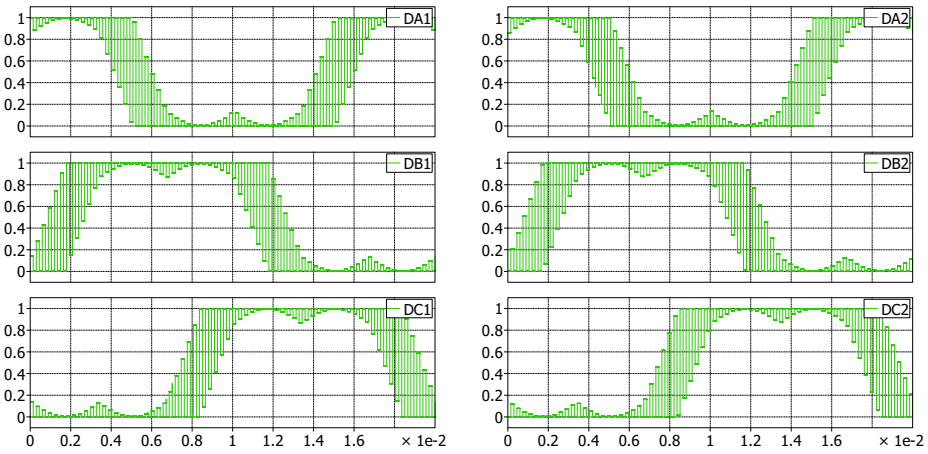
Fig.3.8(b), 3.9(a)and 3.10(a) demonstrate the duty cycles for the modulation techniques described above. The duty cycles in the method in which state H1 is only used are synthesized for the methods where H1 and H2 are swapping each other.



(a) Inverter 1: Duty cycles

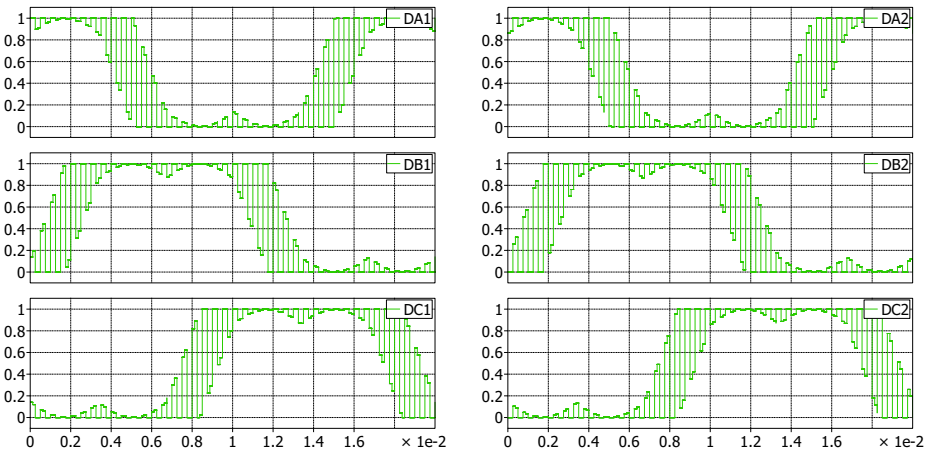
(b) Inverter 2: Duty cycles

Figure 3.8: *Duty cycles of modulation technique where only H1 state is utilized for a) inverter 1, b) inverter 2.*



(a) Inverter 1: Duty cycles (b) Inverter 2: Duty cycles

Figure 3.9: *Duty cycles of modulation technique where H1, H2 are swapping every one sampling period for a) inverter 1, b) inverter 2.*



(a) Inverter 1: Duty cycles (b) Inverter 2: Duty cycles

Figure 3.10: *Duty cycles of modulation technique where H1, H2 are swapping every two sampling periods for a) inverter 1, b) inverter 2.*

The duty cycles presented above have been utilized to create the switching signals by comparison with triangular carrier signal. The method in which H1, H2 are swapping each other every two sampling periods has been chosen for further analysis with $f_{carrier} = 8[kHz]$ which gives $f_{switching} = 5[kHz]$.

3.2.5 Neutral Point Clamped Inverter

In order to have a valid comparison with the other modulation strategies used in system of two parallel connected inverters, the value for the three-phase inductor in the NPC simulation is selected as:

$$L = L1 + L_{LOAD} = 8mH + 7.2mH = 15.2mH \tag{3.2}$$

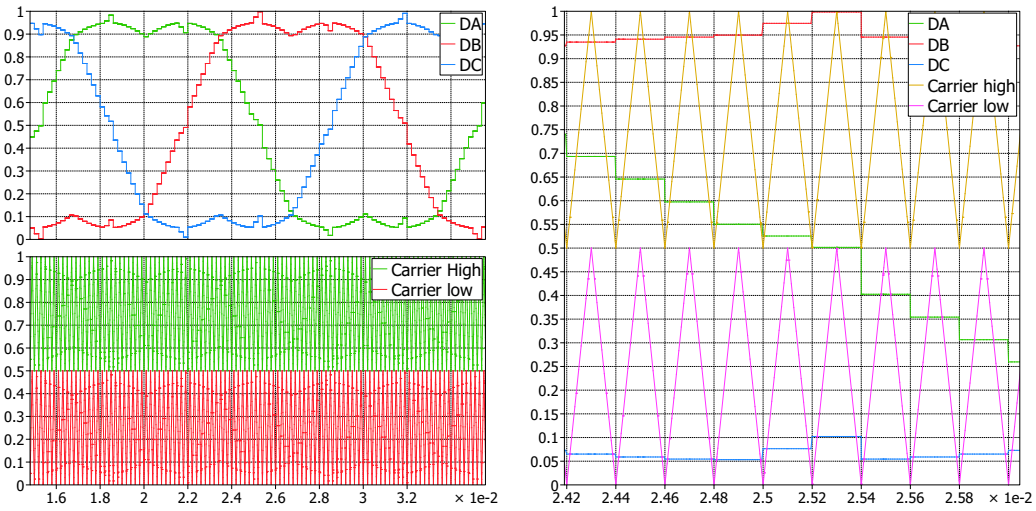
The same resistive load is used for the NPC simulation as for the other simulations.

Parameters for NPC simulation:

- V_{DC} = 540V
- Carrier frequency $f_{carrier}$ = 5000Hz
- Modulation index m_a = 0.9 (Vref = 280V)
- Three-phase inductor = 15.2mH 0.2Ω
- Load resistor = 40Ω

The PWM for the NPC is a bit different than for the two-level inverter, Fig.3.11. The duty cycles will have a shape similar to the duty cycles for a two-level SVM, even though it is a three-level SVM, but the pulse realization is done in a different way. Since the NPC can have three different states, the PWM has to be able to create three states from the duty cycles. This is done by having two triangular carrier waves that are level shifted. This means that the carrier waves will have the same frequency and synchronization but they will operate at different levels, one from 0 to 0.5 and one from 0.5 to 1. By using the statements below, three levels can be created from comparison with the duty cycle. The procedure is the same for all phases.

- if D_A > Carrier high
  then P
- if D_A < Carrier high and D_A > Carrier low
  then H
- if D_A < Carrier low
  then O



(a) Duty cycles and the two carrier waves

(b) The duty cycles and the carriers plotted together

Figure 3.11: *Modulation for three-level SVM for NPC inverter*

For the NPC inverter there is only one way of creating the H state.

3.2.6 Thermal model in PLECS

The PLECS toolbox has the option to model thermal properties of components as long as a thermal description for the actual component is implemented[17]. This makes it possible to investigate the conduction losses and the switching losses for each switch, and to see how the losses are distributed between switches in the same phase. The main idea is to compare the switching and conduction losses between each strategy, not to have a thermal description that is as close to reality as possible. The same thermal description is used for all IGBTs in all simulations.

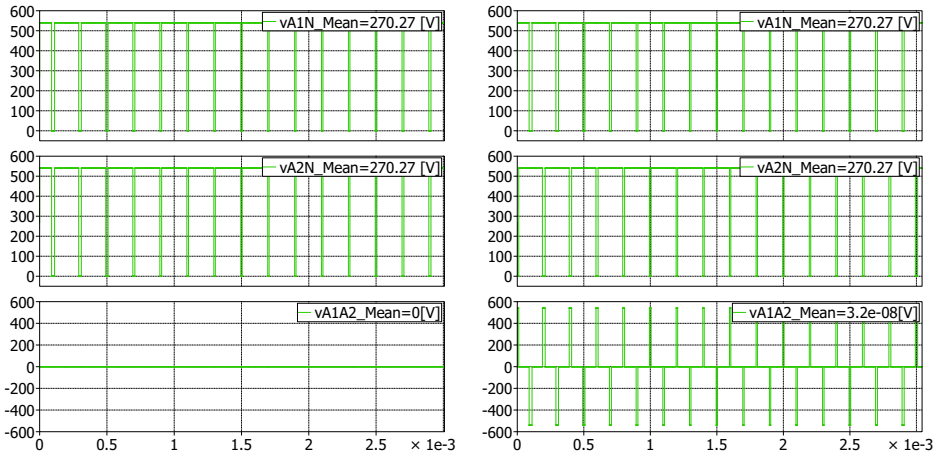
The switches will experience conduction losses due to the forward voltage drop over the switch. The switching turn-on losses occur because the voltage over the switch is decreasing (due to turn-on) while the current is increasing. This means that for a short moment there will be current and voltage present in the switch, and thus a power loss will occur. The same goes for the turn-off state where the voltage increases and the current decreases [11].

The thermal description used for the IGBT switches in the simulations has been obtained from the datasheet of the switch module used in the Danfoss FOC 302 inverter[18]. The thermal description generated in PLECS can be seen in Appendix G.

The losses will be measured in the switches in phase A.

3.3 Simulation results

3.3.1 Voltages between phase A of individual inverters and neutral point; voltages between phase A of inverter one and phase A of inverter two



(a) Synchronized pulses

(b) Interleaved pulses

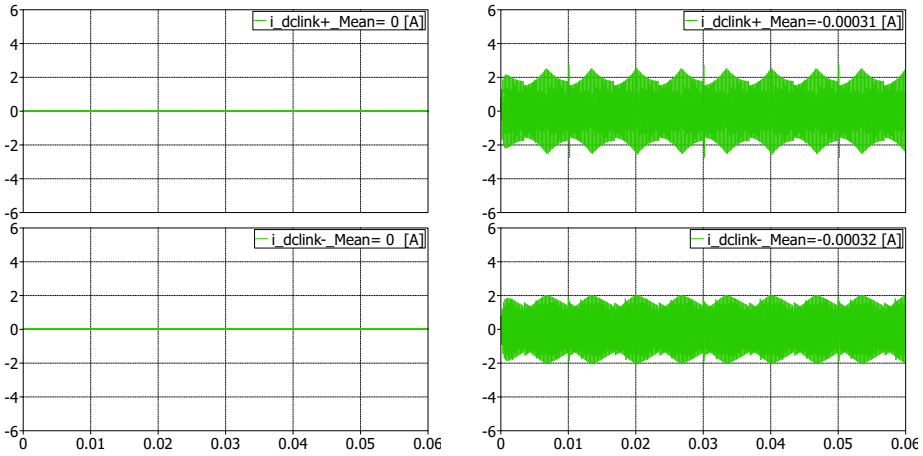
(c) Three-level SVM for parallel inverters

Figure 3.12: *Comparison of v_{A1N}, v_{A2N} and v_{A1A2}*

The relation between v_{A1N}, v_{A2N} and v_{A1A2} can be studied in section 2.2. For synchronized pulses in Fig.3.12(a) it can be seen that the output voltage for the two inverters will be exactly the same and therefore v_{A1A2} will always be zero. For the interleaved strategy, the pulses for v_{A1N} and v_{A2N} are shifted with $180°$. The effect this will have on v_{A1A2} can be seen in Fig.3.12(b). For the proposed three-level SVM strategy in Fig.3.12(c), v_{A1A2} will have a higher mean value than for the other two methods but it will still be very small.

It might seem that the switching frequency for the three-level strategy is lower than for the other strategies, but the average switching frequency will be the same as for the other strategies. This was explained in section 3.2.4.

3.3.2 Currents in the dc-link



(a) Synchronized pulses

(b) Interleaved pulses

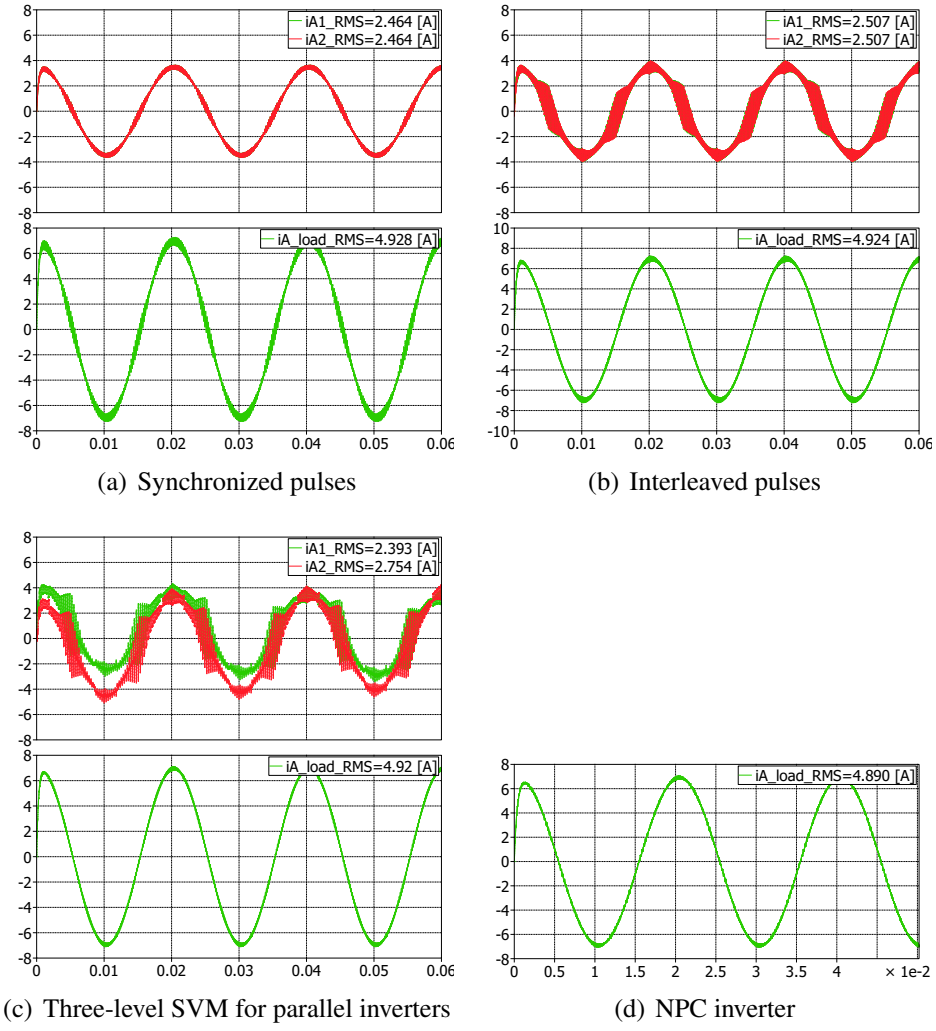
(c) Three-level SVM for parallel inverters

Figure 3.13: *Comparison of the currents in the dc-link*

The currents in the dc-link will appear if there is a voltage different from zero on v_{A1A2}. For the synchronized pulses v_{A1A2} is always zero, so there are no circulating currents. In the two other strategies there are circulating currents and the mean value of the currents can be seen on the figures. The mean value of the dc-link currents is an indication of any dc current circulating in the system. For the interleaved strategy the mean value is very low, but for the three-level strategy the mean value indicates that there is a dc-current

circulating in the system. This shows that if the mean value of v_{A1A2} is not zero, it will result in a circulating dc current. This will give an offset for the two inverter currents. It should be noted that the simulation is carried out in open loop, so there is no balancing controller to eliminate any offset of the currents and thus remove the circulating dc current or any zero-sequence controller that can supress the dc-link currents.

3.3.3 Individual inverters and load currents



(a) Synchronized pulses

(b) Interleaved pulses

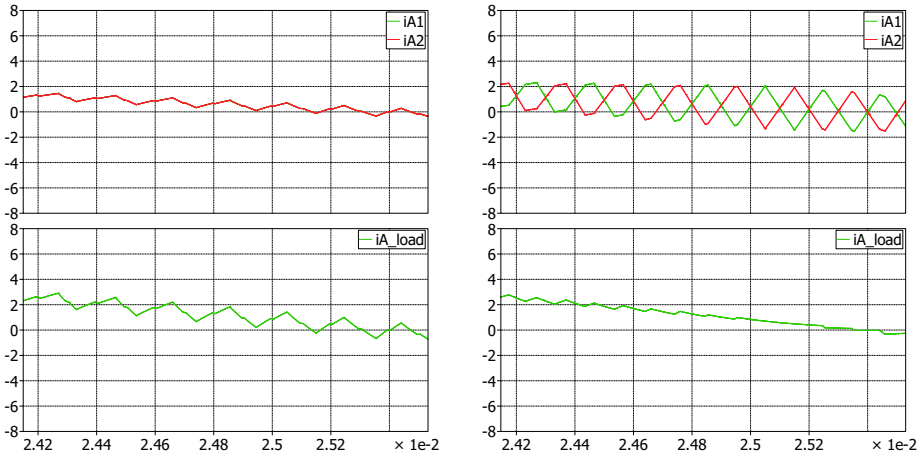
(c) Three-level SVM for parallel inverters

(d) NPC inverter

Figure 3.14: *Comparison of the currents in each inverter and the load current*

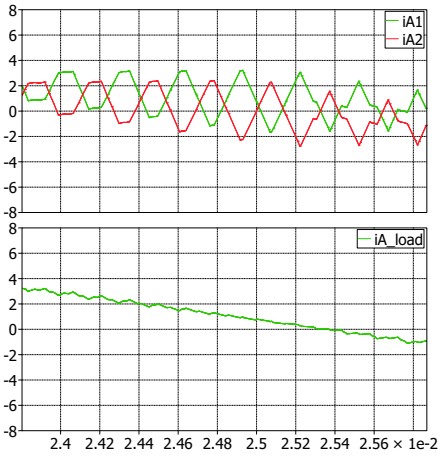
In Fig.3.14(a) it can be seen that the currents from the two inverters with synchronized pulses are exactly the same. This is simply because the two inverters have the exact same output voltages. In the two other methods in Fig.3.14(b) and in Fig.3.14(c) the pulses are not synchronized and will therefore have different shapes, however the load current

which contains both inverter currents will have a smooth sinusoidal waveform. Fig.3.14(d) presents the current in phase A for the NPC inverter. The NPC inverter has only one output per phase, in difference to the parallel inverters which has A1 and A2, so only the load current will be measured for the NPC.



(a) Synchronized pulses

(b) Interleaved pulses



(c) Three-level SVM for parallel inverters

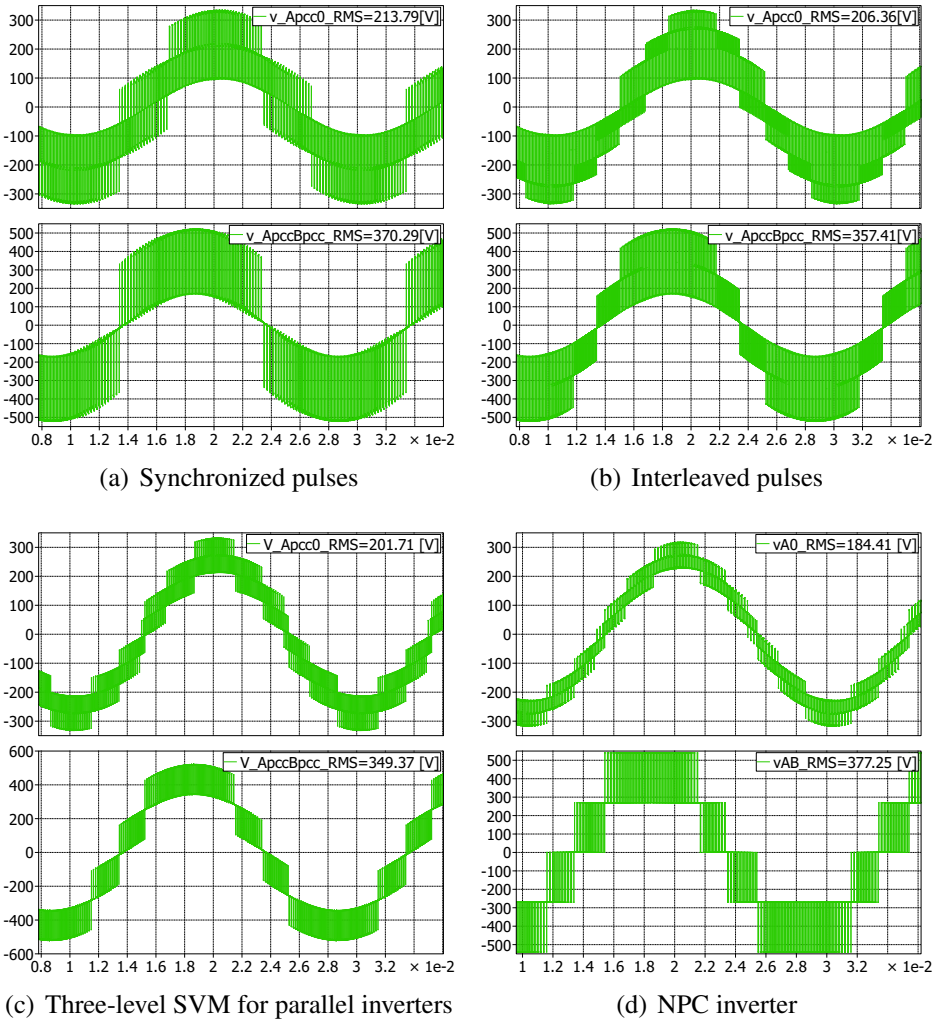
Figure 3.15: *Zoom of the currents in each inverter and the load current.*

It can be seen in Fig.3.15(a) that having parallel inverters with synchronized pulses does not contribute to reducing current ripple or harmonics in the output current, it only gives a higher current capability compared to a single inverter. The current ripple in the phase currents is proportional to the load current ripple. From Fig.3.15(b) and Fig.3.15(c) it can be seen that the ripple in the two inverter currents will be higher compared to Fig.3.15(a) but they will always be opposite so the ripple in the load current will be drastically reduced. The measured THD in the load current from the different methods can be seen in Tab.3.1.

Modulation strategy	THD
Synchronized pulses	4.498%
Interleaved pulses	1.978%
Three level SVM for parallel inverters	1.418%
Three level SVM for NPC	1.417%

Table 3.1: *Load current THD for the different modulation strategies*

3.3.4 Phase voltages and line-to-line voltages



(a) Synchronized pulses

(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

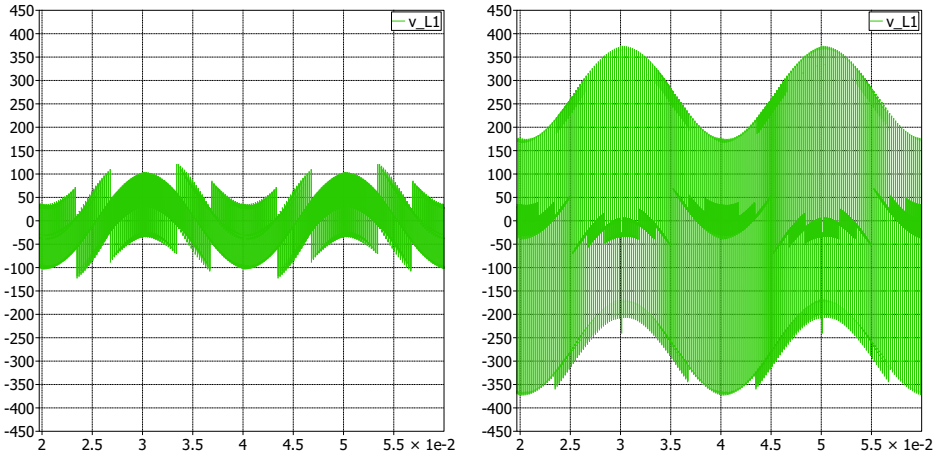
(d) NPC inverter

Figure 3.16: *Comparison of v_{Apcc0} and $v_{ApccBpcc}$*

From Fig.3.16(b) it can be seen that interleaving inverters will give a better representation of the voltage, since there will be more levels on the voltage. However, the levels are all starting from the middle value (zero). The reason for this is discussed in section 2.2. It

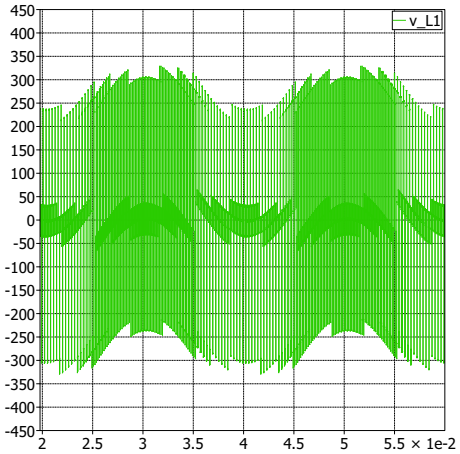
should be noted that the voltage levels will be influenced by L1 and L2, therefore they will fluctuate up and down but it is still possible to see the different levels. This is not the case for the NPC inverter, since it is possible to see the line-to-line voltage for this inverter without the influence of any inductors. It can be seen in Fig.3.16(c) that the proposed three-level SVM strategy for parallel inverters will create the same amount of levels as the NPC inverter in Fig.3.16(d). From the measured RMS value for the different strategies it looks like the voltages has different values. However if the voltages are measured only over the load resistor, the phase voltages for all strategies will be 196 V(RMS) $\pm$0.8%, so the different strategies will produce the same voltage from the same reference.

3.3.5 Stresses for sharing inductors with parallel inverters



(a) Synchronized pulses

(b) Interleaved pulses



(c) Three-level SVM for parallel inverters

Figure 3.17: *Comparison of the stresses for sharing reactor L1*

Taking a look at the voltages over the sharing inductors for the different modulation strategies, it becomes clear that the lowest voltage stress will appear for the synchronized pulses method. Remembering that the individual inverter currents had a much bigger ripple for the two other modulation strategies (Fig.3.14(b) and Fig.3.14(c)), the explanation for the higher voltage stress can be derived.

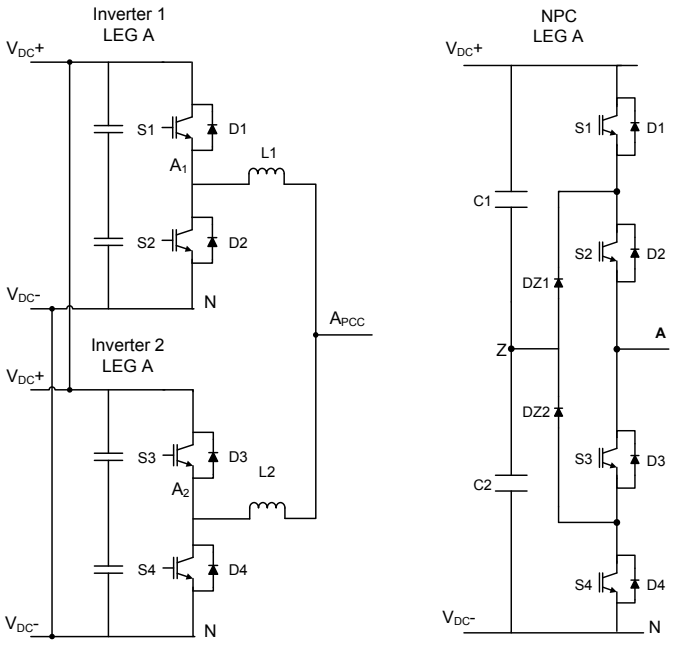
The voltage induced in an inductor

$$v_L(t) = L\frac{di_L}{dt} \tag{3.3}$$

From Eq.3.3 it can be understood why the voltage has a higher peak value in Fig.3.17(b) and Fig.3.17(c). If the current ripple is higher, then the rate of change for the current will also be higher. This means that the induced voltage in the inductor will be higher.

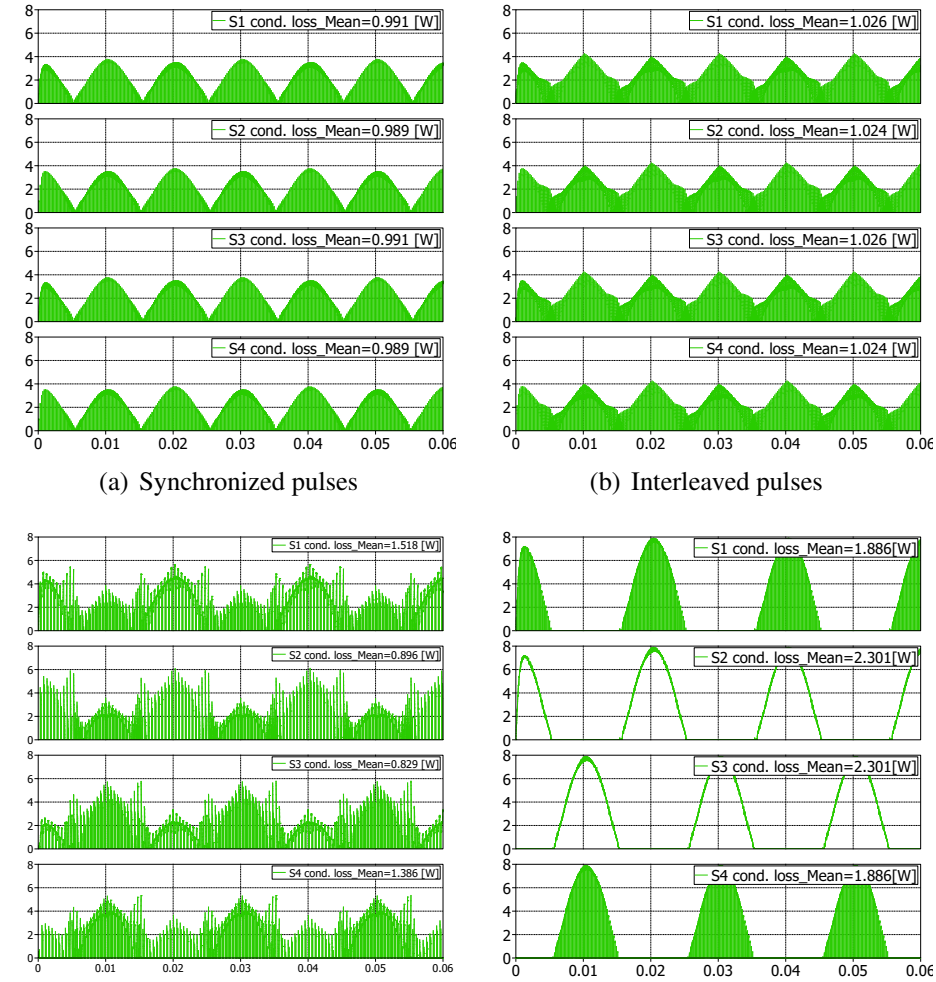
3.3.6 Switching and conduction losses

Fig.3.18(a) presents the phase leg A for the parallel two-level inverters and Fig.3.18(b) presents the phase leg A for the NPC inverter. The figures are introduced to refresh the readers memory of what S1, S2, S3 and S4 will represent in the two different topologies.



(a) Parallel inverters (b) NPC inverter

Figure 3.18: *The two different topologies*

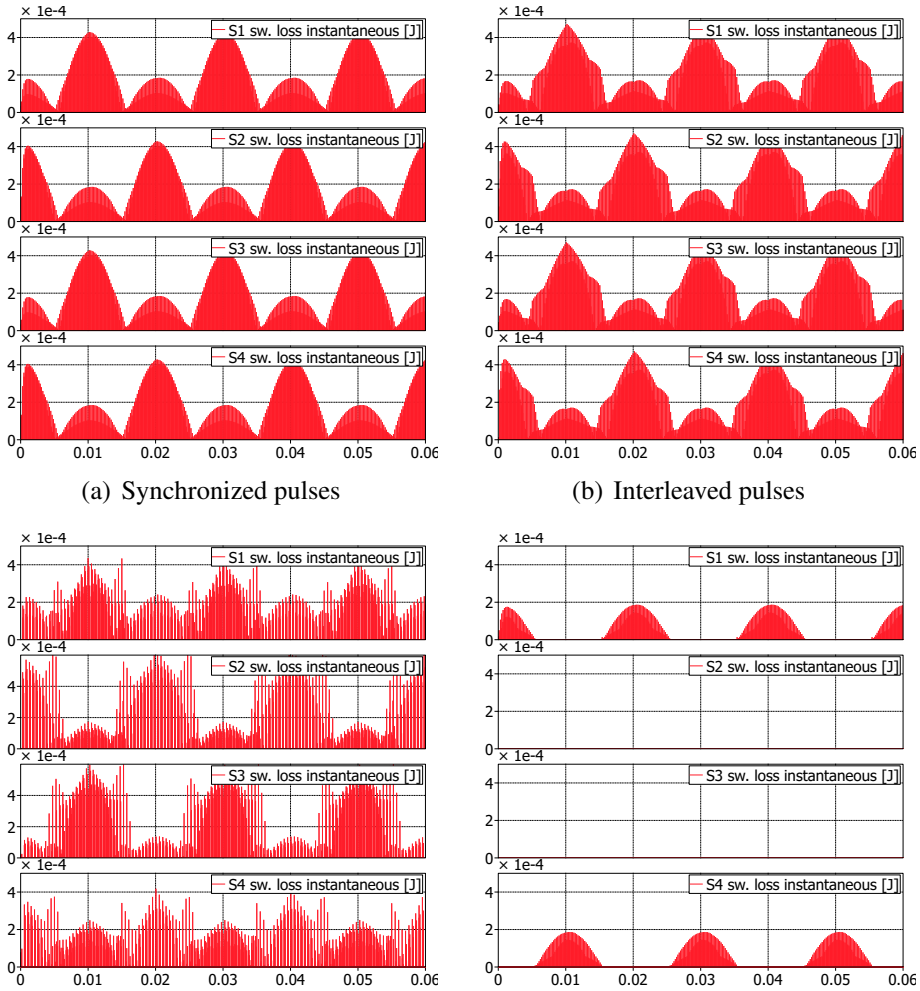


(a) Synchronized pulses (b) Interleaved pulses

(c) Three-level SVM for parallel inverters (d) NPC inverter

Figure 3.19: *Conduction losses for the different strategies Leg A*

The conduction losses is perfectly distributed in the synchronized and interleaved strategy. This can be seen in Fig.3.19(a) and Fig.3.19(b) respectively. The conduction losses for the interleaved strategy are a bit higher since the switches has to conduct the circulating current also. The situation for the three-level SVM for parallel inverters is opposite than for the NPC. In the NPC the middle switches S2 and S3 will have to take the highest conduction losses. This is because S1 will switch on and off during the transition between P and H while S2 will always be on. The same goes for the transition between H and O, where S4 will switch but S3 will always be on. In the three-level SVM for parallel inverters S1 and S4 experience the highest conduction losses. A propable cause for this can be seen in Fig.3.14(c). It can be seen that the two inverter currents are slighty offset. As said previously, this indicates that a dc current is circulating in the system through S1 and S4 and will therefore give higher conduction losses than for S2 and S3. A solution for this could be to use a balancing controller that gives small corrections to the duty cycles for the two inverters, and thus eliminating the dc offset.



(a) Synchronized pulses

(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

(d) NPC inverter

Figure 3.20: *Switching losses for the different strategies Leg A*

The switching losses in Fig.3.20 are displayed as instantaneous values measured in Joule [J]. Switching losses can be calculated as:

$$P_{SW.LOSS} = (e_{TURNON} + e_{TURNOFF}) \cdot f_{SW} = [W] \tag{3.4}$$

The value for the turn-on and turn-off losses are not the same for the whole fundamental period, so the value will be set to an average value for the turn-on loss of 0.25 [mJ] and turn-off loss of 0.2 [mJ] for the three modulation strategies for the parallel inverters. For the NPC inverter the average turn-on loss is set to 0.1 [mJ] and for the turn-off loss to 0.08 [mJ].

This gives a switching loss for the different modualtion strategies of:

- Synchonized pulses, interleaved pulses, proposed three level SVM = 2.25 [W]

- NPC (only S1 and S4)= 0.9 [W]

The switching losses are evenly distributed in all modulation strategies except for the NPC. For the NPC inverter the losses in S2 and S3 are so small that they are almost neglectable. So all of the switching losses appear in S1 and S4. Fig.3.20(c) shows that it is possible to distribute the switching losses evenly between the switches in the three-level SVM for parallel inverters while creating the same voltage levels as the NPC inverter. It can not be concluded that the actual switching losses are higher or lower in the NPC since the inverter topology is different than for the parallel system and will therefore not have the same issues like circulating currents and current sharing. The IGBTs for the NPC will also only experience half of V_D, while in the parallel system all switches experience V_D. The only conclusion that can be drawn from Fig.3.20 is that the switching losses are evenly distributed in the three-level SVM for parallel inverters.

3.4 Conclusion

The proposed three-level SVM for parallel two-level inverters has been derived in this chapter. The method is developed with the reduction of THD in mind by using the same "level"technique used in the NPC inverter. In order to achieve this, the standard three-level SVM has been modified to suit the parallel inverter system. In the simulation, the modified three-level SVM strategy for parallel inverters can operate with a carrier frequency of 8[kHz] giving an average switching frequency for the inverters of 5[kHz].

Four different modulation techniques has been simulated. Synchronized pulses, interleaved pulses and the proposed three-level SVM have been used for the system of two parallel connected two-level inverters. The "normal"three-level SVM has been used for the NPC inverter. The different strategies each have their drawbacks and benefits. From the results obtained from the simulation it can be seen that the synchronized pulses has the best performance with regards to circulating currents, stresses on the sharing inductor and simplicity in implementation. The interleaved strategy gives a reduction in the THD of more than 50% compared to the synchronized pulses, but will have to deal with issues like circulating currents and high voltage stresses for the sharing inductors. Compared to the interleaved strategy, the proposed three-level SVM for parallel inverters achieves a lower THD, lower voltage stresses on the sharing inductor and more and better levels on the line-to-line and phase voltages. However, the proposed strategy has the highest currents in the dc-link and will have to deal with an offset in the inverter currents created by a low frequency current, or possibly a dc current circulating in the system.

The conduction and switching losses are evenly distributed in the synchronized pulses strategy and in the interleaved strategy. The proposed strategy inherits better performance than the NPC with regards to distributing the switching losses. In terms of the conduction losses, the proposed strategy should give an even distribution but this is not the case for this simulation. As discussed in this chapter, the reason for this is propably a low frequency or dc current circulating in the system.

Laboratory experiments

4

In this chapter the setup in the lab will be described and the equipment used for the measurement and implementation will be listed. The implemented protection for the inverters will be explained, before the chapter continues with a comparison of the results obtained from the different modulation methods. At the end of the chapter there will be a conclusion.

4.1 Laboratory setup

Fig.4.1 shows the test setup in the laboratory. The three-phase resistor cannot be seen, since it is placed on the floor.

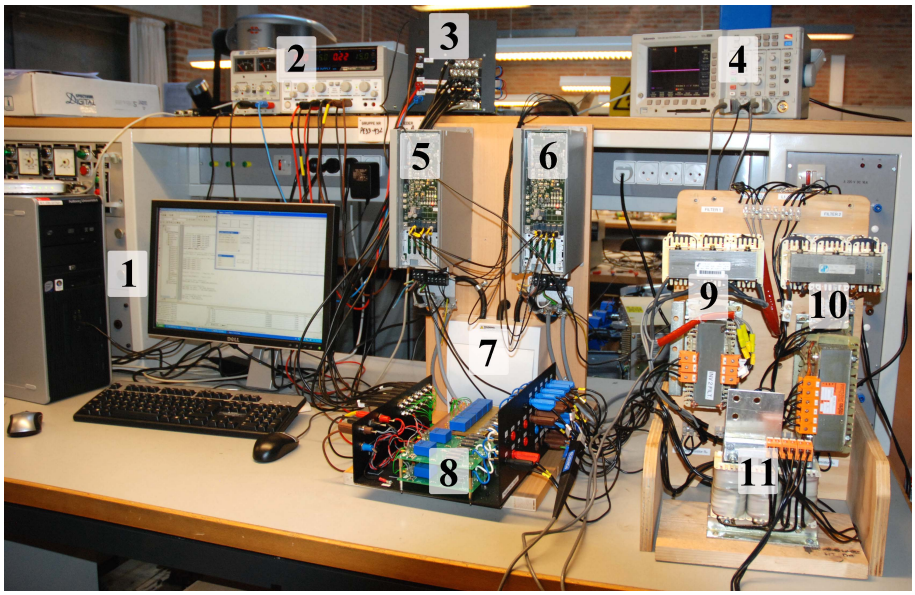


Figure 4.1: *Picture of test setup in the laboratory*

1. Computer used for programming and controlling the DSP
2. DC power supplies for expansion boards and measurement boards
3. DSP with the expansion boards
4. Oscilloscope for taking measurements
5. VLT 1

6. VLT 2
7. Circuit breaker on the mains supply for each inverter
8. Measurement boards (LEM)
9. Inductors L1
10. Inductors L2
11. Common inductor

Fig.4.2 shows the schematics of the setup of the test system in the lab.

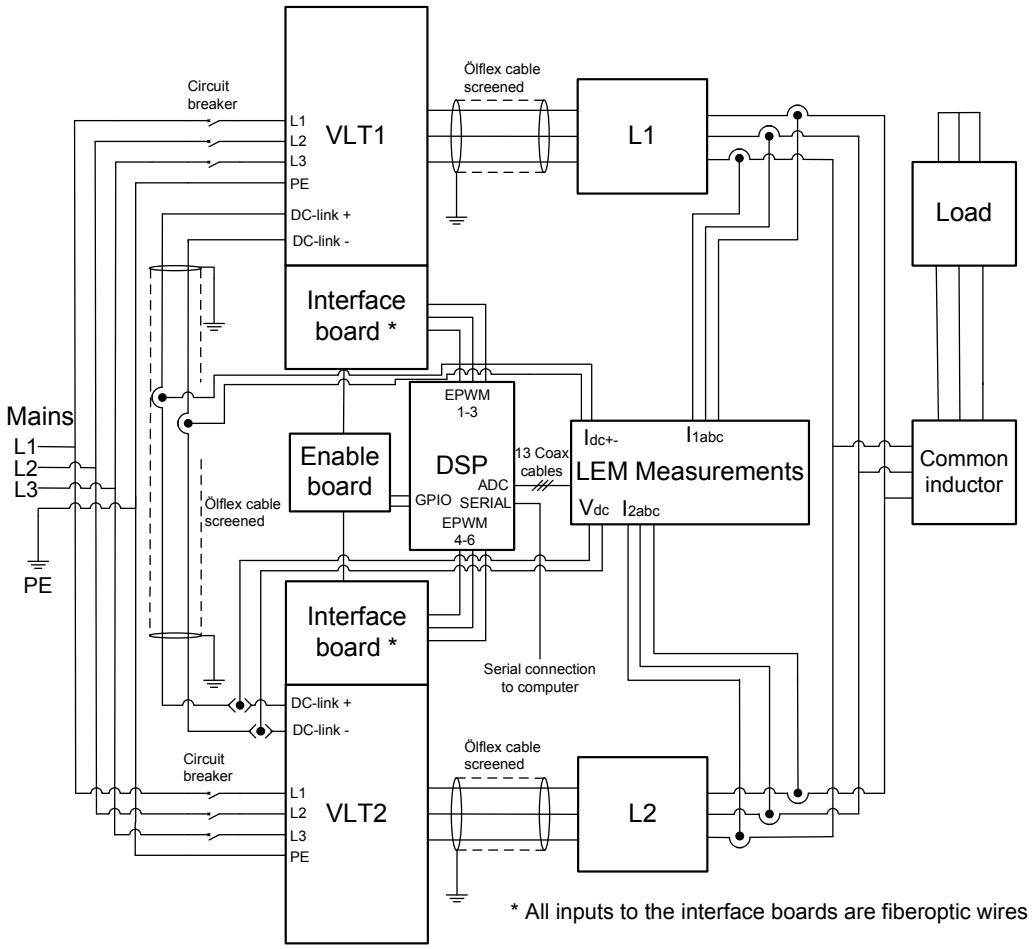


Figure 4.2: *Schematics of the test setup in the laboratory*

The measurement board and the expansion boards were designed in the 9th semester project: "Control of parallel inverters"[19]. The measurements are taken with LEM modules, and the current signal from the LEM modules are converted to voltage signals readable for the DSP (0-3V) in the expansion boards. The expansion boards also contain protection against over voltage on the DSP.

Tab.4.1 presents the main equipment used in the test setup in the laboratory.

VLT	2x Danfoss FC-302P2K2
DSP	TI TMS320F28335
Circuit breaker	2x Merlin Gerlin C60N B6 three-phase
DC power supply	GW INSTEK GPS-4303
DC power supply	GW GPS-3030
Oscilloscope	Tektronix TDS3014B with FFT module
Current Probe	3x Tektronix TCP202
Voltage probes	3x Tektronix P5200 High voltage differential probe

Table 4.1: *Main components used in the test setup*

Code Composer Studio (v.3.3) was used to implement the different modulation strategies on the DSP. The DSP used in the test setup is the eZDSP TMS320f28335 manufactured by Texas Instruments[20][21]. This is a floating point DSP with an internal clock of 150MHz. The DSP contains different modules, where the most important modules used in the project were:

- Enhanced Pulse Width Modulation (EPWM)
- Analogue to Digital Conversion (ADC)
- Serial Communication Interface (SCI)

The c-code for the proposed three-level SVM for parallel inverters are included in Appendix E, and all the code used in Code Composer Studio for the different modulation techniques can be found on the CD-ROM attached to the report.

4.2 Laboratory protections

Inverters are exposed to risk of high circulating currents flowing between them through the dc-link (due to parallel connection). Several protections has been implemented, both software and hardware:

- Circuit braker on the input of rectifier (hardware).
- Overcurrent and overvoltage protection on the interface boards to each inverter (software).
- Overcurrent protection on the output of the VLT implemented on the DSP (software). The following test, Fig.4.3, has been made for current protection set to $i_{A1} = 2[A]$. The disable signal has light blue colour. When the inverters are on, the disable signal has low value. The time which it takes to switch off inverters,

after the current (dark blue signal) hit the desired value, is equal to computation time of the programe.

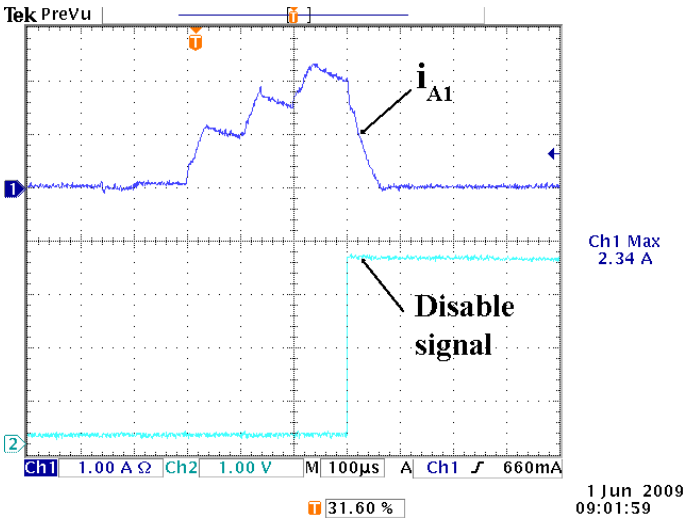


Figure 4.3: *Overcurrent in individual inverter currents*

- Overcurrent protection on the dc-link implemented on the DSP (software). The following test has been made to verify the proper work of dc-link current protection, Fig.4.4. The idea behind this protection is very similar to phase current protection. The value of dc-link current for which inverters tripped is set to $i_{dclink} = 2[A]$. When the dc-current (dark blue signal) hit the desired value the disable signal is sent to inverters (light blue signal changes to high value).

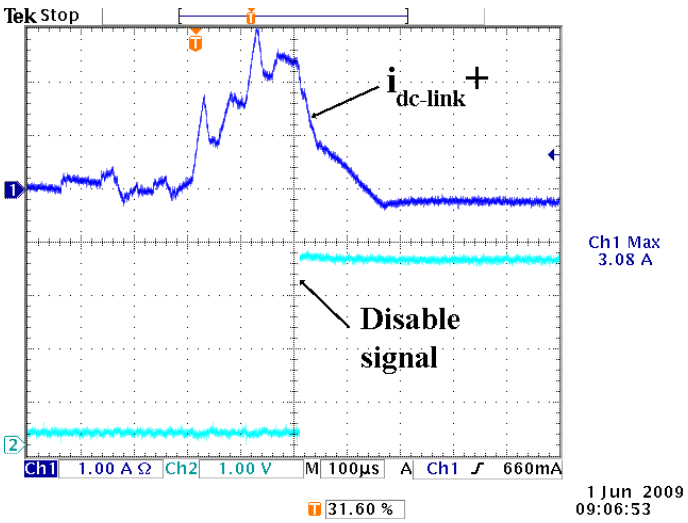


Figure 4.4: *Overcurrent protection in dc-link*

4.3 Laboratory measurements

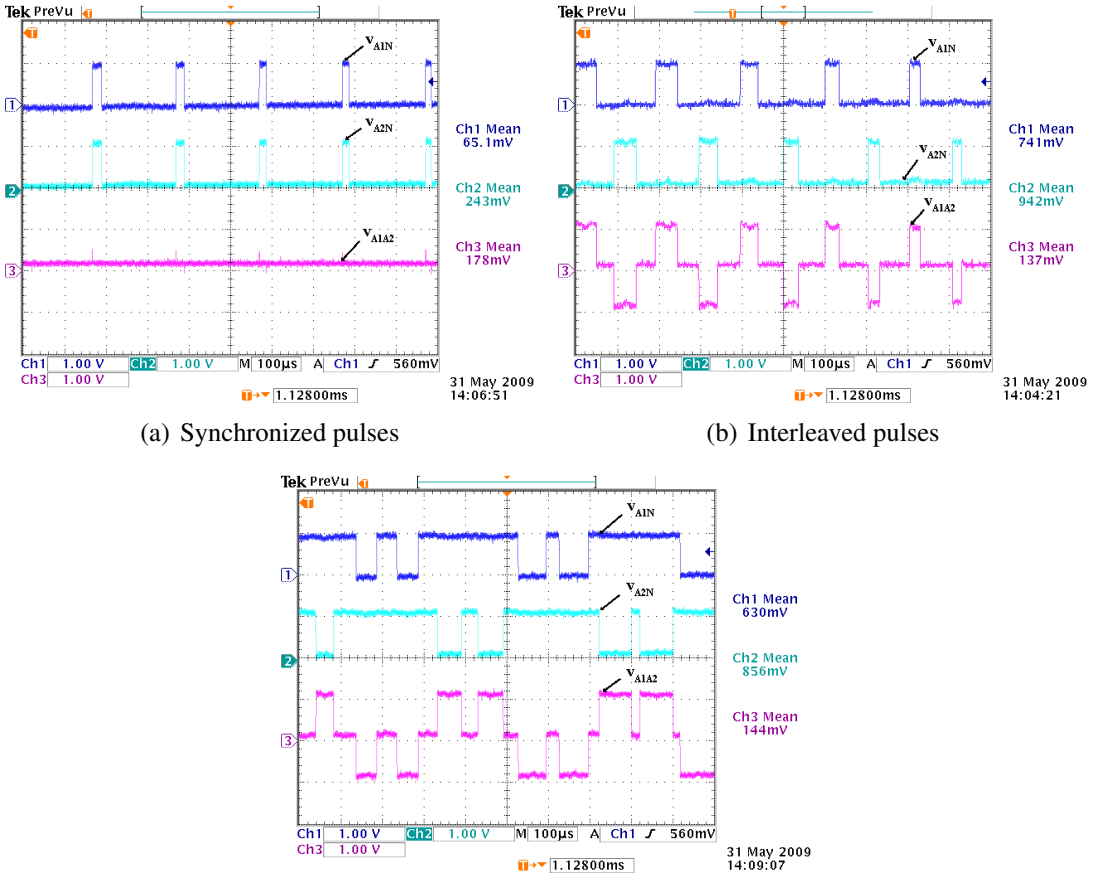
The carrier frequency in the DSP has been increased to $f_{carrier} = 10[kHz]$ in order to obtain $f_{switching} = 5[kHZ]$. Carrier frequency in the laboratory differs from the carrier frequency established in the simulation due to the fact that some of the pulses are lost in the DSP implementation. Every result obtained for the voltage measurements has to be recalculated according to scale of differential probe:

Volts per division	**Real voltage**
1	$500[V]$
$.5$	$250[V]$
$.2$	$100[V]$
$.1$	$50[V]$
$50m$	$25[V]$
$20m$	$10[V]$
$10m$	$5[V]$
$5m$	$2.5[V]$
$2m$	$1[V]$

Table 4.2: *Voltage probe scale.*

In order to compare three different kind of modulation for the system of parallel connected inverters and verify the simulations results following measurements has been taken:

4.3.1 Voltages between phase A of individual inverters and neutral point; voltages between phase A of inverter one and phase A of inverter two



(a) Synchronized pulses

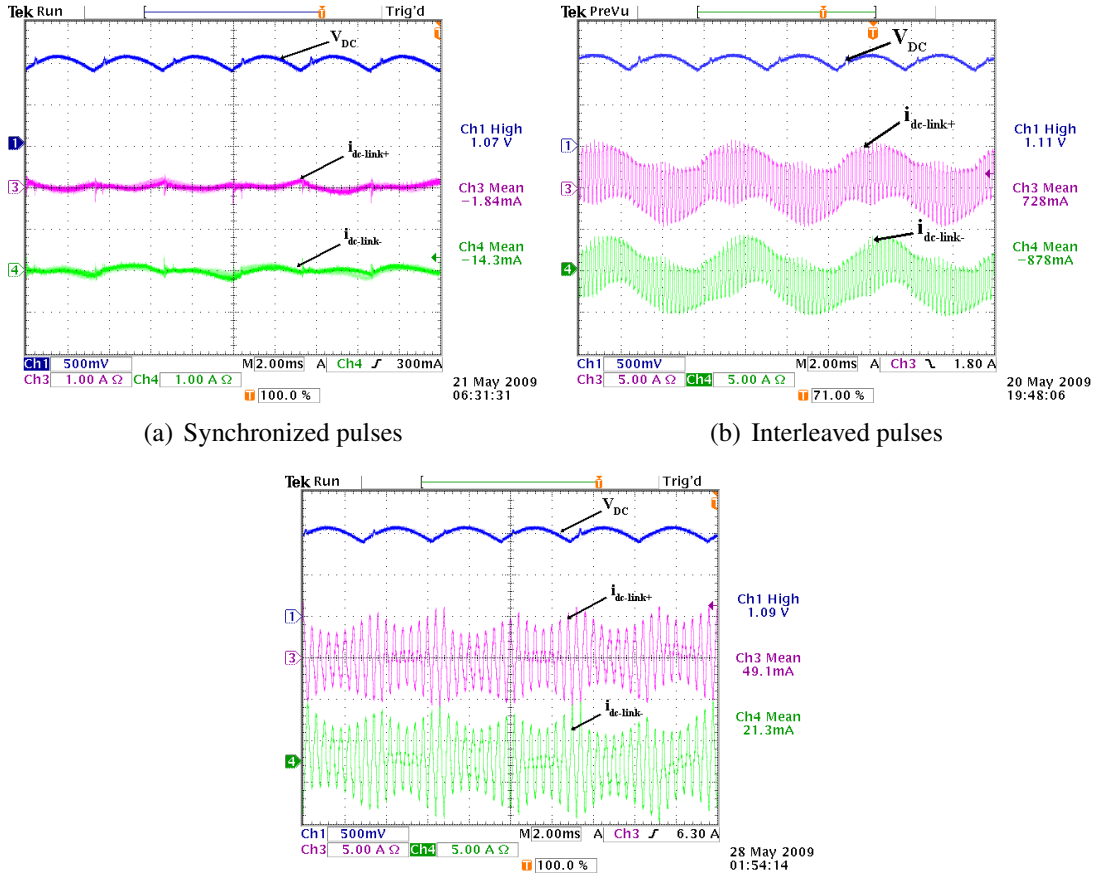
(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

Figure 4.5: *Comparison of* v_{A1N}, v_{A2N} *and* v_{A1A2}

The voltages v_{A1N} and v_{A2N} in Fig.4.5(a) are exactly the same (pulses synchronized method). This gives the value of $v_{A1A2} = 0$. In interleaved method pulses are shifted between each other $180°$, Fig.4.5(b), which results in different output voltages for inverters. The voltage v_{A1A2} is created, but taking into consideration one sampling period the avarage value is closed to zero. Using proposed three-level SVM strategy the v_{A1A2} also exist but during two switching periods $t = 400[\mu s]$ the avarage value of this voltage is very close to zero.

4.3.2 DC-link measurements



(a) Synchronized pulses

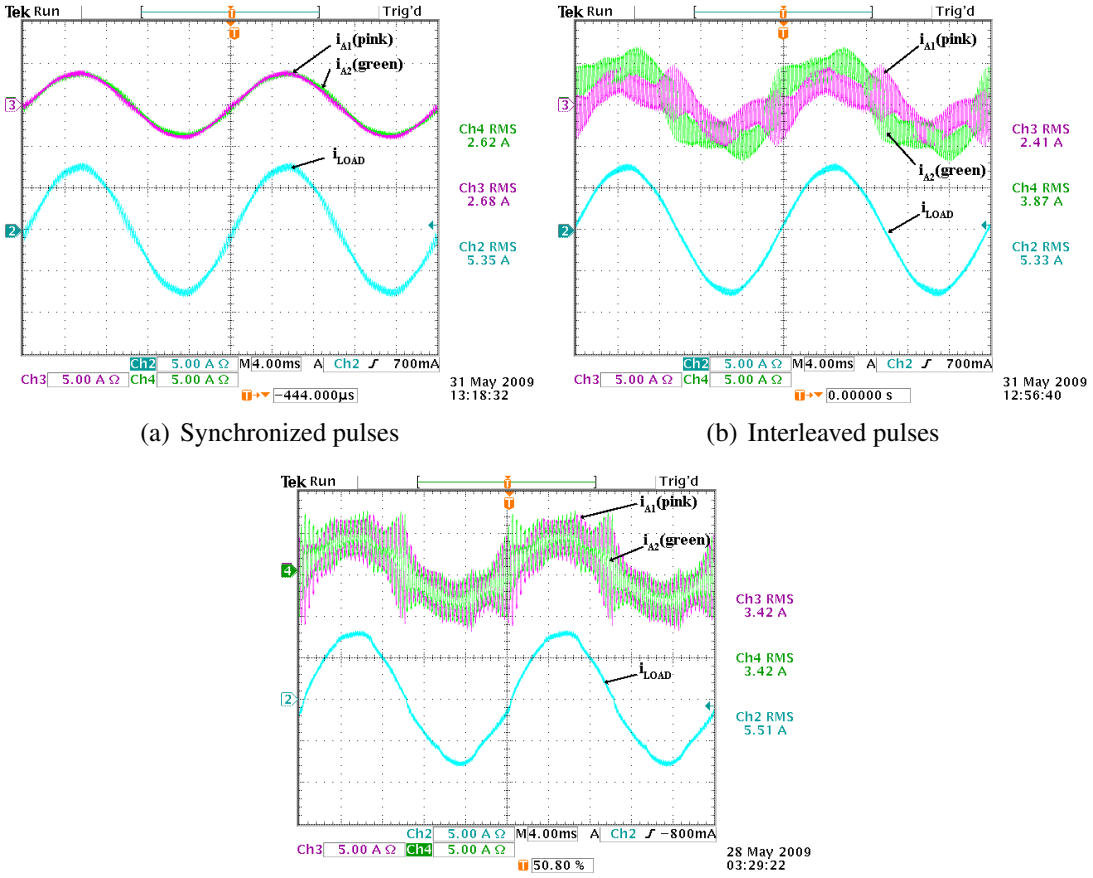
(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

Figure 4.6: *Comparison of the currents in the dc-link and dc-voltage.*

The measurements of the currents on the dc-link has been taken in order to check if any circulating currents appear in the system. For the pulses synchronized method presented on the Fig.4.6(a) the mean value of the currents are almost zero, $i_{dclink+} = 0.00184[A]$ and $i_{dclink-} = 0.0143[A]$. For the interleaved method the mean values of dc-link currents are: $i_{dclink+} = 0.728[A]$ and $i_{dclink-} = -0.878[A]$ (these values will be further discussed in the next subsection). For three-level SVM the mean values of dc-link currents are: $i_{dclink+} = 0.049[A]$ and $i_{dclink-} = 0.021[A]$. The occurrence of circulating currents in interleaved and three-level SVM methods has been explained in section 2.2. The results from this measurements are related to measurements of inverter output voltages and voltage between A phase of inverter one and a phase of inverter two, presented in the section 4.3.1. When v_{A1N}, v_{A2N} where exactly the same there were no circulating currents flowing through circuit like in Fig.4.5(a). The currents in the dc-link appear only in system where v_{A1N} and v_{A2N} have different values like on the Fig.4.5(b), 4.5(c).

4.3.3 Individual inverters and load currents measurements



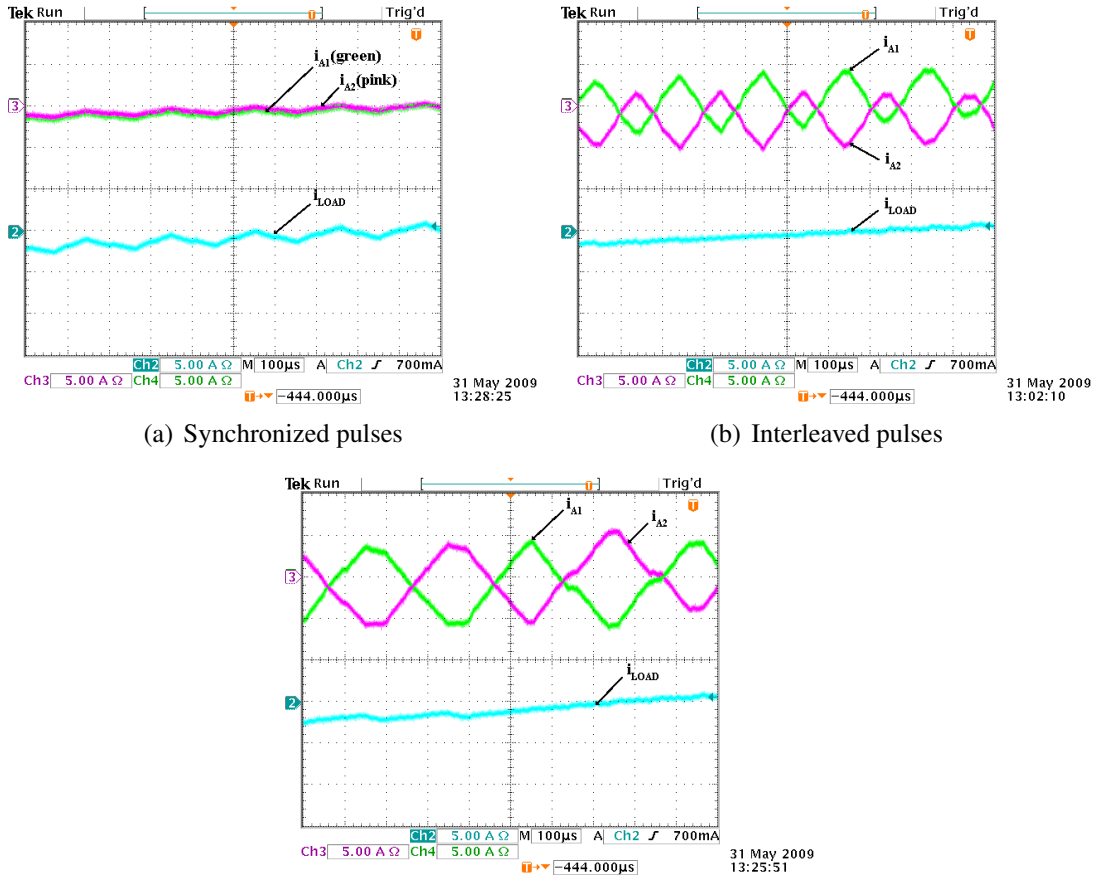
(a) Synchronized pulses

(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

Figure 4.7: *Comparison of the currents in each inverter and the load current.*

The individual currents of each inverter and load currents are presented in this section. As it can be observed on the Fig.4.7(a) the currents has smooth sinewave shape, and they have similar RMS value: $i_{A1} = 2.62[A]$ and $i_{A2} = 2.68[A]$. This results in sinewave load current of RMS value: $i_{LOAD} = 5.35$. In interleaved method ,Fig.4.7(b), the individual currents are distorted and not following each other perfectly due to the problem of implementation/hardware, having RMS value: $i_{A1} = 2.41[A]$ and $i_{A2} = 3.87[A]$ (these values explain the high mean value of dc-link currents presented on the Fig.4.6(b)). In this method the load current has more smooth sinewave curve than in pulse synchronized strategy due to elimination on the load branch current ripples coming from individual inverters branches. In the last modulation technique (three-level SVM) individual currents (with RMS value: $i_{A1} = 3.42[A]$ and $i_{A2} = 3.42[A]$) of the same phase are following each other but they are more distorted than in pulse synchronized method. The resultant current on the load branch has smooth sinewave curve (with RMS value of $i_{LOAD} = 5.51[A]$) comparable to interleaved method load current.



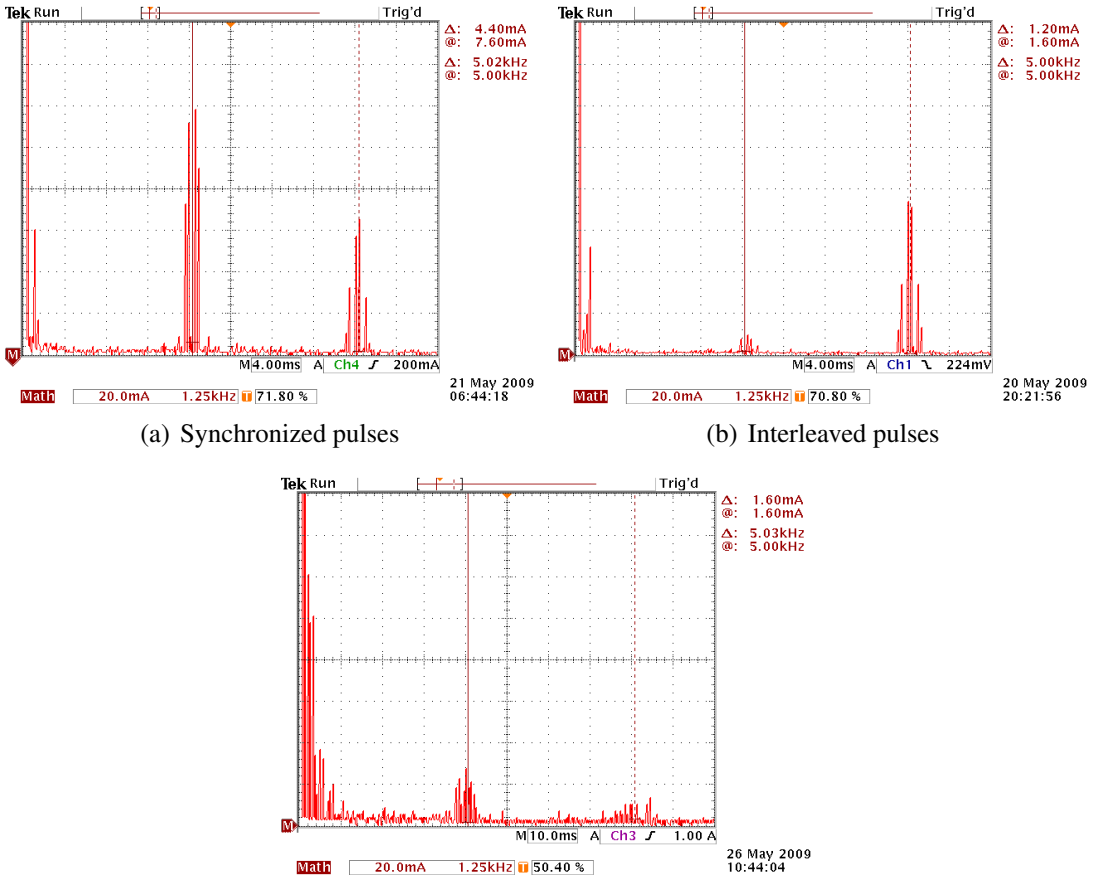
(a) Synchronized pulses

(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

Figure 4.8: *Comparison of the currents in each inverter and the load current.*

The above figures are showing the zoom view of the individual inverters currents (i_{A1} and i_{A2}) and resultant current in the load branch (i_{LOAD}) of phase A. For the pulses synchronized method ,Fig.4.8(a), the ripples in individual inverters currents are summerized in load current. For the two other methods, Fig.4.8(b) and 4.8(c), the inverters current ripple are opposite which result in elimination of them in the load current.



(a) Synchronized pulses

(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

Figure 4.9: *Harmonic spectrum for different kind of modulation.*

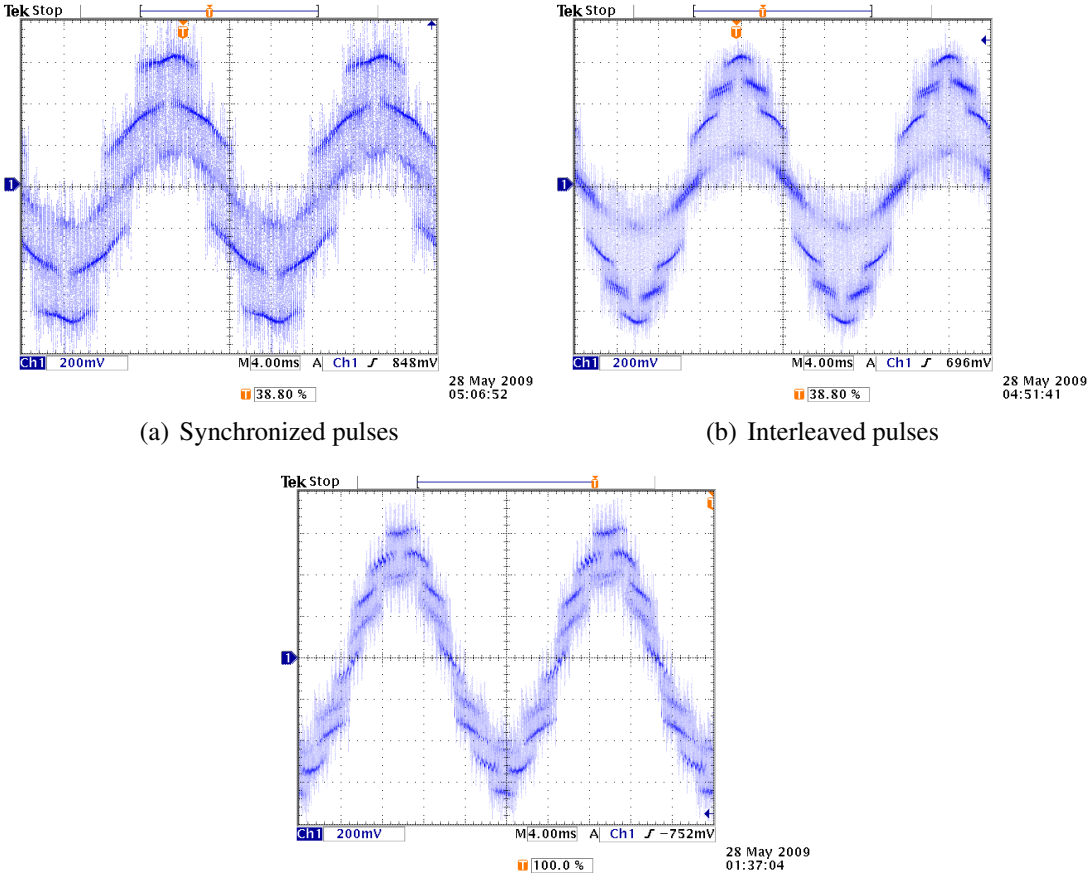
On the figure above the harmonic spectrum of the load currents is presented. For the pulses synchronized method the significant harmonic component appears at the switching frequency ($f_{sw} = 5kHz$) and integer multiplication of this frequency, as is depicted on the Fig.4.9(a). In pulses shifted technique it was possible to circumscribe harmonic component coming from the switching frequency, Fig.4.9(b). In the three-level SVM strategy it was also possible to limit harmonics coming from switching frequency and integer multiplication of this frequency. The drawback of three-level SVM is visible in harmonic spectrum at low frequencies, where significant components appear, which could be refered to shape of load current presented on the Fig.4.7(c). In the three-level SVM technique to obtain switching frequency of $f_{switching} = 5[kHz]$ the frequency of the carrier signal was increased to $f_{carrier} = 10[kHz]$. The data from the laboratory scope has been imported to Matlab/Simulink environment, where THD has been calculated. The table 4.3 presents the THD of different modulation strategies.

As it can be observed the highest THD is observed in the proposed three-levelSVM method (due to implementation problems). This result does not confirm the simulation result. The best performance introduce interleaved method where $THD = 3.25\%$.

Modulation strategy	THD
Synchronized pulses	5.2%
Interleaved pulses	3.25%
Three level SVM for parallel inverters	6.26%

Table 4.3: *Load current THD for the different modulation strategies*

4.3.4 Phase voltages and line-to-line voltages measurements



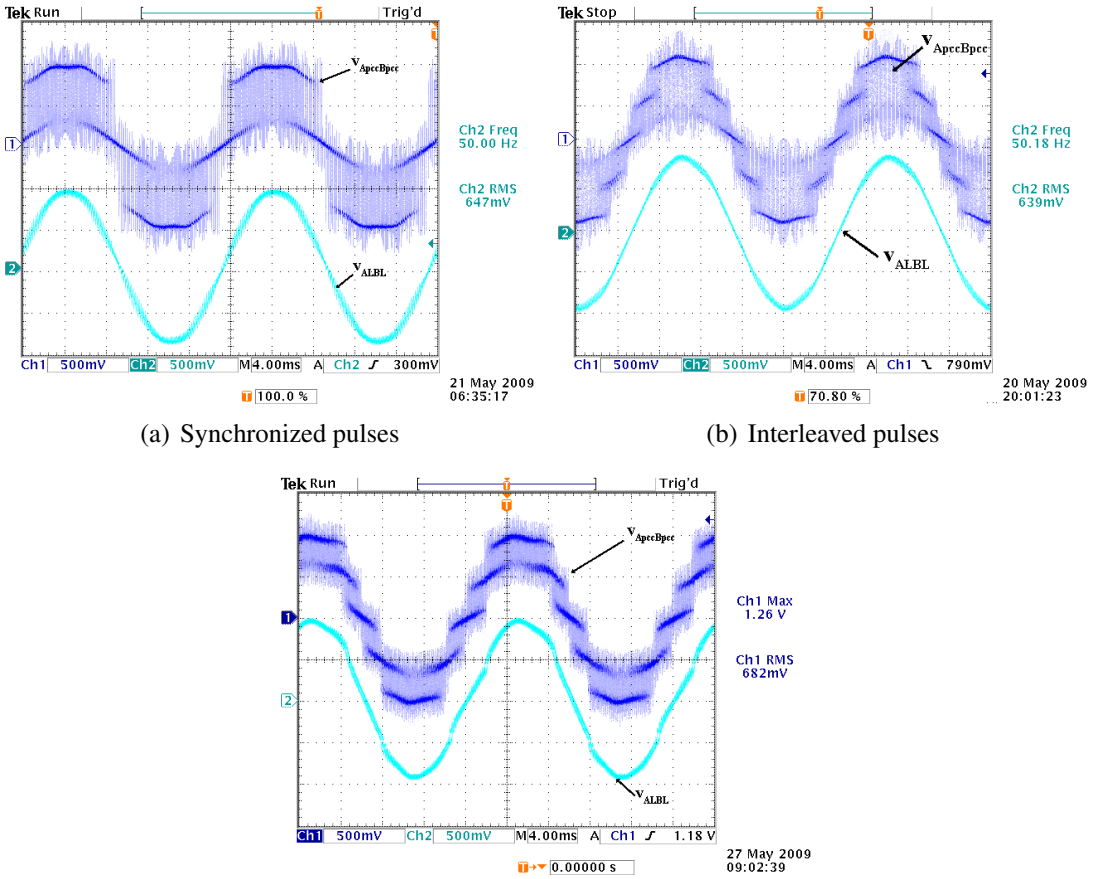
(a) Synchronized pulses

(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

Figure 4.10: *Comparison of the A-phase voltages on the RL-load.*

The main idea of presenting A-phase voltages on the RL-load was to compare the number of voltage levels. The worst performance in this measurements has pulse synchronized method, Fig.4.10(a), where the load voltage is created only from five levels. For interleaved method the load voltage is created from seven voltage levels, Fig.4.10(b). The three-level SVM technique presents the best performance, where load voltage is created from nine levels.



(a) Synchronized pulses

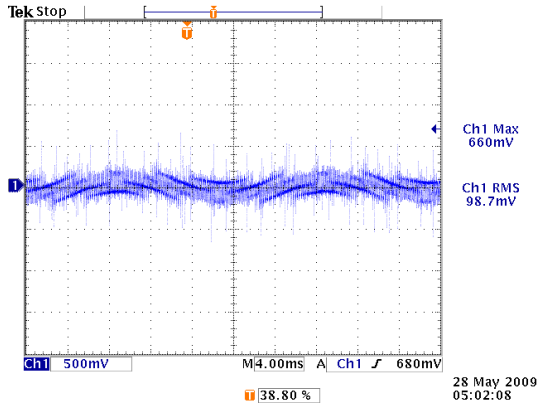
(b) Interleaved pulses

(c) Three-level SVM for parallel inverters

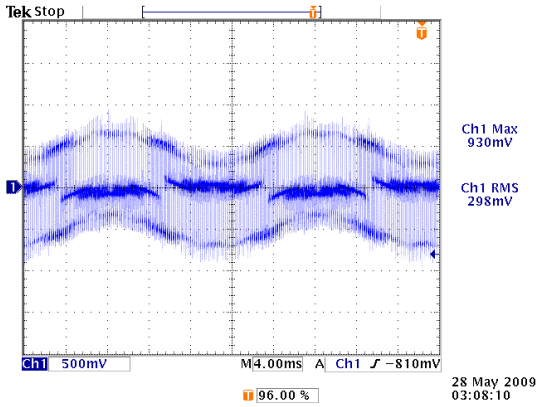
Figure 4.11: *Comparison of the line-to-line voltages before and after load filter.*

Fig.4.11(a), 4.11(b), 4.11(c) are showing line to line voltages before and after load filter. In line-to-line voltage before filter different voltage levels are visible for different modulation techniques. The same like for load voltages the best performance can be indicated in proposed three-level SVM method where line-to-line voltage is created from five levels. The pulses shifted method contains the same amount of levels as proposed method but the difference of voltage between different levels are higher than in three-level SVM. The RMS value of line-to-line voltage for pulses synchronized, shifted and three-level SVM are approximately: $V_{ApccBpcc} = 346[V]$, $V_{ApccBpcc} = 339.4[V]$ and $V_{ApccBpcc} = 353.5[V]$ respectively.

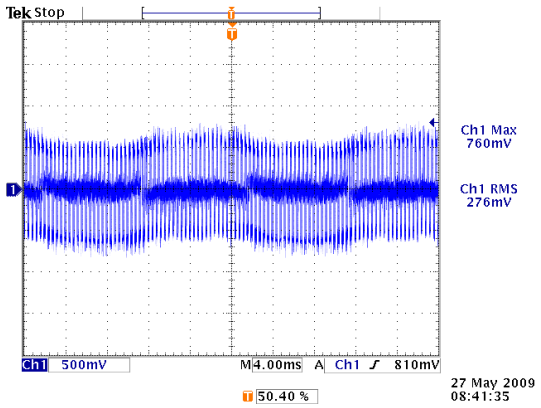
4.3.5 Stresses over inverter inductor measurements



(a) Synchronized pulses



(b) Interleaved pulses



(c) Three-level SVM for parallel inverters

Figure 4.12: *Comparison of stress on inverter one A-phase inductor.*

Fig.4.12(a), 4.12(b) and 4.12(c) present stresses on inverters inductors for different modulation techniques. The highest stresses can be noticed for pulses shifted method and three-level SVM where peaks of the voltage are up to $v_{peak} = 375[V]$. The best performance in case of stresses over the inductors introduce pulse synchronized method with voltage peaks around $v_{peak} = 100[V]$.

4.4 Conclusion

The laboratory setup has been improved (comparing to setup [19] used in previous semester) with new protections: three-phase circuit braker in the hardware and dc-link current protection in the software. Several tests have been performed to check proper work of protection. The DSP code for three-level SVM technique has been developed,

together with code for pulses shifting method. Several measurements have been taken for the different modulation strategies in order to compare them. Regarding to circulating currents, pulses synchronized method introduced the best performance. The circulating currents are not created in this method. In interleaved and proposed three-level SVM strategies the voltage v_{A1A2} is very small but not zero, which results in possibility of creation circulating currents. The currents of individual inverters has the best sinewave curve in pulses synchronized method, but the ripples are summerized at the load currents. In interleaved method the inverters currents are not identically the same but the ripples are eliminating each other on the load. The same situation of ripple elimation is introduced in proposed modulation technique but the individual currents are following each other. Also the low frequency component is introduced in three-level SVM due to problem of implementation/hardware. Regarding the load voltage, line-to-line voltage and voltage between common A and neutral point (v_{ApccN}), the highest performance is introduced in proposed three-level SVM, where these voltages are created of the highest number of levels.

The results obtained in the laboratory differ from the results obtained in the simulations. This could be explained by the fact, that the filter components are not equal (components have been randomly found in the laboratory). Also the load three-phase resistance is not perfect balanced. In simulation everything is ideal, but in the implemented system there can be small differences.

Proposed modulation method for parallel connected inverters introduced good performance regarding to many levels in line-to-line voltage - five levels, load voltage - nine levels. Also the load currents looks very smooth (elimination of high frequency components) but the low frequency component is visible, probably due to problems in implementation and poor filter and load components. This method could also be improved by adding current controller to the system.

5 Conclusions

The proposed three-level Space Vector Modulation for parallel connected inverters has been tested in simulation and implemented on a DSP based setup in the laboratory. The proposed modulation strategy is compared to two other modulation strategies for parallel inverters, synchronized pulses and interleaved pulses, in simulation and in the test setup in the laboratory. A simulation model of the three-level NPC inverter with three-level Space Vector Modulation is realized for comparison with the proposed modulation strategy because of their similarity in terms of voltage levels and number of switches.

From the three modulation strategies for parallel two-level inverters, it is only the proposed strategy which is able to create voltage levels similar to a three-level inverter. This has been verified in simulations and also from results obtained from the test setup. The use of more voltage levels will give a better representation of the fundamental voltage and therefore a lower harmonic content in the current. This is true for the simulation, where the proposed strategy inherits the same performance as the three-level NPC inverter with regards to voltage levels. This results in a load current THD which is similar to that of the NPC inverter. Laboratory results show that when the proposed strategy is implemented on the test setup, it will have the highest load current THD among the three strategies for parallel inverters. The DSP based platform is currently not able to recreate the same pulses for one fundamental period as in the simulation. This means that some of the pulses are "lost", leading to a waveform that is distorted by a low frequency component. This is why the proposed strategy is penalized with respect to the load current THD.

The system of parallel connected inverters has still possibility to transfer power in case if one of the power modules fails. This increases the reliability of the system comparing to single inverter. Since the system of parallel connected inverters is more complex (due to higher number of components like power devices, control boards, etc.) there is a higher possibility of failure in one component. The proposed modulation technique is only possible to realize if all inverters are working. If one of them fail, the modulation strategy should be changed (this introduce more complex control of the system).

The results obtained from simulation and laboratory are gathered in tables 5.1, 5.2 respectively.

	Modulation technique			
Measurement	**P.synch.**	**Interleaved**	**Proposed**	**NPC**
v_{ApccN} levels	2	3	3	3
$v_{line-to-line}$ levels	5	7	9	9
v_{LOAD} levels	3	5	5	5
THD	4.498%	1.978%	1.418%	1.417%
dc-link currents	No	Yes	Yes	N/A
load currents ripple	High	Low	Very low	Very low

Table 5.1: *Comparison of simulations results of different modulation methods for the system of parallel connected inverters.*

	Modulation technique		
Measurement	**P.synch.**	**Interleaved**	**Three-level SVM**
v_{ApccN} levels	2	3	3
$v_{line-to-line}$ levels	5	7	9
v_{LOAD} levels	3	5	5
THD	5.2%	3.25%	6.26%
dc-link currents	No	Yes	Yes
load current ripple	High	Low	Low

Table 5.2: *Comparison of laboratory results of different modulation methods for the system of parallel connected inverters.*

5.1 Future work

- Improve test setup in order to obtain similar performance of the proposed method like in simulation (elimination of low frequency component in load current).
- Introduce current controller for load current and balancing controller for each inverter.
- Eliminate low frequency circulating currents.
- Measure the efficiency of the optimized parallel inverter system modulated with proposed strategy.

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Nomenclature

A

Parameters	***Description of parameters***
D_A, D_B, D_C	Duty cycles
$f_{carrier}$	Carrier frequency
$f_{SW}, f_{switching}$	Switching frequency
i_{A1}	Individual inverter one A-phase current
i_{A2}	Individual inverter two A-phase current
i_{load}	Load current
i_{dclink}	Current in the dc-link
i_L	Inductor current
I_{RATED}	Rated current
ma	Modulation index
N_{switch}	Number of switching signals
s_a, s_b, s_c	Switching signals
T_a, T_b, T_c	Dwell times
θ	Angle of rotation
T_S	Sampling time
v_{0N}	Common mode voltage
v_{A0}	Load voltage of A phase
V_{A1A2}	Voltage between two A phases of inverters
$v_{AB}, v_{ApccBpcc}$	Voltage between load A and B phase
v_{AN}	Voltage between individual inverter A phase and neutral point
v_{ApccN}	Voltage between common A phase and neutral point

Acronyms

B

Acronym	*Description of acronym*
AC	Alternating Current
ADC	Analogue to Digital Converter
ANPC	Active Neutral Point Clamped
DC	Direct Current
DSP	Digital Signal Processor
EPWM	Enhanced Pulse Width Modulation
L	inductance
NPC	Neutral Point Clamped
PV	Photo Voltaic
PWM	Pulse Width Modulation
R	resistance
SCI	Serial Comunication Interface
SVM	Space Vector Modulation
THD	Total Harmonic Distortion

Switching Sequence sector I-VI

C

SECTOR I								
Segment	**1**		**2**		**3**		**4**	
1st	$\vec{V}_0$	[OOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]
2nd	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{13}$	[POO]	$\vec{V}_7$	[PHO]
3rd	$\vec{V}_{2O}$	[HHO]	$\vec{V}_7$	[PHO]	$\vec{V}_7$	[PHO]	$\vec{V}_{14}$	[PPO]
4th	$\vec{V}_0$	[HHH]	$\vec{V}_{1P}$	[PHH]	$\vec{V}_{1P}$	[PHH]	$\vec{V}_{2P}$	[PPH]
5th	$\vec{V}_{2O}$	[HHO]	$\vec{V}_7$	[PHO]	$\vec{V}_7$	[PHO]	$\vec{V}_{14}$	[PPO]
6th	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{13}$	[POO]	$\vec{V}_7$	[PHO]
7th	$\vec{V}_0$	[OOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{2O}$	[HHO]

Table C.1: *Switching pattern for sector I*

SECTOR II								
Segment	**1**		**2**		**3**		**4**	
1st	$\vec{V}_0$	[OOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3O}$	[OHO]
2nd	$\vec{V}_{3O}$	[OHO]	$\vec{V}_8$	[HPO]	$\vec{V}_8$	[HPO]	$\vec{V}_{15}$	[OPO]
3rd	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3P}$	[HPH]	$\vec{V}_{14}$	[PPO]	$\vec{V}_8$	[HPO]
4th	$\vec{V}_0$	[HHH]	$\vec{V}_{2P}$	[PPH]	$\vec{V}_{2P}$	[PPH]	$\vec{V}_{3P}$	[HPH]
5th	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3P}$	[HPH]	$\vec{V}_{14}$	[PPO]	$\vec{V}_8$	[HPO]
6th	$\vec{V}_{3O}$	[OHO]	$\vec{V}_8$	[HPO]	$\vec{V}_8$	[HPO]	$\vec{V}_{15}$	[OPO]
7th	$\vec{V}_0$	[OOO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{2O}$	[HHO]	$\vec{V}_{3O}$	[OHO]

Table C.2: *Switching pattern for sector II*

SECTOR III								
Segment	**1**		**2**		**3**		**4**	
1st	$\vec{V}_0$	[OOO]	$\vec{V}_{3O}$	[OHO]	$\vec{V}_{3O}$	[OHO]	$\vec{V}_{4O}$	[OHH]
2nd	$\vec{V}_{3O}$	[OHO]	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{15}$	[OPO]	$\vec{V}_9$	[OPH]
3rd	$\vec{V}_{4O}$	[OHH]	$\vec{V}_9$	[OPH]	$\vec{V}_9$	[OPH]	$\vec{V}_{16}$	[OPP]
4th	$\vec{V}_0$	[HHH]	$\vec{V}_{3P}$	[HPH]	$\vec{V}_{3P}$	[HPH]	$\vec{V}_{4P}$	[HPP]
5th	$\vec{V}_{4O}$	[OHH]	$\vec{V}_9$	[OPH]	$\vec{V}_9$	[OPH]	$\vec{V}_{16}$	[OPP]
6th	$\vec{V}_{3O}$	[OHO]	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{15}$	[OPO]	$\vec{V}_9$	[OPH]
7th	$\vec{V}_0$	[OOO]	$\vec{V}_{3O}$	[OHO]	$\vec{V}_{3O}$	[OHO]	$\vec{V}_{4O}$	[OHH]

Table C.3: *Switching pattern for sector III*

SECTOR IV								
Segment	**1**		**2**		**3**		**4**	
1st	$\vec{V}_0$	[OOO]	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{5O}$	[OOH]
2nd	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{10}$	[OHP]	$\vec{V}_{10}$	[OHP]	$\vec{V}_{17}$	[OOP]
3rd	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{5P}$	[HHP]	$\vec{V}_{16}$	[OPP]	$\vec{V}_{10}$	[OHP]
4th	$\vec{V}_0$	[HHH]	$\vec{V}_{4P}$	[HPP]	$\vec{V}_{4P}$	[HPP]	$\vec{V}_{5P}$	[HHP]
5th	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{5P}$	[HHP]	$\vec{V}_{16}$	[OPP]	$\vec{V}_{10}$	[OHP]
6th	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{10}$	[OHP]	$\vec{V}_{10}$	[OHP]	$\vec{V}_{17}$	[OOP]
7th	$\vec{V}_0$	[OOO]	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{4O}$	[OHH]	$\vec{V}_{5O}$	[OOH]

Table C.4: *Switching pattern for sector IV*

SECTOR V								
Segment	**1**		**2**		**3**		**4**	
1st	$\vec{V}_0$	[OOO]	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{6O}$	[HOH]
2nd	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{17}$	[OOP]	$\vec{V}_{11}$	[HOP]
3rd	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{11}$	[HOP]	$\vec{V}_{11}$	[HOP]	$\vec{V}_{18}$	[POP]
4th	$\vec{V}_0$	[HHH]	$\vec{V}_{5P}$	[HPP]	$\vec{V}_{5P}$	[HPP]	$\vec{V}_{6P}$	[PHP]
5th	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{11}$	[HOP]	$\vec{V}_{11}$	[HOP]	$\vec{V}_{18}$	[POP]
6th	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{17}$	[OOP]	$\vec{V}_{11}$	[HOP]
7th	$\vec{V}_0$	[OOO]	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{5O}$	[OOH]	$\vec{V}_{6O}$	[HOH]

Table C.5: *Switching pattern for sector V*

SECTOR VI								
Segment	**1**		**2**		**3**		**4**	
1st	$\vec{V}_0$	[OOO]	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{1O}$	[HOO]
2nd	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{12}$	[POH]	$\vec{V}_{12}$	[POH]	$\vec{V}_{13}$	[POO]
3rd	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{1P}$	[PHH]	$\vec{V}_{18}$	[POP]	$\vec{V}_{12}$	[POH]
4th	$\vec{V}_0$	[HHH]	$\vec{V}_{6P}$	[PHP]	$\vec{V}_{6P}$	[PHP]	$\vec{V}_{1P}$	[PHH]
5th	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{1P}$	[PHH]	$\vec{V}_{18}$	[POP]	$\vec{V}_{12}$	[POH]
6th	$\vec{V}_{1O}$	[HOO]	$\vec{V}_{12}$	[POH]	$\vec{V}_{12}$	[POH]	$\vec{V}_{13}$	[POO]
7th	$\vec{V}_0$	[OOO]	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{6O}$	[HOH]	$\vec{V}_{1O}$	[HOO]

Table C.6: *Switching pattern for sector VI*

Switching states for two parallel two-level inverters

D

	Switching States			
Leg A	**O**	**H1**	**H2**	**P**
S1	0	1	0	1
S2	1	0	1	0
S3	0	0	1	1
S4	1	1	0	0

Table D.1: *Switchingstates for Leg A*

	Switching States			
Leg B	**O**	**H1**	**H2**	**P**
S5	0	1	0	1
S6	1	0	1	0
S7	0	0	1	1
S8	1	1	0	0

Table D.2: *Switchingstates for Leg B*

	Switching States			
Leg C	**O**	**H1**	**H2**	**P**
S9	0	1	0	1
S10	1	0	1	0
S11	0	0	1	1
S12	1	1	0	0

Table D.3: *Switchingstates for Leg C*

Matlab/Simulink Model Description

E

The following figure presents the model created in Matlab/Simulink Environment. The C-code of three level space vector modulation has been created in S-Function Builder (the C-code for two-level space vector modulaion has been also created in S-Function Builder). The outputs of SVM3LEVdsp are the six duty cycles (three for inverter one and three for inverter two). These duty cycles are sent to toggle block where the swapping process between them is done (in order to utilize both H1 and H2 states). In modulator one, two and three the comparison with triangular and swapped duty cycles is done. The switching signals are sent to inverter model which is realized with use of PLECS toolbox. The counter has been also created in S-Function Builder in order to count the switching signals and estimate switching frequency.

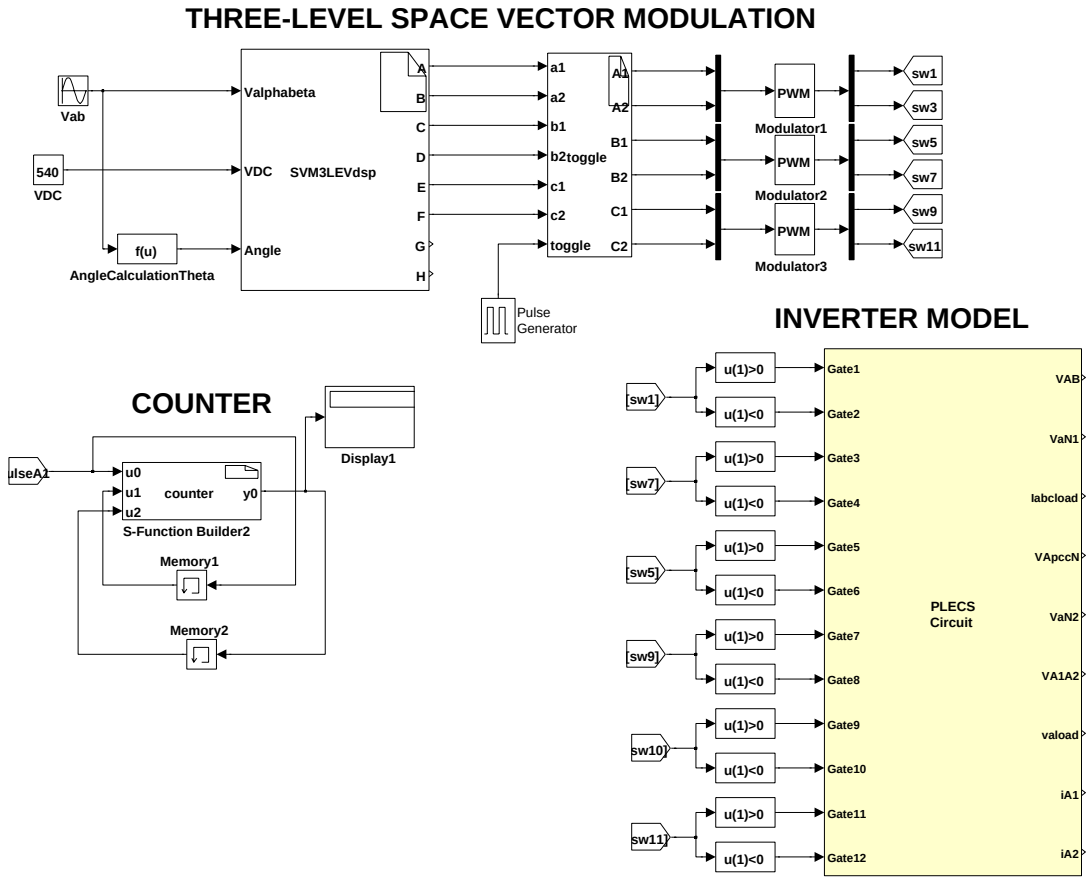

Figure E.1: *Simulink model of the system.*

System of two parallel connected inverters in PLECS:

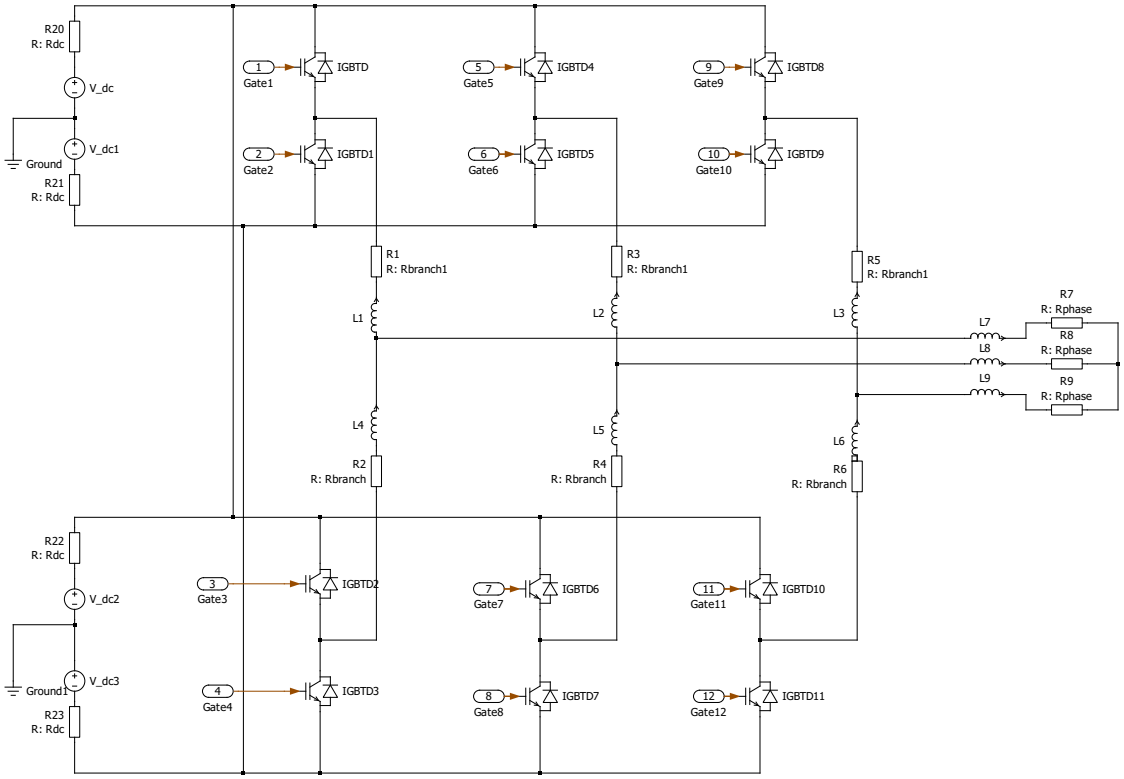

Figure E.2: *PLECS model of two parallel connected inverters.*

NPC inverter model in PLECS:

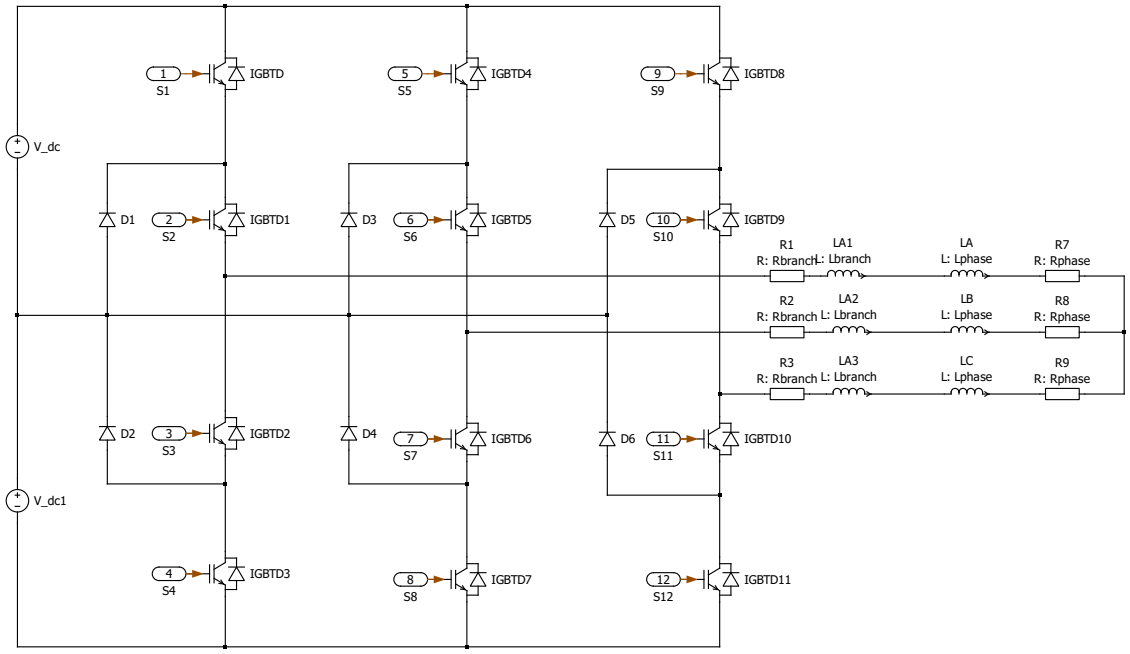

Figure E.3: *PLECS model of NPC inverter.*

C-code for three-level space vector modulation:

```
/****************Declaration of the variables***************/
int Vdc;
double Valpha, Vbeta, sector, theta, angleshift, ta, tb, tc;
double Vmag, sa1, sb1, sc1, sa2, sb2, sc2;
double Va, Vb, Vab, Vmax, region, ma, ts=0.000125;

/******************Setting the input signals***************/

        Valpha=Valphabeta[0];
        Vbeta=Valphabeta[1];
        Vdc=VDC[0];
        theta=Angle[0];

/********************Sector selection***********************/

        if ((theta>0) && (theta<=60))
        {
            sector=1;
                    }
```

```
        else if((theta>60) && (theta<=120))
        { sector=2;
                    }
        else if ((theta>120) && (theta<=180))
        { sector=3;
                    }
        else if ((theta>180)&&(theta<=240))
        { sector=4;
                    }
        else if ((theta>240)&&(theta<=300))
        { sector=5;
                    }
        else
        { sector=6;
                    }
/*******************Region selection**********************/
       angleshift=(theta-(sector-1)*60)*3.1416/180;
        Vmag=(float)sqrt(Valpha*Valpha+Vbeta*Vbeta);
        Va=Vmag*(cos(angleshift)-((float)sqrt(3.0)*sin(angleshift))/3);
        Vb=(2/(float)sqrt(3.0))*Vmag*sin(angleshift);
        Vab=Va+Vb;
        Vmax=0.6667*0.5*Vdc;
        ma=((float)sqrt(3.0)*Vmag)/Vdc;
```

```
        if ((Va<Vmax)&&(Vb<Vmax)&&(Vab<Vmax))
        {
         region=1;
        }

        else if ((Va<Vmax)&&(Vb<Vmax)&&(Vab>Vmax))
        {
         region=2;
        }

        else if ((Va>Vmax))
        {
         region=3;

        }

        else if (Vb>Vmax)
        {
         region=4;

        }

/********Dwell time and duty cycles calculation********/

        if (region==1)

        {
         ta=ts*(2*ma*sin(3.1416/3-angleshift));
         tb=ts*(1-2*ma*sin(3.1416/3+angleshift));
         tc=ts*(2*ma*sin(angleshift));

                if (sector==1)

                {
                 sa1=(2*ta+2*tc+tb)/(2*ts);
                 sb1=(2*tc+tb)/(2*ts);
                 sc1=tb/(2*ts);
                 sa2=0;
                 sb2=0;
                 sc2=0;
                }

                else if (sector==2)
```

```
{
 sa1=(2*ta+tb)/(2*ts);
 sb1=(2*tc+2*ta+tb)/(2*ts);
 sc1=tb/(4*ts);
 sa2=0;
 sb2=0;
 sc2=0;
}

 else if (sector==3)

{
 sa1=tb/(2*ts);
 sb1=(2*tc+2*ta+tb)/(2*ts);
 sc1=(2*tc+tb)/(2*ts);
 sa2=0;
 sb2=0;
 sc2=0;
}

 else if (sector==4)

{
 sa1=tb/(2*ts);
 sb1=(2*ta+tb)/(2*ts);
 sc1=(2*tc+2*ta+tb)/(2*ts);
 sa2=0;
 sb2=0;
 sc2=0;
}

   else if (sector==5)

{
 sa1=(2*tc+tb)/(2*ts);
 sb1=tb/(2*ts);
 sc1=(2*tc+2*ta+tb)/(2*ts);
 sa2=0;
 sb2=0;
 sc2=0;
}

    else if (sector==6)
```

```
                {
                 sa1=(2*ta+2*tc+tb)/(2*ts);
                 sb1=tb/(2*ts);
                 sc1=(2*ta+tb)/(2*ts);
                 sa2=0;
                 sb2=0;
                 sc2=0;
                }
            }

/*********************Setting the output signals*********************

        A[0]=sa1;
        B[0]=sb1;
        C[0]=sc1;
        D[0]=sa2;
        E[0]=sb2;
        F[0]=sc2;
        G[0]=sector;
        H[0]=region;
```

The above C-code is presented just to show calculation of duty cycles in region one, every sector. The same rule of realizing duty cycles for others regions is tha same like for region one. The full C-code can be found on the CD-ROM attached to the project.

Sector and region determination used in three-level SVM:

The sector determination is based on θ angle calculation:

- If $0° \leq \theta < 60°$, than $\vec{V_{ref}}$ is placed in Sector I
- If $60° \leq \theta < 120°$, than $\vec{V_{ref}}$ is placed in Sector II
- If $120° \leq \theta < 180°$, than $\vec{V_{ref}}$ is placed in Sector III
- If $180° \leq \theta < 240°$, than $\vec{V_{ref}}$ is placed in Sector IV
- If $240° \leq \theta < 300°$, than $\vec{V_{ref}}$ is placed in Sector V
- If $300° \leq \theta \leq 360°$, than $\vec{V_{ref}}$ is placed in Sector VI

The idea of region determination has been proposed in [22].

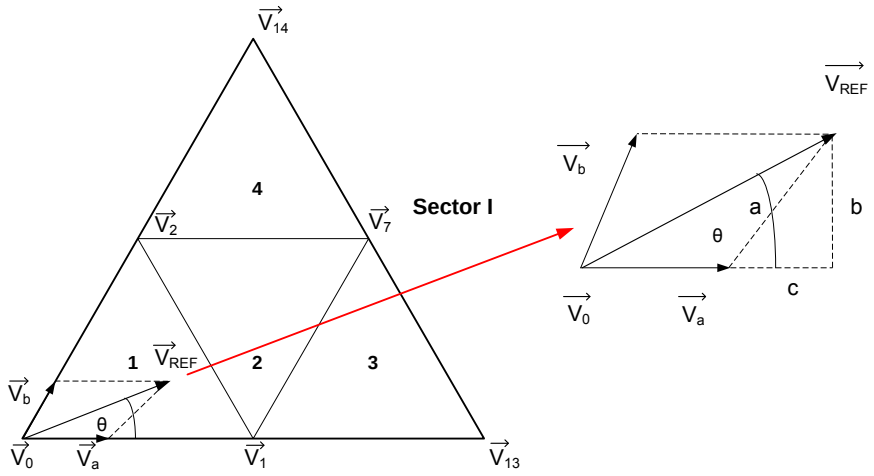

Figure E.4: *Region determination in Sector I.*

From the above Fig.E.4 it can be observed that two additional vectors $\vec{V_a}$ and $\vec{V_b}$ are used to determine the region:

$$a = \vec{V_b} = \frac{b}{sin(\frac{\pi}{3})} = \frac{2}{\sqrt{3}}\vec{V_{ref}}sin(\theta) \tag{E.1}$$

$$\vec{V_a} = \vec{V_{ref}}cos(\theta) - (\frac{2}{\sqrt{3}}\vec{V_{ref}}sin(\theta))cos(\frac{\pi}{3}) \tag{E.2}$$

$$\vec{V_a} = \vec{V_{ref}}(cos(\theta) - \frac{sin(\theta)}{\sqrt{3}}) \tag{E.3}$$

Using equations E.1 and E.3 it is possible to specify the working region:

- If $\vec{V_a}$, $\vec{V_b}$ and $(\vec{V_a} + \vec{V_b})$ are smaller than $0.33V_{DC}$, then $\vec{V_{ref}}$ is placed in Region 1.
- If $\vec{V_a}$, $\vec{V_b}$ are smaller than $0.33V_{DC}$ and $(\vec{V_a} + \vec{V_b})$ is higher than $0.33V_{DC}$, then $\vec{V_{ref}}$ is placed in Region 2.
- If $\vec{V_a}$ is higher than $0.33V_{DC}$, then $\vec{V_{ref}}$ is placed in Region 3.
- If $\vec{V_b}$ is higher than $0.33V_{DC}$, then $\vec{V_{ref}}$ is placed in Region 4.

Transformations

F

The idea of reference frame theory has been presented in [previous report]

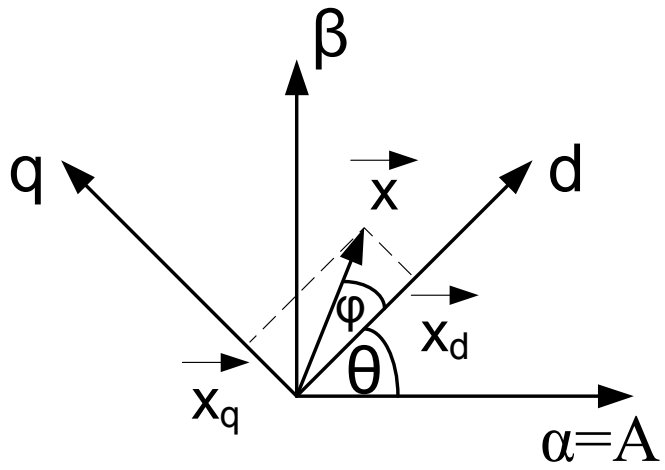

Figure F.1: *Coordinate system transformations.*

- Clarke (a,b,c) to (α, β):

  Clarke transformation converts (a,b,c) system to two time variant coordinate system (α, β).

$$X_\alpha = \frac{2}{3}X_A - \frac{1}{3}X_B - \frac{1}{3}X_C \tag{F.1}$$

$$X_\beta = \frac{\sqrt{3}}{3}X_B - \frac{\sqrt{3}}{3}X_C \tag{F.2}$$

- Park (α, β) to (d,q):

  Park transformation converts two-axis time variant system (α, β) to two-axis time invariant system (d,q).

$$X_d = cos(\theta)X_\alpha + sin(\theta)X_\beta \tag{F.3}$$

$$X_q = cos(\theta)X_\beta - sin(\theta)X_\alpha \tag{F.4}$$

- Inverse Park (d,q) to (α, β):

  Inverse Park transformation converts two-axis time invariant system (d,q) to two-axis time variant system (α, β).

$$X_\alpha = cos(\theta)X_d - sin(\theta)X_q \tag{F.5}$$

$$X_\beta = cos(\theta)X_q + sin(\theta)X_d \tag{F.6}$$

Thermal description of IGBT

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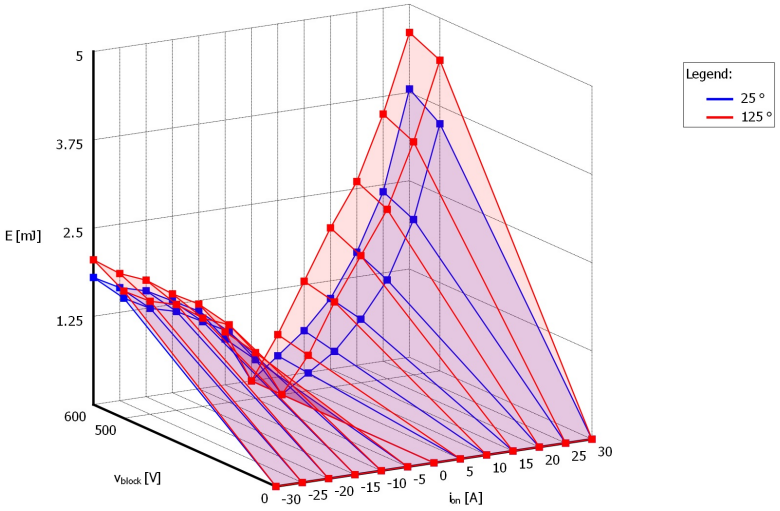
Turn-on losses:



T = 25 °

	-30 A	-25 A	-20 A	-15 A	-10 A	-5 A	0 A	5 A	10 A	15 A	20 A	25 A	30 A
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	1.7 mJ	1.5 mJ	1.4 mJ	1.2 mJ	1 mJ	0.55 mJ	0 mJ	0.25 mJ	0.5 mJ	0.9 mJ	1.4 mJ	2.2 mJ	3.5 mJ
600 V	1.8 mJ	1.6 mJ	1.5 mJ	1.3 mJ	1.1 mJ	0.65 mJ	0 mJ	0.3 mJ	0.6 mJ	1 mJ	1.6 mJ	2.4 mJ	3.8 mJ

T = 125 °

	-30 A	-25 A	-20 A	-15 A	-10 A	-5 A	0 A	5 A	10 A	15 A	20 A	25 A	30 A
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	1.8 mJ	1.6 mJ	1.5 mJ	1.25 mJ	1.1 mJ	0.65 mJ	0 mJ	0.5 mJ	1.2 mJ	1.8 mJ	2.4 mJ	3.3 mJ	4.4 mJ
600 V	2.05 mJ	1.8 mJ	1.65 mJ	1.4 mJ	1.2 mJ	0.75 mJ	0 mJ	0.6 mJ	1.3 mJ	2 mJ	2.6 mJ	3.5 mJ	4.6 mJ

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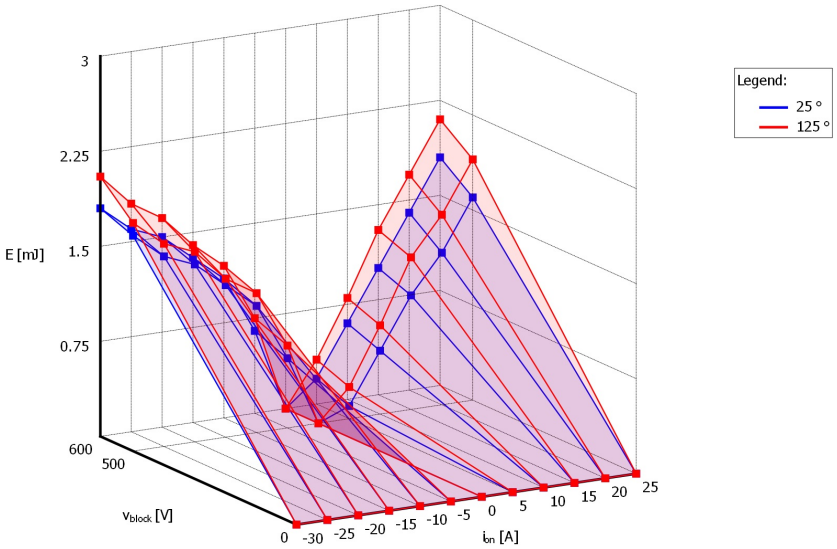
Turn-off losses:



T = 25 °

	-30 A	-25 A	-20 A	-15 A	-10 A	-5 A	0 A	5 A	10 A	15 A	20 A	25 A
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	1.7 mJ	1.5 mJ	1.4 mJ	1.2 mJ	1 mJ	0.55 mJ	0 mJ	0.1 mJ	0.5 mJ	0.9 mJ	1.2 mJ	1.6 mJ
600 V	1.8 mJ	1.6 mJ	1.5 mJ	1.3 mJ	1.1 mJ	0.65 mJ	0 mJ	0.2 mJ	0.6 mJ	1 mJ	1.4 mJ	1.8 mJ

T = 125 °

	-30 A	-25 A	-20 A	-15 A	-10 A	-5 A	0 A	5 A	10 A	15 A	20 A	25 A
0 V	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ	0 mJ
500 V	1.8 mJ	1.6 mJ	1.5 mJ	1.25 mJ	1.1 mJ	0.65 mJ	0 mJ	0.25 mJ	0.7 mJ	1.2 mJ	1.5 mJ	1.9 mJ
600 V	2.05 mJ	1.8 mJ	1.65 mJ	1.4 mJ	1.2 mJ	0.75 mJ	0 mJ	0.35 mJ	0.8 mJ	1.3 mJ	1.7 mJ	2.1 mJ

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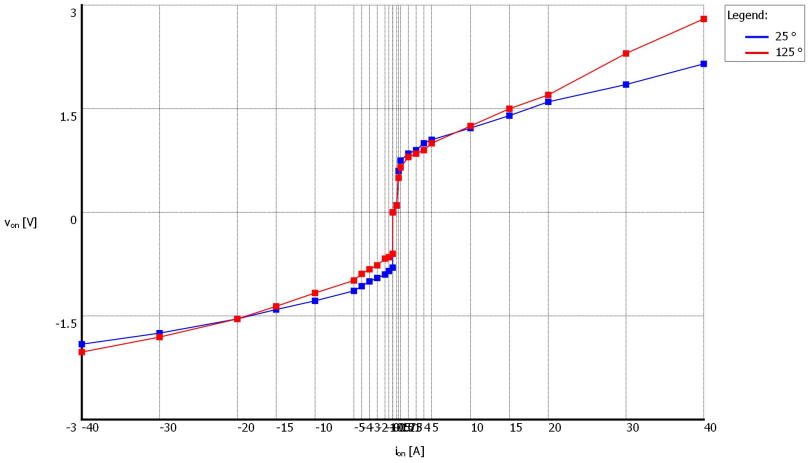
Conduction losses:



	-40 A	-30 A	-20 A	-15 A	-10 A	-5 A	-4 A	-3 A	-2 A	-1 A	-0.5 A	-0.01 A	0 A	0.5 A	0.75 A	1 A	2 A	3 A	4 A	5 A	10 A	15 A	20 A	30 A	40 A
25 °	-1.909 V	-1.749 V	-1.543 V	-1.407 V	-1.281 V	-1.137 V	-1.069 V	-1 V	-0.95 V	-0.9 V	-0.85 V	-0.8 V	0 V	0.1 V	0.6 V	0.75 V	0.85 V	0.9 V	1 V	1.05 V	1.22 V	1.4 V	1.6 V	1.85 V	2.15 V
125 °	-2.023 V	-1.806 V	-1.543 V	-1.361 V	-1.167 V	-0.9868 V	-0.8909 V	-0.8245 V	-0.7674 V	-0.67 V	-0.65 V	-0.6 V	0 V	0.1 V	0.5 V	0.65 V	0.8 V	0.85 V	0.9 V	1 V	1.25 V	1.5 V	1.7 V	2.3 V	2.8 V

Danfoss FP25R12KT3

Comment:
Implemented from the technical datasheet of FP25R12KT3. Module with Diode rectifier, IGBT inverter and brake chopper. Used in Danfoss VLT FOC302 converters

Contents of the CD-ROM

H

- References
- Measurements
- Simulation files
- Report files
- Datasheets
- Programs for Code Composer Studio
- Altium Designer files