Department of Energy Technology
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Control of MMC in HVDC Applications

Master Thesis 30/05/2013

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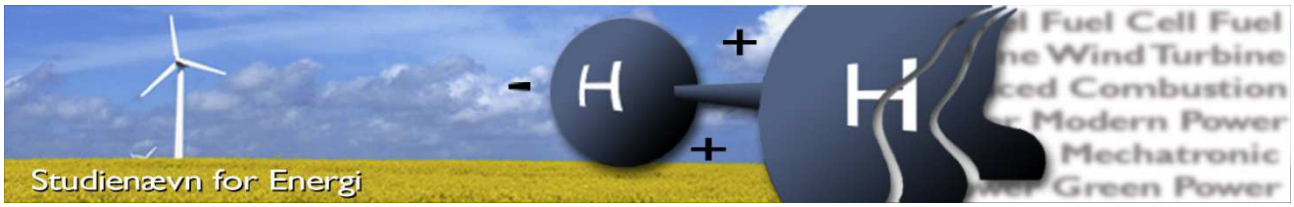

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SYNOPSIS:

The Modular multilevel converter (MMC) is the latest converter topology suitable for transformerless applications in HVDC transmission.

HVDC are required to remain connected during grid fault, provide grid support and completely decouple the healthy side from the faulty one. Due to its complex structure, the inner dynamics of the MMC converter are challenged by this particular condition and by these demands.

This thesis demonstrates the effect of negative and zero sequence current control in MMC-HVDC during asymmetric grid faults. A modified circulating current suppression controller is proposed to eliminate the voltage ripples in the DC-link.

A current limitation strategy for MMC is derived and its impact on the performance of the HVDC transmission system is verified through simulations.

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

Acknowledgements

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1 Introduction

Thanks to the global energy consciousness and the government support, more and more renewable energy sources (RES) are being installed in order to cope with the increasing energy demand [1]. In 2009, the EU Renewable Energy Directive set the goal of producing the 20% of the overall energy mix from RES by 2020. [2]

Aiming to meet this target, the share of renewables in the total new power installations has grown from 20.7% in the year 2000 to 70% in 2012, as shown in Figure 1.1 [3]. The installation of Photovoltaic (PV) generation in the EU has grown at remarkable rates over the last 5 years, moving from 2.0 MW installed in 2007, to 17.2 MW in 2012; covering the 37% of the total installed capacity of that year [4].

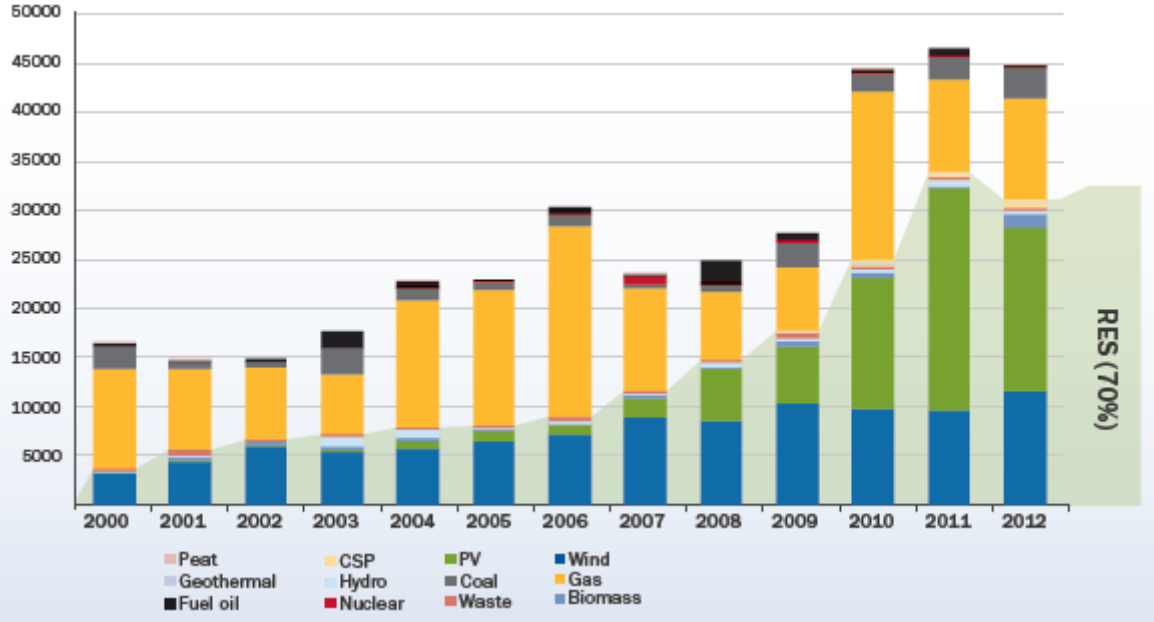

Figure 1.1 – Installed power generating capacity per year in MW [3]

The renewable resources in the world are unequally distributed. In Europe, while most of the wind energy resources are located in the north, the solar resources are located in the south, in countries like Italy and Spain [5]. In addition, the availability of RES has a strong daily and seasonal pattern. [6]

The integration of more renewable generation into the energy mix combined with a rapid growth of the energy consumption are evidence that the actual AC grid will not be suitable for the transmission and distribution of the new power generation.

In order to utilize efficiently the vast potential of RES, the selection of the transmission technology is of critical importance [7]. The high losses associated with long AC lines make HVDC an attractive alternative for the transport of bulk power over long distances. Additionally, HVDC interconnections allow power transmission between unsynchronized AC systems and prevent cascading failures to propagate through

wide transmission grids; increasing the reliability of the system. Due to its stability benefits and reduced losses, many transmission system operators (TSO) have considered a wider use of HVDC technology. [8]

Before the emergence of voltage source converters (VSC), the implementation of HVDC was limited to very large installations located at a long distance or to under-sea cable transmission; due to the elevated costs of the converter infrastructure, the reactive power demand and limited controllability [9]. In Europe HVDC transmission has been used since 1954, mostly for submarine cable transmission, as shown in Figure 1.2.

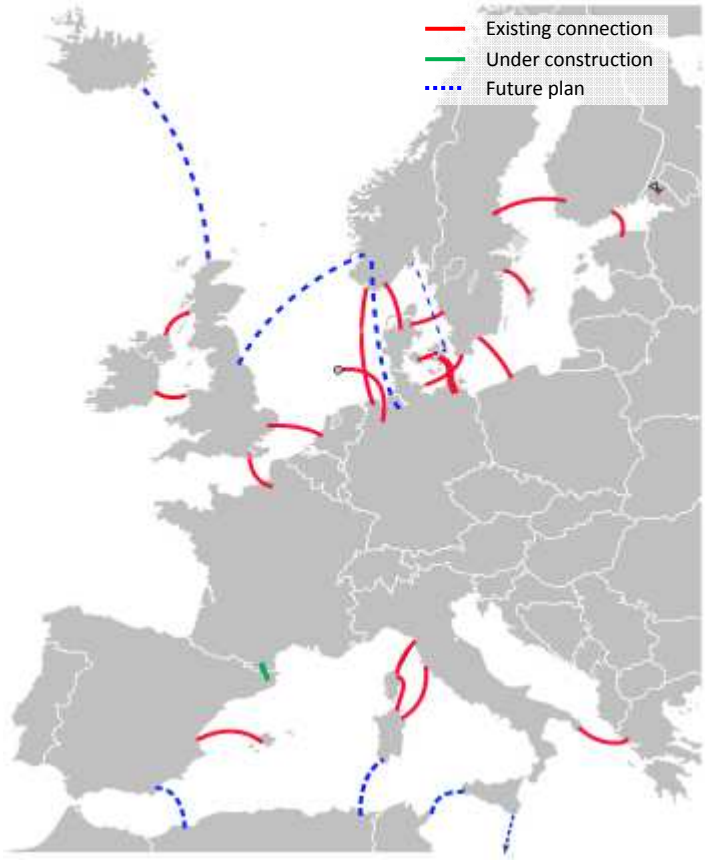

Figure 1.2 - HVDC connections in Europe [10]

The appearance of VSC-HVDC, having a smaller converter size, reduced filters, dynamic reactive power support and fast power reversal, has facilitated the implementation of HVDC technology in a wider range of applications [9]. Since the first successful application of VSC-HVDC in 1997 in Gotland, Sweden; many other installations provided asynchronous interconnections of AC grids all-over the world. Due to its smaller footprint and ability to act as a virtual synchronous generator, VSC is especially suitable for connecting offshore wind power plants.

In 2002, Marquardt and Lesnicar proposed the modular multilevel converter (MMC) topology [11]. Due to the fact that it can achieve high power and high voltage levels using proven semiconductor technology, MMC has been widely accepted in the industry [12]. The HVDC-*Plus* from Siemens, HVDC-*Light* from ABB and HVDC-*MaxSine* from Alstom are examples of the implementation of the MMC concept in applications for VSC-HVDC transmission [13][14][15].

With advantages such as modularity, increased efficiency and reliability, the MMCs aims to substitute the two-level converters in VSC-HVDC applications, becoming a backbone for the future HVDC transmission systems [16].

1.1 State of the Art and Motivation

The origins of the MMC circuits go to the 1970s when synthesising waveform converter topologies were patented [17]. In the last decade, after the design and control of the MMC was proposed [11], an intense research has been done on all aspects of the system.

During steady state operation, a circulating current is observed flowing through the converter phase-leg. In [18] the voltage ripples in the capacitors are studied as a cause for this circulating current component. Later in [19], the circulating current is analyzed and found to have double line-frequency and negative sequence.

Having a large number of sub-modules increases the complexity of the control of the MMC. To assure accurate and stable operation, the sub-modules must share the voltage equally. Different control strategies have been proposed aiming to regulate the equal share of charge within the capacitors in the arm.

Akagi *et al.* propose in [20] a voltage balancing algorithm for the capacitors per phase-leg. The control is performed by adding a balancing component to the modulation index of each sub-module. Later in [21] a modification of this method is proposed to take into consideration the voltage balance between arms.

Another method to eliminate the circulating current and balance the converter arm voltages is proposed in [22]. The method is based on the control of the stored energy in the converter, and two control loops are added to ensure stable operation. A simplification of this method using open-loop approach for the estimation of the arm energy is proposed in [23], proving to have a better stability.

As alternative, a straightforward method to suppress unwanted current component is derived in [24]. The method is based on the vector control of the measured current. Later in [25] a combination of the energy approach presented in [22] with the method presented in [24] is implemented, showing an improved performance for grid connected applications.

The MMC topology has the possibility of synthesising high voltage levels by increasing the number of series connected sub-modules, therefore is especially suitable for HVDC systems. In [16] the MMC is highlighted as the most promising VSC topology to be used in the future HVDC grids. In 2010 Siemens announced the commercial installation of the first MMC-HVDC transmission [13]. Furthermore, several projects using MMC-HVDC for the interconnection of large offshore wind farms are announced to be commissioned in the next few years [14].

Lately, a lot of research is focused on evaluation of MMC performance in HVDC applications under different grid conditions. In [26] the converter operation under unbalanced grid conditions has been analyzed, using a Δ-Y transformer to remove the zero sequence current from the converter terminals. The presence of DC-link voltage ripple due to negative sequence components is described and a controller to compensate for the disturbance is proposed. The transformerless grid connection of the MMC is studied in [27], observing that under unbalanced conditions; the zero sequence current is looped between two AC grids. In [28] an

additional zero sequence current control is proposed for transformerless connections under unbalanced conditions, proving stable HVDC system operation and enhanced fault ride-through capability of the converter.

Technical literature and the growing amount of installations show the success and market acceptance of the MMC topology. However, there are very little publications discussing the implementation of MMC in HVDC applications with transformerless connection.

Motivated by the fast penetration of MMC into the HVDC market and the lack of research published on that topic, the performance of transformerless MMC-HVDC under unbalanced conditions has been studied here. The analysis is focused on the fault propagation over HVDC transmission and its impact on the converter inner dynamics.

1.2 Objectives

The objective of the thesis is modelling and analysis of a VSC-HVDC transmission system based on Modular Multilevel Converters. The main goals of the project are:

- Good understanding of operating principles and inner controls of MMC and VSC-HVDC transmission systems;
- Modelling of the MMC-HVDC system and implementation of the control strategies in PSCAD/EMTDC software;
- Study of the fault propagation in transformerless MMC-HVDC transmission systems;
- Analysis of the system behaviour as response to unbalanced grid conditions;

1.3 Limitations

The main limitations in the project are:

- No communication and control delays were implemented in the simulation;
- The model considered the interconnection of two AC grids through HVDC transmission, therefore converter operation in frequency-controlled mode was not analysed;
- For being the most common fault in the HVAC network [29], only single-line to ground (SLG) fault was analysed. Aiming to prove to concept only, the fault was implemented as an unbalance in the grid voltage;
- The faults on the DC side were not analyzed;
- No laboratory verification of the control strategy was performed due to the unavailability of a prototype.

1.4 Thesis outline

Having explained the objectives and motivations of this project in Chapter 1; a brief background review of the multilevel topologies, modulation strategies and HVDC transmission systems is presented in Chapter 2, highlighting the advantages of MMC that make this topology attractive for HVDC applications.

In Chapter 3 the inner dynamics of the MMC are studied in order to have a better understanding of the converter response for the subsequent chapters. An average model of the converter is derived and validated through simulations. The arm currents present in the converter and the sub-module dynamics are also analyzed.

Chapter 4 describes the development of the MMC-HVDC model under study. The inner control strategies for MMC are discussed. The control loops employed in VSC-HVDC applications are presented with the considerations required for MMC converters.

The operation of the system under asymmetric grid conditions is assessed in Chapter 5. An analysis of the propagation of unbalanced faults in a MMC-HVDC system with a transformerless connection is performed. A control structure is proposed to eliminate fault reflections in the DC-link considering the three sequence components. An evaluation of the power controllability of the converter is presented. The performance of the MMC with current limitation is also evaluated.

The conclusions about the project are drawn in Chapter 6.

2 Background

In this chapter the most common multilevel converter topologies are reviewed. Particular concentration is addressed in the Modular Multilevel Converter, central for this project. Several modulation strategies applicable for MMC are also reviewed. Then, an overview of HVDC systems is presented. Finally, the grid codes applicable for HVDC interconnections are discussed.

2.1 Review of Multilevel Converter Topologies

Multilevel Converters have been a topic of research for more than three decades and are still a developing technology [12]. The reason for the high interest on multilevel topologies over the conventional two-level converters lies in the improved quality of their output waveform, possibility to achieve higher power levels and higher efficiency [12].

Several different multilevel topologies have been proposed. Some of the most common multilevel topologies are [12]:

- Neutral-Point Clamped (NPC);
- Flying Capacitor (FC);
- Cascaded H-Bridge (CHB).
- Modular Multilevel Converters (MMC)

2.1.1 Neutral-Point Clamped converter

The NPC voltage-source converter was initially proposed as a three-level inverter. It is a modification of the two-level converter topology having two extra power semiconductor switches per phase leg as shown in Figure 2.1. The midpoint of the switches is connected to the neutral point of the converter through clamping diodes, enabling the generation of the zero voltage level. By this means, for the same DC-link voltage, the voltage level that the devices have to withstand is reduced to half comparing to the two-level topology.

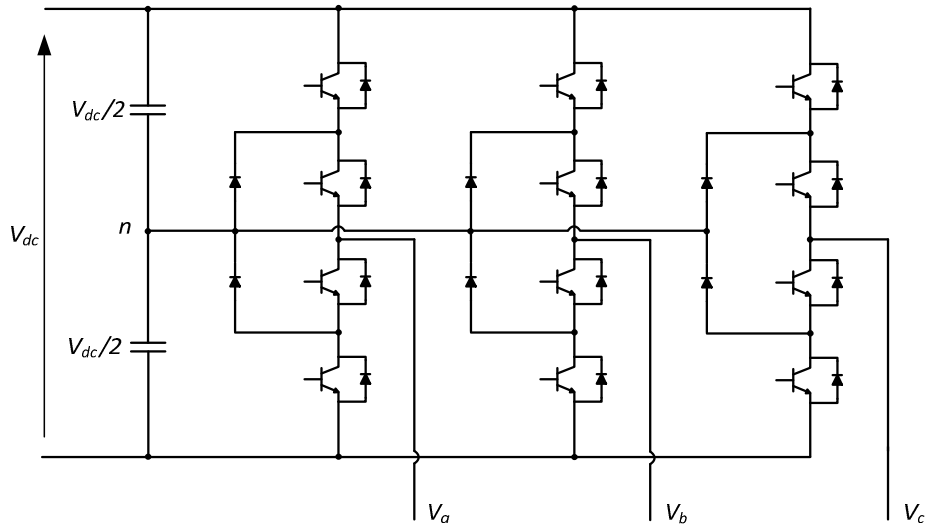

Figure 2.1 – Topology of three level NPC converter

Following the same philosophy, the NPC converter can be extended to more than three voltage levels. However this topology has several drawbacks. Under certain operating conditions the NPC may experience capacitor voltage unbalances, creating a potential between the neutral point and ground and causing distorted output waveforms. This implies the necessity of neutral point or a capacitor balancing control which is a challenging task when the number of output voltage levels is above three. Moreover there is a quadratic relation between the required voltage blocking rate of the clamping diodes and the number of converter levels, which hinders the implementation with a high number of levels. [12]

2.1.2 Flying Capacitor converter

The topology of the FC converter is presented in Figure 2.2. Each capacitor in the phase is charged to a different voltage level, therefore by changing the states of the switches, various output voltage levels can be obtained. [30]

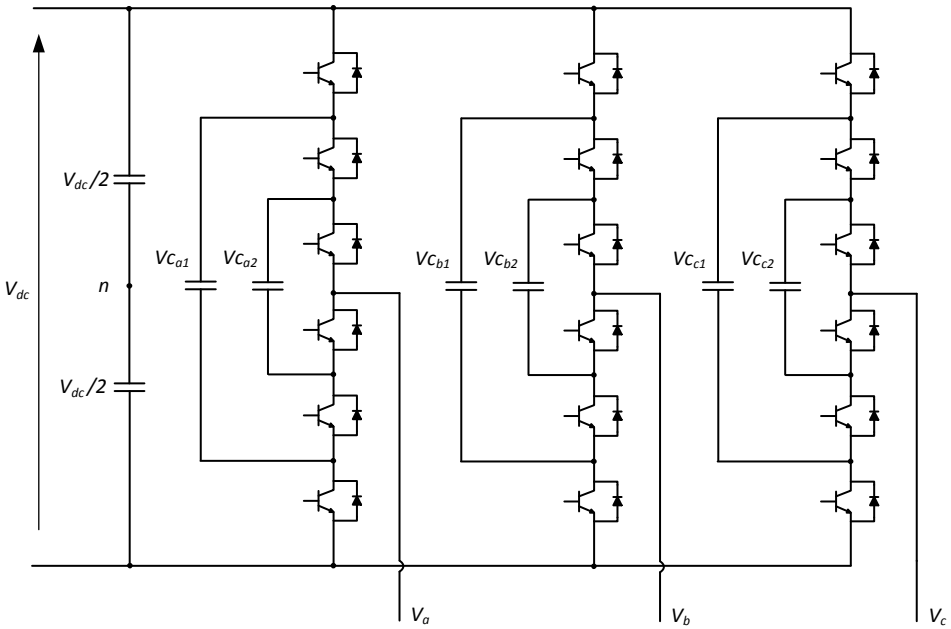

Figure 2.2 – Topology of Flying Capacitor Converter

This topology can have phase redundant switching states that can be used for capacitor voltage regulation, showing an advantage over the NPC topology. Thanks to the energy storage in the capacitors, the converter can ride through short duration outages and deep voltage sags. As a drawback, the pre-charge of capacitors before the start-up, also known as initialisation, is required. Also this topology presents unequal duty distribution between the switches. Even though the FC topology can be extended to an arbitrary number of cells, the addition of capacitors leads to an increase in cost and footprint; therefore the number of levels is usually limited to fours. [12][31]

2.1.3 Cascaded H-Bridge inverter

The CHB topology is based on the series connection of single-phase full-bridge inverter cells with isolated DC supplies (Figure 2.3). The absence of clamping diodes or flying capacitors, as in case of NPC and FC, results in the use of minimum components to produce the desired voltage levels. Each inverter cell can

generate three voltages, i.e. both polarities of the DC supply voltage and zero. The output phase voltage is the result of superimposing the voltages generated by all the cells in the leg. Because the DC sources are usually supplied by multi-pulse secondary windings of the input transformer, there are no balancing or initialisation problems as with NPC or FC. [12][32]

The main advantages of the CHB over the NPC and FC are its modular structure and the possibility to have an independent control over the zero-sequence component in the current. In case of rectifier applications, the need of many isolated DC sources in series limits the number of cells in the leg, keeping this topology unfavourable for bidirectional power applications [12][33]. However, a proposal for CHB in HVDC applications using a reinjection circuit can be found in [31].

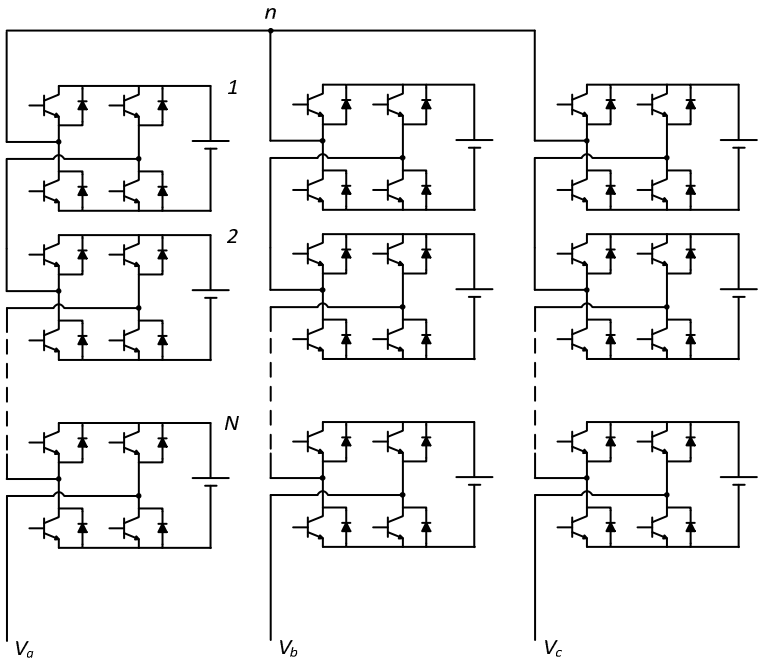

Figure 2.3 – Topology of Cascaded H-Bridge Inverter

2.1.4 Modular Multilevel Converter

The MMC topology is based on a series connection of identical elements, called sub-modules or cells. Each sub-module represents the basic component of the MMC, shown in Figure 2.4-a. The series connection of sub-modules in one phase is known as leg. The leg is divided into upper and lower arms such that the number of the sub-modules in each arm is equal. The AC voltage terminal is the common connection point between both arms. Since the leg capacitors share a common DC-link voltage there is no need of bulky DC-link capacitors, as in case of two-level, NPC or FC topologies. Inductors (L_{arm}) are placed in the arms to limit transient currents. [34]

Different sub-module topologies can be applicable to the MMC depending on the application (STATCOM, HVDC, BTB) [34][35][36]. The difference in the cell structure results in different possible voltage levels at the terminals of the sub-module. However, with the increase of elements, the capacitor balancing becomes more complicated. According to the experimental studies performed in [35] evaluating the capacitor

balance and switching losses, the half-bridge topology is the most favourable topology to be implemented in the sub-modules when bidirectional power conversion is required.

In this project, the term sub-module refers to a half-bridge formed by two bidirectional switches with anti-parallel diodes and a DC capacitor, as shown in Figure 2.4-b. The capacitor acts as an energy buffer and a voltage source. The switches execute the insertion of the sub-module into the arm circuit while the anti-parallel diodes ensure uninterruptable current flow.

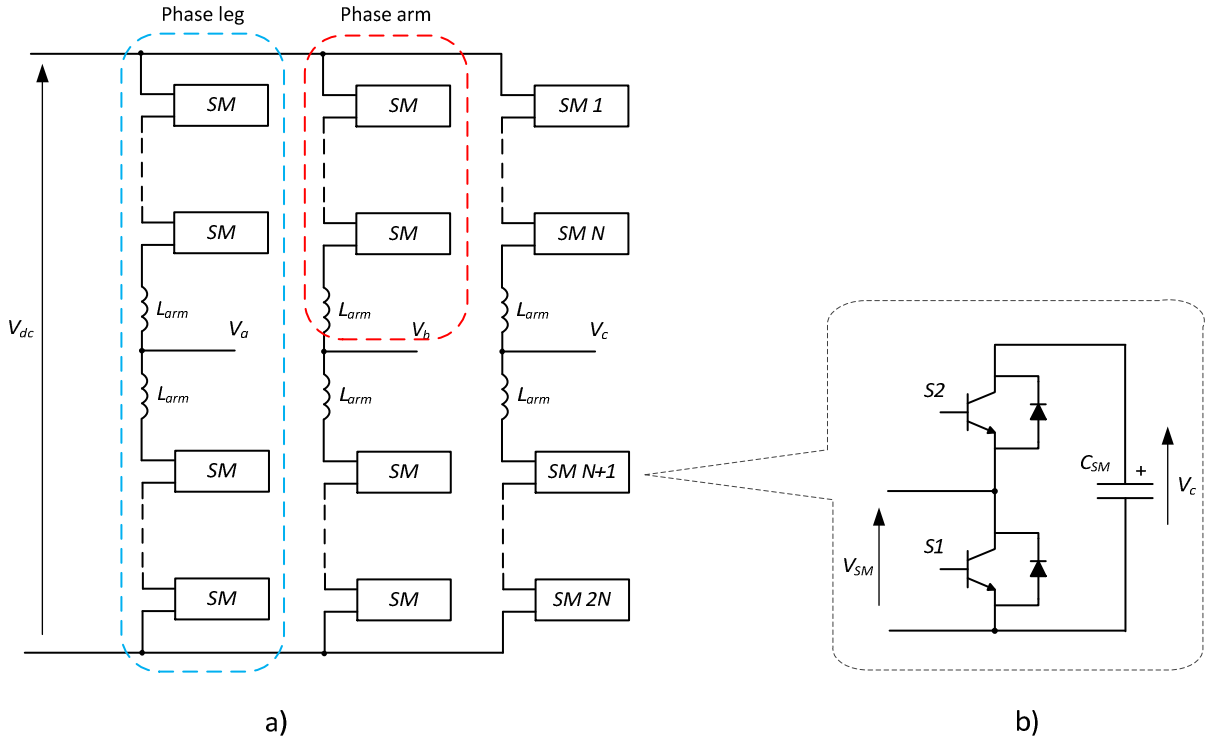

Figure 2.4 – (a) Topology of three-phase MMC (b) Half-bridge sub-module

Since all the sub-modules are identical, the operation principle of MMC can be resumed to the cell level operation. Each sub-module has two states depending on the switch positions. When the switch S1 in Figure 2.4-b is ON and the switch S2 is OFF, the sub-module is inserted into the circuit. The voltage between the terminals V_{SM} is equal to the capacitor voltage V_C. When the lower switch is ON and the upper is OFF the sub-module is bypassed and the terminal voltage is zero. As it can be derived from the sub-module topology, the switches have to operate in complementary way in order not to short circuit the capacitor. By controlling the number of the sub-modules inserted and bypassed, a staircase output voltage can be obtained at the AC terminals of the converter.

The direction of the arm current affects the capacitor voltage profile. In Figure 2.5 is shown the current flow in the sub-module for different states. The assumed positive direction of the arm current i_x is represented with red colour and the negative with blue. When the sub-module is inserted, the positive current will charge the capacitor, passing through the upper diode (a) whereas the negative current will discharge the capacitor (b). When the sub-module is bypassed the capacitor voltage remains constant.

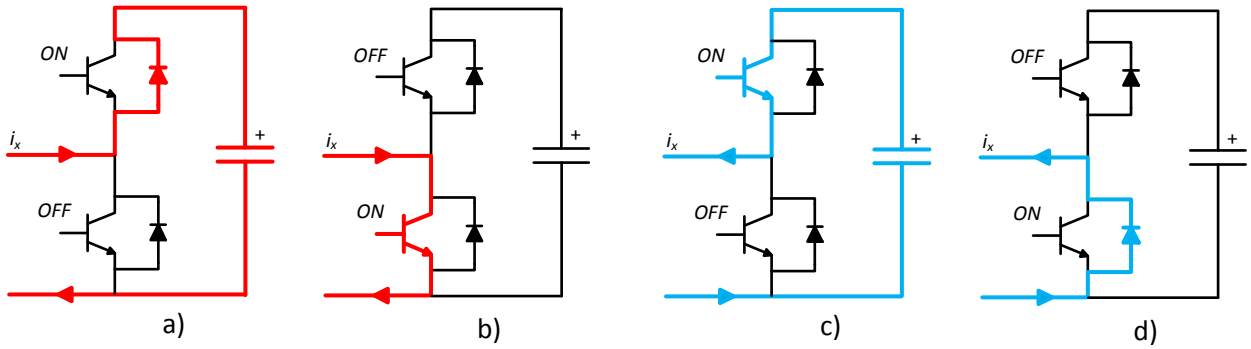

Figure 2.5 – Positive and negative current flow in a sub-module with different switching states

In Table 2.1 the sub-module terminal voltages and capacitor status depending on the switching states and the direction of the arm current are summarized. The condition when both switches are off can be used for the initial charging of the cell capacitors.

Table 2.1 - Switch States of a Sub-module

Switch state		SM terminal voltage	Arm current polarity	Status of the capacitor
S1	S2			
1	0	V_C	(+)	Charging
0	1	0	(+)	By-passed
1	0	V_C	(-)	Discharging
0	1	0	(-)	By-passed
1	1	Capacitor Shorted		
0	0	Open Circuit		

The main advantages of the MMC can be summarized as follows [37][27]:

- Modularity. The converter can be easily scaled in terms of power or voltage ratings;
- Increased output quality. Because the converter can be easily scaled to a large number of the sub-modules, nearly sinusoidal output can be obtained;
- Reliability. Use of redundant sub-modules in the case of a cell failure;
- Increased efficiency. Due to low switching frequency of each sub-module;
- Reduced footprint. Due to significant reduction or even elimination of the AC filters and no use of bulky DC-link capacitors.

Due to its possibility to be scaled to high voltage levels, achievable efficiency, ease of implementation, low harmonics output and reliability, the MMC proves to be the most suitable topology for modern HVDC applications. [16]

2.2 Modulation Techniques for MMC

The modulation and control methods have been the subject of intensive research during the last decades, when numerous techniques were developed for both; two-level and multilevel inverters [38]. In general the

multilevel modulation methods can be split into two main categories: Space Vector Modulation (SVM) and Voltage level Based Modulation; i.e. Carrier PWM (CPWM) and Nearest Level Modulation (NLM) [12].

2.2.1 Space Vector Modulation

The Space Vector Modulation theory is well established nowadays. Due to its advantages, such as easy digital implementation and the possibility of optimizing the switching sequences, it is an attractive modulation technique for multilevel converters. The principle applied for the calculation of the voltage vectors in two or three level converters can be extended to multilevel converters. However, the complexity of the algorithms for the calculation of the state vectors and computational costs increase with the number of levels. Recent publications have presented strategies where simpler algorithms are used; accordingly the computational efforts are significantly reduced, comparing with conventional SVM techniques. [39][40][41]

The space vector plane for a N-level converter is shown in Figure 2.6. Each connection point on the plane represents a specific state of the three-phase voltages of the converter. The point (2, 1, 0), for example, means that with respect to ground, phase A is at $2V_c$, phase B is at $1V_c$, and phase C is at 0; where V_c is the voltage of the DC capacitor in one sub-module.

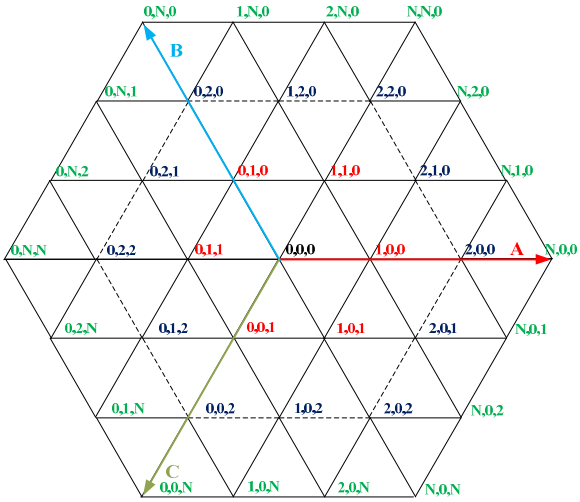

Figure 2.6 – Space vector for N-level converter

The phase voltages of the converter can be represented in matrix form by the switching states of the sub-modules (H_{abc}) and the voltages of the DC capacitors. For converters with N+1 voltage levels, the following equations applies,

$$V_{ref,abc} = H_{abc}V_c \tag{2.1}$$

$$V_c = \left[V_{c\_1}, V_{c\_2}, \ldots V_{c\_N}\right]^T \tag{2.2}$$

$$V_{ref,abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} \tag{2.3}$$

$$H_{abc} = \begin{bmatrix} h_{a1} & h_{a2} & \dots & h_{aN} \\ h_{b1} & h_{b2} & \dots & h_{bN} \\ h_{c1} & h_{c2} & \dots & h_{cN} \end{bmatrix} \tag{2.4}$$

Because some output voltages can be generated by several switching combinations, redundant switching states are possible. The number of possible switching combinations is equal to the cube of the converter voltage levels (N^3) while the number of unique states can be calculated by [42]:

$$n_{uni} = N^3 - (N-1)^3 \tag{2.5}$$

Following a similar approach as with two-level converters, the reference vector for N-level converter is obtained from the three nearest stationary vectors, which form the vertices of a triangle in which the reference vector lies. The dwell times of the stationary vectors should satisfy the equation:

$$\begin{cases} \vec{V}_{ref} T_s = \vec{V}_{1,N} t_{1,N} + \vec{V}_{2,N} t_{2,N} + \vec{V}_{3,N} t_{3,N} \\ T_s = t_{1,N} + t_{2,N} + t_{3,N} \end{cases} \tag{2.6}$$

In [40] is derived a transformation matrix for the calculation of the dwell times of a N-level converter, having the times for a two-level. Further improvements regarding multilevel SVM can be found in [43].

2.2.2 Multi-carrier PWM

The Carrier-based Pulse-Width Modulation concept is based on comparison of a reference (modulating) signal with a high-frequency triangular waveform (the carrier). The carrier can have a periodic bipolar or unipolar waveform. The switching instants are determined by the intersections of the modulating and carrier signals. [44]

When the reference is sampled through the number of carrier waveforms, the PWM technique is considered as a multicarrier PWM [44]. The multicarrier PWM implementation in multi-cell converter topologies is especially advantageous because each carrier can be assigned to a particular cell which allows independent cell modulation and control. [12]

The carriers can be displaced within levels (Level-shifted PWM), have phase shifts (phase-shifted PWM) or have a combination of them. The level-shifted PWM (LS-PWM) has N-1 carrier signals with the same amplitude and frequency, relating each carrier with the possible output voltage level generated. Depending on the way the carriers are located, they can be in phase disposition (PD-PWM), phase opposition disposition (POD-PWM), or alternate phase opposition disposition (APOD-PWM) as shown in Figure 2.7. [44]

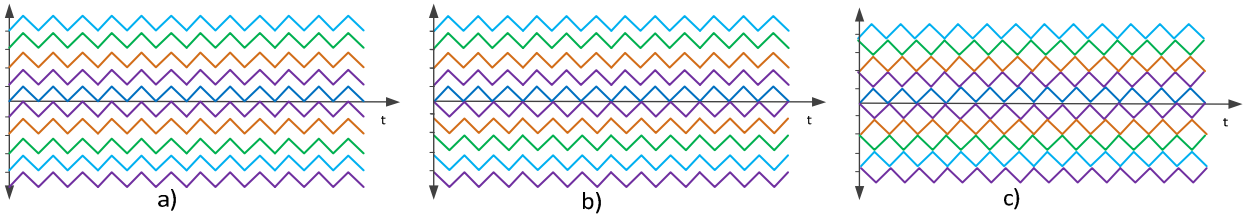

Figure 2.7 - Level shifted PMW carriers. (a) Phase Disposition (PD) (b) phase opposition disposition (POD) (c) alternate phase opposition disposition (APOD)

The LS-PWM methods produce an unequal duty and power distribution among the sub-modules since the vertical shifts relate each carrier and output level to a particular cell [12]. These can be corrected by implementing carrier rotation and signal distribution techniques [44].

The Carrier phase shifted method (PS-PWM) has N-1 carrier signals with the same amplitude and frequency. To achieve a staircase multilevel output waveform, the phase shift between the carriers is calculated as $\varphi = 360^0/(\mathrm{N}-1)$ [12]. The multicarrier PS-PWM process is shown in Figure 2.8, the

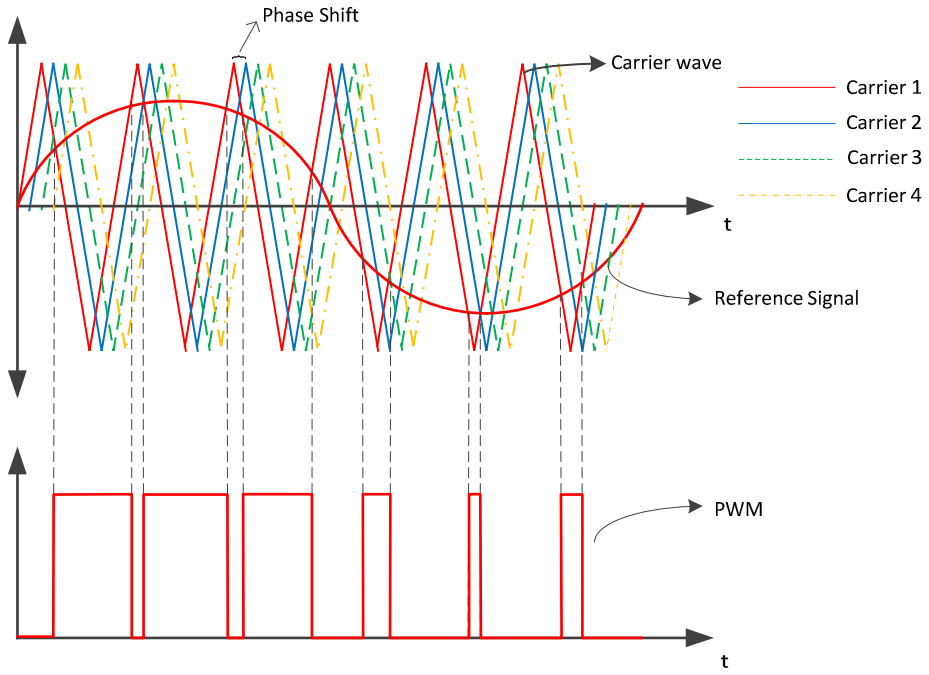

Figure 2.8 – Phase Shifted PWM

This approach provides equal duty and power distribution between the cells and, by selecting an adequate carrier frequency, capacitor voltage balancing can be achieved.

A comprehensive analysis of the Multicarrier PWM techniques was performed in [44], where the mentioned methods were extended and analysed particularly for MMC applications. The harmonic distortion of the generated waveforms and the possibility of sub-module capacitor voltage balancing were the main assessment criteria. It was concluded that the Carrier phase shifted PWM is more suitable for control of MMC.

2.2.3 Nearest level modulation

The Nearest Level Modulation strategy has been proposed for converters with an arbitrary number of voltage levels [45][46]. The main idea lies in deciding the number of cells to be inserted and bypassed based on the comparison of the modulating signal $V_{ref}(t)$ with the voltage steps that represent idealised cell capacitor voltages.

For MMC, assuming that the cell voltages are constant, $V_C(t) = V_{dc}/N$, the converter arms can generate one of the $N+1$ discrete voltage levels (0, V_{dc}/N, $2V_{dc}/N$,…, V_{dc}). The number of sub-modules to be inserted and bypassed can be calculated as

$$\begin{aligned} n_{ON,u} &= round\left[N\left(\frac{1}{2} - \frac{V_{ref}(t)}{V_{dc}}\right)\right] \quad , \quad n_{OFF,u} = N - n_{ON,u} \\ n_{ON,l} &= round\left[N\left(\frac{1}{2} + \frac{V_{ref}(t)}{V_{dc}}\right)\right] \quad , \quad n_{OFF,l} = N - n_{ON,l} \end{aligned} \tag{2.7}$$

By inserting or bypassing the cells according to (2.7), the average of the generated output voltage matches the reference voltage, as shown in Figure 2.9. This modulation strategy is suitable for converters with a large numbers of cells due to the small voltage steps and fundamental switching frequency.

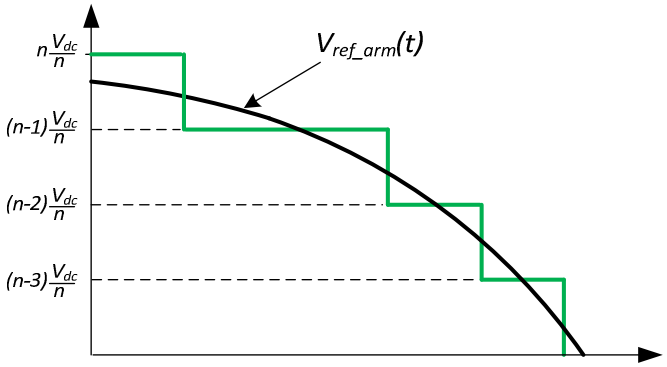

Figure 2.9 –Nearest Level Modulation, arm voltage waveform

Having a low number of voltage levels, the harmonic generation can be improved by modulating one cell in each arm. When the modulating signal lies between two adjacent voltage levels $k_1 V_C(t) < V_{ref}(t) < (k_1+1)V_C(t)$ with $k_1 = 0 \ldots (N-1)$; k_1 cells have to be selected as ON to provide the base voltage and one cell should be pulsewidth-modulated to generate the voltage remaining. The number of cells ON to provide the base voltage can be calculated as:

$$\begin{aligned} n_{ON,u} &= floor\left[N\left(\frac{1}{2} - \frac{V_{ref}(t)}{V_{dc}}\right)\right] \quad , \quad n_{OFF,u} = N - (n_{ON,u} + 1) \\ n_{ON,l} &= floor\left[N\left(\frac{1}{2} + \frac{V_{ref}(t)}{V_{dc}}\right)\right] \quad , \quad n_{OFF,l} = N - (n_{ON,l} + 1) \end{aligned} \tag{2.8}$$

The modulating signal to be used for the PWM cell can be obtained as,

$$m_{a,u} = N\left(\frac{1}{2} - \frac{V_{ref}(t)}{V_{dc}}\right) - n_{ON,u}$$
$$m_{a,l} = N\left(\frac{1}{2} + \frac{V_{ref}(t)}{V_{dc}}\right) - n_{ON,l} \quad (2.9)$$

In Figure 2.10 the generated arm voltage waveform is presented. In black is marked the reference voltage for the arm [$V_{ref\_arm}(t)$], in red is shown the base voltage calculated by (2.8), the PWM voltage is marked blue.

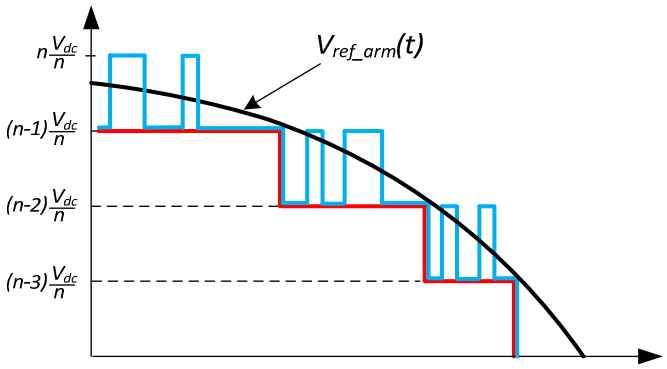

Figure 2.10 – Nearest Level Modulation, arm voltage waveform with SM modulation

2.3 HVDC Transmission System

The decision for the installation of HVDC over HVAC involves capital investments and losses. A DC line with two conductors can carry the same amount of power as an AC line with three conductors of the same size and insulation parameters. This results in smaller footprint and simpler design of towers, reduced conductor and insulation costs. Moreover, line investments are reduced by absence of compensation devices, since DC lines do not consume reactive power. Power losses are reduced due to 30% reduction in conduction losses, minimized corona effect and smaller dielectric losses in case of a cable. The breakeven distance, where DC system tends to be more economic than AC for the overhead lines can vary within 400-700 km, while for the cable systems it is around 25-50 km, depending on particular requirements. [47][48]

The HVDC transmission technology based on high-power electronic devices is widely used nowadays in electrical systems for the transmission of large amounts of power over long distances. The transformation from AC to DC and vice versa is realized by two converter types:

- Current-Source Converters (CSC);
- Voltage-Source Converters (VSC).

Traditional CSCs with mercury-arc valves were used since 1950s, until they were substituted by thyristors in the mid-1970s. Thanks to the rapid development of self-commutated devices and micro controllers, an

alternative as VSC became economically feasible; resulting in the first VSC-HVDC project installed in 1997. Both converter technologies have different operational principles as well as advantages and drawbacks. The decision of which option to select depends on the requirements of particular project. [47][49]

2.3.1 Configuration of HVDC transmission

Depending on functional aspects, three main HVDC configurations shown in Figure 2.11 are used. [47][48]

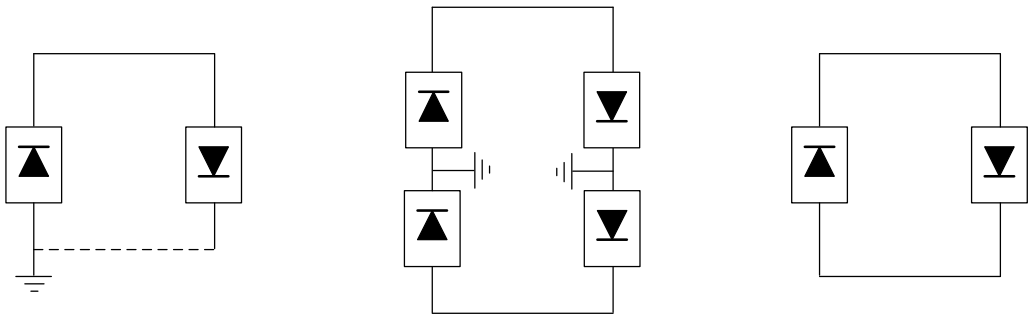

Figure 2.11 - HVDC system configurations. (a) Monopolar. (b) Bipolar. (c) Back-to-back

- Monopolar configuration (a) - interconnects two converter stations via a single line, with the possibility to operate at both DC polarities. Ground, sea or metallic conductor can be used for return path.
- Bipolar configuration (b) - involves two conductors, operating at opposite polarities. This results in two independent DC circuits, rated at half capacity each. During outages of one pole, a monopolar operation can be used. This is the most common configuration for modern HVDC transmission.
- In Back-to-Back configuration (c) - the DC sides of two converters are directly connected, having no DC transmission line. This arrangement is used for the interconnection of asynchronous AC systems.

2.3.2 VSC-HVDC transmission

Even though traditional CSC-HVDC transmission is well established for high power and voltage ratings (typically up to several GW and ±800 kV), it is predicted, that from now on the VSCs will be dominant in the future high power HVDC interconnections due to numerous advantages in economic and technical features [47][49]. The main advantages of VSC-HVDC over CSC-HVDC are summarized below [48][49][50]:

- Independent reactive power control at the both terminals, possibility of four quadrant operation (Figure 2.12). The elimination of reactive power compensation devices results in significant footprint reduction;
- Dynamic support of the AC grid voltage. Operation as STATCOM increases transfer capability and stability of the AC grid;
- Possibility of connection to the weak and passive grids. Low short-circuit capacity requirements of the AC grid. Since a VSC can be considered as a virtual synchronous generator, it can be used for forming offshore AC collector systems for wind power parks;
- Possibility of safe fault ride-through and black start capability;

- Fast active power reversal;
- No need for special converter transformers;
- Fast installation and commissioning.

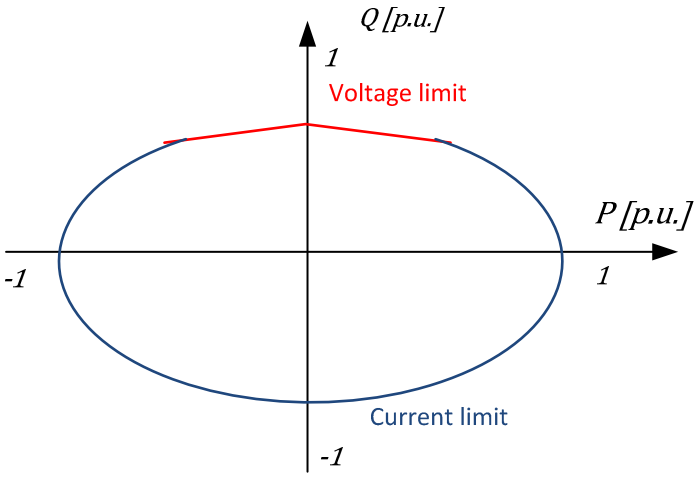

Figure 2.12 - Active-reactive locus diagram of VSC-HVDC transmission system [13]

The typical configuration of modern VSC-HVDC transmission system is shown in Figure 2.13. Two DC conductors of opposite polarity interconnect two converter stations. The polarity of the DC-link voltage remains the same while the DC current is reversed when the direction of the power transfer has to be changed. The DC side capacitors ensure support and filtering of the DC voltage. The converter AC terminals are connected with phase reactors and harmonic filters. The phase reactors ensure control of power exchange between the converter and AC system, the limitation of fault currents and blocking of current harmonics appearing due to PWM. The AC filters reduce harmonics content on the AC bus voltage. Power transformers are used to interface the AC system, adapting converter and AC system voltages as well as participate in power regulation by means of tap changers. [51][52]

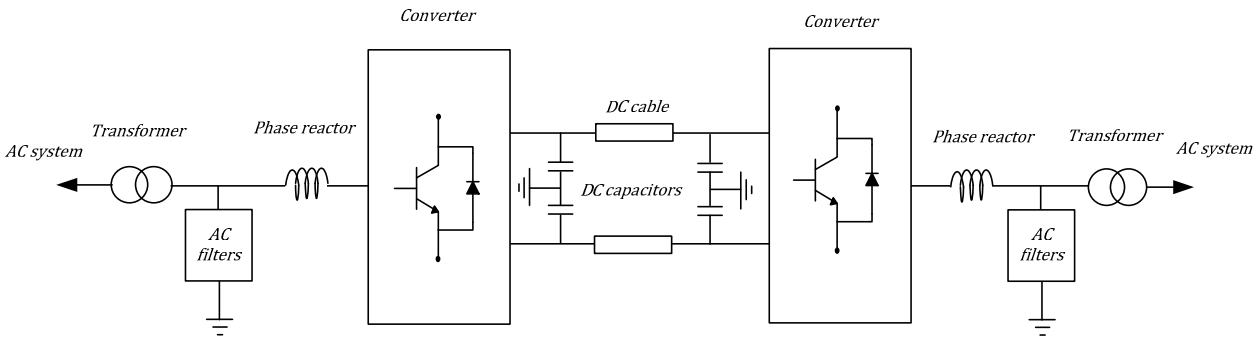

Figure 2.13 - VSC-HVDC system configuration

Theoretically all the multilevel topologies presented in this chapter can be used in VSC-HVDC configurations. However, due to the complex structure, voltage balancing issues and economical considerations, most of the real life applications of VSC-HVDC systems rely on the proven two-level and three-level NPC converter technologies. [16][49]

With the introduction of MMC, the application areas of VSC-HVDC transmission can be broadened significantly. Due to the numerous advantages such as modularity, increased efficiency and reliability that MMC presents, it aims to substitute the existing VSC-HVDC topologies in the nearest future. [16]

The configuration of MMC-HVDC transmission system is shown in Figure 2.14. Compared to the topology presented in Figure 2.13, it can be noticed, that depending on the number of voltage levels and quality requirements of output voltage; AC filters can be significantly reduced or eliminated. Transformers become also optional, since the converter can be scaled to meet the voltage levels of the transmission systems. Due to distributed energy storage in the leg sub-modules, the DC capacitors are also eliminated. [37]

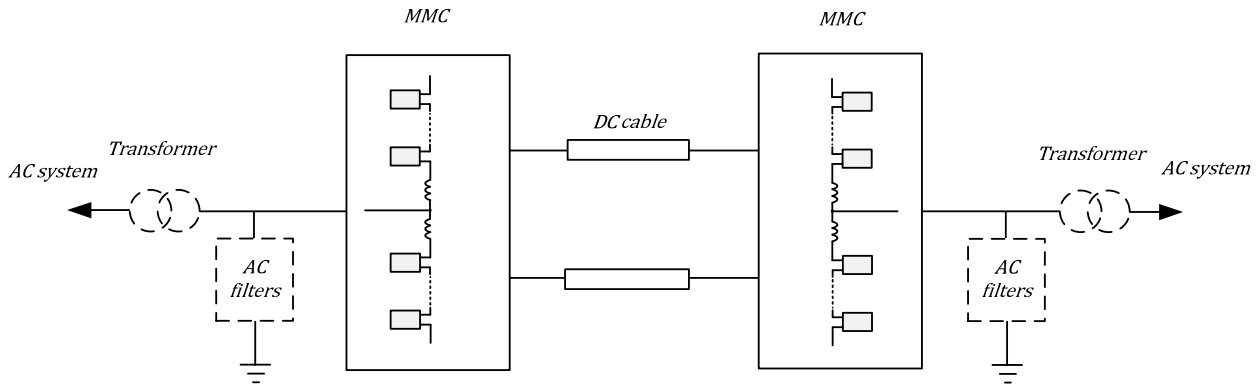

Figure 2.14 - MMC-HVDC system configuration

The mentioned technical aspects result in reduced complexity and footprint of the converter station, making it especially suitable for offshore platforms, where size and reliability are the major selection criteria. [17]

2.4 Grid Code Requirements for HVDC Systems

The Grid Code is an official document which governs the relationship between the participants of the electrical system. Its main purpose is to provide the minimum technical, design and operational specifications for the electricity generation, transmission and distribution as a part of a large network. Most of the national Grid Codes are focused on AC power systems, having very superficial cover of DC interconnections or not mentioning them at all. Moreover, the technical and grid-connection specifications for HVDC systems are not standardized at present. However, information regarding DC interconnections is provided in the UK Grid Codes [53]. The main aspects regarding operational and control requirements, as well as fault ride-through requisites for HVDC are summarised below.

2.4.1 Operation requirements

Since the AC grid is a dynamic system, its main parameters such as voltage at different network points and frequency are subjected to variation due to change in power balance and structure of the grid. These variations to some extent should not affect the operation of the HVDC transmission. The minimum operation capabilities are defined in [53].

The converter station is required to:

- Operate continuously at constant active power output at transmission system frequencies in the range 49.5Hz to 50.5Hz;
- Operate and remain connected to the transmission system at frequencies within the range 47.5Hz to 52.0Hz;
- Remain connected to the transmission system at frequencies within the range 47.0Hz to 47.5Hz for a duration of 30s required each time the frequency is below 47.5Hz;
- Remain synchronised to the transmission system during rate of frequency change up to 1 Hz/s;
- Remain connected providing constant active power output at transmission system voltage variations within the ranges of ±10% of nominal.

The relation of the converter active power and the grid frequency for both inverter and rectifier modes is shown in Figure 2.15. It can be observed, that in inverter mode, when grid frequency is decreasing, active power output can be reduced only by 5% of rated. In contrary, active power input has to be reduced up to 40% when rectifying. This restriction provides frequency support when unbalanced generation-load conditions in the AC system.

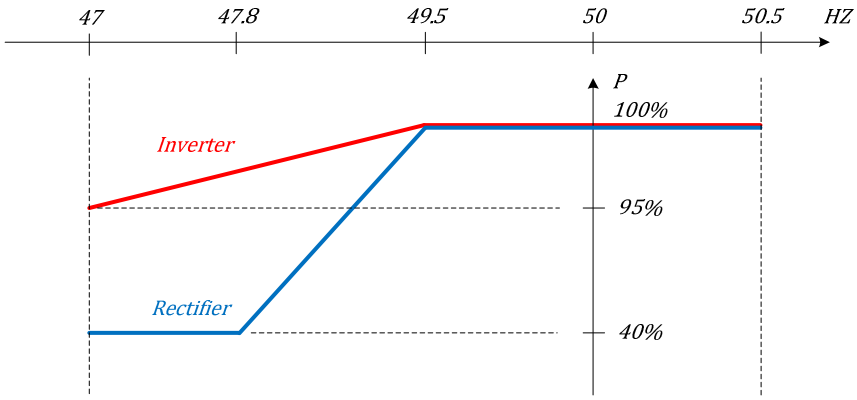

Figure 2.15 – Active power/frequency ratio. [53]

In addition, the converter station should:

- Remain connected to the transmission system during a negative phase sequence load unbalance;
- Be capable of reversing the power at a rated capacity within 5s when emergency;
- Provide ramp-up and ramp-down capability not less than the greater of 10% of the rated capacity per minute or 50 MW per minute.

2.4.2 V/Q Control requirements

The VSC-HVDC interconnection is required to have full control over the reactive power at any point between the 0.95 lagging and 0.95 leading power factor. The reactive power limits in accordance to the active power output are specified in Figure 2.16-a. At steady-state operation, the converter should also provide continuous voltage control at the PCC. Set points and slope characteristics are detailed in Figure 2.16-b.

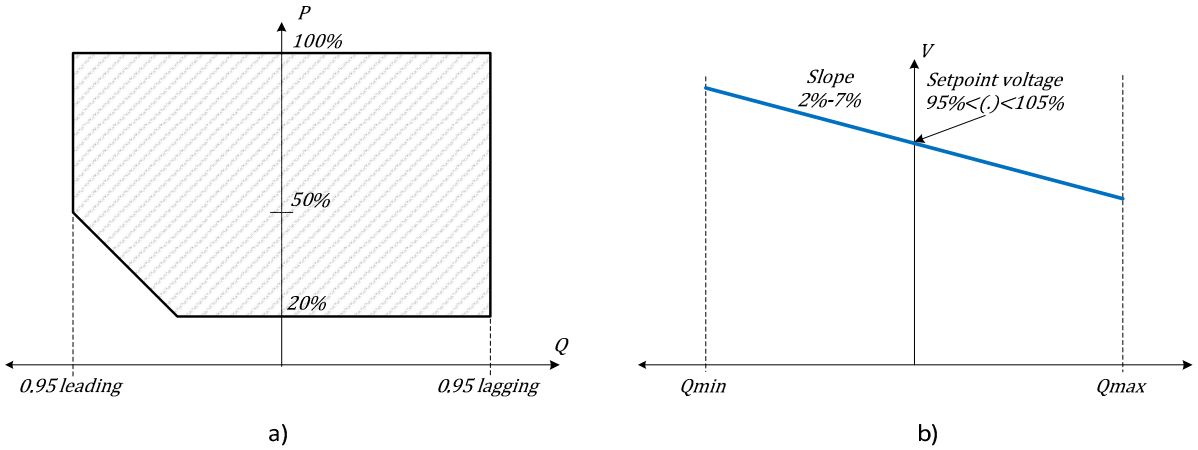

Figure 2.16 – (a) Reactive power requirements. (b) Voltage control requirements. [53]

The reactive power response should start within 0.2s of the application of the step. Full reactive power capability should be reached within 1s.

2.4.3 Fault Ride-Through requirements

Fault ride-through capability is defined as the ability of the power converter to withstand different types of faults. According to [53], the converter must remain stable and connected to the system without tripping for a close-up solid three-phase or any unbalanced short circuit fault for up to 140 ms as shown in Figure 2.17. Each point on the line represents grid voltage level and the associated time duration which converter must stay connected. When voltage level is below the line, converter disconnection is allowed.

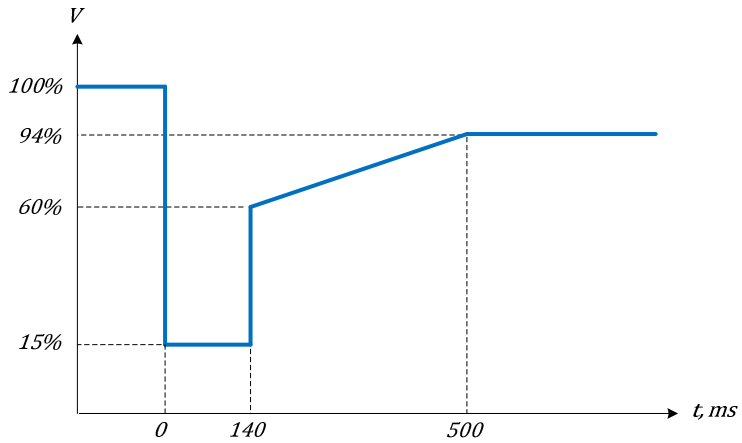

Figure 2.17 – Fault ride-through requirement [53]

Upon clearance of the fault and within 0.5 seconds of the restoration of the voltage to the 90%, active power output should be restored to at least 90% of the pre-fault level. The fault will affect the level of transferred active power, therefore a load reduction or rejection in the other side of HVDC transmission is acceptable. With active power reduction, the converter should generate maximum reactive current without exceeding the transient rating limits of the device, thus supporting the grid voltage during the fault. Moreover, presence of the fault should not be indicated in the other side of the HVDC transmission. [53]

3 Modelling and Analysis of MMC

This chapter studies the interactions of inner voltages and currents in MMC. An average model of MMC is derived and compared with the detailed model in simulations. The arm currents and voltage ripples in the converter are also analyzed.

To have a better understanding of the DC/AC power conversion by the MMC, an average mathematical model of the converter is derived. The model is validated by comparing its steady state and step response against a 9-level switching model built in PSCAD/EMTDC.

During normal operation voltage variations are observed in the sub-modules which influence the currents flowing in the converter. With the intention of understanding the impact of sub-module dynamics on the converter; a detailed analysis of the converter arm currents and the ripples in the sub-module capacitors is included.

3.1 Average Model of MMC

Considering that the sub-module voltages are well balanced and assuming an infinite number of the sub-modules per arm, it is possible to represent the converter arms as variable capacitances in series with an equivalent resistance and the arm inductance, as shown in Figure 3.1. Moreover, it is considered an infinite switching frequency, resulting in the generation of a perfect sinusoidal AC voltage at the converter terminals. [22]

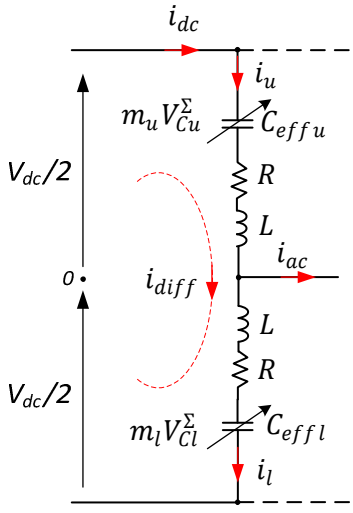

Figure 3.1 – MMC average model

Under these considerations it is possible to represent the insertion of the arm capacitors with a continuous value ($m_{u/l}$); going from 0, when all the sub-modules are bypassed, to 1, when all the sub-modules are inserted. If the sum of the voltages in the arm capacitors is V_{Cx}^{Σ}, the inserted arm voltage can be represented as:

$$V_x(t) = m_x(t) \cdot V_{Cx}^{\Sigma} \tag{3.1}$$

Where x is used to denote either upper (u) or lower (l) arm. Naming the capacitance of one sub-module, C_{SM}, the effective arm capacitance can be calculated as:

$$C_{effx} = \frac{C_{SM}}{N \cdot m_x(t)} \tag{3.2}$$

When the arm current $i_x(t)$ is flowing through the effective capacitance, the total capacitor voltage dynamics are described by:

$$\frac{d}{dt}V_{Cx}^{\Sigma} = \frac{i_x(t)}{C_{effx}} \tag{3.3}$$

Having defined the direction of the arm currents according to Figure 3.1, the output phase current calculated by Kirchhoff's current law (KCL) as:

$$i_u - i_l = i_{ac} \tag{3.4}$$

Considering the difference current i_{diff} flowing through the converter leg, and having an equal contribution from the upper and lower arm currents to the output AC current, i_{ac}, the relation between the arm currents can be expressed as:

$$i_u = i_{diff} + \frac{i_{ac}}{2} \tag{3.5}$$

$$i_l = i_{diff} - \frac{i_{ac}}{2} \tag{3.6}$$

Adding (3.5) and (3.6) leads to,

$$i_{diff} = \frac{i_u + i_l}{2} \tag{3.7}$$

The expression of capacitor voltage dynamics from (3.2) and (3.3) can be expanded for the upper and lower arms:

$$\frac{d}{dt}V_{Cu}^{\Sigma} = \frac{Nm_u i_u}{C_{SM}} \tag{3.8}$$

$$\frac{d}{dt}V_{Cl}^{\Sigma} = \frac{Nm_l i_l}{C_{SM}} \tag{3.9}$$

Analyzing the circuit given in Figure 3.1 it is possible to derive expression for the generated AC voltage (e_v) as:

$$e_v = \frac{V_{dc}}{2} - R_{arm}i_u - L_{arm}\frac{di_u}{dt} - m_u V_{Cu}^{\Sigma} \tag{3.10}$$

$$e_v = -\frac{V_{dc}}{2} + R_{arm}i_l + L_{arm}\frac{di_l}{dt} + m_l V_{Cl}^{\Sigma} \tag{3.11}$$

Subtracting (3.10) from (3.11) the expression for the difference current can be obtained as follows:

$$0 = V_{dc} - 2R_{arm}i_{diff} - 2L_{arm}\frac{di_{diff}}{dt} - \left[m_l V_{Cl}^{\Sigma} + m_u V_{Cu}^{\Sigma}\right] \tag{3.12}$$

From (3.10), (3.11) and substituting for the currents from (3.7) in (3.12) the phase leg of the converter can be described by the following system of differential equations:

$$\frac{d}{dt}\begin{bmatrix} i_{diff} \\ V_{Cu}^{\Sigma} \\ V_{Cl}^{\Sigma} \end{bmatrix} = \begin{bmatrix} -\frac{R_{arm}}{L_{arm}} & -\frac{m_u}{2L_{arm}} & -\frac{m_l}{2L_{arm}} \\ \frac{Nm_u}{C_{SM}} & 0 & 0 \\ -\frac{Nm_l}{C_{SM}} & 0 & 0 \end{bmatrix}\begin{bmatrix} i_{diff} \\ V_{Cu}^{\Sigma} \\ V_{Cl}^{\Sigma} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{2} \\ \frac{Nm_u i_{ac}}{2C_{SM}} \\ \frac{Nm_l i_{ac}}{2C_{SM}} \end{bmatrix} \tag{3.13}$$

It can be noticed from (3.10) and (3.11) that the output voltage does not depend on i_{diff}. At the same time, i_{diff} only depends on the DC-link voltage, V_{dc}, and the total inserted arm voltage, $m_x V_{Cx}^{\Sigma}$. Therefore, the difference current, i_{diff}, can be influenced without disturbing the AC side quantities by adjusting the lower and upper arm insertion index in the same amount [22].

3.2 Switching Model of MMC

In order to evaluate the dynamic performance of MMC under different control structures, a detailed converter model is necessary. As presented in previous sections, besides semiconductor switches, the most important components are the sub-module capacitors and arm inductors. Therefore a selection of the mentioned components is required. The volume of the capacitors is based on the power rating of the converter and the number of sub-modules per arm. Considering the new trends in offshore wind technology and the predictions of the capacity of future offshore wind power plants [54], the rated apparent power for the converter is chosen as 850 MVA [55]. The DC-link voltage is selected as ±320 kV [56]. Due to computational limits, the number of the sub-modules per arm is selected as 8. This results in 80 kV rated sub-modules, which in the real life would require a large number of series connected switches to represent a cell valve.

3.2.1 Selection of cell capacitor

The selection of the cell capacitance is a trade-off between the voltage requirements of the sub-module and the capacitor size. In [57] the total cell capacitance is proposed to be 30-40 kJ per MVA of the converter, resulting in 10% voltage ripple. For the simulation model cell capacitance is calculated as 220 µF for 40 kJ/MVA. However, in [11] is presented an analytical expression that can be used for the capacitance calculation based on the desired ripple factor.

3.2.2 Selection of arm inductor

Inductors are placed in the converter arms to suppress transients in the circulating and fault currents. For the simulation model the arm inductance is selected to be 0.15 p.u. on converter base which is a conventional value used for HVDC projects [55]. Nevertheless, several methods have been proposed to

calculate the inductance based on the desired circulating current amplitude or the limits of fault currents, as presented in [19].

3.2.3 Model Parameters

A switching model of MMC is implemented in PSCAD/EMTDC software with the circuit parameters summarised in Table 3.1. The semiconductors have 0.01 Ω ON-state resistance.

Table 3.1 – Circuit parameters used for MMC model 8-SM

Description	*Abbreviation*	*Value*
Rated apparent power	S_N	850 MVA
Rated cell voltage	V_{SM}	80 kV
DC link voltage	V_{dc}	±320 kV
Arm resistance	R_{arm}	0.1 Ω
Arm inductance	L_{arm}	70 mH (0.15 p.u.)
Cell capacitance	C_{SM}	220 µF (40 kJ/MVA)
Number of sub-modules per arm	N	8

3.3 Comparison of Average and Switching models

To validate the analytical expressions derived in Section 3.1, a comparative analysis of one-phase average and switching models is done. Two different tests are performed; first, the DC-side voltage V_{dc} is stepwise reduced by 20%. Second, the system is subjected to a step change of -20% in the AC voltage reference. The difference current i_{diff} and sum of the arm capacitor voltages V_{Cu}^{Σ}, V_{Cl}^{Σ} are the assessment criteria.

Additionally, the PS-PWM method with carrier frequency $f_C = 301\ Hz$ is implemented in the switching model (the switching frequency is selected to have a natural balancing of the sub-module capacitors). Both models are subjected to direct modulation with modulation index 0.9. The load at the AC terminal is $R_L = (180 + j0.05)\ \Omega$, corresponding to the nominal load of the converter system.

3.3.1 Response to the DC-side voltage step

In Figure 3.2 the response of the switching and average models is shown with black and red lines respectively. The step is applied at the instant t=1.4s. It can be noticed that the capacitor voltages of both models are close during steady operation having error of 3%. After the transient the DC value of the sum capacitor voltages is changed from 640 kV to 512 kV which represents the 20% reduction in DC-side voltage. The relative error between both models is increased to 8% during the transient. The difference currents have an average error within 5%.

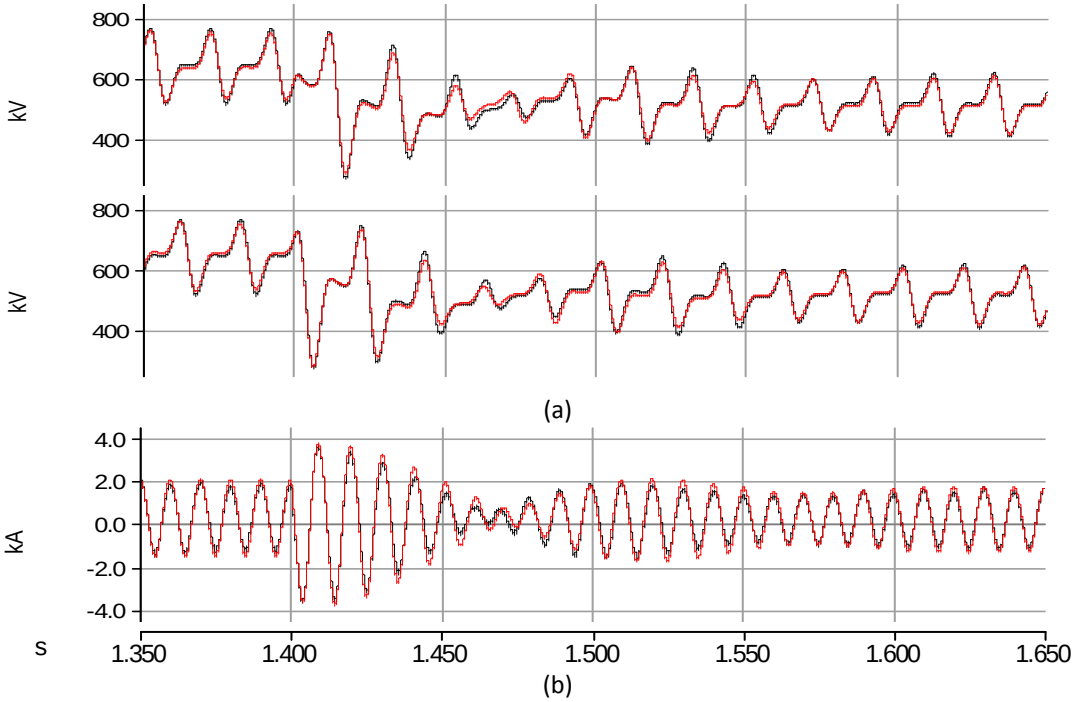

Figure 3.2 – Average vs Switching model, response to DC step. (a) V_{Cu}^{Σ}, V_{Cl}^{Σ}. (b) Difference current

3.3.2 Response to the AC voltage reference step

In Figure 3.3 the response of both models to the AC reference change is shown. The step is applied at the instant t=1.4s. The sum of the capacitor voltages of both models are close during steady and transient having relative error within 4%. After the step is applied the ripple is reduced as a consequence of change in the power output. The difference currents have an average error within 5%.

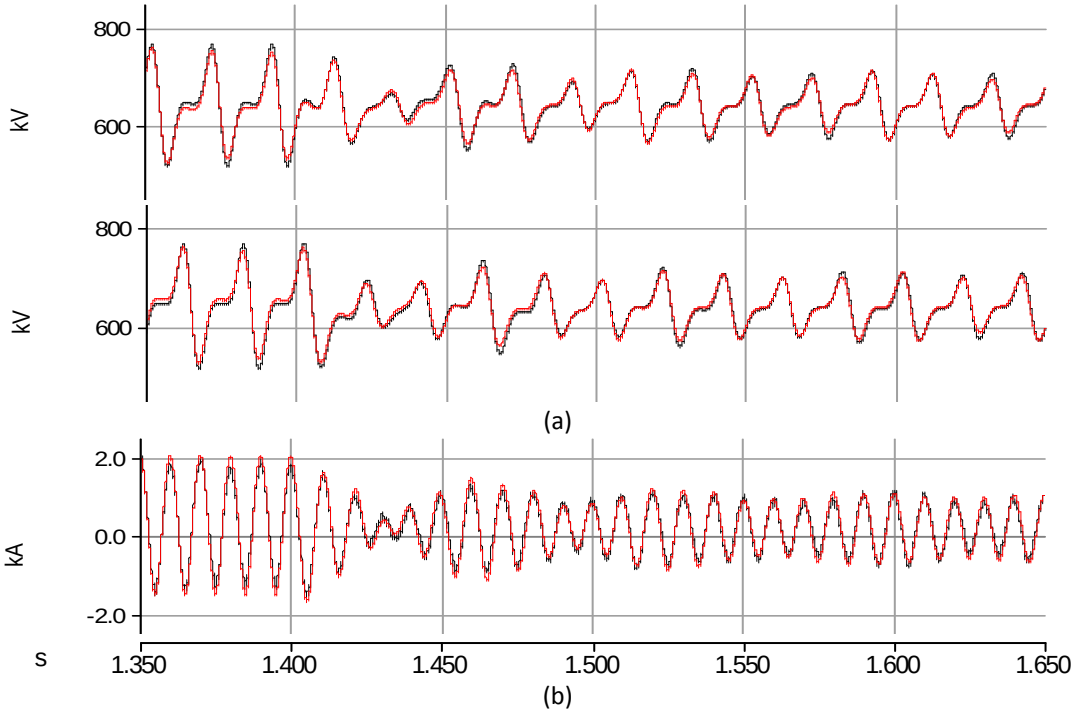

Figure 3.3 - Average vs Switching model, response to AC step. (a) V_{Cu}^{Σ}, V_{Cl}^{Σ}. (b) Difference current

It can be concluded that the average model represents the dynamics of the MMC system acceptably, having mean error of 4% in the simulations performed, with a maximum error of 8% during transients. The difference between the switching model and the average model is proportional to the number of sub-modules and the switching frequency, thus in simulations with a higher number of sub-modules the accuracy should be significantly improved. The average model can be used for preliminary design of the outer control loops and steady-state analysis of the MMC system. However, with the average model, it is not possible to verify control strategies implemented at cell level.

3.4 Analysis of the Arm Currents

In this section the converter arm currents are analyzed based on the study presented in [19]. Having the arm voltages defined in (3.1), (3.10) and (3.11), it is possible to select the reference for the arm voltages as,

$$v_u^{ref} = \frac{V_{dc}}{2} - e_v = \frac{V_{dc}}{2} - \hat{e}_v cos\,(\omega t) \tag{3.14}$$

$$v_l^{ref} = \frac{V_{dc}}{2} + e_v = \frac{V_{dc}}{2} + \hat{e}_v cos\,(\omega t) \tag{3.15}$$

where $\hat{e}_v$ is the peak value of the generated *emf*. Considering a pure DC difference current, in a 1-phase system, it is possible to substitute i_{diff} in (3.5) and (3.6) by the DC current i_{dc} as follows,

$$i_u = i_{dc} + \frac{i_{ac}}{2} = i_{dc} + \frac{\hat{\imath}_{ac}}{2} cos\,(\omega t + \varphi) \tag{3.16}$$

$$i_l = i_{dc} - \frac{i_{ac}}{2} = i_{dc} - \frac{\hat{\imath}_{ac}}{2} cos\,(\omega t + \varphi) \tag{3.17}$$

where $\hat{\imath}_{ac}$ is the peak value of the AC current. Using (3.14) – (3.17), the power in the upper and lower arms is calculated as,

$$P_u = i_u v_u^{ref} = \frac{i_{dc}V_{dc}}{2} - \frac{\hat{\imath}_{ac}\hat{e}_v}{4} cos(\varphi) - i_{dc}\hat{e}_v co\,s(\omega t) + \frac{\hat{\imath}_{ac}V_{dc}}{4} co\,s(\omega t + \varphi) - \frac{\hat{\imath}_{ac}\hat{e}_v}{4} cos(2\omega t + \varphi) \tag{3.18}$$

$$P_l = i_l v_l^{ref} = \frac{i_{dc}V_{dc}}{2} - \frac{\hat{\imath}_{ac}\hat{e}_v}{4} cos(\varphi) + i_{dc}\hat{e}_v co\,s(\omega t) - \frac{\hat{\imath}_{ac}V_{dc}}{4} co\,s(\omega t + \varphi) - \frac{\hat{\imath}_{ac}\hat{e}_v}{4} cos(2\omega t + \varphi) \tag{3.19}$$

Adding the power in the upper and lower arms to calculate the power in the phase-leg results in,

$$P_{leg} = P_u + P_l = i_{dc}V_{dc} - \frac{\hat{\imath}_{ac}\hat{e}_v}{2} cos(\varphi) - \frac{\hat{\imath}_{ac}\hat{e}_v}{2} cos(2\omega t + \varphi) \tag{3.20}$$

where the first two terms represent the DC power and the third term is a double line-frequency AC component present in the arm. Integrating (3.20), the AC component of the energy stored in the phase-leg is given by,

$$W_{leg,ac} = \int P_{leg} dt = -\frac{\hat{\imath}_{ac}\hat{e}_v}{4\omega} sin(2\omega t + \varphi) \tag{3.21}$$

The energy stored in the phase is located in the sub-module capacitors. The energy stored in the capacitors has a quadratic relation with the capacitor voltage, thus from (3.21) can be derived that the voltage across the phase-leg must contain a double line-frequency AC component and a DC component.

In a three-phase system the DC components of the leg voltages are equal, and the double frequency components are shifted by $2\pi/3$ in a-c-b sequence [19]. Including the double frequency component into the arm voltage equations presented previously (3.14)(3.15),

$$v_u = \frac{V_{dc}}{2} - \hat{e}_v cos(\omega t) - \frac{v_{2f}}{2} sin\,(2\omega t + \varphi) \tag{3.22}$$

$$v_l = \frac{V_{dc}}{2} + \hat{e}_v cos(\omega t) - \frac{v_{2f}}{2} sin\,(2\omega t + \varphi) \tag{3.23}$$

The double line-frequency voltage excites the leg impedance, creating a double line-frequency component on the difference current also called circulating current i_{circ},

$$i_{circ} = -\frac{v_{2f}}{4Z_{arm}} sin(2\omega t + \varphi - arg(Z_{arm})) = \hat{\imath}_{circ} cos\,(2\omega t + \gamma) \tag{3.24}$$

where the arm impedance is calculated from the arm inductance L_{arm} and the equivalent resistance R_{arm}. The arm currents can then be decomposed as,

$$i_u = i_{diff} + \frac{i_{ac}}{2} = i_{dc} + \hat{\imath}_{circ} cos(2\omega t + \gamma) + \frac{\hat{\imath}_{ac}}{2} cos\,(\omega t + \varphi) \tag{3.25}$$

$$i_l = i_{diff} - \frac{i_{ac}}{2} = i_{dc} + \hat{\imath}_{circ} cos(2\omega t + \gamma) - \frac{\hat{\imath}_{ac}}{2} cos\,(\omega t + \varphi) \tag{3.26}$$

Analyzing (3.25) and (3.26) can be concluded that the circulating current has no effect on the AC current. This current flows through the converter phase-leg, increasing the RMS value of the arm currents, resulting in higher converter losses. From (3.20) can be noticed that the DC component of the difference current is responsible for the DC/AC power transfer.

3.5 Analysis of the sub-module dynamics

During normal operation voltage variations are observed in the sub-modules. With the intention of understanding the impact of sub-module dynamics on the converter arm voltages, the ripples in the capacitors are analysed according to the study presented in [58].

The analysis is started with the description of the cell capacitor current and voltage and its effect on the generated arm voltage. In Figure 3.4 the parameters of the generalised sub-module under study are detailed; where i_x is the arm current, i_{c_i} is the capacitor current, V_{c_i} is the capacitor voltage, V_{SM_i} is the sub-module voltage and i is the sub-module number in the arm going from 1 to N.

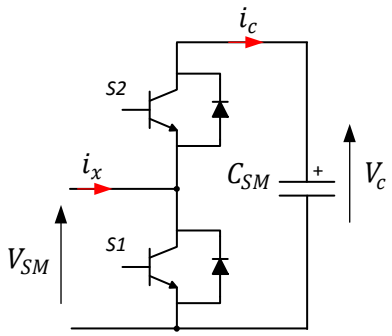

Figure 3.4 – Sub-module, voltages and currents

The arm current interacts with the capacitors of the sub-modules by means of their switching function (S_i), defined as follows,

$$S_i(t) = \begin{cases} 1, & \text{the sub} - \text{module is inserted } (\text{S1} = \text{ON}, \text{S2} = \text{OFF}) \\ 0, & \text{the sub} - \text{module is bypassed } (\text{S1} = \text{OFF}, \text{S2} = \text{ON}) \end{cases} \tag{3.27}$$

The current flowing through the capacitor can be expressed as

$$i_{c\_i}(t) = S_i(t) i_x(t) \tag{3.28}$$

During normal operation, due to the power transfer the capacitors get charged and discharged, imposing a ripple component (Δv_{c_i}) on the capacitor DC voltage (V_{c_dc}). In general, the z-th harmonic of the capacitor voltage ripple ($\Delta v_{c\_i}^{(z)}$) can be expressed by capacitor current and impedance as:

$$\Delta v_{c\_i}^{(z)}(t) = \frac{i_{c\_i}^{(z)}(t)}{j\omega_z C_{SM}} \tag{3.29}$$

where ω_z is the angular frequency of the z-th order component and C_{SM} is the sub-module capacitance.

The volume of the capacitor is inversely proportional to the amplitude of the voltage ripple; therefore the selection of the capacitors is a trade off between the acceptable ripple and the capacitor size. The voltage in the sub-module capacitor can be generally expressed as:

$$V_{c\_i}(t) = V_{c\_dc} + \sum_{z=1}^{\infty} \Delta v_{c\_i}^{(z)}(t) \tag{3.30}$$

The capacitor voltage is reflected in the terminal voltage of the sub-module by means of its switching function as follows:

$$V_{SM\_i}(t) = S_i(t) \left(V_{c\_dc} + \sum_{z=1}^{\infty} \Delta v_{c\_i}^{(z)}(t) \right) \tag{3.31}$$

where the ripple itself is given by:

$$\Delta v_{SM\_i}(t) = S_i(t) \sum_{z=1}^{\infty} \Delta v_{c\_i}^{(z)}(t) \tag{3.32}$$

Subsequently, the voltages generated by the upper and lower arms of the converter can be expressed as:

$$V_u(t) = \sum_{i=1}^{N} S_{ui}(t) V_{c\_dc} + \sum_{i=1}^{N} \Delta v_{SM\_u\_i}(t) \tag{3.33}$$

$$V_l(t) = \sum_{i=1}^{N} S_{li}(t) V_{c\_dc} + \sum_{i=1}^{N} \Delta v_{SM\_l\_i}(t) \tag{3.34}$$

The sum of the sub-module switching functions in the arm is called insertion index $m_x(t)$, presented in Section 3.1. In ideal conditions, at any time instant the sum of the inserted sub-modules in the upper and lower arms should be equal to the number of the sub-modules in the arm (N). That implies the following relation between the switching functions of the arms:

$$\sum_{i=1}^{N} S_{ui}(t) + \sum_{i=1}^{N} S_{li}(t) = m_u + m_l = N \tag{3.35}$$

Since each leg of the converter is composed of two arms, the voltage across the leg can be obtained by adding the voltages generated by the arms. Adding (3.33) to (3.34) and using relation from (3.35) the expression for the leg voltage can be obtained,

$$V_{leg}(t) = N V_{c\_dc} + \Delta v_{leg}(t) \tag{3.36}$$

where Δv_{leg} is the voltage ripple across the leg defined as:

$$\Delta v_{leg}^{(z)}(t) = \sum_{i=1}^{N} \Delta v_{SM\_u\_i}^{(z)}(t) + \sum_{i=1}^{N} \Delta v_{SM\_l\_i}^{(z)}(t) \tag{3.37}$$

Having the DC-link voltage of the converter formed by V_{leg} and the voltage drop across the arm impedance; from (3.36) and (3.37) can be concluded that, by reducing the ripples in the capacitors, the DC-link voltage ripples can be reduced.

3.5.1 Influence of the sub-module dynamics on the converter

Assuming a large number of sub-modules or high switching frequency, the higher order components can be eliminated and the upper and lower arm insertion index of one phase become continuous, given as:

$$m_u = \frac{1}{2} - m(t) = \frac{1}{2} - \frac{1}{2} M cos(\omega t) \tag{3.38}$$

$$m_l = \frac{1}{2} + m(t) = \frac{1}{2} + \frac{1}{2} M cos(\omega t) \tag{3.39}$$

where $m(t)$ is the sinusoidal reference in p.u. to one phase terminal and M indicates the modulation index of the reference voltage. It is possible to derive average currents in the capacitors by multiplying the insertion index given in (3.38) and (3.39) with the corresponding arm current from (3.25) and (3.26). The resulting average capacitor currents in the upper and lower arms are shown in (3.40) and (3.41) respectively.

$$i_{cu\_av}(t) = \underbrace{\frac{1}{2}i_{dc} - \frac{1}{8}M\hat{\imath}_{ac}cos(\varphi)}_{dc\ component} \underbrace{-\frac{1}{2}Mi_{dc}cos(\omega t) + \frac{1}{4}\hat{\imath}_{ac}\,cos(\omega t+\varphi) - \frac{1}{4}Mi_{circ}\,cos(\omega t+\gamma)}_{fundamental\ component} \\ \underbrace{-\frac{1}{8}M\hat{\imath}_{ac}cos(2\omega t+\varphi) + \frac{1}{2}i_{circ}\,cos(2\omega t+\gamma)}_{2^{nd}\ harmonic\ component} \underbrace{-\frac{1}{4}Mi_{circ}\,cos(3\omega t+\gamma)}_{3^{rd}\ harmonic\ component} \tag{3.40}$$

$$i_{cl\_av}(t) = \underbrace{\frac{1}{2}i_{dc} - \frac{1}{8}M\hat{\imath}_{ac}cos(\varphi)}_{dc\ component} \underbrace{+\frac{1}{2}Mi_{dc}cos(\omega t) + \frac{1}{4}\hat{\imath}_{ac}\,cos(\omega t+\varphi) + \frac{1}{4}Mi_{circ}\,cos(\omega t+\gamma)}_{fundamental\ component} \\ \underbrace{-\frac{1}{8}M\hat{\imath}_{ac}cos(2\omega t+\varphi) + \frac{1}{2}i_{circ}\,cos(2\omega t+\gamma)}_{2^{nd}\ harmonic\ component} \underbrace{+\frac{1}{4}Mi_{circ}\,cos(3\omega t+\gamma)}_{3^{rd}\ harmonic\ component} \tag{3.41}$$

Multiplying the fundamental term of the arm currents with the capacitor reactance, the fundamental voltage ripple for both arm capacitors can be obtained:

$$\Delta v_{cu}^{(1)}(t) = -\frac{Mi_{dc}}{2\omega C_{SM}}cos(\omega t) + \frac{\hat{\imath}_{ac}}{4\omega C_{SM}}cos(\omega t+\varphi) - \frac{Mi_{circ}}{4\omega C_{SM}}cos(\omega t+\gamma) \tag{3.42}$$

$$\Delta v_{cl}^{(1)}(t) = +\frac{Mi_{dc}}{2\omega C_{SM}}cos(\omega t) + \frac{\hat{\imath}_{ac}}{4\omega C_{SM}}cos(\omega t+\varphi) + \frac{Mi_{circ}}{4\omega C_{SM}}cos(\omega t+\gamma) \tag{3.43}$$

In similar way the 2nd and 3rd harmonic components of the arm capacitor ripples can be derived:

$$\Delta v_{cu}^{(2)}(t) = -\frac{M\hat{\imath}_{ac}}{16\omega C_{SM}}cos(2\omega t+\varphi) + \frac{i_{circ}}{4\omega C_{SM}}cos(2\omega t+\gamma) \tag{3.44}$$

$$\Delta v_{cl}^{(2)}(t) = -\frac{M\hat{\imath}_{ac}}{16\omega C_{SM}}cos(2\omega t+\varphi) + \frac{i_{circ}}{4\omega C_{SM}}cos(2\omega t+\gamma) \tag{3.45}$$

$$\Delta v_{cu}^{(3)}(t) = -\frac{Mi_{circ}}{12\omega C_{SM}}cos(3\omega t+\gamma) \tag{3.46}$$

$$\Delta v_{cl}^{(3)}(t) = \frac{Mi_{circ}}{12\omega C_{SM}}cos(3\omega t+\gamma) \tag{3.47}$$

From (3.44)-(3.47) the relation between upper and lower arm capacitor ripples can be noticed. The corresponding components are equal in magnitude but have different signs as shown in (3.48).

$$\begin{cases} \Delta v_{cu}^{(1)}(t) = -\Delta v_{cl}^{(1)}(t) \\ \Delta v_{cu}^{(2)}(t) = \Delta v_{cl}^{(2)}(t) \\ \Delta v_{cu}^{(3)}(t) = -\Delta v_{cl}^{(3)}(t) \end{cases} \tag{3.48}$$

Having determined the arm capacitor voltage ripples as the result of the average arm currents, the voltages across the upper and lower arms can be expressed from (3.33), (3.34) and using arm switching functions from (3.38) and (3.39):

$$\begin{cases} V_u(t) = m_u V_{c\_dc} + m_u \Delta v_{cu}(t) \\ V_l(t) = m_l V_{c\_dc} + m_l \Delta v_{cl}(t) \end{cases} \tag{3.49}$$

where Δv_{cu} and Δv_{cl} represent the total voltage ripple on the arm capacitors and are described as:

$$\begin{cases} \Delta v_{cu}(t) = \Delta v_{cu}^{(1)}(t) + \Delta v_{cu}^{(2)}(t) + \Delta v_{cu}^{(3)}(t) \\ \Delta v_{cl}(t) = \Delta v_{cl}^{(1)}(t) + \Delta v_{cl}^{(2)}(t) + \Delta v_{cl}^{(3)}(t) \end{cases} \tag{3.50}$$

By substitution of (3.50) into (3.49) using the relationship given in (3.48) the arm voltages can be represented as follows:

$$V_u(t) = \frac{NV_{c\_dc}}{2} - m(t)V_{c\_dc} - \Delta v_{dm}(t) + \Delta v_{com}(t) \tag{3.51}$$

$$V_l(t) = \frac{NV_{c\_dc}}{2} + m(t)V_{c\_dc} + \Delta v_{dm}(t) + \Delta v_{com}(t) \tag{3.52}$$

where Δv_{dm} is the differential mode ripple component and Δv_{com} is the common mode ripple component expressed through the lower arm ripple component as:

$$\Delta v_{dm}(t) = \frac{N}{2}\left[\Delta v_{cl}^{(1)}(t) + \Delta v_{cl}^{(2)}(t)\, M cos(\omega t) + \Delta v_{cl}^{(3)}(t)\right] \tag{3.53}$$

$$\Delta v_{com}(t) = \frac{N}{2}\left[\Delta v_{cl}^{(1)}(t)\, M cos(\omega t) + \Delta v_{cl}^{(2)}(t) + \Delta v_{cl}^{(3)}(t)\, M cos(\omega t)\right] \tag{3.54}$$

From (3.51) and (3.52) it becomes clear, that converter arm voltages during steady operation are composed of several frequency components. The second harmonic of Δv_{com} generate the circulating current observed in the previous section. Since the third harmonic in all three phases is equal, the corresponding ripple of Δv_{com} generates a zero sequence current that flows to the DC-link. The differential mode voltage ripple, Δv_{dm}, produces a current component that flows to the AC side.

3.6 Chapter Summary

In this chapter the average model of the MMC was derived and compared with a 9-level switching model. Analyzing their response to a step change, the average model demonstrated an accurate representation of the converter dynamics.

The converter arm currents were studied, demonstrating the presence of a double frequency AC component product of the DC/AC power transfer. It was observed that this component does not contribute to the power transfer; therefore it only increases the RMS value of the arm current, increasing the converter losses.

The effect of the sub-module dynamics on the converter was mathematically analyzed, showing the influence of the capacitor current harmonics on the ripples of the converter arm voltages.

4 MMC-HVDC Model Development

In this chapter a model of MMC-HVDC transmission system is developed and tested. First, the inner control techniques for the MMC are discussed and proven through simulations. Then, the outer control loops for the VSC-HVDC transmission systems are presented. The chapter ends with the analysis of the simulation results.

In this project, the MMC Inner Control shall be referred to the control of the sub-module capacitor voltages and the circulating current. The outer controls denote the control loops implemented for the regulation of the output parameters of the converter; e.g. current control, DC voltage control and PQ control.

4.1 Inner Control of MMC

Having a series connection of sub-modules with floating capacitor voltages brings the advantages of a staircase output waveform with low switching frequencies, as shown in the previous chapter. However it increases the level of complexity of the system from the control point of view. To assure an accurate and stable operation of the converter, the sub-modules must be charged to the same voltage level. Moreover, in order to maintain the output voltage level of the converter, the capacitor voltages must be kept at a reference value.

The balance between the sub-modules can be maintained by two approaches; adding a balancing component to the modulation index of each sub-module [20] or by sorting the sub-modules to be inserted during the charging and discharging cycle [37].

The first approach has the disadvantage of a difficult controller design and implementation, since a distributed control structure must be implemented. Also, because each sub-module can modify its own modulation index independently, this approach may generate even harmonics in the output voltage.

In the second approach, the voltage in the capacitors is measured several times per fundamental period. The sub-modules are sorted in order, according to their capacitor voltages. When the arm current is positive, the sub-modules with the lowest voltage are switched first; and thus their capacitors get charged. The opposite action is done when the current is negative [37]. This procedure must be done periodically; as a result, even if the number of inserted sub-modules is not changed, unnecessary switching operations would be performed. This increases the switching frequency and therefore the switching losses.

Even though these two approaches assure equal voltage share among the arm sub-modules, the voltage share between arms must also be taken into consideration.

As proven in Chapter 3, the difference current contains a strong double line-frequency component that circulates through the converter legs [22]. If not controlled, this current component will increase the losses in the system, but most important it may create unbalances and disturbances during transients [22].

Many strategies have been proposed in order to keep the DC capacitors voltage to a desired value and eliminate the AC component present in the difference current. In this section three of the most popular control strategies are discussed in conjunction with their modulation and balancing algorithm.

At the end of this section, a control strategy or combination of strategies is selected for further implementation into the HVDC transmission system.

4.1.1 Energy Control

This method was first proposed by Antonopoulos in [22], where the arm capacitor voltages are kept to a reference through the control of the total stored energy W_c^{Σ} in the phase leg and the difference between the energy stored in the upper and lower arms W_c^{Δ}.

Following the closed loop approach proposed in [22]; aiming to compensate for the capacitor ripples, the ideal insertion indices can be calculated as,

$$m_u = \frac{V_{dc}/2 - e_v^{ref} - v_{diff}^{ref}}{V_{cu}^{\Sigma}} \tag{4.1}$$

$$m_l = \frac{V_{dc}/2 + e_v^{ref} - v_{diff}^{ref}}{V_{cl}^{\Sigma}} \tag{4.2}$$

where the difference voltage is defined as $v_{diff} = Ri_{diff} + L\frac{di_{diff}}{dt}$. Unfortunately, as proved in [59][60], when using this selection of insertion indexes two additional control loops must be implemented in order to gain stability.

An open loop approach using the estimation of the stored energy is proposed in [23] with the intention of increasing the stability of the system and avoiding the need of a continuous measurement of the capacitors voltage to calculate the converter stored energy.

In this approach the measurement of the sum of the voltages in the arm capacitors ($V_{cu,l}^{\Sigma}$) is replaced with an estimated value ($\tilde{V}_{cu,l}^{\Sigma}$). The insertion indices are calculated as follows:

$$m_u = \frac{V_{dc}/2 - e_v^{ref} - v_{diff}^{ref}}{\tilde{V}_{cu}^{\Sigma}} \tag{4.3}$$

$$m_l = \frac{V_{dc}/2 + e_v^{ref} - v_{diff}^{ref}}{\tilde{V}_{cl}^{\Sigma}} \tag{4.4}$$

The estimated values are obtained by integrating (3.18) and (3.19), and considering a constant difference current i_{diff} and difference voltage v_{diff}.

The obtained insertion indexes compensate for the ripples in the capacitor voltages, as the result circulating current is suppressed.

A block diagram of this control strategy is presented in Figure 4.1. The nearest level modulation is used (Section 2.2.3) and the sub-module balance is done by means of sorting algorithm.

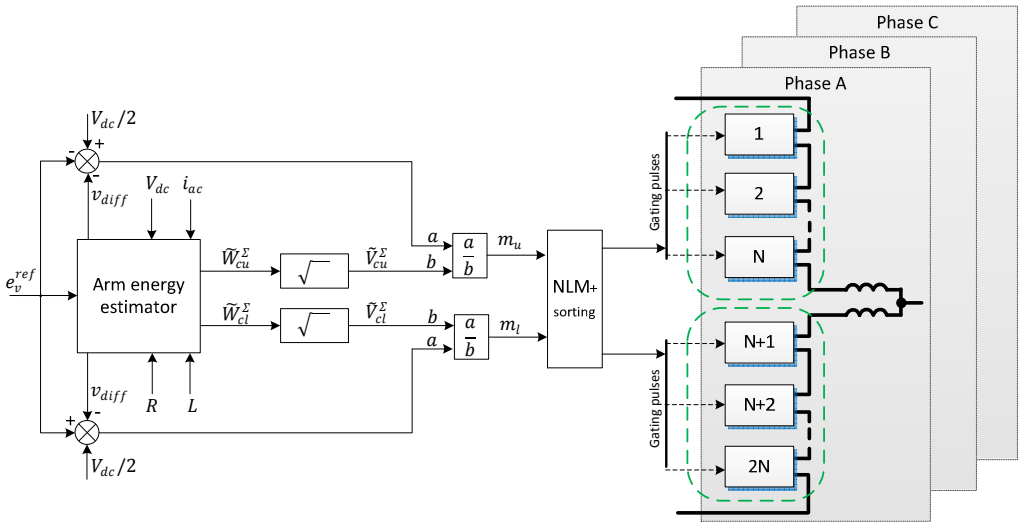

Figure 4.1 - Open-Loop Energy Control, block diagram

4.1.1.1 Simulation results

The described strategy is implemented in the simulation to verify its performance in switching model of MMC. In Figure 4.2 the arm capacitor voltages and differential current of converter phase A are shown. At time t=1s the energy control is enabled. The ripple factor in the upper and lower arm is reduced from 9% to 6%. The double line-frequency circulating current is almost eliminated after 0.18s (c). At time t=1.2s a 10% step change in arm energy reference is applied. After a transient of 0.1s the capacitor voltages are stabilised, reaching the new average value of 88 kV.

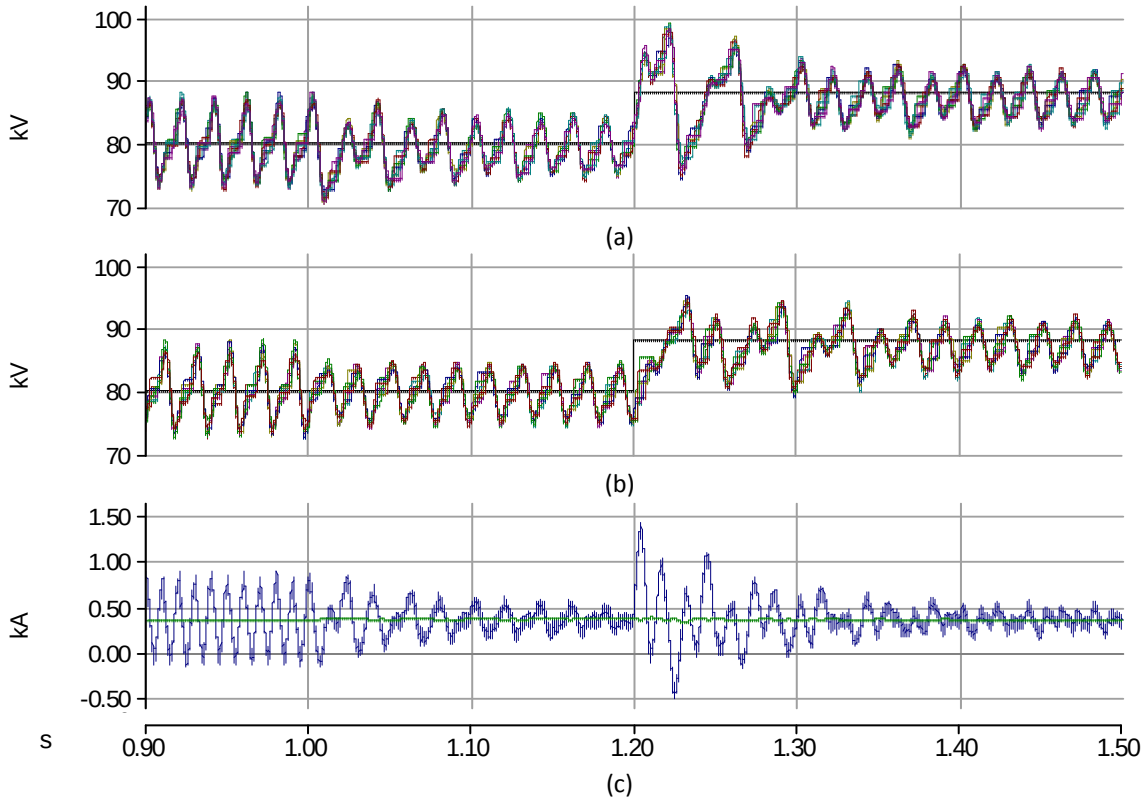

Figure 4.2 – Open-Loop Energy Control, simulation results. (a) Upper arm capacitor voltages. (b) Lower arm capacitor voltages. (c) Difference current

The method presented good response to a change in the arm energy reference and effective elimination of the circulating current. The capacitor voltages remain well balanced in steady state and transients, which is achieved by the sorting algorithm.

However, implementing this control strategy, it was observed that distortions appear in the converter output currents. In [61] a method is proposed to eliminate this problem, but due to time constrains it was not further investigated.

4.1.2 Distributed control

In this method, proposed by Akagi in [20], the cell capacitor voltages are controlled independently. The control is implemented in two parts:

- Averaging part, implemented per phase-leg;
- Balancing part, implemented in each sub-module.

In Figure 4.3 the block diagram of the distributed control method is presented. As it can be observed, the averaging control is implemented in two loops, outer voltage loop and inner current loop. The voltage loop is responsible of controlling the mean value of the capacitor voltages in the leg by influencing each cell individually. The error signal is processed in the controller, resulting in the reference signal for the difference current loop. Under the balanced conditions, the DC component of the difference current is equal to 1/3 of the DC-link current, therefore a feed-forward term is added to increase the response of the controller as highlighted in Figure 4.3.

If the average voltage $V_{C,av}$ is lower than the desired value, V_C^{ref}, a positive current reference is obtained. The current reference is subtracted from the measured value, reducing the control command. By this means, the DC component of the difference current is increased, rising the charge in the capacitors.

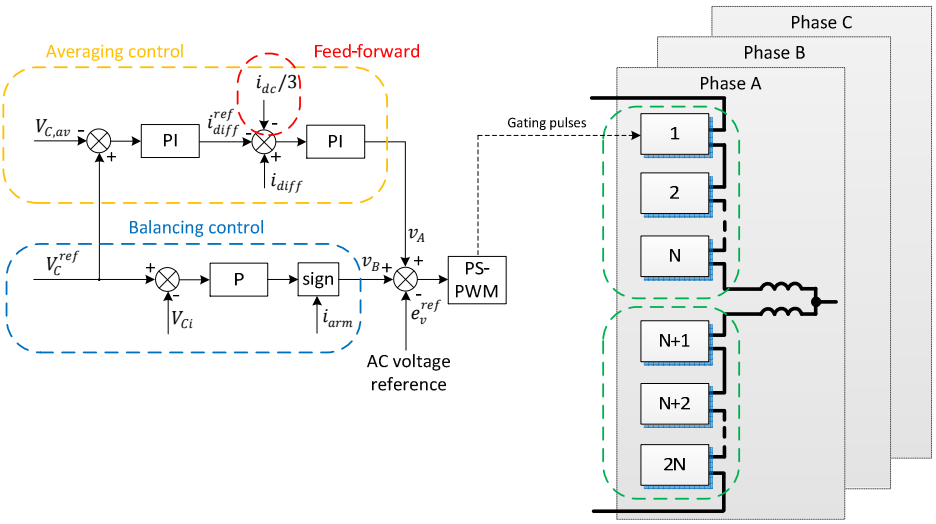

Figure 4.3 – Distributed Control, block diagram

The average charge of the capacitors depends on the DC component of the difference current. If only an integral compensator is used, the DC value of the difference current is controlled, making in no effect on

the circulating current. The compensator in the current loop acts on the AC component of the difference current. The Balancing control is implemented in each sub-module individually. The control signal is generated based on the capacitor voltage and the direction of the corresponding arm current.

The final sub-module voltage reference is obtained by adding both averaging and balancing control signals to the voltage reference.

4.1.2.1 Simulation results

Figure 4.4 depicts the voltages of the phase-leg capacitors with only balancing control. The controls is activated at t=0.5s, it can be observed that after 0.1s the capacitor voltages are effectively balanced.

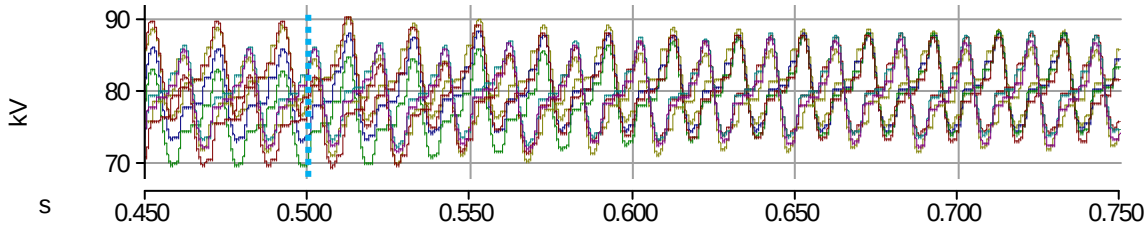

Figure 4.4 – Sub-module capacitor voltages with Balancing control

In Figure 4.5 the arm capacitor voltages (a,b) and difference current (c) of converter phase A are shown. The averaging control is activated at t=1s, after the stabilisation the amplitude of the circulating current is reduced by 35% and the ripple factor in the capacitor voltages is reduced from 9% to 5%. At time t=1.2s a 10% step change in arm voltage reference is done. The new voltage value of 88 kV is reached within 2 fundamental cycles.

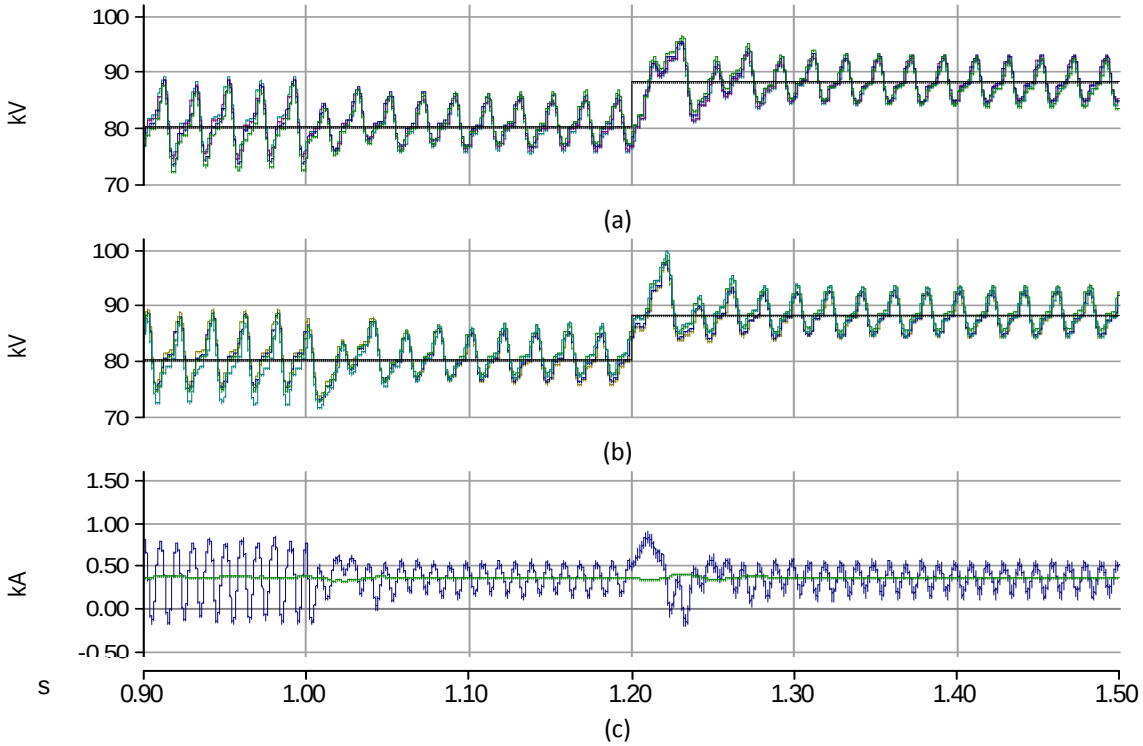

Figure 4.5 - Distributed Control, simulation results. (a) Upper arm capacitor voltages. (b) Lower arm capacitor voltages. (c) Difference current

The method has shown a fast response to changes in the voltage reference. However, the circulating current amplitude was just reduced by 35%, when the objective is to suppress it. The capacitor voltages were effectively balanced in steady state and during transients.

4.1.3 Direct Suppression of Circulating current

This method first proposed in [24] aims to eliminate the double line-frequency circulating current. The circulating current suppressing controller (CCSC) is implemented as vector current control, as shown in Figure 4.6.

The three phase difference currents are calculated and transformed to a double line-frequency negative-sequence rotational reference frame. The current references for the control loops are set to zero since the objective is to eliminate the circulating current. The output signal is transformed back to three phase signals, which are subtracted from the upper and lower arm voltage commands of the corresponding phase. In this manner, the arm currents can be influenced without affecting the output voltage.

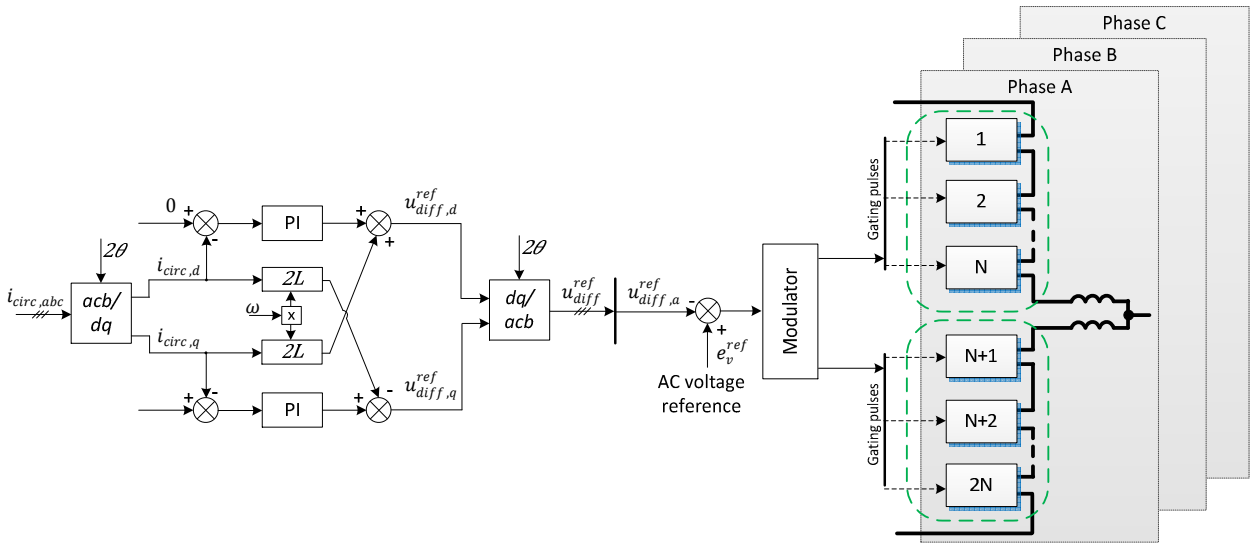

Figure 4.6 - Circulating Current Suppression Control, block diagram

4.1.3.1 Simulation results

Using the described control strategy, the results of the simulation are presented in Figure 4.7. The CCSC is activated at t=1s. It can be observed that after 0.15s the circulating current is effectively eliminated and the amplitude of the ripples in the arm capacitors is reduced from 9% to 5% (a,b).

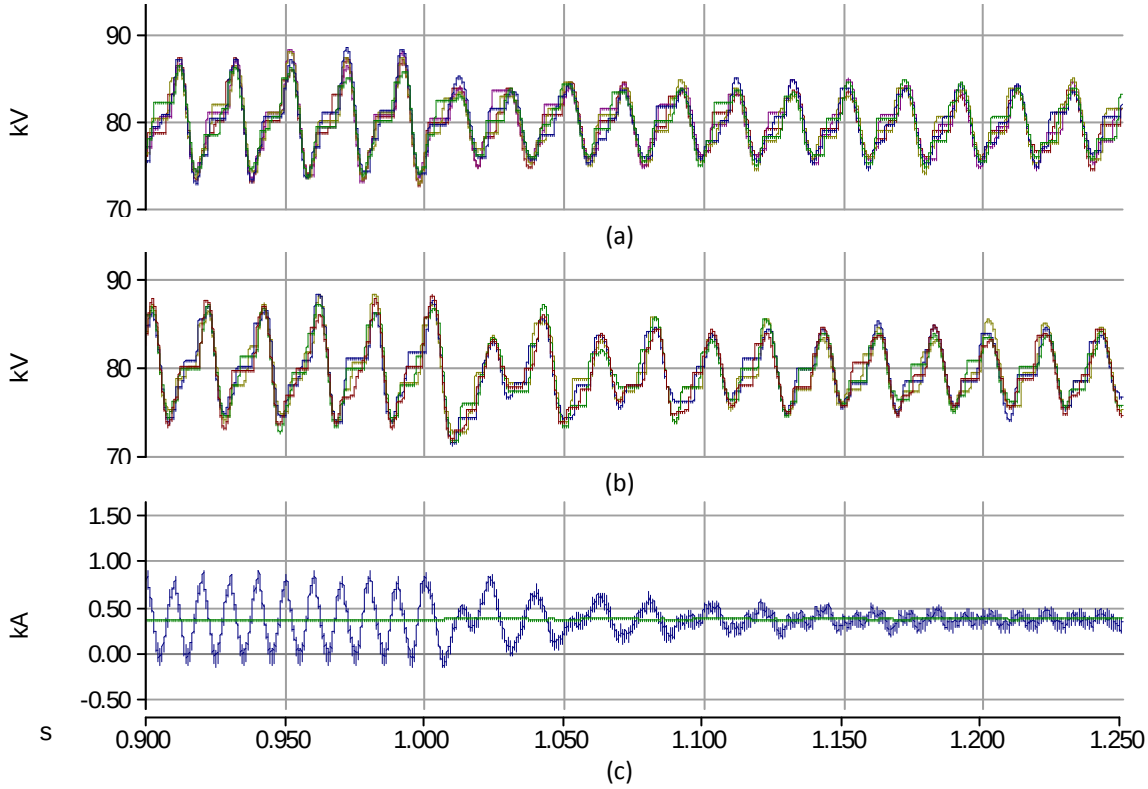

Figure 4.7 - Ciculating Current Suppression Control, simulation results. (a) Upper arm capacitor voltages. (b) Lower arm capacitor voltages. (c) Difference current

A modification of this method is presented in [62], implementing quasi-PR controllers on each phase to suppress higher order harmonics of the circulating current. By this means, the harmonic content of the output voltage can be reduced even more. Because of the limited advantages presented in this method, adding a more complex structure, the modified CCSC was not implemented and tested.

Due to the satisfactory results shown in simulations and simple implementation, the Direct suppression strategy together with the Distributed control were selected for further integration into an HVDC transmission system.

4.2 HVDC Controls

In HVDC transmission system the outer control regulates the power transfer between the AC and DC systems. The active and reactive power is regulated by the phase and the amplitude of the converter line currents with respect to the PCC voltage. The control structure for conventional VSC-HVDC systems consists of a fast inner current control loop and outer control loops, depending on the application requirements, as shown in Figure 4.8. [33]

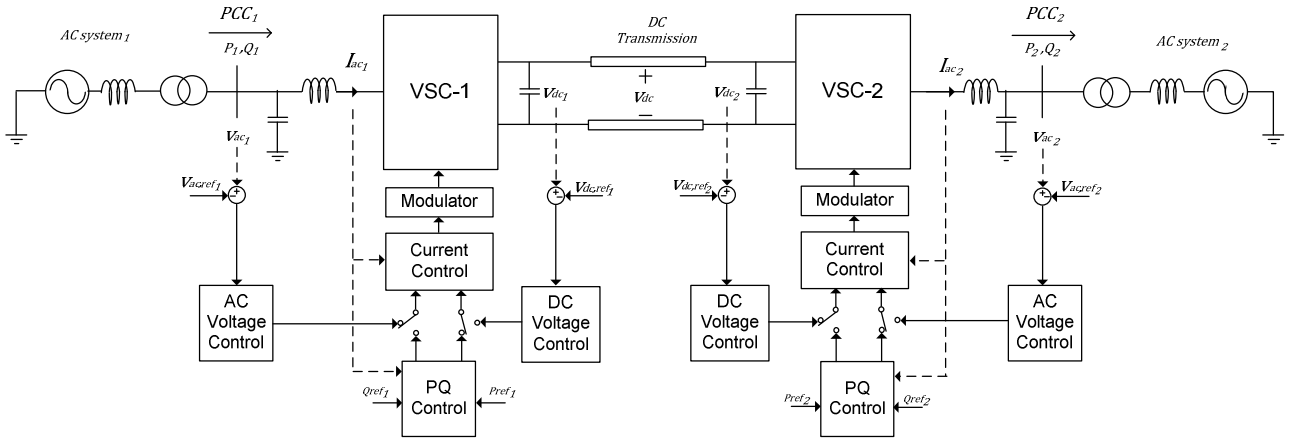

Figure 4.8 - VSC-HVDC system

The current loop is responsible for fast tracking of references generated in the power controller, DC or AC voltage controllers. When operating in inverter mode, the converter controls the DC-link voltage at predefined value. To achieve this, the DC voltage controller adjusts the active current reference in such a way, that the net imbalance of power exchange between the DC and AC systems is kept to zero. In rectifier mode, the converter tracks active power references directly. The reactive power at both sides can be controlled independently. It can be regulated to track a reference, thus regulating power factor at the PCC; or to control of the AC grid voltage at the PCC [33]. A phase locked loop (PLL) is used for the synchronisation with the grid voltage. The PLL mechanism is able to detect phase angle and the magnitude of the grid voltage, to be later used in the controls. The grid frequency can also be obtained from PLL.

In the following sections, the application of the control loops presented in Figure 4.8 is investigated for MMC-HVDC system.

4.2.1 Phase Locked Loop

The synchronous reference frame PLL is the most extended technique used for the synchronisation with the three-phase grid. In Figure 4.9 is presented the structure of PLL where the three-phase voltages are transformed into vectors in the *dq* rotating frame by means of Park's transformation (Appendix). The feed-forward loop includes an integrator, which is resettable at $\omega = 2\pi$, to calculate the grid angle θ and a PI controller, which adjusts the angle θ to the objective$\theta(t) \approx \omega t + \Psi_0$, thus making grid voltage component V_{sq} in the steady-state equal to zero. In that case V_{sd} represents the amplitude of the balanced three-phase voltage. The obtained angle θ and angular grid frequency ω are used for *abc/dq* voltage and current transformations and are fed into the control loops as part of de-coupling terms. [33][31]

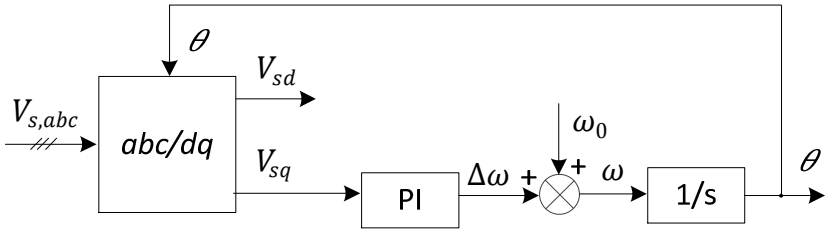

Figure 4.9 – Phase Locked Loop, structure

The transfer function of the PLL is given by [63]:

$$H(s) = \frac{K_p s + \frac{K_p}{T_i}}{s^2 + K_p s + \frac{K_p}{T_i}} \tag{4.5}$$

The structure of $H(s)$ is similar to the general second-order transfer function, therefore PI parameters can be obtained as follows:

$$K_p = \frac{9.2}{t_s} \tag{4.6}$$

$$T_i = \frac{t_s \xi^2}{2.3} \tag{4.7}$$

Where t_s is the desired settling time and ξ is the damping factor. [63]

4.2.2 Current Control Loop

The dynamics of the converter AC side in *dq* reference frame are given by [33]:

$$L\frac{d}{dt}i_d = i_q \omega L - i_d R + V_{td} - V_{sd} \tag{4.8}$$

$$L\frac{d}{dt}i_q = -i_d \omega L - i_q R + V_{tq} - V_{sq} \tag{4.9}$$

where i is the output current, L and R are the impedance of the system, V_t is the terminal voltage and V_s is the grid voltage.

Based on (4.8) and (4.9) the *dq* current control structure is designed, as shown in Figure 4.10. Since the tracking signals are DC values, a proportional-integral (PI) controller is used. A voltage feed-forward and current de-coupling terms are added in order to improve the performance of the controller. [33]

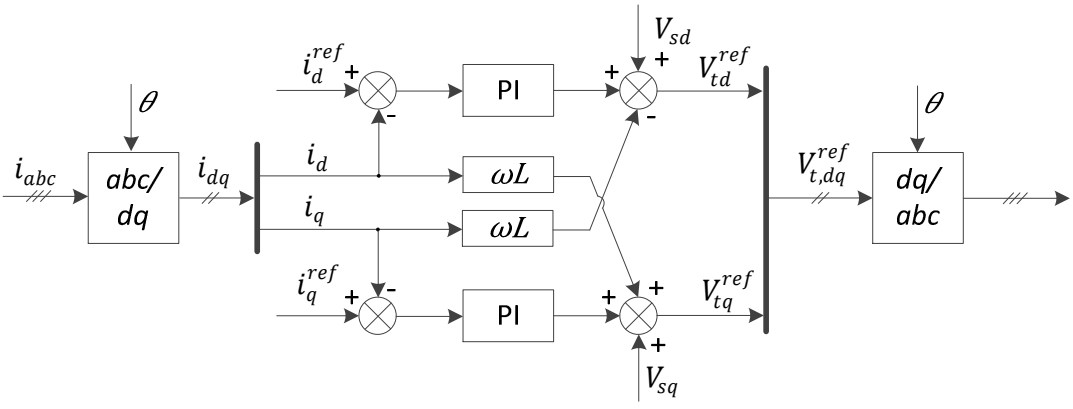

Figure 4.10 - Current control, structure

Since both *d* and *q* loops have the same dynamics, the tuning of PI controllers was realised for one loop.

The current control loop is designed to achieve fast response. The tuning is based on the modulus optimum principle, due to cascaded control structure [64]. Neglecting the coupling and feed-forward terms, the reduced block diagram of current control loop is shown in Figure 4.11.

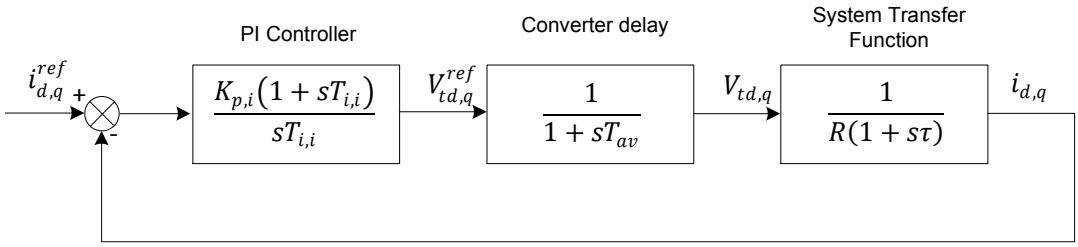

Figure 4.11 – Current control, block diagram

where T_{av} is the average time delay, which equals to half of the switching cycle.

The open loop transfer function of the system is:

$$G_{curr,ol} = \frac{K_{p,i}(1+sT_{i,i})}{sT_{i,i}} \cdot \frac{1}{1+sT_{av}} \cdot \frac{1}{R(1+s\tau)} \tag{4.10}$$

where $\tau = L/R$ is the time constant of the plant. By choosing the controller zero as $T_{i,i} = \tau$, the cancellation of slow system pole is achieved. The open loop transfer function becomes:

$$G_{curr,ol} = \frac{K_{p,i}}{s\tau R} \cdot \frac{1}{(1+sT_{av})} \tag{4.11}$$

The proportional gain of the controller is calculated based on the condition:

$$\left| \frac{G_{curr,ol}}{1+G_{curr,ol}} \right| = 1 \tag{4.12}$$

Resulting in:

$$K_{p,i} = \frac{\tau R}{2T_{av}} \tag{4.13}$$

The closed loop transfer function of the system becomes:

$$G_{curr,cl} = \frac{1}{2T_{av}^2 s^2 + 2T_{av}s + 1} \tag{4.14}$$

Substituting system values into derived equations, controller parameters are obtained as $K_{p,i} = 194$, $T_{i,i} = 0.81$. These values were used as starting point for, to be adjusted in PSCAD simulations. The final

gains implemented are $K_p = 194$, is $T_i = 0.0005$. In Figure 4.13 the step response of the current control is presented. It can be observed that the influence of the step imposed in to one current component has a minimum impact on the other. The reference is closely tracked.

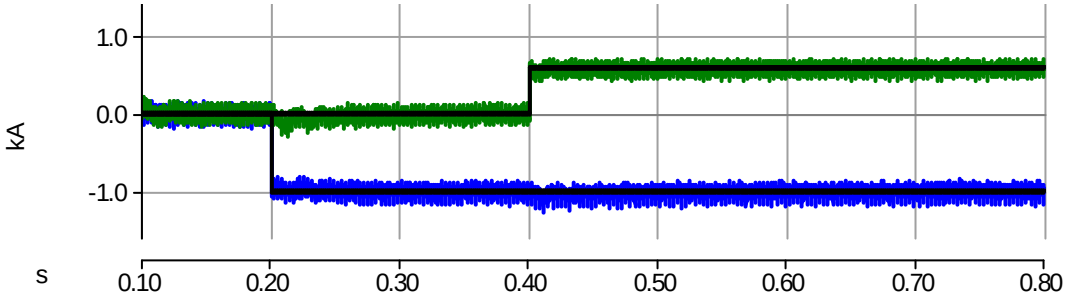

Figure 4.12 – Current control response to a Step. (blue) i_d , (green) i_q .

4.2.3 DC voltage Control

The DC voltage control loop adjusts active current reference to keep the net power exchange between the DC and AC systems to zero. The tuning method is based on the symmetrical optimum criterion [64][65]. The simplified block diagram of the DC voltage control is shown in Figure 4.13. The inner current controller is substituted by an equivalent first order approximation, having $T_{eq} = 2T_{av}$ [64].

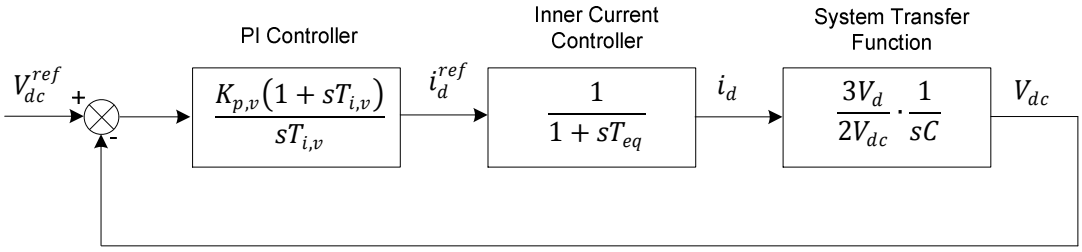

Figure 4.13 – Block diagram of DC voltage control

The DC system transfer function is obtained from the DC-link capacitor current equation, linearised around the steady-state voltage reference. The open loop transfer function of the system is:

$$G_{volt,ol} = \frac{K_{p,v}(1+sT_{i,v})}{sT_{i,v}} \cdot \frac{1}{1+sT_{eq}} \cdot \frac{3V_d}{2V_{dc}} \cdot \frac{1}{sC} \tag{4.15}$$

Applying symmetric optimum conditions [64], the controller parameters can be obtained as:

$$T_{i,v} = a^2 T_{eq} \tag{4.16}$$

$$K_{p,v} = \frac{2V_{dc}C}{3V_d T_{eq}} \tag{4.17}$$

where a is the symmetrical tuning parameter, usually taken within the range of 2-4 [65].

In the MMC topology there is no capacitor between the DC terminals; the DC-link voltage is formed by the inserted sub-modules in the three phases and the voltage drops across arm inductances. Assuming that at any time instant the number of inserted sub-modules in one leg is equal to N, the equivalent DC-link capacitance is:

$$C_{dc\_eq} = 3\frac{C_{SM}}{N} \tag{4.18}$$

where coefficient 3 comes from the number of converter legs. Using the equivalent capacitance and system parameters, the controller gains are obtained as $K_{p,v} = 0.025$, $T_{i,v} = 0.015$. In PSCAD implementation the gains are $K_p = 0.025$, is $T_i = T_{i,v}/K_{p,v} = 0.62$. The response of the DC voltage control to a 10% step change is presented in Figure 4.14. It can be observed that the voltage settles around the reference after 0.1s, having an overshoot of 21%.

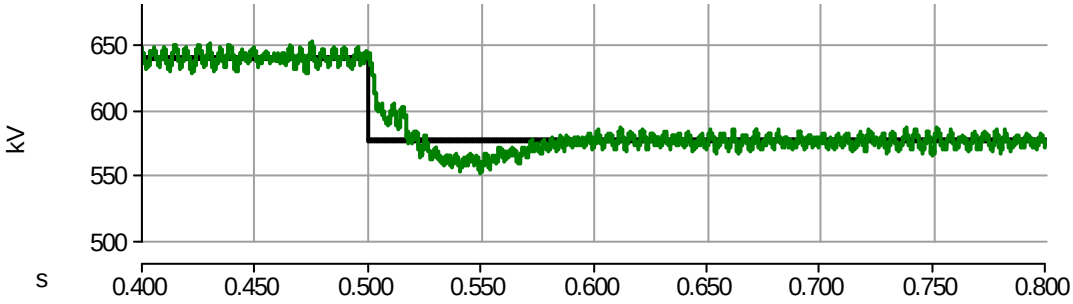

Figure 4.14 – DC voltage control response to a 10% Step.

4.2.4 Active/Reactive power control

The instantaneous power delivered to the AC grid in *dq* reference frame can be calculated by [33]:

$$P_{s,dq}(t) = \frac{3}{2}[V_{sd}(t)i_d(t)] \tag{4.19}$$

$$Q_{s,dq}(t) = -\frac{3}{2}[V_{sd}(t)i_q(t)] \tag{4.20}$$

where $V_{sd,q}$ are the grid voltage components and cannot be controlled. The references for the currents can be obtained from (4.19) and (4.20) as follows [33]:

$$i_d^{ref}(t) = \frac{2}{3V_{sd}}P_s^{ref}(t) \tag{4.21}$$

$$i_q^{ref}(t) = -\frac{2}{3V_{sd}}Q_s^{ref}(t) \tag{4.22}$$

To ensure precise tracking of power references, the power control is implemented in a closed-loop manner as shown in Figure 4.15. This implies additional pair of controllers that provide error reference signals for currents.

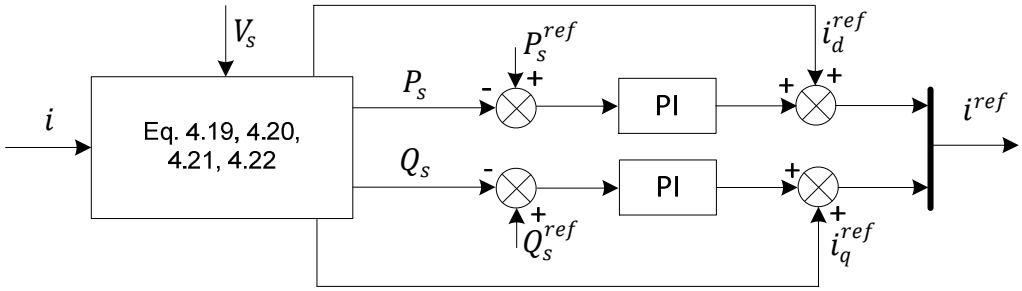

Figure 4.15 – Power Controllers

The controller gains are calculated based on symmetrical optimum criterion and adjusted in the simulation model to achieve desired response. In PSCAD implementation the gains are $K_p = 0.0006$, $T_i = 0.2$.

4.2.5 AC voltage control

Alternatively to the power controller, the reactive power can be controlled indirectly, through the AC voltage control at the PCC. The AC voltage control loop provides reactive current reference based on the measured grid voltage as seen in Figure 4.16.

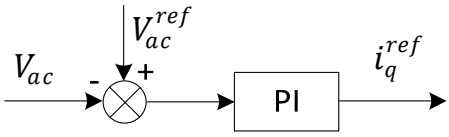

Figure 4.16 - AC voltage controller

The control signal is determined comparing the grid voltage RMS with the reference vale. If the grid voltage level at the PCC is lowered, the reactive power output of the converter increases, boosting the AC voltage.

The controller gains used in PSCAD implementation are $K_p = 0.05$, $T_i = 0.1$.

4.2.6 Model of MMC-HVDC system

The described control loops were implemented in the simulation of HVDC transmission system, shown in Figure 4.17. The system consists of two MMC stations, interconnected with 100 km long DC cable (parameters in Appendix). The three-phase MMC with parameters from Table 3.1 are transformerlessly connected to the AC grids. The grid stiffness is indicated by the short-circuit ratio of 10. The AC line-to-line RMS voltage is 350 kV resulting in converter operation at 0.9 modulation index, which ensures good controllability margins.

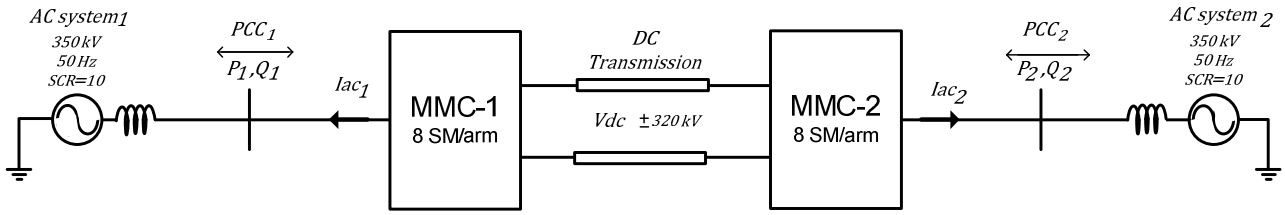

Figure 4.17 - MMC-HVDC system

Both MMC stations have similar control loops as shown in Figure 4.18 having the possibility of changing the operation mode, i.e. power transfer reversal. The output of the MMC inner controls is added to voltage reference from the current control loop and sent to the modulator.

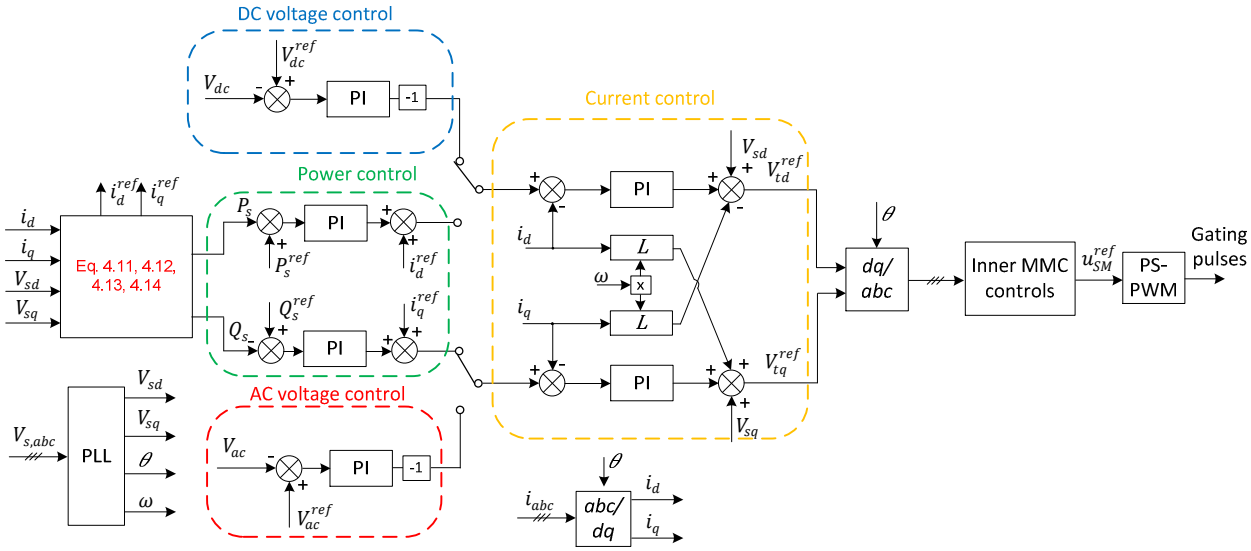

Figure 4.18 – Structure of MMC outer controls

4.2.6.1 *System response to power ramp*

The dynamics of HVDC transmission subjected to ramp changes in active and reactive power were studied. In Figure 4.19 are shown AC system response to power ramp changes. Initially both stations have zero active and reactive power references, operating in DC voltage control mode. At time t=0.5s, the active power ramp reference of -800 MW is set to MMC-2. This implies that MMC-2 operates in power control mode, while MMC-1 maintains DC-link voltage to a reference. The active power, delivered to the AC system-1 is the result of DC voltage controller action on the MMC-1 side. The active power controller of the MMC-2 ensures precise reference tracking. At time t=0.8s ramp references of 150 MVAr and 300 MVAr were set to reactive power controllers for MMC-1 and MMC-2 respectively. Since current control loops are de-coupled, the control of the active and reactive power is independent.

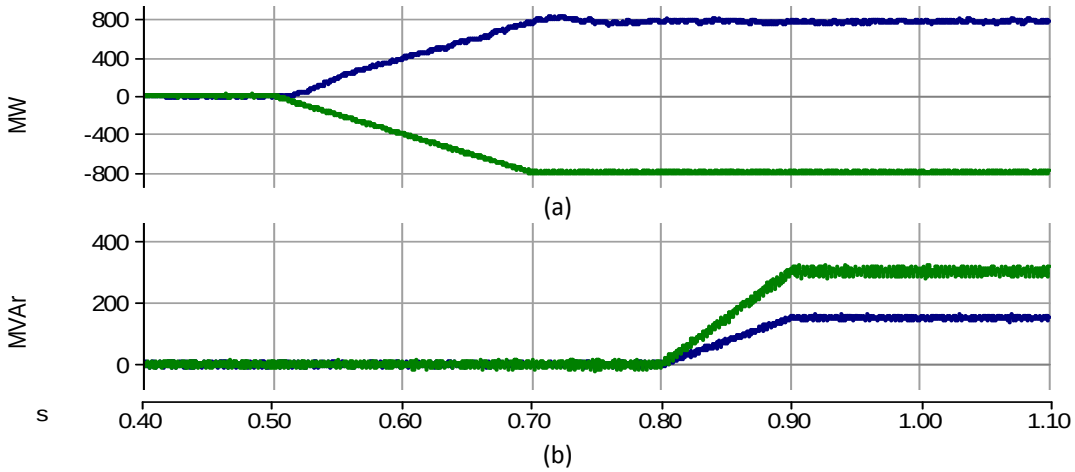

Figure 4.19 – HVDC system response to P,Q ramps. (a) blue - MMC-1 Active power, green - MMC-2 Active power. (b) blue - MMC-1 Reactive power, green - MMC-2 Reactive power.

Voltage profile at both sides of the DC transmission is shown in Figure 4.20. Before the power transfer is activated, DC voltage level at the converter stations is maintained to the reference of 640 kV. After the active power transmission starts from MMC-2 to the DC-link, the voltage rises by 4% at the rectifier side (green) and 1.5% at the inverter (blue) during the power ramp. Since DC voltage control is active at MMC-1, the reference voltage is reached within 0.05s after active power stabilisation. The differences between the voltages at the two terminals are a consequence of the DC-cable impedance. The noise in the DC voltage reflects switching of the converter sub-modules.

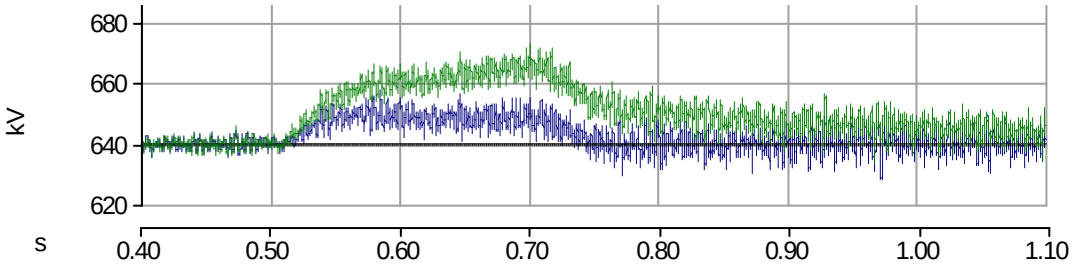

Figure 4.20 – HVDC system response to ramp, (blue) DC-link voltage in MMC-1 terminal, (green) DC-link voltage in MMC-2 terminal.

Since operational conditions of both converter stations are similar, only the capacitor voltages of MMC-1 are presented (Figure 4.21). The capacitor voltages present ripple factor of 5% at rated active power, after t=0.8s the ripple factor is increased to 9% as a result of the reactive power exchange between the converter and the grid. During the power changes, the capacitor voltages remain balanced and follow the reference of 80 kV.

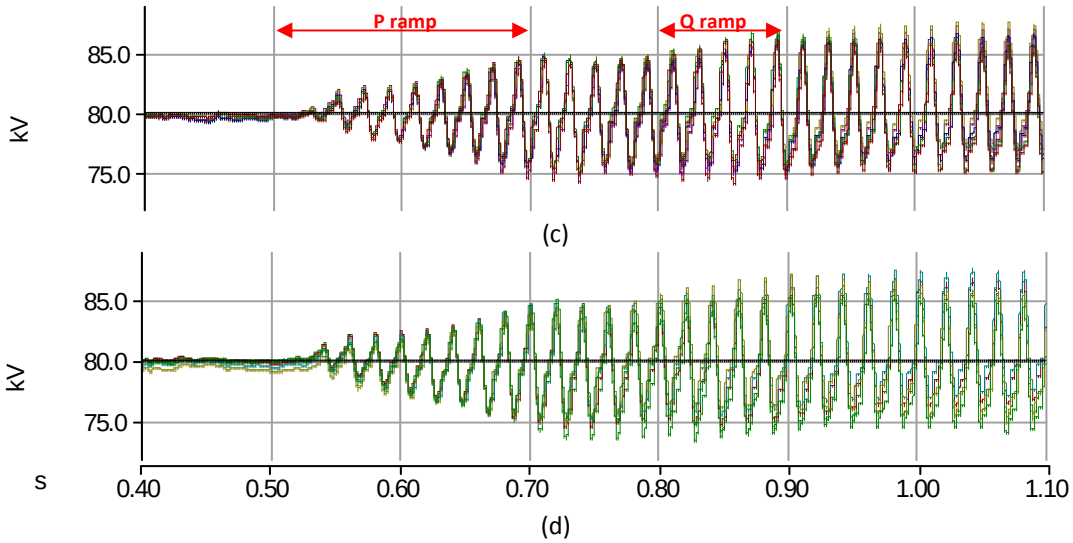

Figure 4.21 - HVDC system response to ramp. (a) Upper arm capacitor voltages. (b) Lower arm capacitor voltages.

4.2.6.2 Full active power reverse

In the British grid codes [53][66] the time for full active power reverse in HVDC interconnections is defined as 5s. This time was used as a reference for testing the model developed. In Figure 4.22 are shown the active power and DC-link voltages at the two HVDC terminals. Initially MMC-1 is operating in inverter mode, controlling DC-link voltage, while MMC-2 in rectifier mode, managing the active power transfer to -800

MW. At time t=1.5s a ramp command for full active power reversal is activated. When power reference is crossing zero at t=4s, the task of DC voltage control automatically is assigned to MMC-2. During the whole simulation time the DC-link voltage at both terminals closely follows the reference (b).

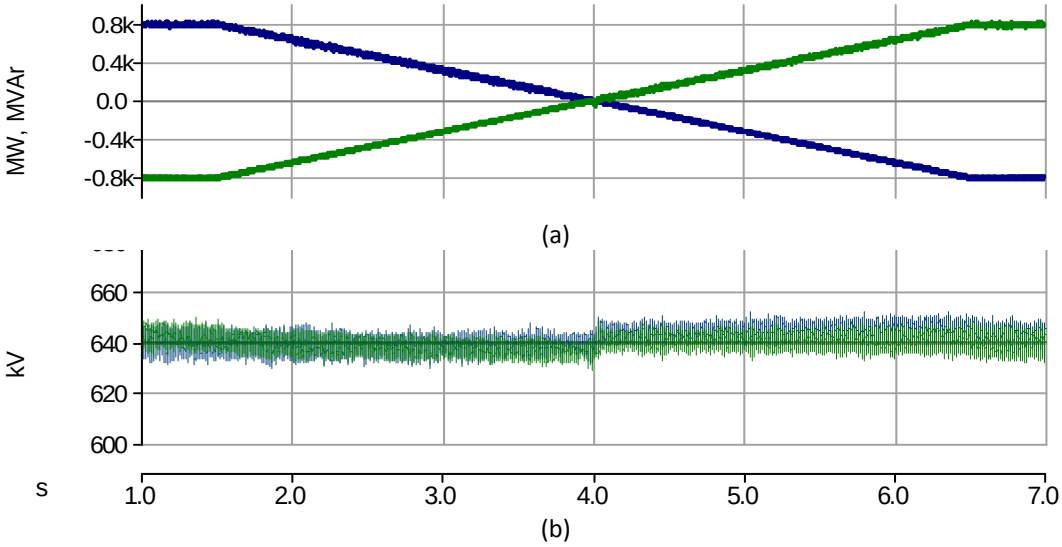

Figure 4.22 - HVDC system power reverse. (a) blue – Active power MMC-1, green – Active power MMC-2. (b) blue – DC voltage MMC-1, green – DC voltage MMC-2.

4.3 Chapter Summary

The inner control strategies for MMC were discussed and implemented in a switching model, proving effective circulating current suppression, capacitor balancing and control of the converter arm voltage. It was observed that the reduction in the amplitude of the circulating current is directly reflected on the amplitude of the capacitors voltage ripples.

The HVDC controls were implemented and validated in the simulation. Power ramp and active power reversal was tested and both AC and DC side dynamics of the HVDC transmission systems were analysed. The power and DC voltage controllers showed good performance during both cases, ensuring the control objectives. The inner controls of the converter showed good performance during changes in the system, ensuring stable operation of the converter.

5 Control of HVDC under Unbalanced conditions

In this chapter the control of MMC under unbalanced grid conditions is studied. Appropriate current controls methods are presented and verified through simulation. Special attention is paid to the fault propagation through HVDC interconnection. The performance of different control strategies is analysed based on the simulation results. A current limitation strategy applicable for MMC is derived and tested.

Faults in the grid usually result in unbalanced voltages at the PPC of the converter. As a consequence, the converter currents injected may lose sinusoidal shape. The interaction of the unbalanced currents and voltages result in oscillations in active and reactive power delivered to the grid. Under such conditions the converter control becomes a challenging issue. Different control strategies can be applied depending on the grid requirements. By choosing proper current references, the power oscillations can be effectively damped, or on the other hand, the balance in the output currents can be maintained. [67]

The different control strategies have distinct impact on the inner dynamics of the MMC as it will be studied in this chapter.

5.1 Symmetrical components

According to Fortescue, any set of three-phase unbalanced phasors can be represented by three sets of balanced sequence components namely positive, negative and zero sequence as shown,

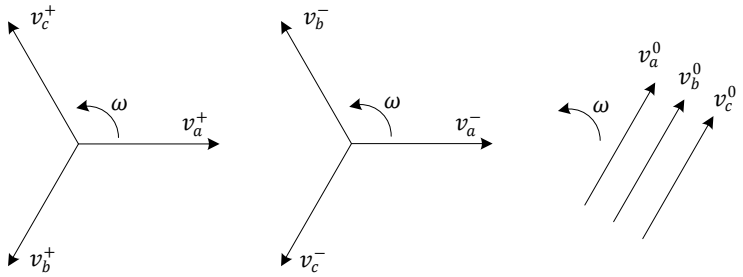

Figure 5.1 – Symmetrical components of unbalance voltage [68].

Where (+/-/0) superscript denotes positive, negative or zero sequence of voltage v.

To extract the sequence components, the three phase voltages are first converted to stationary $\alpha\beta$ reference frame using Clark's transformation (Appendix). To obtain the direct and in-quadrature components, the Decoupled double synchronous reference frame (DDSRF) and the second-order generalized integrator (SOGI) methods were investigated. The SOGI-QSG was selected due to its improved filtering characteristics. The sequence components are calculated as follows, [69]

$$v_{\alpha\beta}^{+} = [T_{\alpha\beta}][T_{+}]v_{abc} = [T_{\alpha\beta}][T_{+}][T_{\alpha\beta}]^{-1}v_{\alpha\beta}$$
$$\begin{bmatrix} v_{\alpha}^{+} \\ v_{\beta}^{+} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix}\begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} \quad (5.1)$$

$$v_{\alpha\beta}^{-} = [T_{\alpha\beta}][T_{-}]v_{abc} = [T_{\alpha\beta}][T_{-}][T_{\alpha\beta}]^{-1}v_{\alpha\beta}$$
$$\begin{bmatrix} v_{\alpha}^{-} \\ v_{\beta}^{-} \end{bmatrix} = \frac{1}{2}\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix}\begin{bmatrix} v_{\alpha} \\ v_{\beta} \end{bmatrix} \quad (5.2)$$

Where $q = e^{-\frac{j\pi}{2}}$ is a phase lagging operator by $90°$ used to obtain the quadrature components of the input signal. From (5.1) and (5.2) can be noticed that the positive component v_{α}^{+} is in phase with v_{α} while v_{β}^{+} is lagging v_{α} by $90°$. Also the negative sequence component v_{α}^{-} is in phase with v_{α} while v_{β}^{-} leads v_{α} by $90°$.

The implementation diagram of the SOGI-QSG, together with the positive and negative sequence calculation is shown in Figure 5.2.

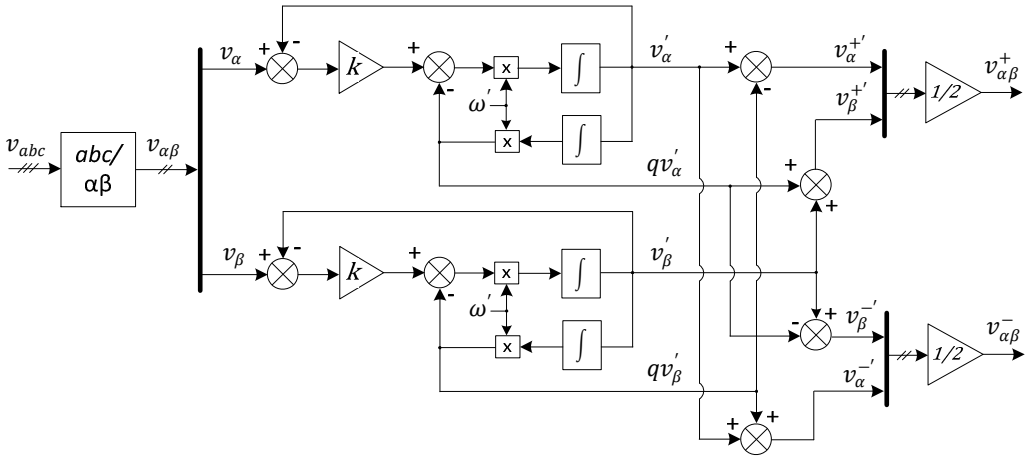

Figure 5.2 – DSOGI-QSG, block diagram [69]

The transfer functions of the SOGI-QSG for the in-phase and quadrature components are [69],

$$\frac{v_{\alpha}}{v_{\alpha}'}(s) = \frac{2k\omega' s}{s^2 + 2k\omega' s + \omega'^2} \quad (5.3)$$
$$\frac{qv_{\alpha}}{v_{\alpha}'}(s) = \frac{2k\omega'^2}{s^2 + 2k\omega' s + \omega'^2} \quad (5.4)$$

Where k determines the bandwidth, chosen to be $\sqrt{2}$ to have a damping factor $\xi = 1/\sqrt{2}$, and the centre frequency obtained from the PLL is $\omega' \approx \omega = 2\pi \cdot 50$ rad/s.

The same procedure can be applied to obtain the sequence components of the current. In Figure 5.3 are presented the $\alpha\beta$ positive and negative components of the grid voltage. At t=0.5s the voltage in phase A is reduce to 20%, as shown in (a). It can be observed that, when the unbalance is imposed, the negative component of the voltage appears and the amplitude of the positive component is reduced. Although the calculated settling time of SOGI-QSG is 20.7 ms, because of the PLL dynamics, the time obtained in simulations is approximately 40 ms.

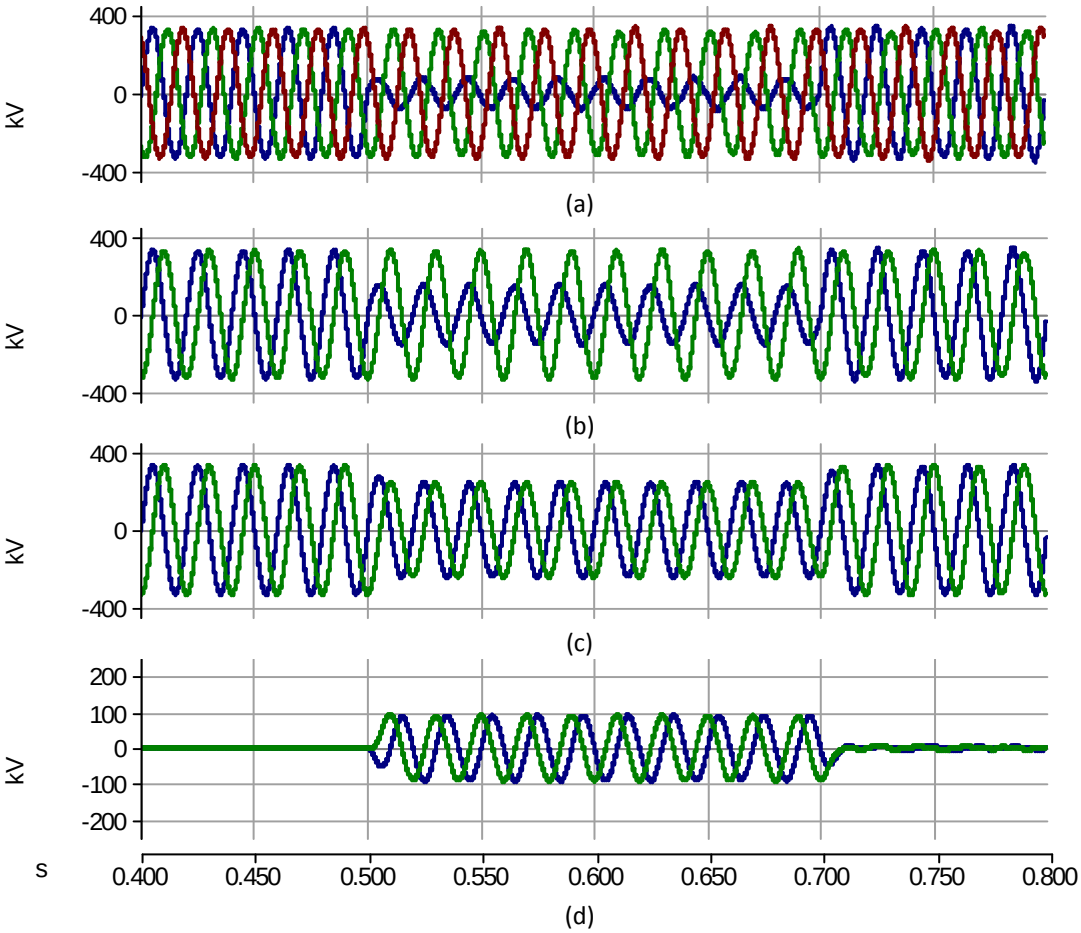

Figure 5.3 – Extraction of sequence components from unbalanced three phase voltage using DSOGI-QSG. (a) Three phase grid voltages. (b) $v_{\alpha\beta}$. (c) $v_{\alpha\beta}^{+}$. (d) $v_{\alpha\beta}^{-}$.

The angle of the positive and negative voltage components, θ'^{+} and θ'^{-}, is obtained by implementing the PLL structure presented in Section 4.2.1 for the positive and negative voltage components respectively. In Figure 5.4 are shown θ'^{+} and $\theta'^{-}$when the unbalance is introduced at t=0.5s. It can be observed that the positive angle is not affected by the unbalance, and the calculation of the negative angle settles 0.025ms after the fault appears. Since the q-axis component is used in the PI controller to get the frequency and the phase angle; a phase shift of $90°$ appears between the calculated angle and the grid.

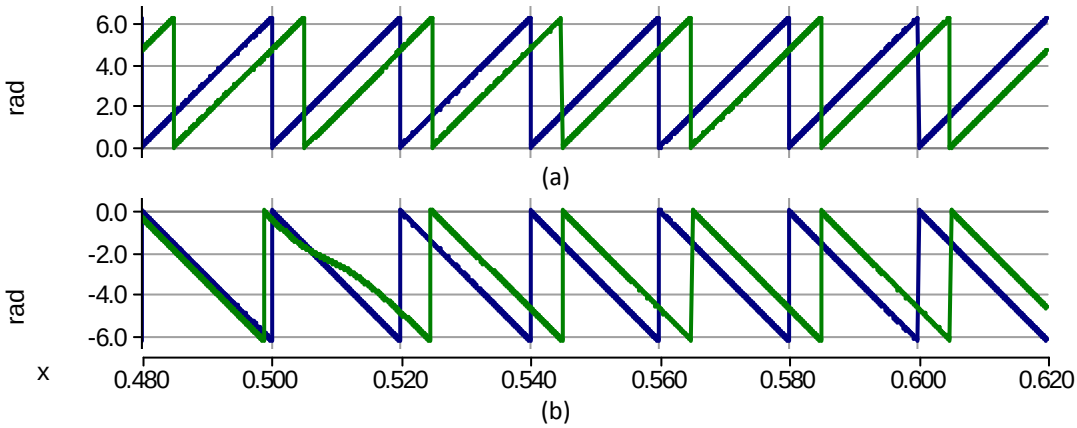

Figure 5.4 – DSOGI-PLL, simulation results. (a) blue – Positive sequence grid angle θ^{+}, green – Positive PLL angle θ'^{+}. (b) blue – Negative sequence grid angle θ^{-}, green – Negative PLL angle θ'^{-}

The positive and negative sequence PLL is implemented to align the d-axis with the grid voltage, thus the q-axis components under steady state and unbalanced conditions are zero ($V_{sq}^{+} = V_{sq}^{-} = 0$). By this means, the instantaneous power equations used in the subsequent sections can be simplified.

5.2 Test Conditions

With the intention of highlighting the strengths of the MMC in HVDC application and pursuing the use standard voltage levels in the simulations, the model parameters used for the simulations were adjusted and the number of sub-modules was increased to 32; as shown in Table 5.1. An equivalent Thevenin model of the series connection of sub-modules in the arm, proposed in [70], was utilized in order to reduce the computational time of the simulations. The Thevenin model was found to have an error of 0.04% compared with the switching model, therefore it was accepted for the subsequent simulations.

Table 5.1 – Circuit parameters used for MMC-HVDC transmission model

Description	*Abbreviation*	*Value*
Rated apparent power	S_N	850 MVA
Rated cell voltage	V_{SM}	25 kV
DC link voltage	V_{dc}	±400 kV
Arm resistance	R_{arm}	0.1 Ω
Arm inductance	L_{arm}	90 mH (0.15 pu)
Cell capacitance	C_{SM}	570 µF (40 kJ/MVA)
Number of sub-modules per arm	N	32

The Distributed control method together with the CCSC presented in Chapter 4 was implemented as inner control strategies.

To assess the performance of the MMC based HVDC transmission system under unbalanced conditions; the system is subjected to a single-line-to-ground (SLG) fault on the bus PCC-1 (Figure 5.5), dropping the voltage of phase A in the AC system-1 to 20%. The MMC-1 station operates in inverter mode, controlling DC-link voltage while the MMC-2 station has active power reference set to 800 MW. Reactive power references for both stations are set to 0 MVAr. The fault is imposed at 0.5s and cleared after 0.2s.

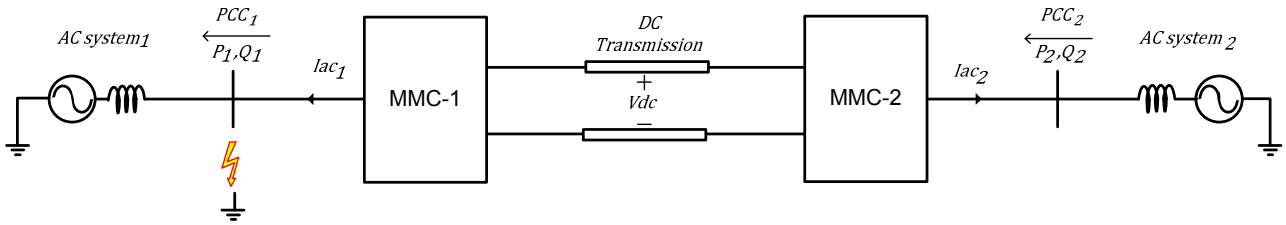

Figure 5.5 – Simulation conditions for unbalanced faults

5.3 Fault propagation in transformerless HVDC

In order to study the impact of unbalanced grid conditions on the transformerless MMC-HVDC system, a test with only positive sequence control was performed, leaving negative and zero sequence current flow uncontrolled.

In Figure 5.6 the currents in MMC-1 are shown. During the fault, the AC currents are highly distorted, specially the faulted phase with a peak of 400% compared to the pre-fault value. In addition, the positive sequence component current is increased by 55% during the fault. If left uncontrolled, such currents could trip the protection systems or damage the converter components.

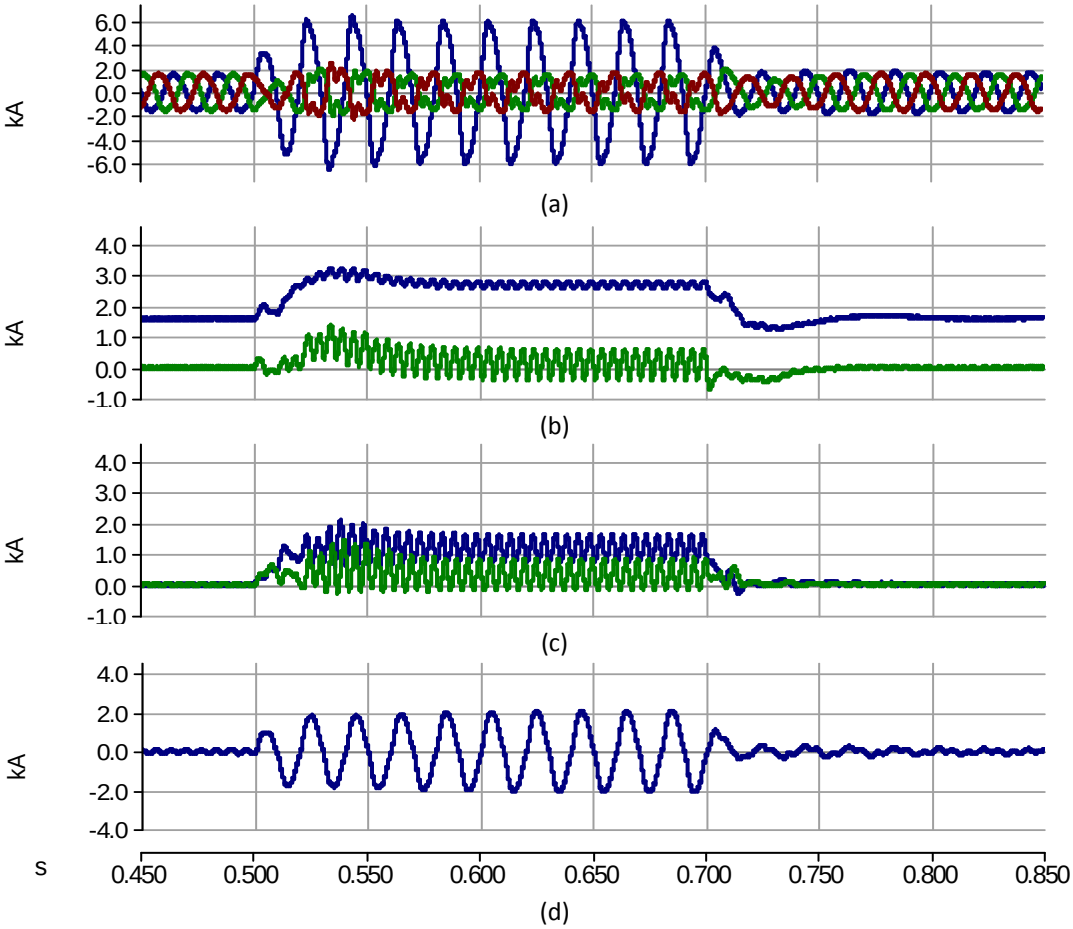

Figure 5.6 – Fault propagation, currents in MMC-1. (a)Three phase currents. (b) blue - i_d^+, green - i_q^+. (c) blue - i_d^-, green - i_q^-. (d) i_0.

In Figure 5.7 the voltages in MMC-1 are shown. In the absence of a grounded midpoint in the DC-link, the zero sequence current from the grid is transmitted to the DC side, causing undesired oscillations at fundamental frequency between the DC-link neutral point and ground (a). Moreover, as a result of the power oscillations caused by the presence of negative sequence components in the grid, double line-frequency ripples with amplitude of 5% appear in the DC-link (b). The voltage profile of one capacitor in upper and lower arms of phase A, B and C are shown in (c,d,e) respectively.

It can be observed that capacitor voltage waveforms are affected by the corresponding phase currents in the converter arms. As demonstrated in Section 0; the voltage ripples of the capacitors in the faulted phase reflect the increment of the phase current, having ripple factor of 28% (c). Phase B and C capacitors have change in voltage shape due to current distortions.

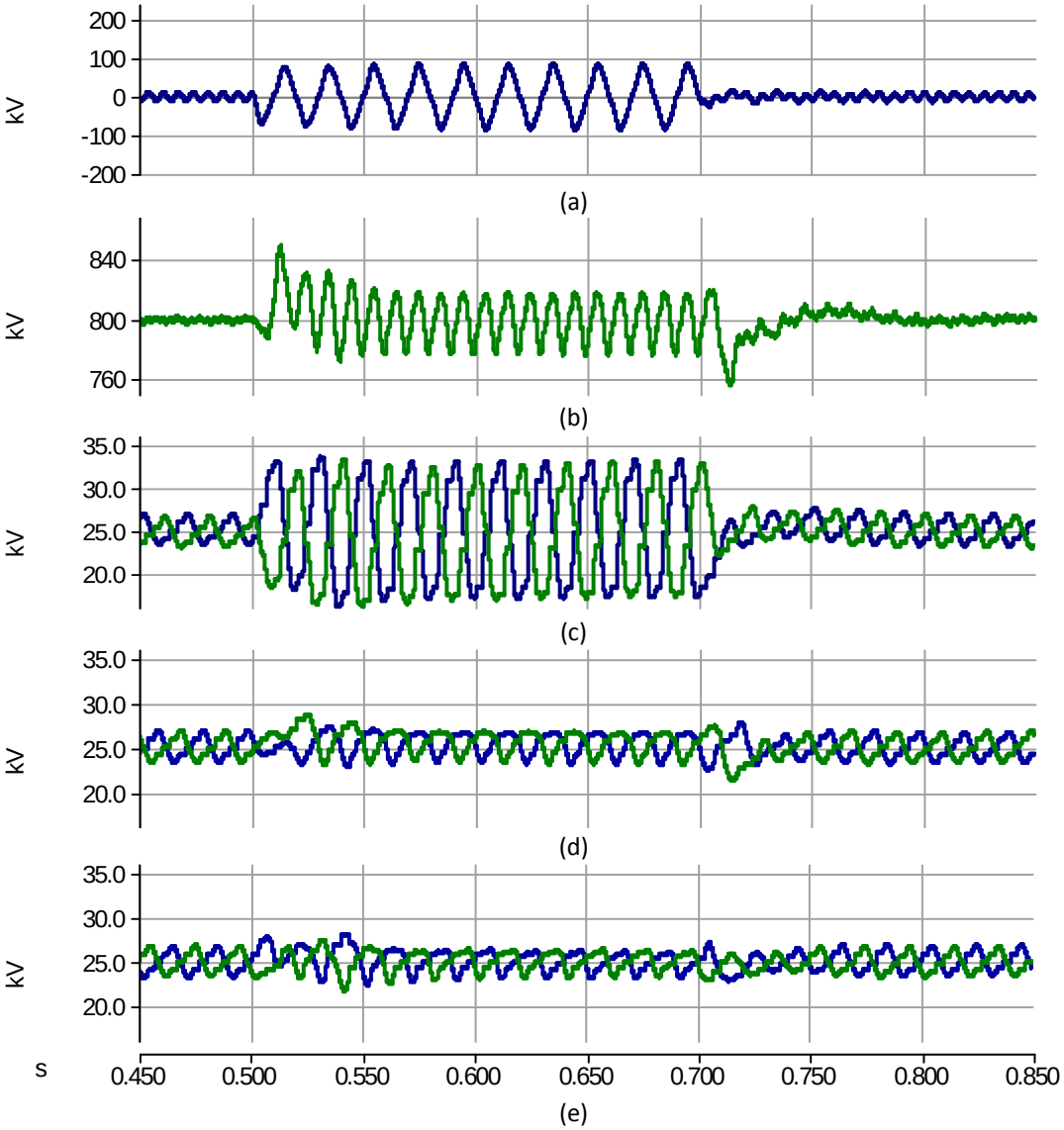

Figure 5.7 - Fault propagation, voltages in MMC-1. (a) Neutral point voltage. (b) DC-link voltage. (c,d,e) Phase A, B, C capacitor voltages respectively.

The presence of negative and zero-sequence current components affects the performance of the whole HVDC transmission system. The currents of MMC-2 are shown in Figure 5.8, where a strong presence of the zero-sequence in the converter output currents can be noticed. This could force the overcurrent protections to trip as well as have negative impact on the AC System-2. Furthermore, the double line-frequency ripples present in the DC-link voltage are reflected in the three-phase difference currents of the MMC-2 (b), stressing the converter components.

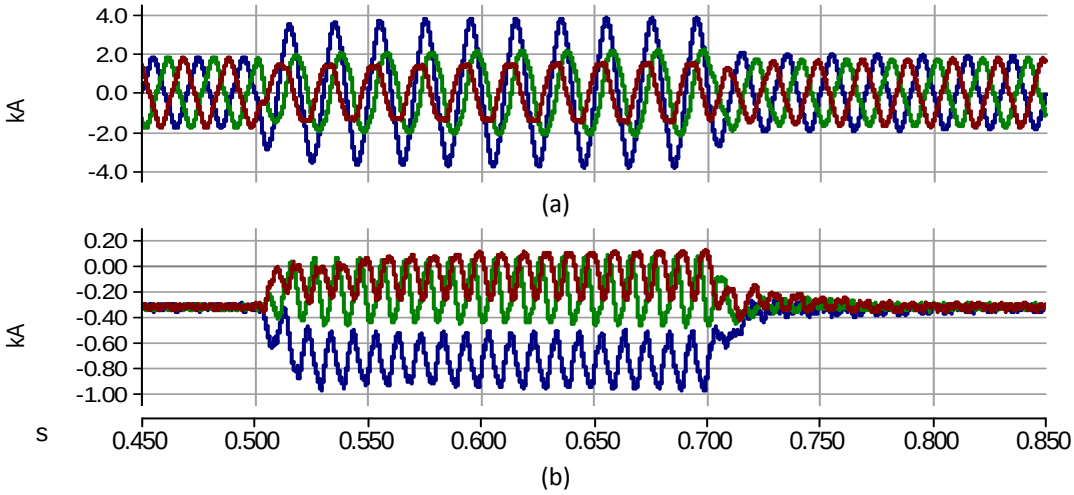

Figure 5.8 - Fault propagation, currents in MMC-2. (a)Three phase AC currents. (b) Difference currents

In transformerless MMC-HVDC transmission systems, without the proper control, faults are propagated through DC-link and reflected in the healthy converter station affecting the AC grid. Moreover, the fault currents presented could damage the converter components or require unrealistic over ratings. The next section focuses on reducing the fault reflection in the HVDC system and mitigating the impact of the unbalance in the faulty side.

5.4 Control of Symmetrical components

While in two level converters only the positive and negative sequence components are controllable, in MMC, due to the distributed capacitive energy storage, it is also possible to control the zero-sequence current components [37].

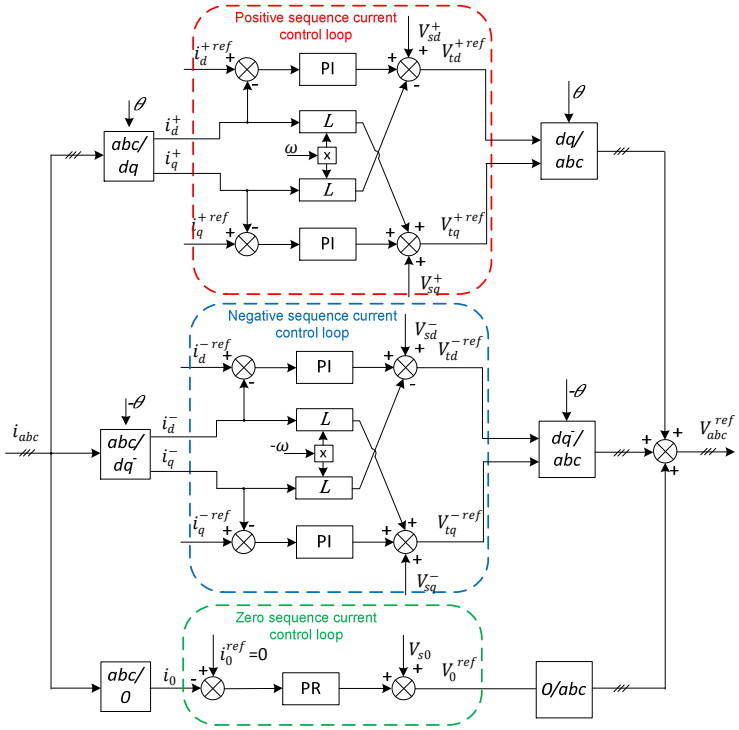

Figure 5.9 – Current control structure for unbalanced conditions

To overcome the problems mentioned previously, a current control method that involves three sequence components is implemented. In Figure 5.9 is presented current control structure. The measured AC currents are transformed into positive and negative sequence components in *dq* reference frame, using the appropriate transformation angles. The control of the zero-sequence current, due to its sinusoidal behaviour, is implemented in stationary reference frame with a PR controller, as proposed in [71].

5.4.1 Zero Sequence Control

In order to reduce the fault reflection in the other side of the HVDC system, one of the control targets for the current control is the elimination of the zero sequence current, i.e. $i_0^{ref} = 0$.

In Figure 5.10 the simulation waveforms of the MMC-1 system with only positive and zero sequence control are shown. The control is active during both balanced and unbalanced conditions. The presence of the negative sequence currents is reflected in the distorted AC currents (a). According to the control objective, the zero sequence current is effectively suppressed (d); as a result, the oscillations between the DC-link neutral point and ground are eliminated.

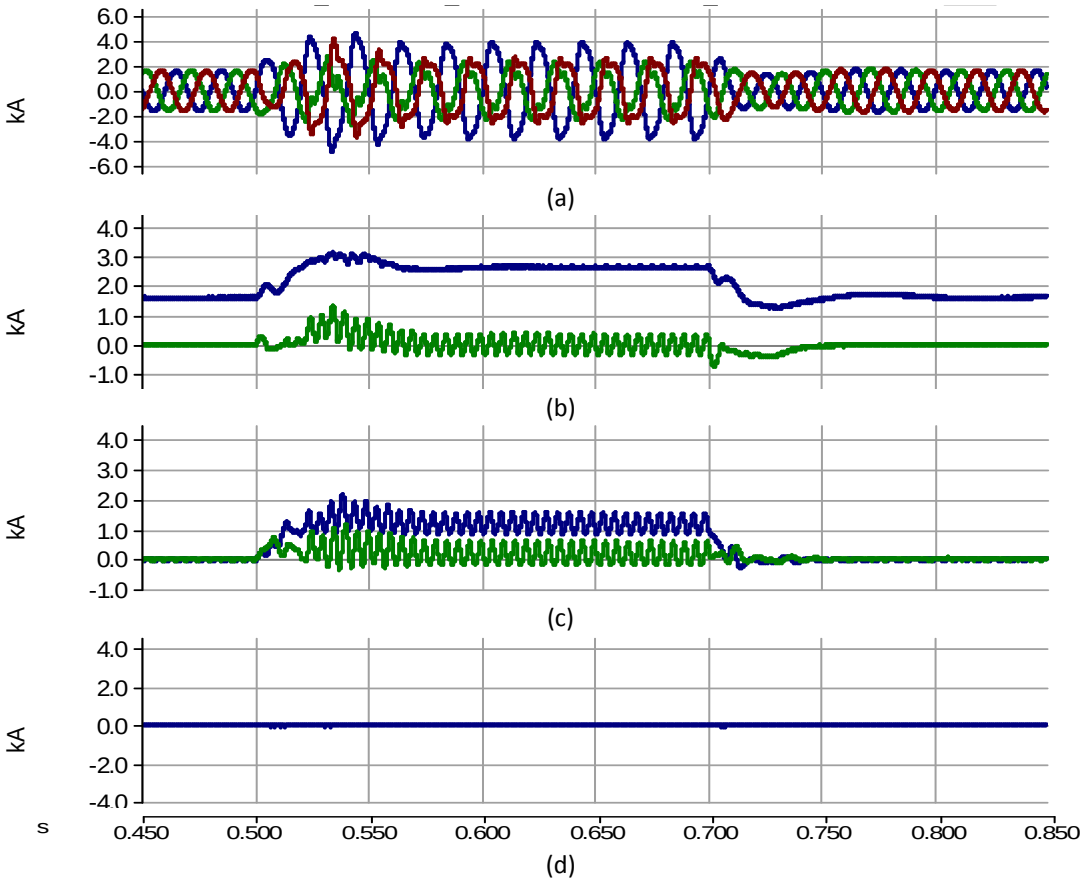

Figure 5.10 – Zero sequence control, results in MMC-1. (a)Three phase currents. (b) blue - i_d^+, green - i_q^+. (c) blue - i_d^-, green - i_q^-. (d) i_0.

In Figure 5.11 can be observed that the DC-link voltage ripples of 2% are still present (a). These ripples are product of the power oscillations caused by the negative sequence components in the AC system-1.

The elimination of zero sequence current implies lower converter phase currents, therefore the amplitude of the capacitor ripple is reduced. However, in the faulted phase voltage ripple it is still 22% (b). Phase B and C capacitors have change in voltage shape due to unbalanced currents in the grid, having voltage ripple factor of 14%.

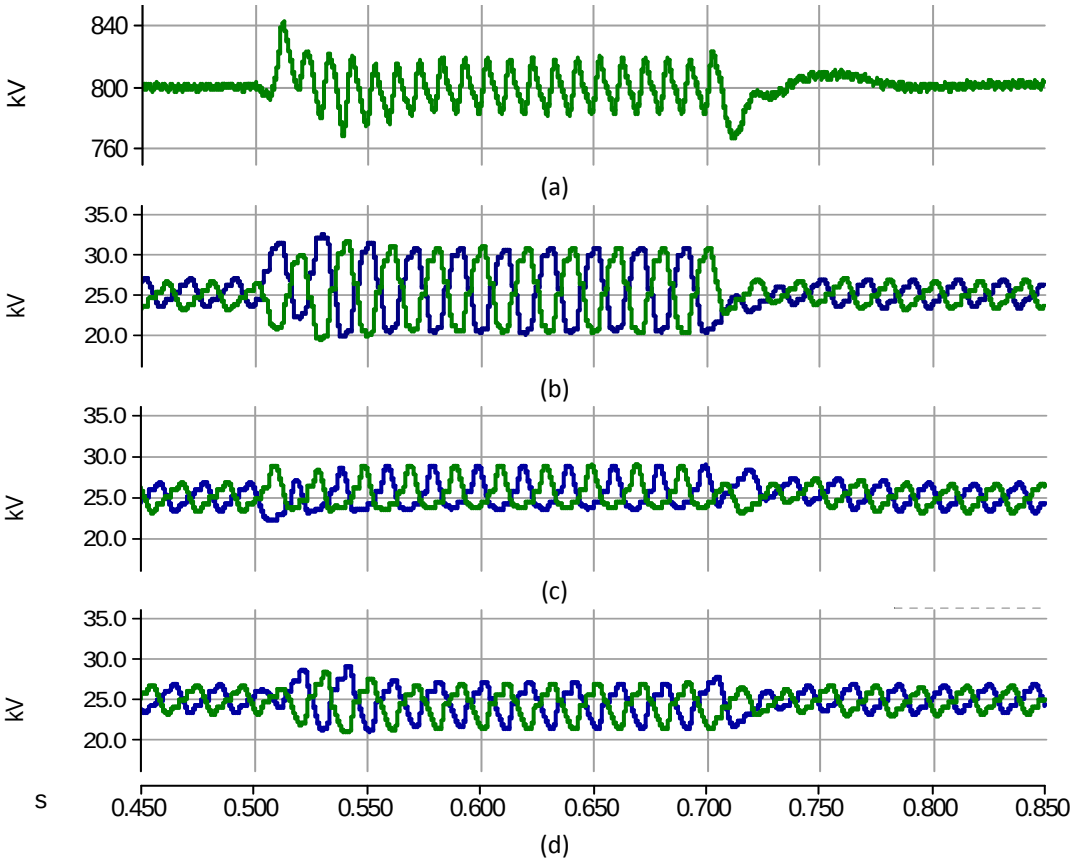

Figure 5.11 – Zero sequence control, results in MMC-1. (a) DC-link voltage (b,c,d) Phase A, B, C capacitor voltages respectively.

Having eliminated the zero sequence current, the fault is not reflected in the output currents of the MMC-2 as shown in Figure 5.12-a. Though, the ripples in the DC-link are transmitted to the three phases of MMC-2 causing double line-frequency zero sequence ripples in the difference currents (b).

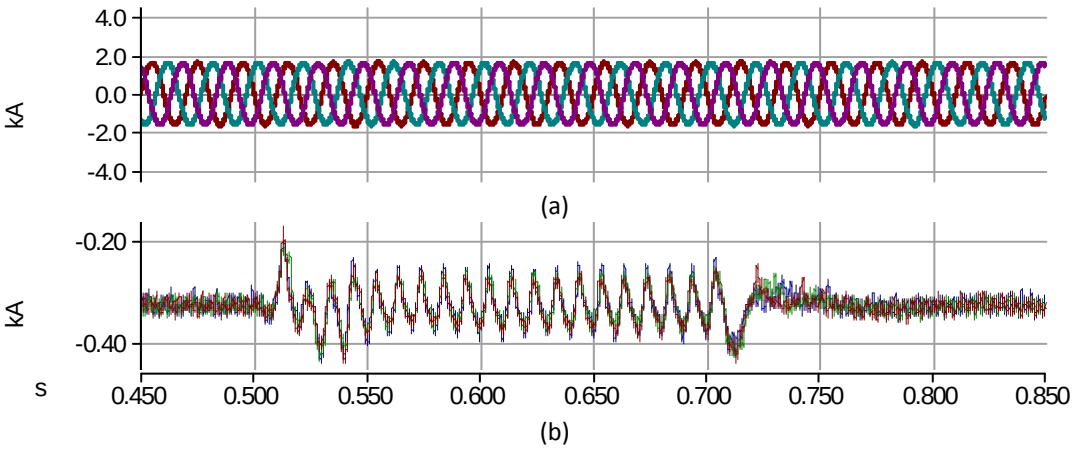

Figure 5.12 - Zero sequence control, currents in MMC-2. (a) AC currents. (b) Difference currents

5.4.2 Negative Sequence Control

Aiming to suppress the ripples in the DC-link, the references for the negative sequence currents are set to 0 ($i_{dq}^{-ref} = 0$), as proposed in [72]. The zero sequence controller described in the previous section is active during the simulation study with $i_0^{ref} = 0$.

In Figure 5.13 the simulation waveforms of the MMC-1 system with negative sequence control are shown. According to the control objective, the negative sequence current (a) is effectively suppressed during the unbalanced conditions; subsequently the ripples in the DC-link voltage are reduced to 1% (b). The amplitude of the capacitor voltage ripples comparing to the previous case is decreased, resulting in 10% for the faulted phase (c) and 8% for B, C converter phases (d,e). Since only positive sequence in the AC currents is present, the voltage profile of B, C phase capacitors is similar to normal operation conditions.

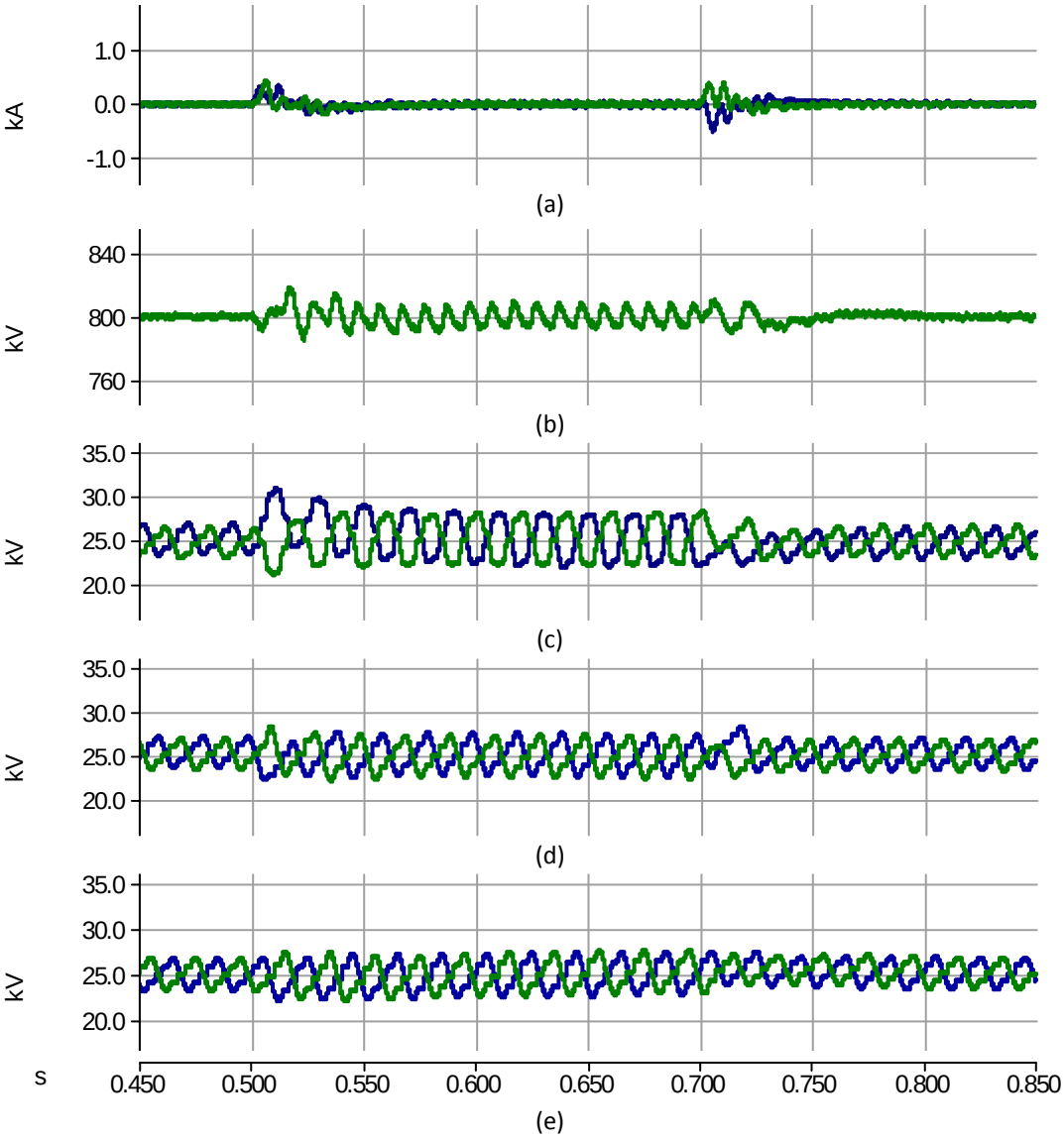

Figure 5.13 – Negative sequence control, results in MMC-1. (a) blue - i_d^-, green - i_q^-. (b) DC-link voltage. (c,d,e) Phase A, B, C capacitor voltages respectively.

The presence of the double line-frequency ripples in the DC-link voltage, similar to the previous case, is reflected in the difference currents of the MMC-2 station, as shown in Figure 5.13. However, the amplitude of the ripples is decreased, comparing to Figure 5.12-b.

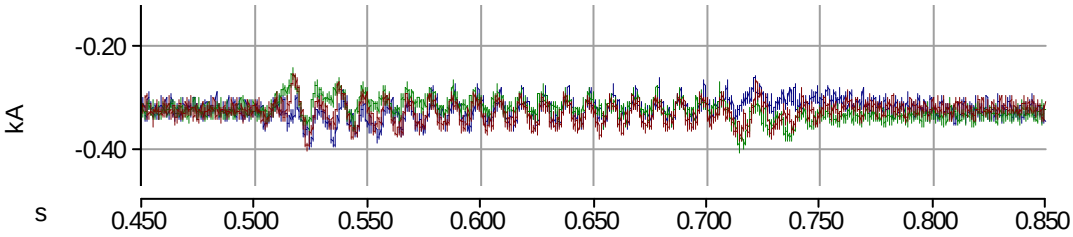

Figure 5.14 - Negative sequence control, difference currents in MMC-2.

It can be observed that suppressing the negative sequence current results in the reduction of the DC-link ripples; yet, the presence of the unbalance is still reflected on the difference currents of the unfaulted converter station.

5.5 Impact of unbalances on the Inner dynamics of MMC in HVDC transmission

Depending on the structure of the Inner controls implemented in the MMC, the unbalanced grid conditions can affect the converter performance. As presented in Section 4.1, two inner control strategies are implemented; the Distributed control, in charge of the voltage level of the sub-module capacitors, and the CCSC that eliminates the double line-frequency circulating current in the converter.

Although having higher AC currents can increase the amplitude of the voltage ripples in the sub-modules, it does not affect the voltage balance, since it affects equally all the sub-modules in the arm. Furthermore, the averaging part of the distributed control is not affected either; while the higher currents discharge more the sub-modules, it also charges more the sub-modules when the current direction is reversed, keeping a constant average value.

Nevertheless, the asymmetric grid conditions affect the performance of the CCSC implemented, since it takes into consideration only balanced negative sequence difference currents. Also, as observed in Section 5.4, even when the zero and negative sequence current components are eliminated, double line-frequency ripples appear in the DC-link. A modification of CCSC is proposed in order to compensate the mentioned problems.

5.5.1 Modified Circulating Current Suppression Controller

The CCSC implemented in Chapter 4, acts on the negative sequence double line-frequency component of the difference currents, transformed into *dq* signals. Under asymmetric grid conditions, the converter difference currents get distorted, appearing a positive sequence component. Having unbalanced difference currents, the PI controller in the *dq* frame is not able to track the reference. To overcome this problem, implementation of the CCSC in $\alpha\beta$ reference frame using PR controllers is proposed. The PR controllers are tuned at double line-frequency, acting on both sequences, therefore ensuring elimination of the desired components.

Moreover, the presence of double line-frequency zero sequence difference current, observed in the previous section may be produced by the current control strategy used for unbalanced conditions, as

proven in [26]. Aiming to compensate the unbalances in the grid, the converter generates an unbalanced *emf*, which produces a zero sequence power component at the converter arms. This component appears as a double line-frequency current circulating through the converter arms and transmitted over the DC-link. To eliminate this current, a supplementary zero-sequence control loop with a PR controller tuned at double line-frequency was added to the CCSC.

The control diagram of the modified circulating current suppression controller is shown in Figure 5.15.

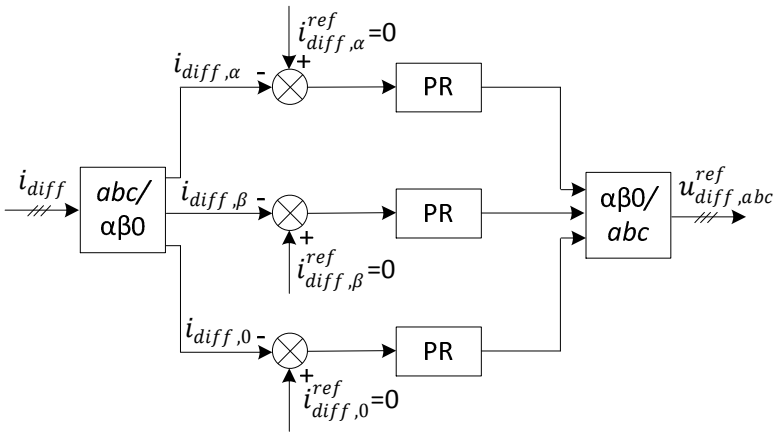

Figure 5.15 – Modified CCSC

In Figure 5.16 the performance of standard and modified CCSC is compared. As seen in (a), the control implemented in *dq* frame does not ensure effective suppression of the circulating current during unbalanced conditions. Comparing both results, it can be observed, that the modified control eliminates the oscillatory terms in the difference currents of unfaulted phases and reduces significantly the ripples in the faulted phase.

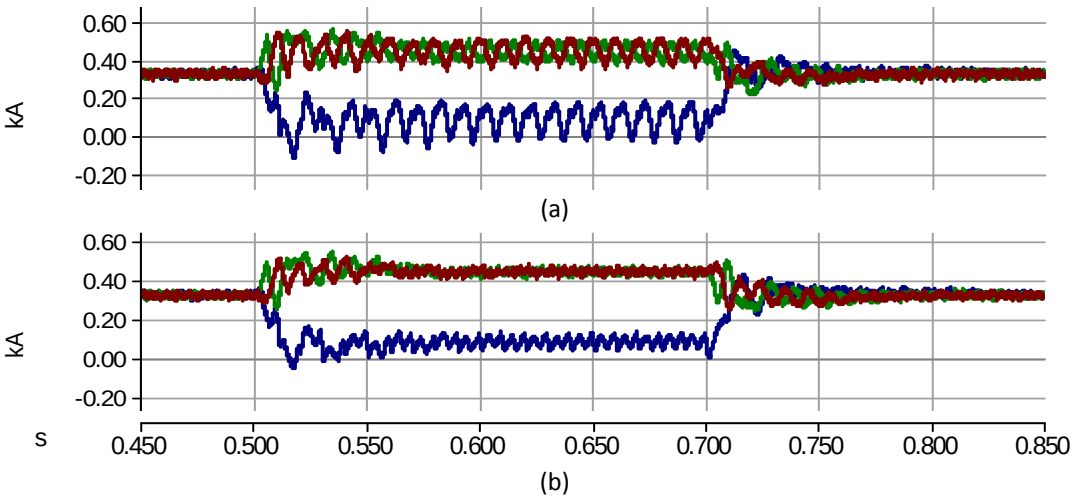

Figure 5.16 – Difference currents in MMC-1 with (a) conventional CCSC. (b) modified CCSC

The effective reduction of the zero-sequence oscillations in the difference currents is reflected in the DC-link voltage ripples, as shown in Figure 5.17-a. This, results in the suppression of the ripples in MMC-2

difference currents (b), which remain as pure DC values except for the short transients at the fault occurrence and clearance.

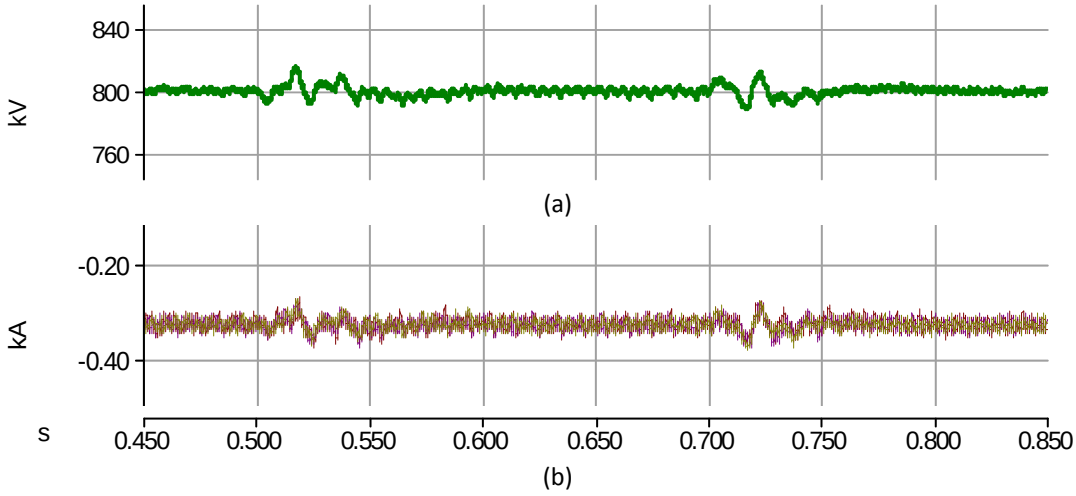

Figure 5.17 – Results on MMC-2 with modified CCSC. (a) DC-link voltage. (b) Difference current

The presented simulation cases have shown the effectiveness of using negative and zero sequence controls under unbalanced conditions to avoid the fault propagation through the DC-link.

5.6 Control Strategies Under Unbalanced Grid Conditions

Under unbalanced grid conditions, the interaction between the symmetrical components gives rise to uncontrolled active and reactive power oscillations between the converter and the grid. The instantaneous powers in a four-wire connection under unbalanced grid conditions can be written as [69]:

$$\begin{bmatrix} P \\ Q \\ P_0 \end{bmatrix} = \begin{bmatrix} \bar{P} + P_{c2}cos\,(2\omega t) + P_{s2}sin\,(2\omega t) \\ \bar{Q} + Q_{c2}cos\,(2\omega t) + Q_{s2}sin\,(2\omega t) \\ \bar{P}_0 + P_{0c2}cos\,(2\omega t) \end{bmatrix} \tag{5.5}$$

Where $\bar{P}$, $\bar{Q}$, $\bar{P}_0$ are the average powers and P_{c2}, P_{s2}, Q_{c2}, Q_{s2}, P_{0c2} represent the magnitude of the oscillating terms. The sub-index 0 is used to denote the active power delivered by the zero sequence. If the zero sequence current is eliminated by appropriate control, P_0 term can be neglected. Transforming the three-phase currents and voltages into synchronous reference frame and splitting into positive and negative, the power components can be represented as [70]:

$$\begin{bmatrix} \bar{P} \\ P_{c2} \\ P_{s2} \\ \bar{Q} \\ Q_{c2} \\ Q_{s2} \end{bmatrix} = \frac{3}{2} \begin{bmatrix} V_{sd}^{+} & V_{sq}^{+} & V_{sd}^{-} & V_{sq}^{-} \\ V_{sd}^{-} & V_{sq}^{-} & V_{sd}^{+} & V_{sq}^{+} \\ V_{sq}^{-} & -V_{sd}^{-} & -V_{sq}^{+} & V_{sd}^{+} \\ V_{sq}^{+} & -V_{sd}^{+} & V_{sq}^{-} & -V_{sd}^{-} \\ V_{sq}^{-} & -V_{sd}^{-} & V_{sq}^{+} & -V_{sd}^{+} \\ -V_{sd}^{-} & -V_{sq}^{-} & V_{sd}^{+} & V_{sq}^{+} \end{bmatrix} \begin{bmatrix} i_d^{+} \\ i_q^{+} \\ i_d^{-} \\ i_q^{-} \end{bmatrix} \tag{5.6}$$

The given relation of sequence components and instantaneous power can be used for calculating the current references depending on the grid conditions and application requirements. It can be noticed in

(5.6) that the converter has four degrees of freedom to control the AC currents. Selecting the average active and reactive powers to follow the reference,

$$\begin{aligned} \bar{P} &= P_s^{ref} \\ \bar{Q} &= Q_s^{ref} \end{aligned} \tag{5.7}$$

two degrees of freedom are left, which means that two control targets can be selected. Three simulation cases are presented with the following objectives:

- Elimination of negative sequence currents;
- Suppression of active power ripples;
- Suppression of reactive power ripples.

5.6.1 Case-1. Elimination of negative sequence currents

The elimination of the negative sequence currents results in balanced converter AC currents under unbalanced grid voltages. This feature is important for Grid Connected Inverters due to the restrictions provided by Grid Operators regarding the injection of unbalanced currents into the grid. The control objectives are defined as:

$$\begin{aligned} i_d^- &= 0 \\ i_q^- &= 0 \end{aligned} \tag{5.8}$$

As a result, having $V_{sq}^+ = V_{sq}^- = 0$ ensured by positive and negative sequence PLL, the references for the positive sequence current are:

$$\begin{aligned} i_d^{+\,ref} &= \frac{2}{3V_{sd}^+} P_s^{ref} \\ i_q^{+\,ref} &= -\frac{2}{3V_{sd}^+} Q_s^{ref} \end{aligned} \tag{5.9}$$

The response of MMC-1 is shown in Figure 5.18. During the fault, the positive component of the d-axis current i_d^+ is increased by 38% (c), in order to maintain the average output power when phase A voltage drops by 80%. The negative sequence components are effectively controlled to zero, resulting in balanced AC converter currents with the increased amplitude. The active and reactive power experience double line-frequency oscillations of ±300 MW/MVAr, with the average value maintained at the reference level (e).

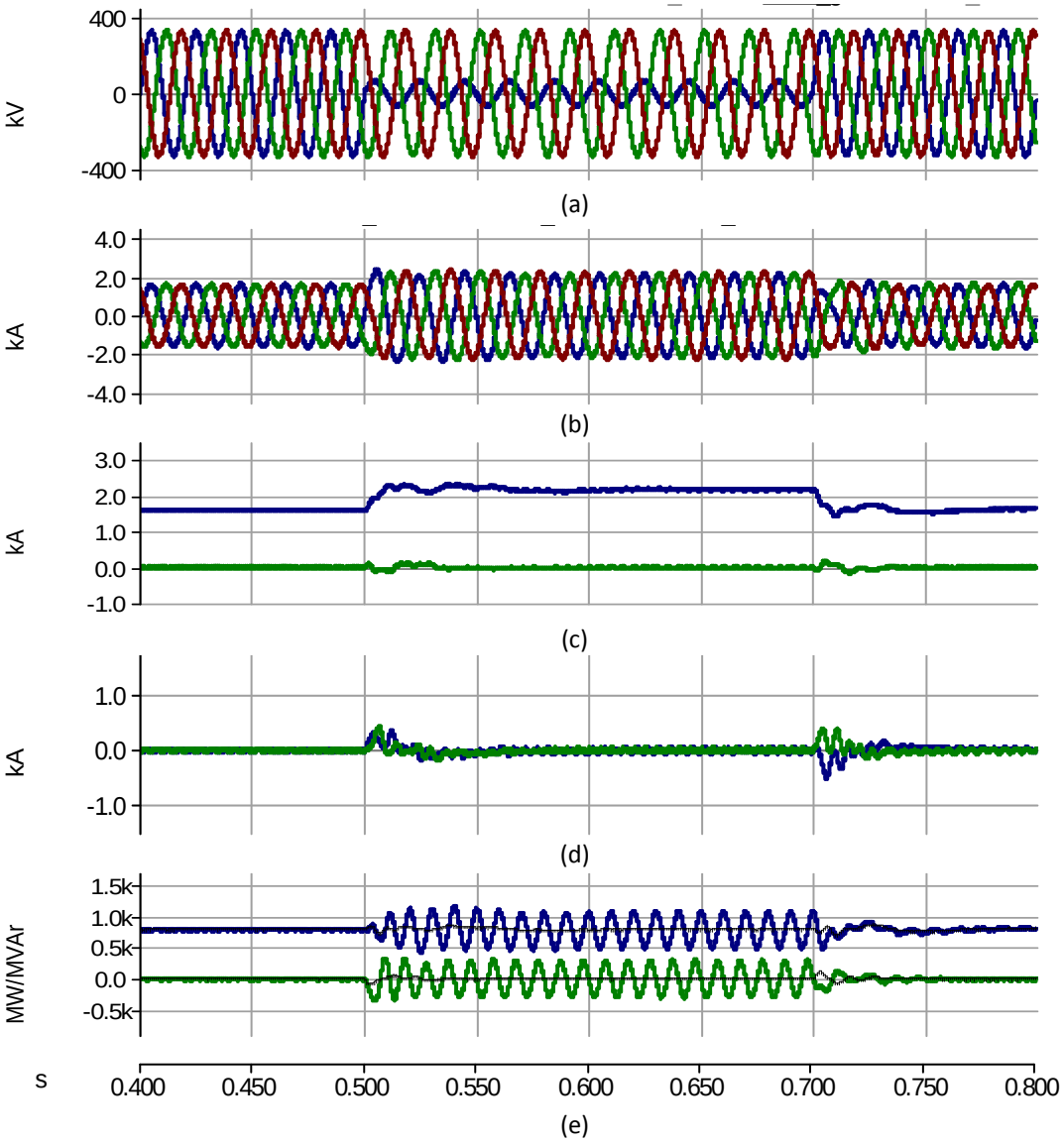

Figure 5.18 – Case 1, results in MMC-1. (a) Grid three phase voltage. (b) Three phase AC currents. (c) blue - i_d^+, green - i_q^+. (d) blue - i_d^-, green - i_q^-. (e) blue – Active power, green – Reactive power.

In Figure 5.19 are shown the inner parameters of the MMC-1 together with the DC-link voltage. Due to change in the active power distribution, the difference currents of phase B and C have an increment of 38% (a). The reduction in the A-phase difference current corresponds to the 74% decrease in active power supplied by the phase.

The voltage ripples in the sub-module capacitors are affected by the unbalanced conditions. In (b), the voltage profile of one capacitor in upper and lower arm of phase A is shown. During the fault, the capacitor voltage ripple contains mainly fundamental component. This is the reflection of the almost pure AC arm current, since loading of the phase is drastically reduced. The ripple amplitude is increased from 6% to 12%, having transient peak of 22%. The ripple factor in the capacitor voltages of phase B and C (c,d) is raised up to 10% due to the increased loading of the mentioned phases. The phase angle of the ripple components in all the phases remains unchanged due to balanced currents provided by the converter. The DC-link voltage replicates transients in the sub-modules, with 2.5% peak increase in magnitude. After 0.05s all system

parameters are reaching steady values, showing stable operation under unbalanced grid conditions. When the fault is cleared, pre-fault characteristics of the system are reached within 3 fundamental cycles.

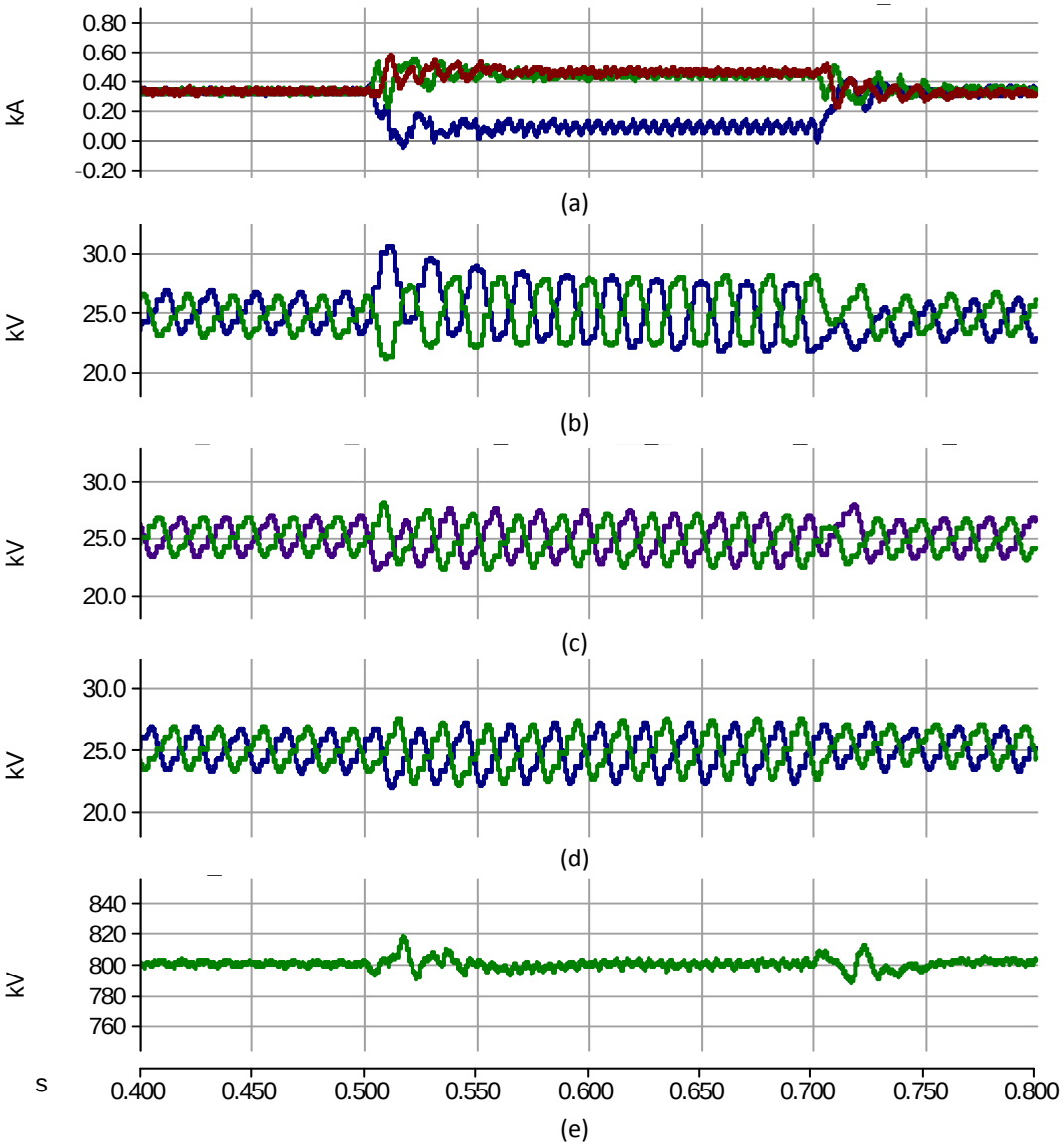

Figure 5.19 – Case 1, results in MMC-1. (a) Difference currents. (b,c,d) Phase A, B, C capacitor voltages respectively. (e) DC-link voltage

5.6.2 Case-2. Elimination of active power oscillations

In a HVDC system rated in hundreds of MW, the active power oscillations between the converter station and the grid might affect the AC system. This could trip the grid relay protections, worsen the fault conditions. To compensate for the active power oscillations, the control objectives are defined as:

$$P_{c2} = 0 \\ P_{s2} = 0 \tag{5.10}$$

Using (5.6), the positive and negative sequence current references are obtained:

$$
\begin{aligned}
i_d^{+\,ref} &= \frac{2V_{sd}^{+}P_s^{ref}}{3[(V_{sd}^{+})^2-(V_{sd}^{-})^2]} \\
i_q^{+\,ref} &= -\frac{2V_{sd}^{+}Q_s^{ref}}{3[(V_{sd}^{+})^2+(V_{sd}^{-})^2]} \\
i_d^{-\,ref} &= -\frac{2V_{sd}^{-}P_s^{ref}}{3[(V_{sd}^{+})^2-(V_{sd}^{-})^2]} \\
i_q^{-\,ref} &= -\frac{2V_{sd}^{-}Q_s^{ref}}{3[(V_{sd}^{+})^2+(V_{sd}^{-})^2]}
\end{aligned}
\tag{5.11}
$$

In Figure 5.20 are shown currents and powers of MMC-1. During the fault, the positive component of the current i_d^+ is increased by 56%. The faulted phase has an increment in the amplitude of 212% and the unfaulted phases of 38%. The objective of the control strategy is met, having suppressed oscillations in the active power (d). However, the presence of the i_d^- increases reactive power oscillations to ±650 MVAr.

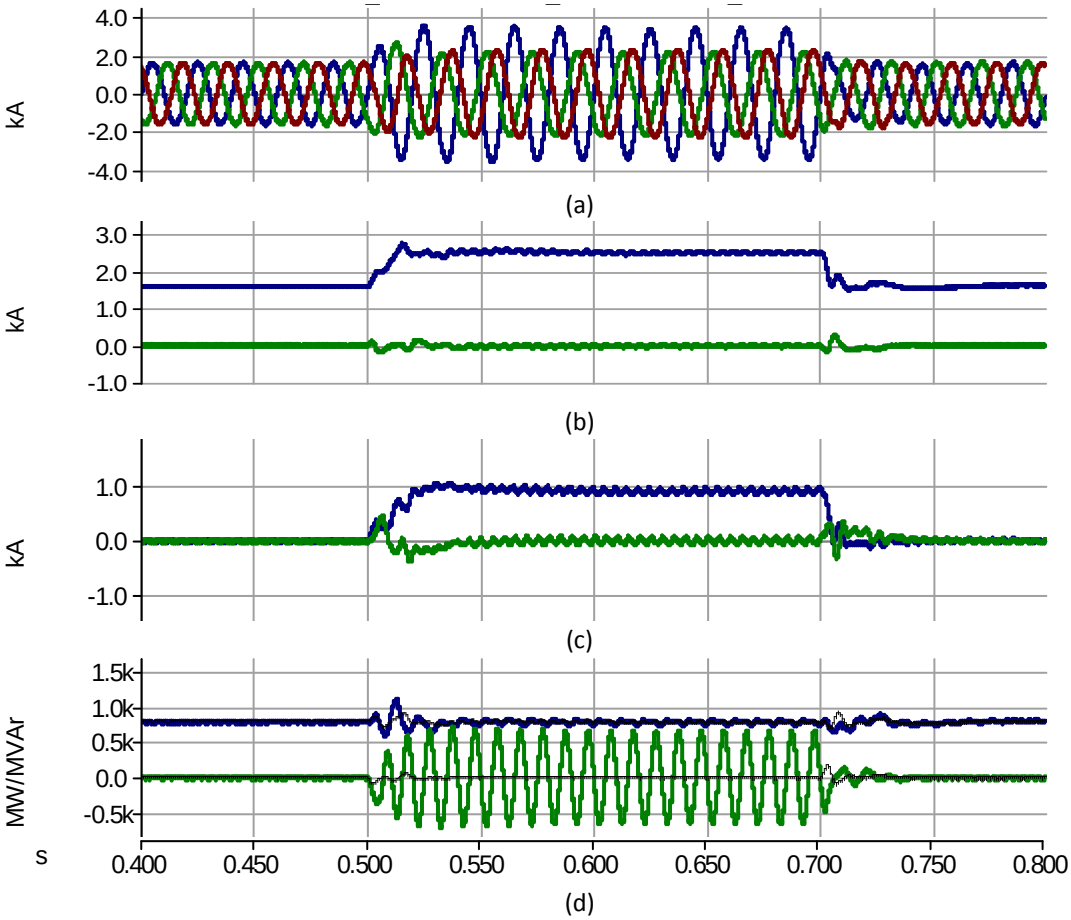

Figure 5.20 - Case 2, results in MMC-1. (a) Three phase AC currents. (b) blue - i_d^+, green - i_q^+. (c) blue - i_d^-, green - i_q^-. (d) blue – Active power, green – Reactive power

In Figure 5.21 are presented the inner parameters of the MMC-1 and the DC-link voltage. It can be observed in (a) a 30% increase in the difference currents of the two unfaulted phases, in order to compensate the 60% reduction in the active power delivered by phase A. The sub-module capacitors have ripples of 20% in phase A and 10% in B and C respectively. The phase angle of the voltage ripples in the phase-legs is changed according to the AC currents, which is slightly reflected in the DC-link voltage ripple.

When the fault is imposed, the DC-link voltage presents ±2.5% ripples, reaching steady-state after 0.05s under unbalanced grid conditions. The pre-fault characteristics of the system are reached within 3 fundamental cycles after the unbalance is cleared.

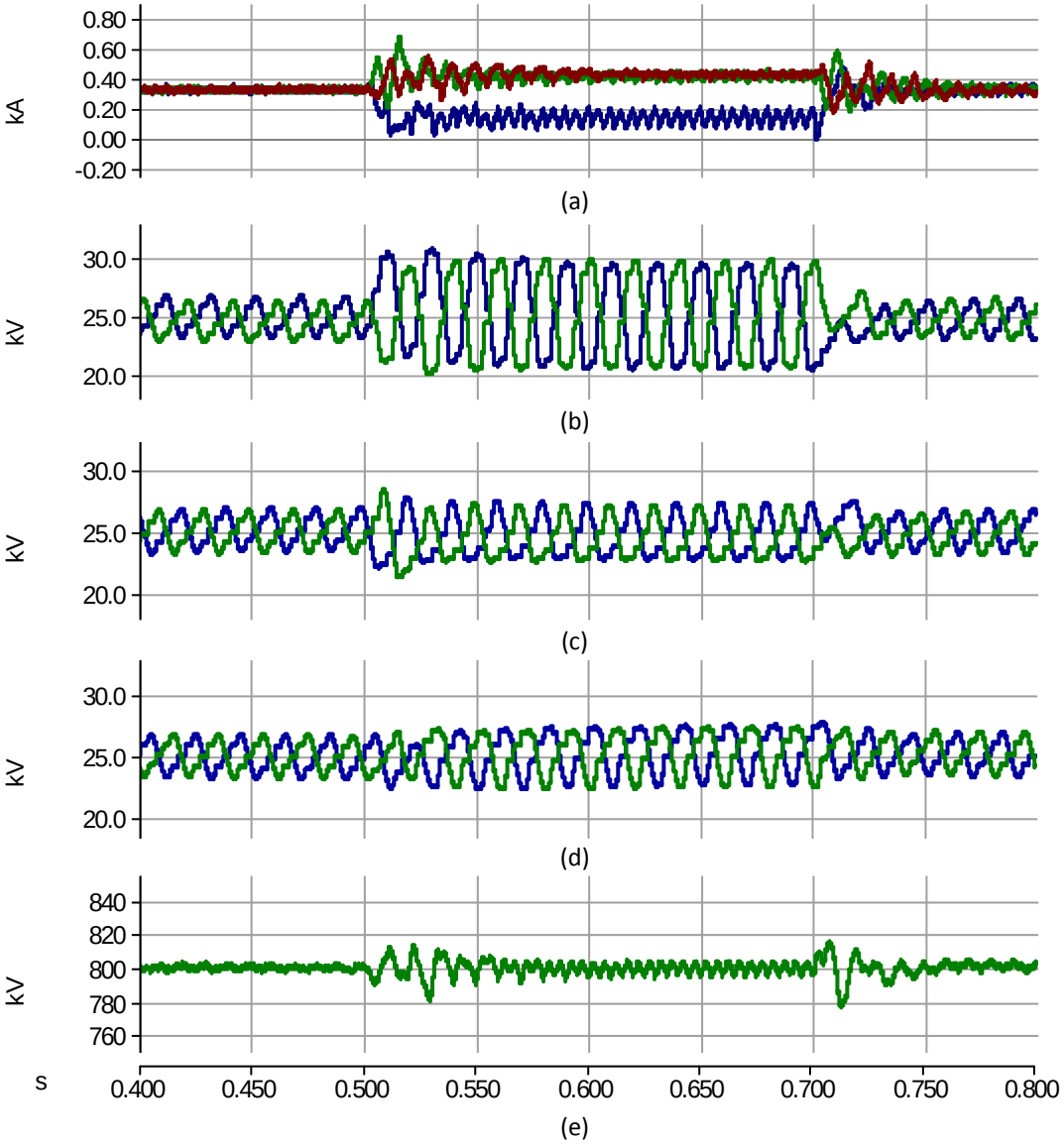

Figure 5.21 - Case 2, results in MMC-1. (a) Difference currents. (b,c,d) Phase A, B, C capacitor voltages respectively. (e) DC-link voltage

5.6.3 Case-3. Elimination of reactive power oscillations

Reactive power oscillations between the converter station and the grid have negative impact on the AC voltage profile, which could worsen the fault conditions. To compensate for the mentioned oscillations, the control objectives are defined as:

$$\begin{aligned} Q_{c2} &= 0 \\ Q_{s2} &= 0 \end{aligned} \tag{5.12}$$

Operating (5.6), the current references are obtained:

$$
\begin{aligned}
i_d^{+\,ref} &= \frac{2V_{sd}^{+}P_s^{ref}}{3[(V_{sd}^{+})^2-(V_{sd}^{-})^2]} \\
i_q^{+\,ref} &= -\frac{2V_{sd}^{+}Q_s^{ref}}{3[(V_{sd}^{+})^2-(V_{sd}^{-})^2]} \\
i_d^{-\,ref} &= \frac{2V_{sd}^{-}P_s^{ref}}{3[(V_{sd}^{+})^2-(V_{sd}^{-})^2]} \\
i_q^{-\,ref} &= \frac{2V_{sd}^{-}Q_s^{ref}}{3[(V_{sd}^{+})^2-(V_{sd}^{-})^2]}
\end{aligned}
\tag{5.13}
$$

During the fault, the positive component of the current i_d^+ is increased by 23%, as shown in Figure 5.22. Grid currents are unbalanced, having 40% decrease in the magnitude of the faulted phase and 50% increase in the unfaulted phases respectively (a). The objective of the control strategy is fulfilled having suppressed oscillations in the reactive power after 0.05s. The presence of i_d^- increases active power oscillations which are ±500 MW (66% higher than in Case-1). The average value of power is following the reference.

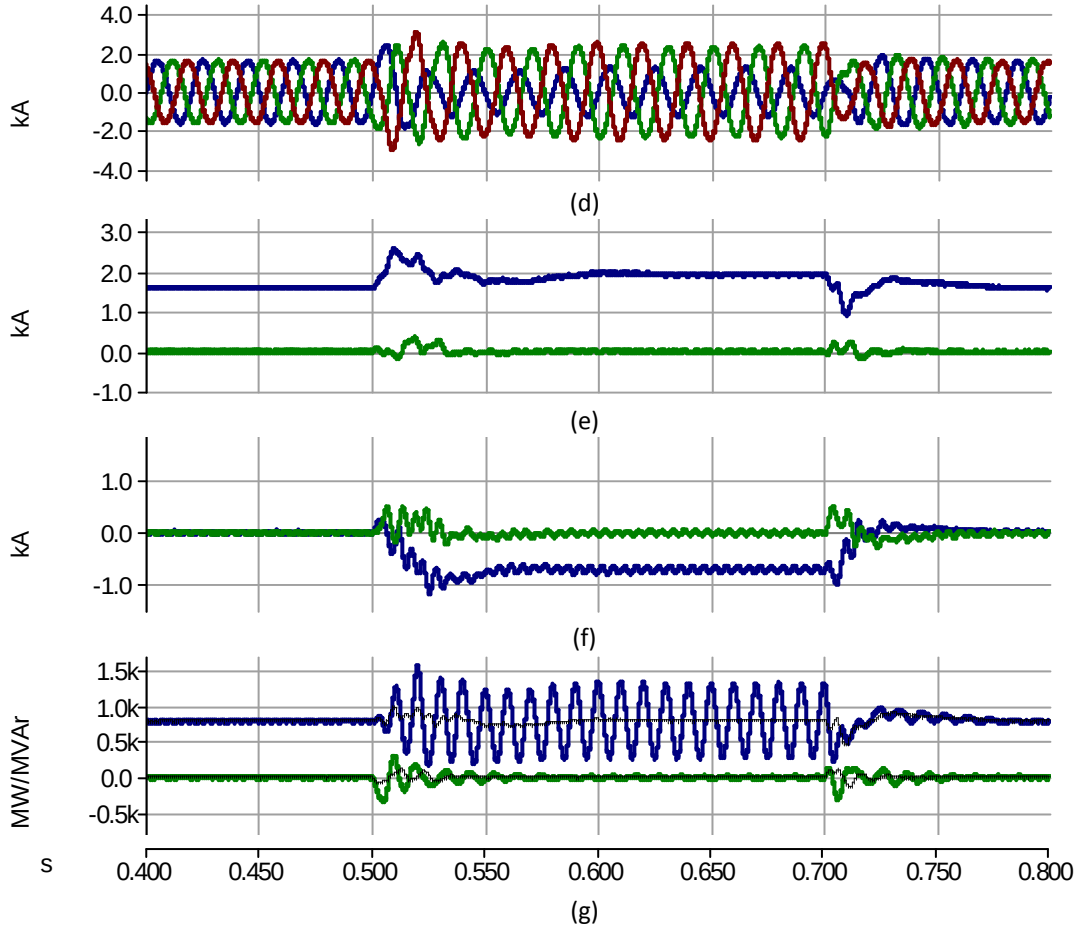

Figure 5.22 - Case 3, results in MMC-1. (a) Three phase AC currents. (b) blue - i_d^+, green - i_q^+. (c) blue - i_d^-, green - i_q^-. (d) blue – Active power, green – Reactive power

In Figure 5.23 are presented the inner dynamics of the MMC-1 and the DC-side. Since the power delivered by phase A is reduced by 75% during the fault, the difference currents of the two unfaulted phases is increased by 40% to avoid a drop in the average active power produced (a). It can be noticed that, phases B and C share active power loading unequally due to unbalance in the AC currents. In phases B and C the 12%

raise in the ripple amplitude corresponds to the increase in the loading (c,d). The phase angle of the capacitor voltage ripples is changed according to the present unbalanced currents. The DC-link voltage has transient peaks of 4.5%. After 0.08s converter reaches stable operation with unbalanced grid conditions. The pre-fault characteristics of the system are reached within 4 fundamental cycles after the fault is cleared.

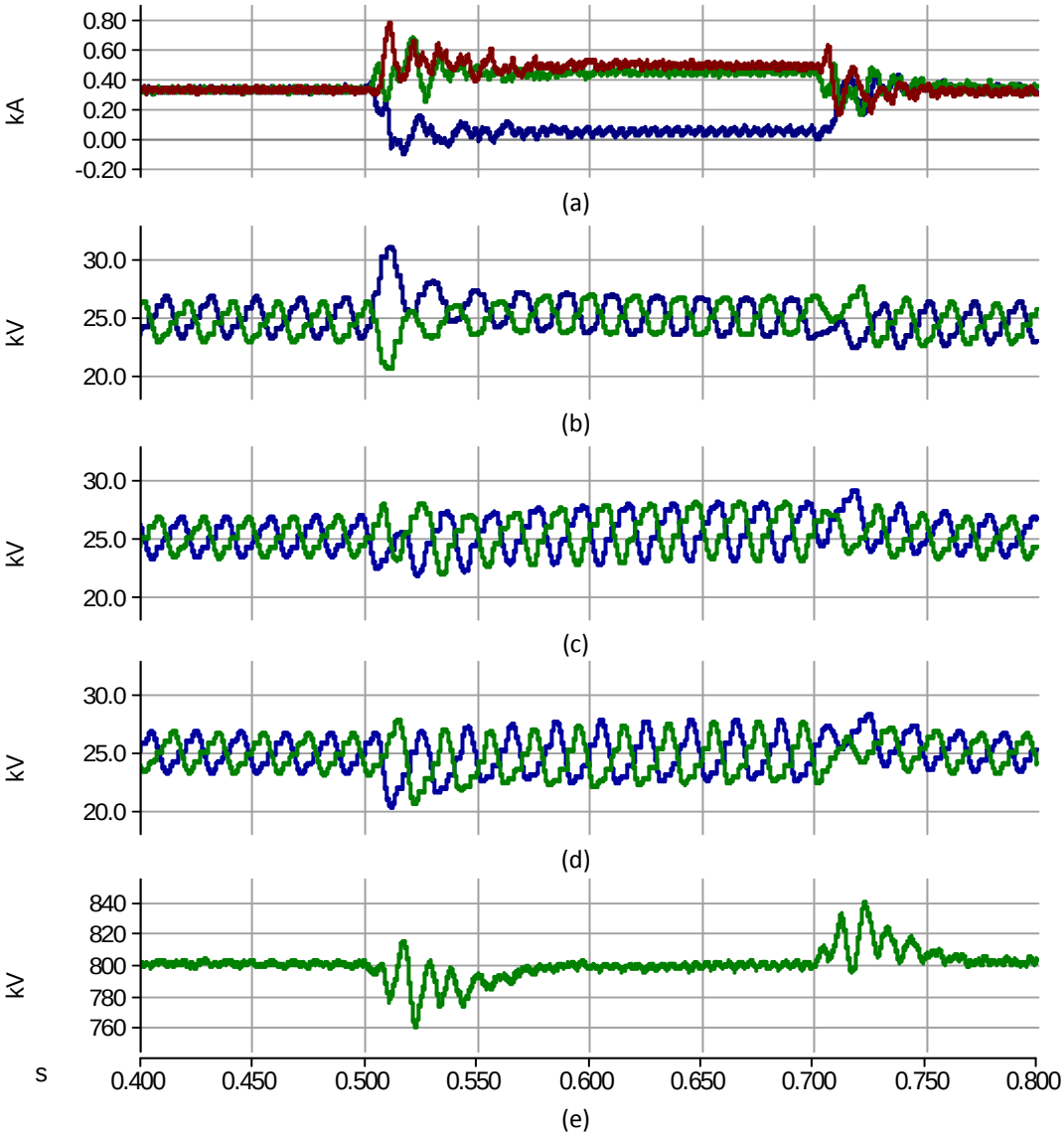

Figure 5.23 - Case 3, results in MMC-1. (a) Difference currents. (b,c,d) Phase A, B, C capacitor voltages respectively. (e) DC-link voltage

In Table 5.2 results of the three control strategies are summarized.

Table 5.2 – Impact of different control strategies on performance of MMC-HVDC

Control objective	Amplitude of AC currents (%)			Amplitude of Power oscillations (MW/MVAr)		Amplitude of capacitor voltage ripples (%)			DC-link voltage peak (%)	Comments on AC currents
	A	B	C	P	Q	A	B	C		
$\bar{i_d} = \bar{i_q} = 0$	+38			300	300	12	10	10	2.5	balanced
$P_{c2} = P_{s2} = 0$	+212	+38	+38	-	650	20	10	10	2.5	unbalanced
$Q_{c2} = Q_{s2} = 0$	-40	+50	+50	500	-	6	12	12	4.5	unbalanced

Analyzing the results it can be noticed that elimination of the negative sequence currents results in lower phase currents. Between the two power compensation methods, the elimination of reactive power oscillations implies less stresses to the converter in terms of currents and sub-module voltage ripples. However, it injects unbalanced currents to the grid, which might have limitations defined by the Grid Operator. To have flexible control over the power oscillations, a modification to the calculation of injected current sequence components is proposed in [69].

During simulations it was observed that the ripples in the DC-link, when the fault occurs and when is cleared, were reflected in the difference current of MMC-2. The highest peak current ripple was of 6.3% and appeared in Case 3. As analyzed in Chapter 3, the ripples in the difference current are not reflected in the output currents; therefore AC-system 2 is not affected.

All the control strategies ensured stable operation of the converter under unbalanced conditions. The inner controls of the MMC maintained leg voltages at the reference and balancing effectively the cell voltages during transients (detailed plots in Appendix). The pre-fault parameters of the system were reached within 3-4 fundamental cycles after the fault was cleared, depending on the control strategy. This complies with the Grid Code requirements presented in Chapter 2.

5.7 Converter current limitation

The described control strategies have shown an increase in the AC currents due to change in grid conditions. Depending on the particular conditions of the grid unbalance, these currents may exceed the limits of the converter devices, thus tripping the overcurrent protection. A current-limiting mechanism should be implemented in order to ensure stable and continuous converter operation during faults.

The amplitude of the AC current at rated operational conditions can be calculated based on the system and converter parameters:

$$\hat{\imath}_{ac} = \frac{S_{nom}}{V_s} \tag{5.14}$$

Knowing the permissible overcurrent, it is possible to obtain the maximum AC currents allowed. However, the currents in the converter arms do not represent the AC currents directly. As it was presented in Chapter 3, the converter arm currents are composed of the DC, fundamental AC and double line-frequency circulating components. Assuming effective suppression of the circulating current, the arm currents can be expressed as shown:

$$i_u = i_{dc} + \frac{i_{ac}}{2} \tag{5.15}$$

$$i_l = i_{dc} - \frac{i_{ac}}{2} \tag{5.16}$$

Where the DC component represents the active power transfer and the AC component is half of the grid current, due to its equal share between the arms. Neglecting the losses in the converter, the DC component of the arm current in a three-phase converter under balanced conditions can be calculated as:

$$i_{dc} = \frac{P_s}{3V_{dc}} \tag{5.17}$$

Knowing the desired maximum active power and the allowable currents in semiconductors ($i_{arm,max}$), the limit for the AC grid current amplitude can be obtained as:

$$\hat{\imath}_{ac,lim} = 2\left(i_{arm,max} - i_{dc,max}\right) \tag{5.18}$$

Then, having the limits obtained, the grid currents can be effectively controlled by estimating the instantaneous active or reactive power references from (5.14), depending on the grid voltage:

$$P_s^{ref} = \sqrt{V_s^2 \hat{\imath}_{ac,lim}^2 - Q_s^2} \tag{5.19}$$

$$Q_s^{ref} = \sqrt{V_s^2 \hat{\imath}_{ac,lim}^2 - P_s^2} \tag{5.20}$$

5.7.1 Calculation of AC current limits

For the converter with rated apparent power of 850 MVA connected to the 400 kV grid, the peak rated current is:

$$\hat{\imath}_{ac} = \frac{S_{nom}}{V_s} = \frac{\sqrt{2} \cdot 850}{\sqrt{3} \cdot 400} = 1.74\ kA \tag{5.21}$$

The converter peak arm current when P=800 MW is:

$$\hat{\imath}_{arm,nom} = i_{dc} + \frac{\hat{\imath}_{ac}}{2} = \frac{800}{3 \cdot 800} + \frac{1.74}{2} = 1.2\ kA \tag{5.22}$$

Assuming that the maximum device current $\hat{\imath}_{arm,max}$ is 125% of the rated and considering the scenario when one phase is lost and the active power should be delivered by the two phases left, the limits for the AC grid currents are obtained from (5.18) as:

$$\hat{\imath}_{ac,lim} = 2\left(\hat{\imath}_{arm,max} - i_{dc,max}\right) = 2\left(1.25 \cdot 1.2 - \frac{800}{2 \cdot 800}\right) = 2\ kA \tag{5.23}$$

5.7.2 Validation of current limitation strategy

In order to highlight the results obtained with the current limitation strategy the unbalance in Phase A is imposed at t=0.5s, dropping the voltage to zero. At t=0.6s the current limitation is activated. Two cases are simulated; in the first case the active power reference is changed to comply with the current limitations. In the second case the active power is reduced to 0 while full reactive power injection is activated to provide grid voltage support. The objective of the current-control strategy is the elimination of negative sequence currents (Section 5.4.2).

5.7.2.1 Maximum active power injection

In Figure 5.24 is presented the response of the MMC-1 when the grid unbalance is imposed. The amplitude of AC currents is increased by 50% with peak value of 2.8 kA, exceeding the calculated limit of 2 kA.

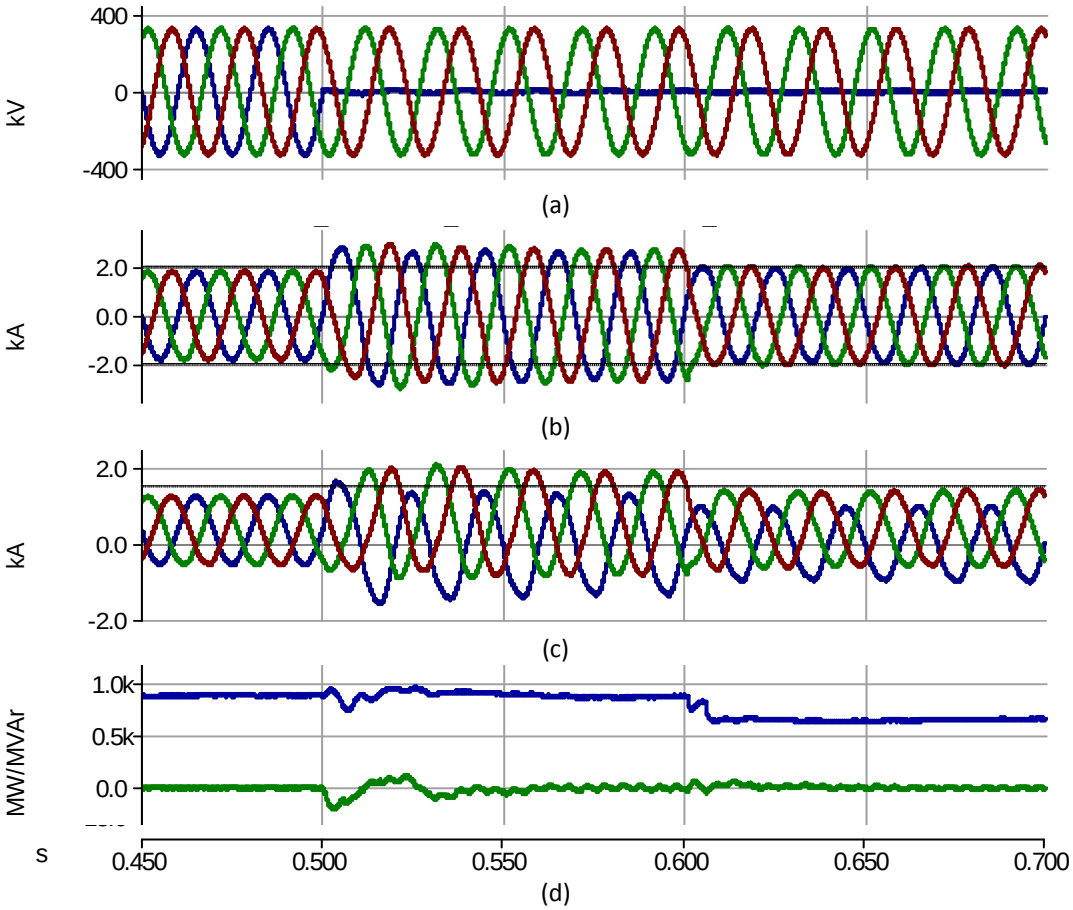

Figure 5.24 – Current limitation, results in MMC-1 with maximum active power injection. (a) Grid voltages (b) Three phase AC currents. (c) Upper arm currents in the three phases. (d) blue – Active power, green – Reactive power

When the current limitation is activated, a new power reference is calculated from (5.19) in order to produce maximum active power without exceeding the current limits (d). The new power reference is 630 MW, which represents the reduction in 21% of active power delivered to the grid. The upper arm currents of the three-phases are shown in (c). After the limitation is activated, the arm currents are effectively kept under de limit of 1.5 kA. It can be noticed that the arm current of phase A (blue) is purely sinusoidal due to no active power transfer while B and C contain a DC component responsible of the active power transfer.

5.7.2.2 Maximum reactive power injection

It can be observed in Figure 5.25 that during the fault, the amplitude of AC currents increases to 2.8 kA while the arm currents rise to 2 kA, exceeding the limits by 0.5 kA. At time t=0.6s the current limitation is activated and the active power is ramped to zero. The new AC current limit is calculated using (5.23) as 3 kA (b). The reactive power reference is calculated according to (5.20) having a value of 1030 MVAr (d).

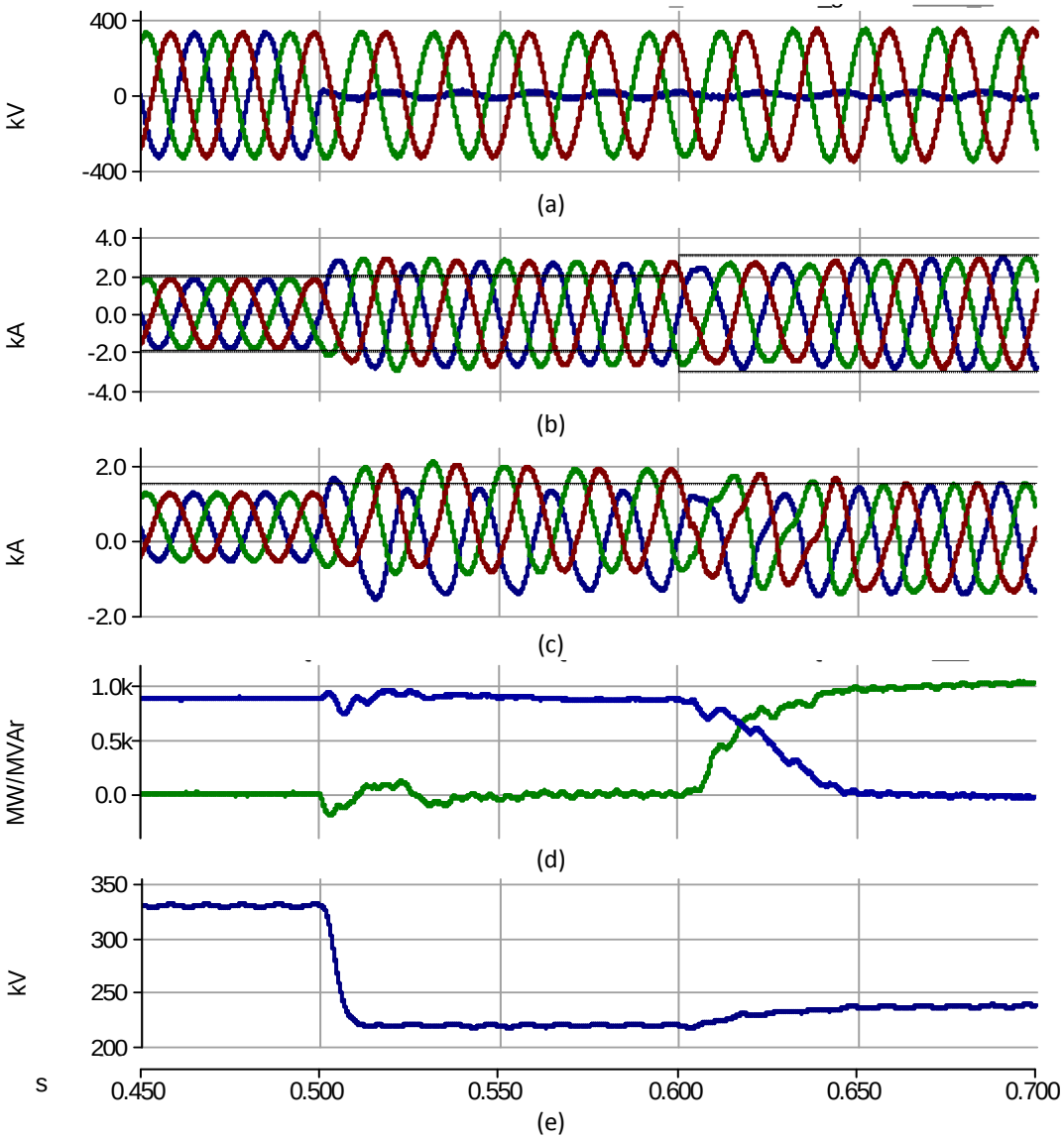

Figure 5.25 - Current limitation, results in MMC-1 with maximum reactive power injection. (a) Grid voltages (b) Three phase AC currents. (c) Upper arm currents in the three phases. (d) blue – Active power, green – Reactive power. (e) Positive sequence component of the Grid voltage

The arm currents fall into the imposed limits within 3 fundamental cycles, because of the ramped change of power references. However, after stabilisation, the limits for the arm and AC currents are not exceeded. With the injection of reactive power, the grid voltage is raised by 8% (e), thus the converter provides grid voltage support with maximum allowed reactive current injection.

5.8 Chapter Summary

In this chapter, the operation of the HVDC system under unbalanced grid conditions was studied. First, propagation of unbalanced faults through the DC transmission system was analyzed. It was observed the presence of high zero sequence current in the converter, together with voltage ripples in the DC-link. To compensate these problems, two additional loops for negative and zero sequence current control were implemented. Furthermore, a modification to the circulating current control was proposed to improve the converter performance during unbalanced conditions.

Also, three strategies to calculate the current references under unbalanced grid conditions were studied and verified in simulations. Their effect on the inner parameters of the converter and DC transmission was analyzed.

It was noticed that during the fault high currents appear in the converter arms, therefore a current limitation strategy was presented. A method to calculate the limits for the MMC output currents, based on the arm current limits was derived.

6 Conclusions

The simulation model of the transformerless MMC-HVDC transmission system implemented in PSCAD/EMTDC was presented. For the inner controls of the converter, a combination of Distributed control and Direct suppression of circulating current was selected. The HVDC system controls were based on fast inner current loop, implemented in *dq* reference frame, and outer power and voltage loops. Grid synchronisation was achieved by PLL. The step response of the current and DC voltage control was assessed independently in the simulation. The performance of the MMC-HVDC transmission system was verified for ramp changes in active and reactive power as well as full active power reverse. The effectiveness of the inner converter controls was proven, having balanced capacitor voltages and effectively suppressed circulating current throughout the simulations.

The operation of the MMC-HVDC system under unbalanced grid conditions was tested. First, the propagation of unbalanced grid faults through the DC-link was investigated. It was concluded, that zero sequence currents flow through the DC-link, causing voltage oscillations between the neutral point and ground. These oscillations are directly transmitted to the three phase output currents of the healthy AC system, which is not acceptable by the Grid Codes. For that reason, an additional loop with zero sequence current control was implemented. It was observed that by suppressing the zero sequence current, it was possible to eliminate the propagation of the fault to the healthy AC system. This enhances the feature of HVDC transmission to act as isolation between the two AC grids. Moreover, the voltage oscillations in the DC-link neutral point were removed and the capacitor voltage ripples were reduced, minimizing the stresses on the faulted converter station. However, the presence of the unbalance was still reflected as a ripple in the DC-link voltage, disturbing the inner currents of the unfaulted converter station. To solve this problem a negative sequence current control was implemented. It was observed that, although the negative sequence currents got eliminated, the ripples in the DC-link were still present. A modification to the inner current control of the MMC was proposed to eliminate the zero sequence component of the difference current and, as a consequence, the voltage ripples in the DC-link. The disturbance to the unfaulted converter was effectively reduced to short transients in the arm currents.

Three strategies to calculate the current references under unbalanced grid conditions were studied. The possibility of compensating the power oscillations by means of negative sequence current injection was verified in simulations. The effect of different strategies on the inner parameters of the converter and the DC-link was analyzed. It was concluded that by maintaining balanced AC currents, less stresses on the converter are applied due to smaller voltage ripples in the capacitors. The inner controls of the converter presented good performance under unbalanced conditions.

Although the mentioned control strategies presented a satisfactory performance, the current in the converter during the fault increased to unacceptable values that could trip an overcurrent protection or damage the converter components. For this reason, a strategy to limit the converter currents was implemented. The relation between the grid and converter arm currents was derived, making current limitation approach straightforward. Two cases with current limitation were simulated. First, the active power of the converter was reduced based on the grid voltage and the converter current limits. This approach showed a fast response without significant transients. In the second case, the converter active

power was reduced to zero with full reactive power injection. The injection of reactive power boosted the grid voltage, thus supporting the grid during the fault. The effectiveness of the converter current limitation was verified, demonstrating the fault ride-through capability of the converter. Both studied cases required partial or full reduction in active power transmission through the DC-link. This might have a negative impact, since the other converter station will be force to reduce or stop power transmission.

The results obtained in the simulations demonstrate the great potential that MMC has for HVDC applications, having the possibility of being implemented in transformerless connection with a good fault ride-through capabilities.

6.1 Future Work

The following subjects can be investigated further, to contribute to the project:

- Analysis of the converter performance under different types of balanced and unbalanced faults;
- Evaluation of delays on the controllability of the converter;
- Implementation of different control architectures using advanced control techniques (model predictive control, deadbeat control, multivariable control);
- Investigation of MMC-HVDC performance in meshed DC transmission grids;
- Implementation of the control strategies in small-scale converter prototype.

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Appendix

Park's Transformation

Three phase variables are transformed into rotating reference frame *dq*.

$$\begin{bmatrix} v_d \\ v_q \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} cos\theta & cos\left(\theta - \frac{2\pi}{3}\right) & cos\left(\theta - \frac{4\pi}{3}\right) \\ -sin\theta & -sin\left(\theta - \frac{2\pi}{3}\right) & -sin\left(\theta - \frac{4\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

Clarke's Transformation

Three phase variables are transformed into stationary reference frame αβ. $\theta = 0$

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix}$$

DC cable parameters

DC cable is implemented in frequency-dependent PSCAD model.

- Cable lengths - 100km;
- Conductor outer radius – 0.022m;
- Insulator outer radius – 0.0395m;
- Insulator relative permittivity – 4.1;
- Copper resistivity – $16.8 \cdot 10^{-6}$ Ω/km;
- Capacitance – $0.389 \cdot 10^{-6}$ F/km;
- Inductance – $0.167 \cdot 10^{-6}$ H/km.

Case-1. Elimination of negative sequence currents. Sub-module capacitor voltages of MMC-1 (left) and MMC-2 (right). Fault at MMC-1 at t=0.5-0.7s

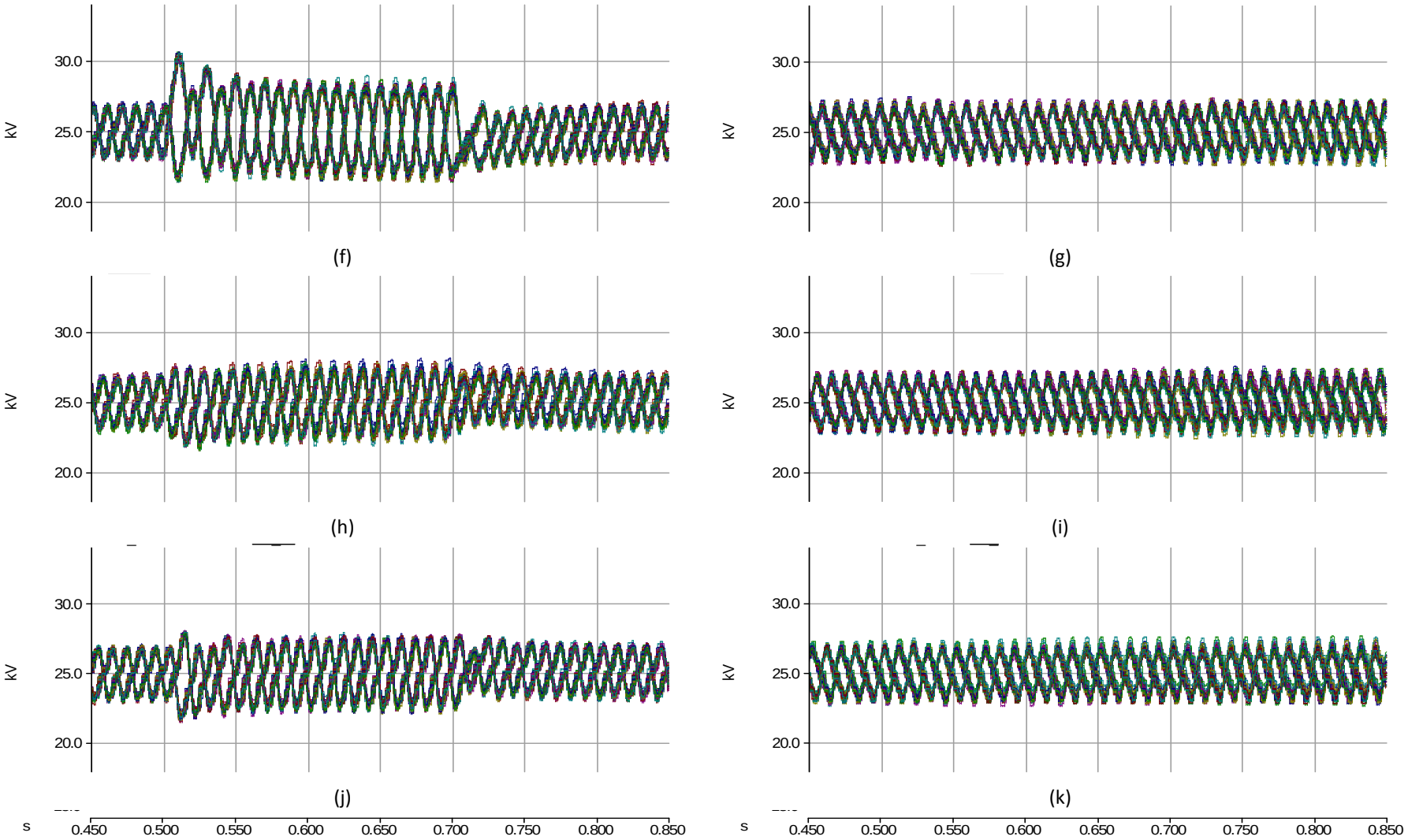

Figure 0.1 – Case 1. (a, b) Phase A. (c, d) Phase B. (e, f) Phase C.

Case-2. Elimination of active power oscillations. Sub-module capacitor voltages of MMC-1 (left) and MMC-2 (right). Fault at MMC-1 at t=0.5-0.7s

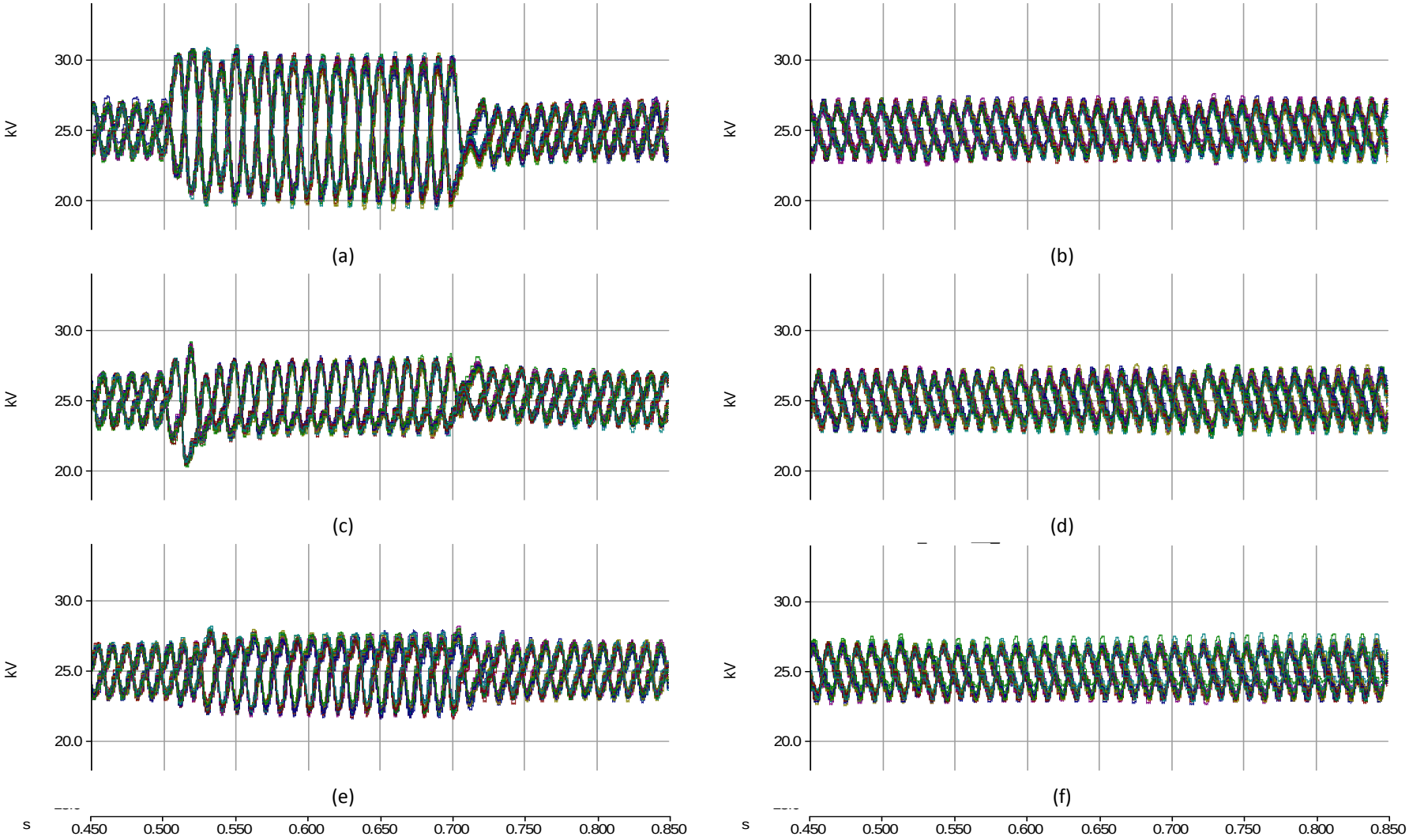

Figure 0.2 – Case 2. (a, b) Phase A. (c, d) Phase B. (e, f) Phase C.

Case-3. Elimination of reactive power oscillations. Sub-module capacitor voltages of MMC-1 (left) and MMC-2 (right). Fault at MMC-1 at t=0.5-0.7s

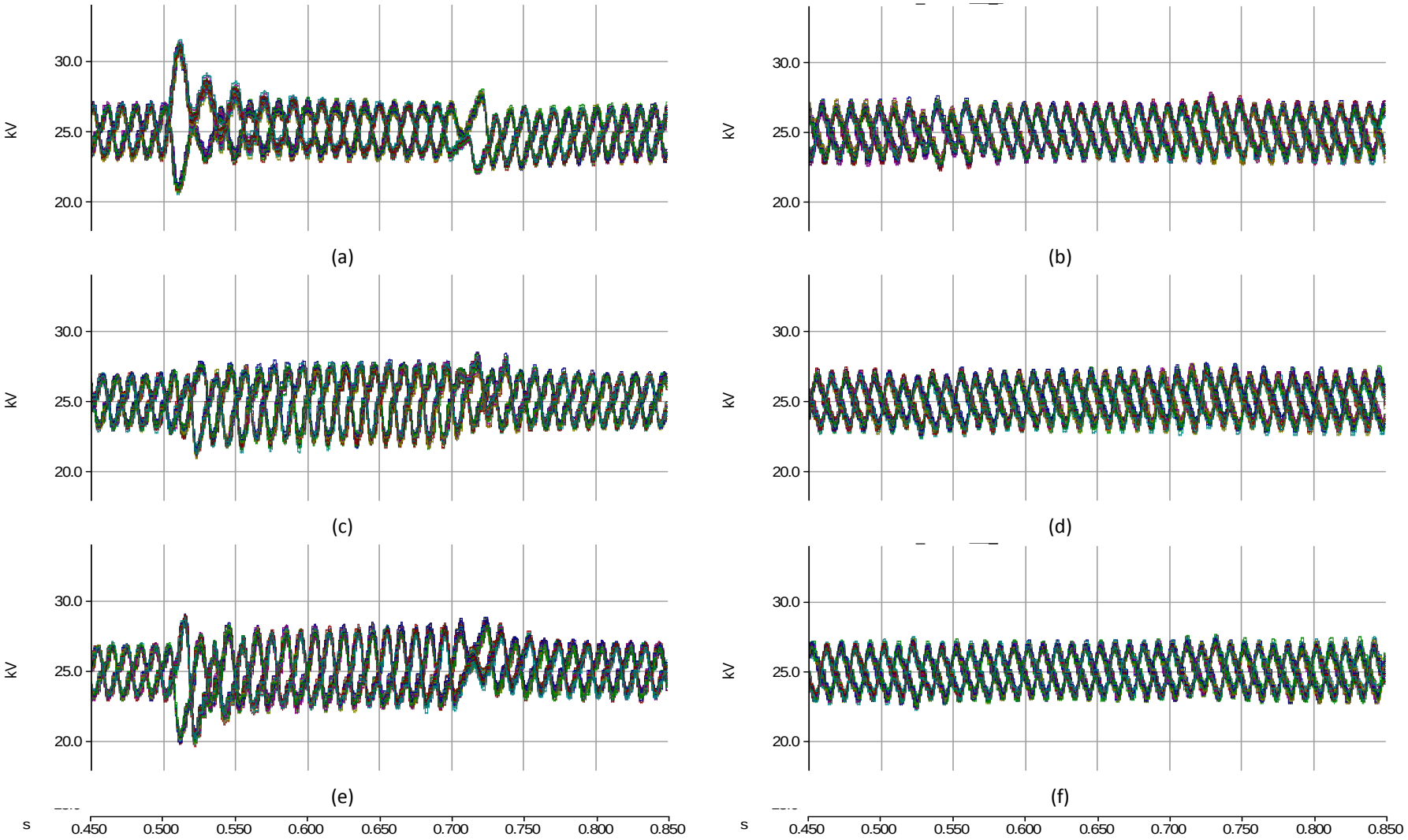

Figure 0.3 – Case 3. (a, b) Phase A. (c, d) Phase B. (e, f) Phase C.