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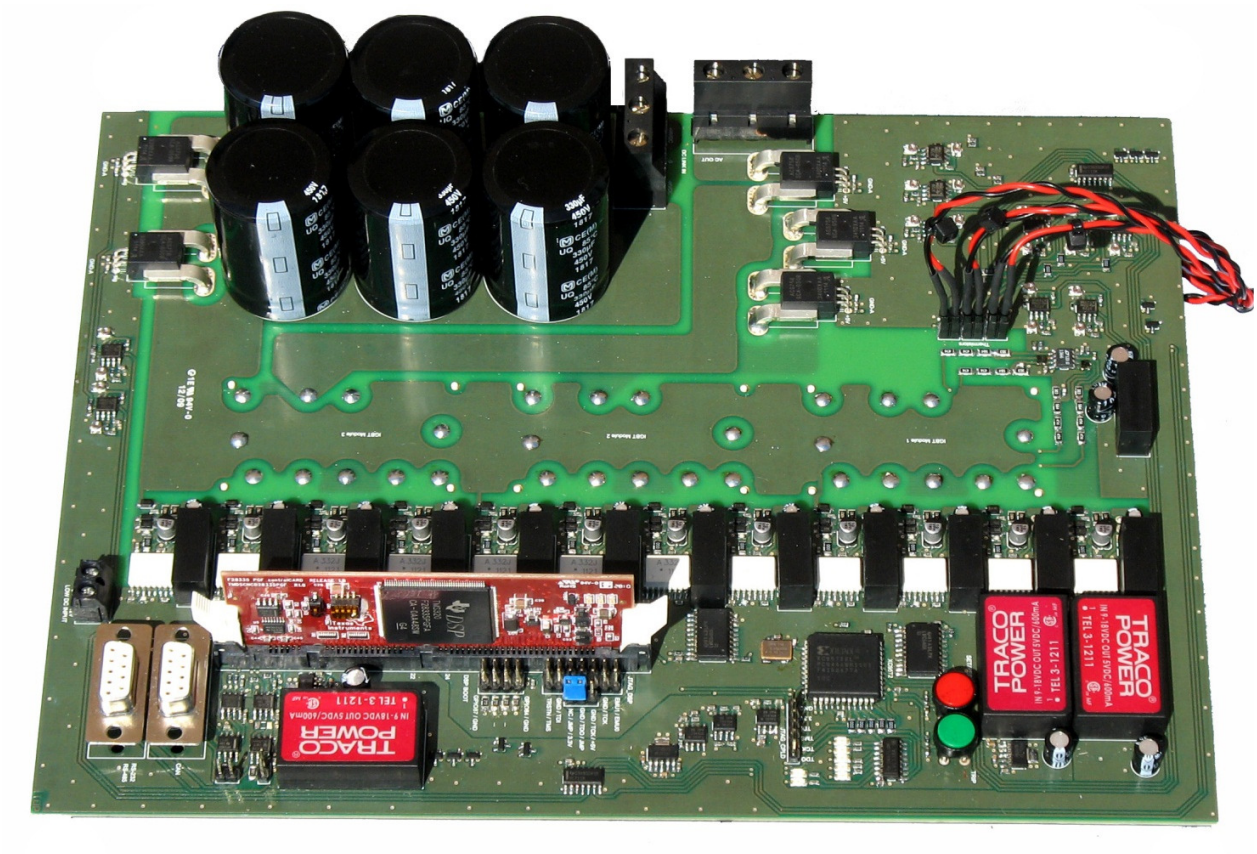
Development of Modulation Strategies for NPC Inverter Addressing DC Link Balancing and CMV Reduction



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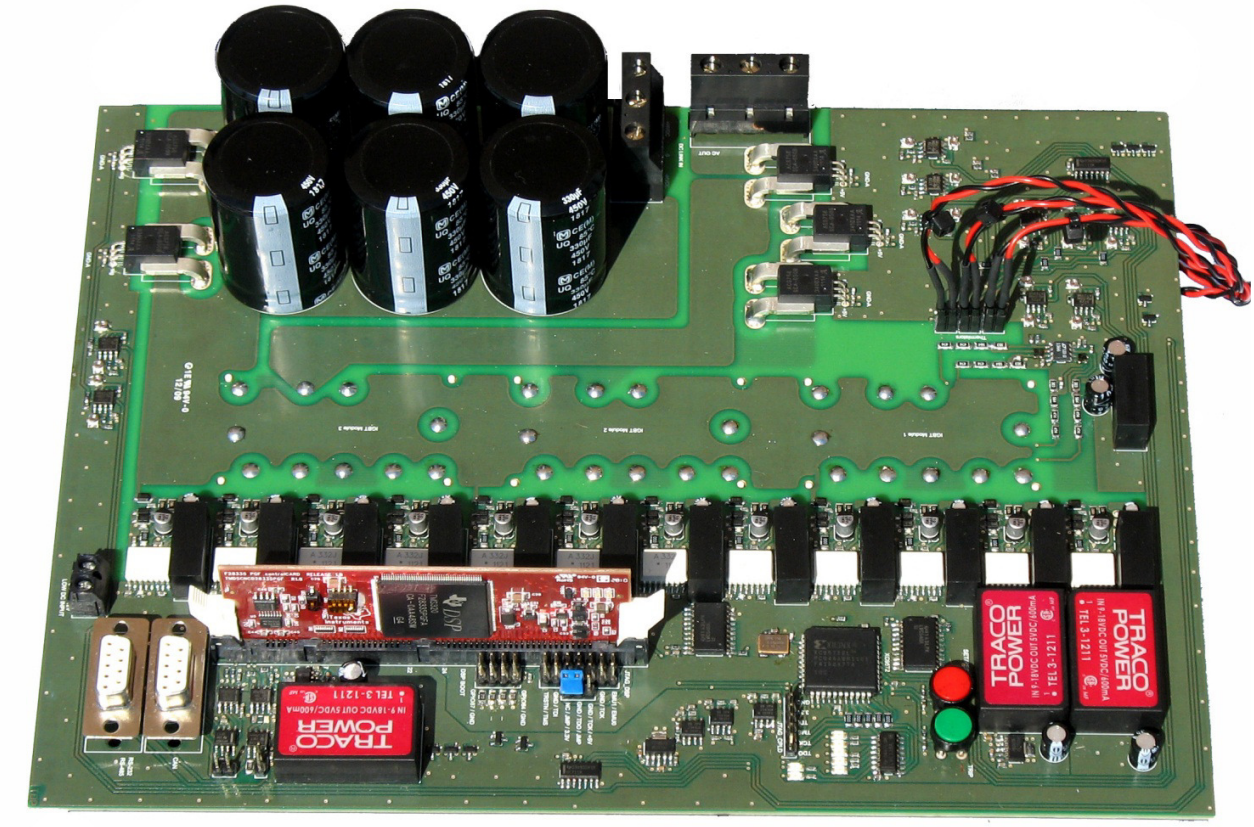
AALBORG UNIVERSITY
STUDENTS STUDYREPORT

Master Thesis

Department of Energy Technology-Pontoppidanstraede 101

Aalborg University, Denmark

Development of Modulation Strategies for NPC Inverter Addressing DC Link Balancing and CMV Reduction



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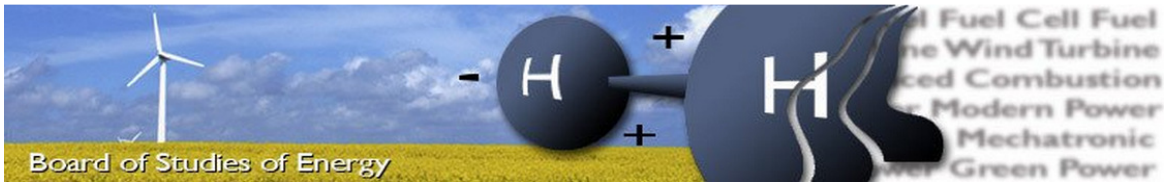

Title:	**Development of Modulation Strategies for NPC Inverter Addressing DC Link Balancing and CMV Reduction**
Semester:	**9th – 10th**
Semester theme:	**Master Thesis**
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Supervisors:	**Remus Teodorescu**
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Project group:	**PED1041**

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SYNOPSIS:

Two level inverters generate Common Mode Voltage (CMV) in the motor windings, causing motor failures due to bearing currents. Furthermore, a leakage current will flow throughout the stator windings and motor frame creating common mode electromagnetic interference. Taking these problems into consideration and the fact that the multilevel inverters offer better Total Harmonic Distortion (THD) as well as the possibility to reduce the CMV by modulation strategy, they it became a point of interest. Compared to higher level topologies, a good ratio between complexity and performance is offered by the three-level topology. As this type of inverter synthesises the output voltage from series connected DC link capacitors, problems such as neutral point balancing might appear, causing voltage stress on the semiconductors.

The aim of this project is to develop modulation strategies that address both DC link voltage balancing and CMV reduction.

Four modulation strategies that address these problems were developed and validated through simulation. Furthermore, in order to experimentally validate them, a Neutral Point Clamped (NPC) inverter was designed and built. Analysis, regarding CMV and Electromagnetic Interference (EMI) together with neutral point balance assessment, was performed on each developed modulation which concluded that all proposed strategies offer better CMV and EMI spectrum compared with classical NTV and ZCM.

Copies:	[3]
Pages:	[110]
Appendix:	[11]
Supplements:	[1 CD]

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

Preface

The Master in Science thesis was carried out during 9th and 10th semester at Aalborg University in the Department of Energy Technology starting from 1st of September 2011 until 31st of May 2012. The project "Modulation of three-level inverter with common-mode voltage elimination and DC-link balancing" was chosen by the authors from the Vestas catalogue containing proposals for students from Energy Technology department.

Acknowledgments

The authors would like to thank their supervisors: Remus Teodorescu, Michal Sztykiel and Osman Selcuk Senturk for their guidance during the master thesis.

They would like to give special thanks to Stig Munk-Nielsen, Carsten Karup Nielsen and Laszlo Mathe for their help during inverter design, as well as to Adrian Hasmasan.

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The Master in Science Thesis was conducted by:

Daniela Boian _____

Ciprian Biris _____

Summary

As well known the two-level topology generates CMV in the motor windings furthermore causing motor failures due to bearing currents. As there are parasitic capacitive couplings between the stator windings and the motor frame a common mode leakage current will flow, hence there will be common mode electromagnetic interference. Taking these problems into consideration, multilevel inverters have gained interest. These types of inverters offer lower THD in the phase-to-phase voltage as well as the possibility to reduce the CMV through modulation strategy. As the phase-to-phase waveform is produced form series connected capacitors an unbalance may appear causing voltage stress on the IGBTs.

Solutions to reduce the common mode voltage and to balance the DC link through modulation strategies have been studied in this project due to their cost effectiveness.

This thesis is structured in six chapters and has ten appendixes. The background of the three-level NPC inverter together with the problem formulation regarding CMV and DC link balance is presented in the first chapter. Furthermore, the study and development of new and improved modulation strategies as well as the hardware design represent the objectives. Also, project limitations are stated.

Chapter two is focused on the NPC inverter topology and its background. Further in this chapter space vector modulation and switching states make an introduction for the classical modulation strategies studied: Nearest Three Vectors with Even Harmonic Elimination (NTV-EHE) and Zero Common Mode (ZCM). Also the DC link balancing problem and mitigation for NPC converters is studied as well as CMV and its mechanism together with its effects. The end of second chapter presents the methods for measuring the CMV and EMI.

The new proposed modulation strategies are presented in the third chapter. The theoretical basics together with the validation through simulations are part of the acknowledgement of these strategies. The chapter ends with a comparative evaluation of the developed strategies compared with the classical ones.

The fourth chapter is dedicated entirely to hardware design. A NPC inverter was built featuring reduced size, snubberless design due to newly introduced NPC leg Insulated Gate Bipolar Transistor (IGBT) modules, protections, RS-232 and CAN communications and mixed analogue and digital design. The overview of the developed platform is made after which, the sizing and implementation of the DC link is described, IGBT modules, gate drivers, microcontroller and protections. The thermal cooling solution is presented together with its validation through thermal imaging. This chapter ends with an overview of the implemented control on the Digital Signal Processor (DSP) and Complex Programmable Logic Device (CPLD) is followed by hardware validation tests.

The experimental validation and analysis of the developed modulation strategies is the main focus of chapter 5. The results and waveforms of the new strategies as well as the classical ones are presented and analysed together with the DC link balancing capability assessment and CMV evaluation. The chapter is ended with results regarding the conductive EMI produced by these strategies.

The last chapter presents conclusions regarding the results of CMV, DC link balancing and conductive EMI of the developed modulation strategies, in comparison with classical ones.

Furthermore, the appendixes are included as follows:

- Appendix 1: Project Proposal
- Appendix 2:
- Appendix 3: Experimental Setup Data
- Appendix 4: CPLD/DSP Pin Assignment
- Appendix 5: CPLD Functional Schematic
- Appendix 6: PCB Photos
- Appendix 7: PCB Layers
- Appendix 8: Electrical Schematic
- Appendix 9: Bill of Materials
- Appendix 10: Paper
- Appendix 11: Contents of the CD

Contributions

This project brings the following contributions:

- NPC inverter design with NPC leg IGBT modules
    - ❖ Reduced size
    - ❖ RS-232, RS485 and CAN communication
    - ❖ Software and hardware protections
    - ❖ Snubberless design
    - ❖ Embedded DSP
- Modulation Strategies that address both DC link balancing problem and CMV reduction

During this project a paper has been written. This paper has been accepted in the IEEE PEDG conference held in Aalborg, Denmark in June 2012. This paper can be seen in Appendix 10.

- Daniela Boian, Ciprian Biris, Remus Teodorescu, Michal Sztykiel, "Development of Modulation Strategies for NPC Converter Addressing DC Link Voltage Balancing and CMV Reduction"

Abbreviation	Full form
AC	Alternative Current
ADC	Analogue to Digital Converter
ASD	Adjustable Speed Drive
CAL	Controlled Axial Lifetime
CAN	Controller Area Network
CM	Common Mode
CMC	Common Mode Current
CMR	Common Mode Rejection
CMV	Common Mode Voltage
CPLD	Complex Programmable Logic Device
CSI	Current Source Inverter
DC	Direct Current
DCB	Direct Copper Bonded
DMOS	Double Diffused Metal Oxide Semiconductor
DSP	Digital Signal Processor
EDM	Electric Discharge Machine
EHE	Even Harmonic Elimination
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ePWM	enhanced Pulse Width Modulator
FFT	Fast Fourier Transformation
FLC	Flying Capacitor
FLIR	Forward Looking Infra-Red
GPIO	General Purpose Input Output
HF	High Frequency
HV	High Voltage
HVDC	High Voltage DC
I/O	Input/ Output
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
ISR	Interrupt Service Routine
LCI	Load Commutated Inverter
LED	Light Emitting Diode
LISN	Line Impedance Stabilisation Network
NP	Neutral Point
NPC	Neutral Point Clamped
NPT	Non Punch Through
NTC	Negative Temperature Coefficient
NTV	Nearest Three Vectors
NTV-EHE	NTV with Even Harmonic Elimination
OLOM	One Large One Medium
OSOM	One Small One Medium
PCB	Printed Circuit Board
PSRR	Power Supply Rejection Ratio
PWD	Pulse Width Distortion

PWM	Pulse Width Modulation
RAM	Random Access Memory
RC	Resistive - Capacitive
RCD	Random Centre Distribution
RL	Resistive - Inductive
RLL	Random Lead-Lag
RMS	Root Mean Square
RS3N	Random Sequence of 3 with Neutral Balancing
RZD	Random Zero Distribution
SARAM	Single Access RAM
SHE	Selective Harmonic Elimination
SOIC	Small Outline Integrated Circuit
SVM	Space Vector Modulation
TBCTR	Time Based Counter
THD	Total Harmonic Distortion
TNPC	Type Neutral Point Clamped
UVLO	Under Voltage Lock-Out
V/f	Volt/hertz
VSI	Voltage Source Inverter
ZCM	Zero Common Mode
ZSML	Zero Small Medium Large

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1. Introduction

This chapter introduces the problems that appear in Adjustable Speed Drives (ASD) - which affect both the inverter and motor, as well as presenting advantages and disadvantages for the three-level NPC inverter. Furthermore, problem formulation, motivation, objectives and limitations are stated.

1.1. Background

A widely discussed subject is the one of saving energy. Electrical motors are widely used to generate motion from electrical energy [**1**]. Industrial and domestic applications use electric motors with a large variety of power ratings. In most countries**,** electric motors use approximately 70% of the produced electric energy [**2**]. In the past**,** DC machines were used due to their simplicity in speed control. Nevertheless**,** these types of machines compared with AC ones, have some disadvantages such as higher cost, higher rotor inertia and maintenance issues with the brushes. Due to these problems, DC machines have been progressively replaced by AC machines. These types of machines cannot be efficiently controlled with direct connection to the grid, thus ASD for control of the magnitude and frequency of the output voltage are needed. These types of drives have a large scale of utilization in industrial applications. Due to the development of adjustable drives**,** the reliance in three phase AC motors has increased [**1**]. As a consequence of the rotor simplicity, induction motors have allowed solutions with lower cost [**3**].

As most applications require variable speed the chosen application for this project is ASD. Its principle is to convert the constant AC voltage into a variable one with the purpose of controlling the speed of the AC motor. A typical structure can be seen in Figure 1-1.

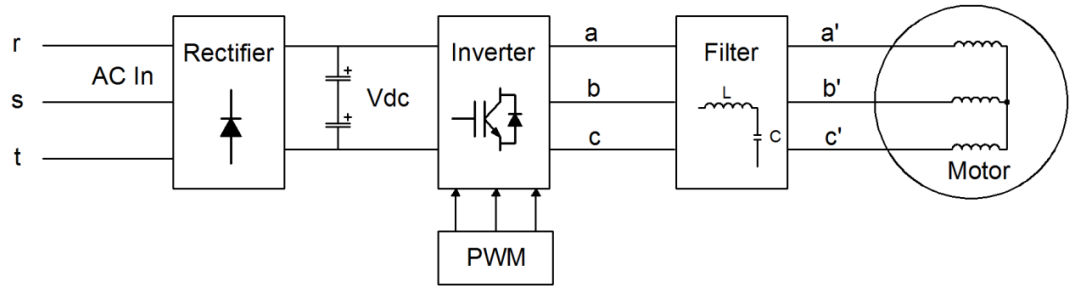


Figure 1-1 - Typical ASD

The Pulse Width Modulation (PWM) inverter needs to synthesise the input voltage in order to obtain the desired variable output voltage with a corresponding pulse shape sinusoidal.

When long cables are required in order to connect the inverter to the motor, a LC filter is used [**3**]. The variation in time has to be taken into account as it is dependent on the rise and fall time of the switching device that might lead to stress at the motor terminals.

Adjustable speed drives can be classified based on the inverter topologies according to [**4**]:

- Voltage Source Inverter (VSI) drives: have a constant DC link voltage. The DC link capacitors are used in order to supply reactive power to the motor and to smooth the DC link voltage.
- Multi-level Voltage Source Inverter drives: uses series connected low voltage IGBTs.
- Current Source Inverter (CSI) drives: makes use of DC link current.
- Load Commutated Inverter (LCI) drives: takes part of the CSI. This type of drive store energy in the DC link inductor in order to supply quasi-sinusoidal current.
- Cycloconverter: does not have the ability to store energy in the DC link. Each phase of the Cycloconverter modifies the fixed line AC voltage into an alternating voltage at a variable load frequency.
- Cascade drives: makes use of a three phase diode rectifier that operates at slip frequency and feds back the power to the supply network through a reactor and line commutated inverter. The motor speed is controlled by the DC current.

Nowadays**,** the need to increase efficiency and reduce production cost is the most discussed subject. This can be achieved by increasing the size and power of all electrical drives and equipment. The power increase can be done in two ways [**5**]:

- Developing High Voltage (HV) semiconductors with increased voltage blocking capabilities
- Development of multilevel inverters

The dominant topology for low voltage is two-level VSI. At medium and high voltage there are a variety of topologies. In high voltage**,** it is possible to use direct converters (cyclo-converters) and indirect converters (with current or voltage in DC link). Figure 1-2 presents the structure for high power converters [**5**].

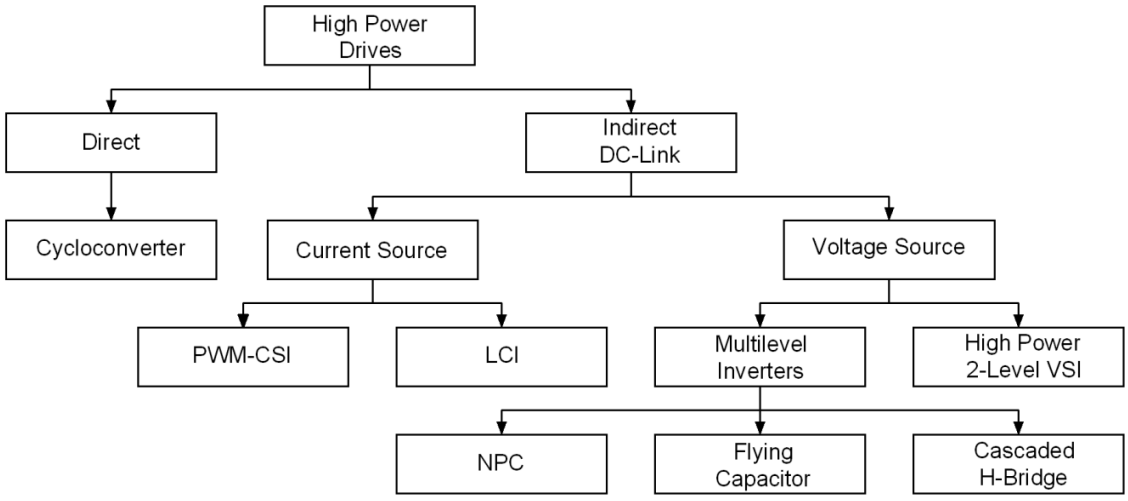


Figure 1-2 – Family of High – Power Converters [**5**]

The type of inverter used in this project is NPC Converter with the schematic from Figure 1-3. As it can be seen, this inverter has the neutral point clamped to the midpoint of the DC link. This configuration uses series IGBTs, thus the stress on the devices is reduced. Furthermore, the NP is used in order to generate at the inverter output three levels of voltage: $\frac{V_{DC}}{2}, 0, -\frac{V_{DC}}{2}$, based on commutation of the twelve switching devices. The combination of these semiconductors allows 27 switching vectors.

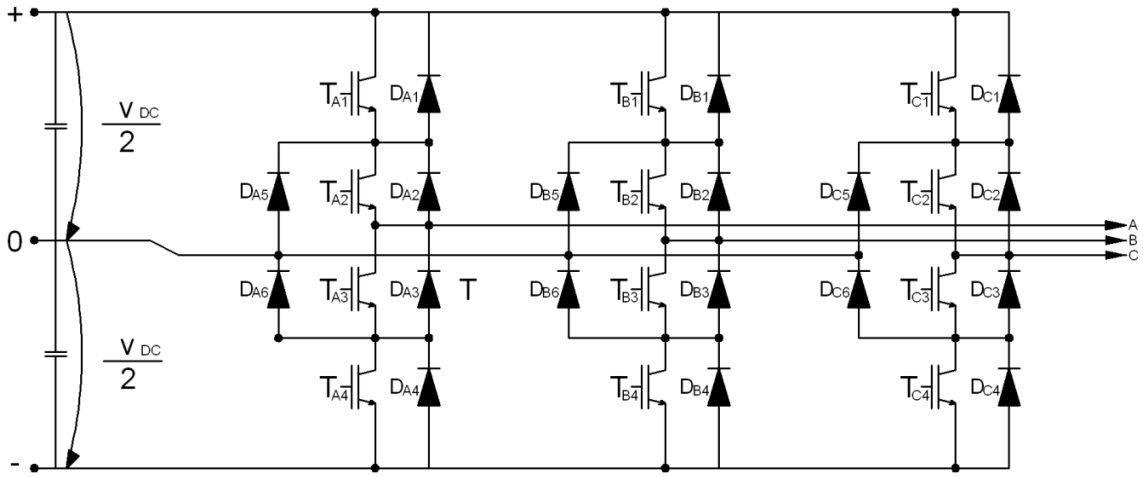


Figure 1-3 – Three-Level NPC Converter Schematic

A three phase inverter provides leg voltages (V_{a0}, V_{b0}, V_{c0}), phase voltages (V_{an}, V_{bn}, V_{cn}) and phase-to-phase voltages (V_{ab}, V_{bc}, V_{ca}). Aside from these voltages, another one appears between the neutral point of the motor and the neutral point of the inverter, acknowledged as common mode voltage (CMV). This voltage can be calculated based on the influence of each switching vector; however the general formula for calculating CMV is presented in [**6**] and can be seen in equation (1-1).

$$V_{\mathrm{N0}} = \frac{V_{A0} + V_{B0} + V_{C0}}{3} \tag{1-1}$$

Based on equation (1-1) it can be noticed that the CMV is created by the switching pattern on each device, thus this voltage can be reduced by using appropriate switching patterns.

The effect of high frequency PWM voltage is generally neglected in the electromagnetic performance of the induction motor. From the motor point of view it needs to be said that there exist small capacitive couplings, however they can be neglected in low frequency analysis. At high frequencies, a low impedance path is created and current flows through the capacitive couplings. As a consequence of high dv/dt applied to the motor, high frequency leakage currents flow through the capacitive couplings created between the stator winding and motor frame. Furthermore, as the motor frame is connected to the ground the high frequency currents may cause electromagnetic interference (EMI) [**7**].

As the semiconductors are improved the switching speed increases making the effect of capacitive couplings to be dominant. Considering this, two important parasitic capacitances can be observed: the one between stator winding – stator iron and stator winding – rotor iron [**8**]. These capacitances in interaction with CMV

and high dv/dt can cause shaft voltage, leading to bearing currents, and leakage currents, which further lead to noise and EMI, in the induction motor [**3**].

The main problems in ASD are CMV and high dv/dt. The two problems cause issues such as [**3**]:

- Grounding currents – circulating between the parasitic capacitance inside the motor and ground
- Shaft voltages – that result in bearing currents
- Conductive and radiated noise
- Overvoltage at motor terminals

There have been developed multiple techniques with the purpose of reducing or eliminating the shaft voltage and CMV. The PWM techniques based can be summarised according to [**3**] as:

- Bearing current reduction methods
- Leakage current mitigation techniques

Three level inverters present advantages such as reduced voltage ratings for the semiconductors, good harmonic spectrum and good dynamic response, that makes them very popular. As disadvantage they have is increased control complexity over conventional VSI [**9**].

1.2. Problem Formulation and Motivation

When referring to three-level Voltage Source Inverters (VSI) it needs to be mentioned that since their invention they have been considered to be used in high capacity, high performance AC drives applications [**10**]. Taking this into account this thesis focuses mainly on the ASD application.

ASD are often used in industrial and household applications, like ventilation system, pumps and electric drives for machine tools. The output speed can be modified through magnitude and frequency of the output voltage by means of PWM [**3**].

Common Mode Voltage (CMV) is defined as the voltage between the neutral point of the inverter and neutral of the wye connected load, and it is generated by the PWM strategies. This type of voltage creates important problems in high switching frequencies. The techniques regarding attenuation of high frequency problems in AC motor drives systems have at base the reduction of CMV. This voltage has a very important influence over the shaft voltage. One important solution for reducing the shaft voltage and leakage current is the reduction of CMV. This can be achieved using two methods [**3**]:

- Attenuation of the shaft voltage through motor design
- CMV attenuation through PWM strategy

Further on, in low frequency analysis these capacitances can be neglected due to their small values, but their effects become important when the switching frequency of the converter is increased as the switching devices are improved. These capacitances offer a flow path for high frequency currents.

One important problem discovered in three – level NPC converter is the balancing of the DC link Neutral Point (NP). This type of inverter is exposed to problems like fluctuations in the NP due to irregular and unpredictable charging and discharging of the upper and lower DC link capacitors [**10**]. As it is defined in literature [**10**] , there is an unbalance regarding the charging and discharging in each capacitor, thus the voltage across the capacitor may rise or fall and the NP voltage will not be able to maintain half of the DC link voltage. Due to this problem a high voltage may be applied to the semiconductors or DC link capacitors causing damage. This can be solved through three methods:

- Separate DC sources [**11**]
- Voltage regulators for each level using an additional small leg [**12**]
- Modified PWM pattern and voltage vector selection [**11**] [**13**]

The main focus of the thesis is to reduce the CMV and to balance the DC link voltage through appropriate PWM strategies due to their cost effectiveness.

1.3. Objectives

The following objectives have to be addressed according to Appendix 1: Project Proposal.

- Development of modulation strategies that address DC link balancing and CMV reduction
  - ❖ Study of classical modulation strategies
  - ❖ Study of DC link unbalance and CMV
  - ❖ Development of simulation model to test different modulation strategies before experimental implementation
  - ❖ CMV Analysis
  - ❖ Analysis of DC link unbalance
- Hardware design of the three-level NPC inverter
  - ❖ Study of NPC converter
  - ❖ DSP implementation of the modulation strategy for the three level converter
  - ❖ Comparison of the emitted common mode EMI from conventional modulations and the developed ones
  - ❖ CMV Analysis
  - ❖ Analysis of DC link unbalance

1.4. Project Limitations

During the development of this project some limitations had to be imposed, due to limited time and/or resources. The main limitations are:

- Only conducted EMI up to 20 MHz– radiated EMI requires special chamber and equipment
- Current <16 A – for analysing the developed modulation strategies this current is enough
- Application – The developed methods are tested only for induction motor adjustable speed drives
- DC link voltage, $V_{DC} = 600\ V$ – for analysis purposes and due to the fact that most wye connected induction motors available in the Aalborg University laboratories have the rated voltage of 380 – 420 V. Hence, the DC link has to be large enough in order to produce the rated voltage: $V_{DC} = \sqrt{2} * V_L = \sqrt{2} * 420 = 593.94 \approx 600\ V$.

2. Neutral Point Clamped Converter

This chapter begins with the general theory regarding the three-level NPC inverter, followed by an introduction into SVM and theory concerning classical modulation strategies. A general simulation structure was developed. Simulation results are presented for further comparison with the proposed modulation strategies. The problems that need to be addressed in this project, DC link balancing and CMV reduction are presented.

2.1. Background of NPC

In the last few years interest in multilevel converters has increased. Different topologies for utility grid and drives have been studied among years. The ability to synthesise waveforms with the improvement in harmonic spectrum and acquirement of higher voltages with a limited maximum device rating made three level inverters suitable for high voltage and high power applications [**14**].

The oldest topology of three level inverters was introduced by Nabae in 1981 [**11**], the neutral point clamped topology. The layout of three level diode – clamped inverter is also called three – level NPC inverter. Compared with two level voltage source inverters this topology has better spectral performance. Multilevel inverters reduce voltage stress on the devices. Bhagwat and Stefanovic improved the spectral structure of output waveforms in multilevel inverters. The original topology with the neutral point clamped has been expanded to higher number of levels. The required voltage blocking capability of the clamping diodes varies with the levels, thus multiple diodes at higher levels may be required [**14**].

According to [**15**] a general comparison between two level and three level inverter can be done. This is presented in Table 2-1.

Table 2-1 – Comparison between two level inverter and three level inverter [**15**]

	Two Level	**Three Level**
Driver	Better	Worst
PWM Algorithms	Better	Worst
DC Link	No difference	No difference
Output Filters	Worst	Much better
THD	Worst	Much better
Current Ripple Losses	Worst	Much better
IGBT Voltage	V_{DC}	$\frac{V_{DC}}{2}$
Losses (switching/conduction)	Much worst	Much better

Multilevel converters supply ingenious methods of series connection of the switches, therefore enabling the processing of voltages that are higher than the device ratings. These converters are effective by means of reduction of harmonic distortion and dv/dt output voltage, thus making the devices useful for utility interface and drives [**16**]. One of the major disadvantages in multilevel inverters is the voltage unbalance between different levels. The output voltage of a three level inverter is a quasi-sinusoidal waveform [**17**].

Problems created by common mode voltages are encountered in conventional two level drives. These voltages are responsible for the shaft voltages and bearing failures, thus both need to be eliminated or reduced within certain bounds. Four leg inverters, passive filters, passive elements with active circuitry and dual bridge inverters have been investigated for reduction of common mode voltages [**3**].

Multi-level inverters can be divided into three main categories based on their topology [**9**]:

- Neutral Point Clamped (NPC)
- Flying Capacitor (FLC)
- H – Bridge

By means of PWM, quasi-sinusoidal waveform can be obtained at the output of the inverter. In order to have a high quality waveform, filtering and high switching frequency is required. Flexibility can be obtained by splitting the DC link voltage in two equal sources [**18**]. Now the output can have the voltage levels: 0 and $\pm\frac{V_{DC}}{2}$. This configuration can be seen in Figure 2-1:

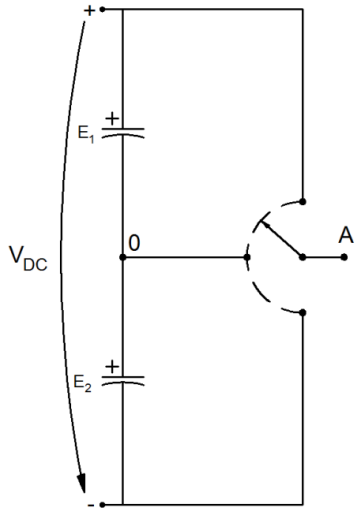


Figure 2-1 – General Inverter Leg

The idea can be expanded in order to obtain a generalized three level inverter that can be seen in Figure 2-2. In order to raise the blocking capacity of conventional two level inverters the switching devices are connected in series. Fast switching devices connected in series that switch simultaneous will generate a high dv/dt at the output terminal of the inverter. The short rise time of the output of the inverter correlated with a long cable is potentially hazardous for the insulation of a motor and for the cable due to the fact that high dv/dt generates partial discharges and as a result the aging of the insulation is accelerated. This phenomenon appears in the motor as leakage current. In motor drives this current leads to electromagnetic

interference noise, thus causing trip of the inverter, problems with the protections of the supply transformer and interference with electronic equipment from the vicinity [**2**].

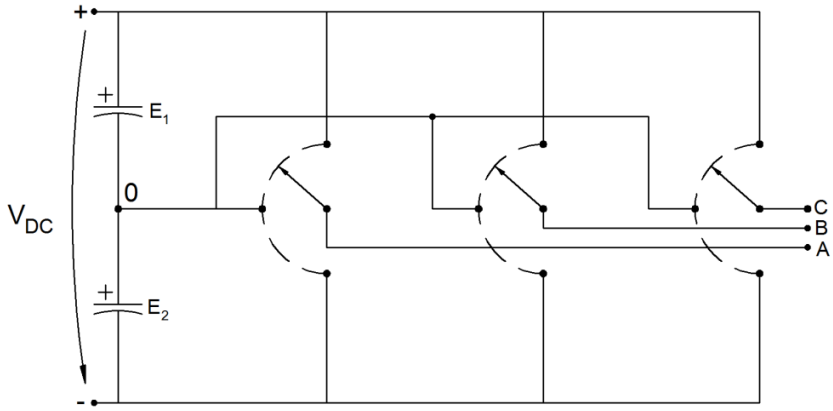


Figure 2-2 – General Three Level Inverter

The switching states can be described using three variables in order to show where each phase leg is connected. The variables are: m_0 for connection to neutral point, m_- for connection to the negative bus and m_+ for connection to the positive bus. These variables are Boolean. Only one of the variables can be on high state for each leg. This property can be written as in equation (2-1):

$$m_0 + m_+ + m_- = 1 \tag{2-1}$$

If the voltages on the DC link capacitors are equal, $E_1 = E_2$ and x is one of the three phases of the load then the leg voltage of the inverter can be written as in equation (2-2):

$$V_{x0} = m_{x+} - m_{x-} \tag{2-2}$$

This results in three possible phase voltages: $\frac{V_{DC}}{2}$, $-\frac{V_{DC}}{2}$ and 0. If x and y are two different phases, the phase to phase voltage can be written as in equation (2-3):

$$V_{xy} = V_{x0} - V_{y0} = \frac{V_{DC}}{2}(m_{x+} - m_{x-} - m_{y+} + m_{y-}) \tag{2-3}$$

Furthermore, five levels of line voltage can be obtained: 0, $\frac{V_{DC}}{2}$, $-\frac{V_{DC}}{2}$, V_{DC} and $-V_{DC}$. The phase voltage is defined as in equation (2-4). If switching variables are introduced in this equation, another equation (2-5) will result.

$$V_{an} = V_{a0} - V_{no} = V_{a0} - \frac{1}{3}(V_{a0} + V_{b0} + V_{c0}) = \frac{2}{3}V_{a0} - \frac{1}{3}V_{b0} - \frac{1}{3}V_{c0} \tag{2-4}$$

$$V_{an} = \frac{V_{DC}}{2}\left(\frac{2}{3}m_a - \frac{1}{3}m_b - \frac{1}{3}m_c\right) \tag{2-5}$$

If the stationary vectors are introduced into equation (2-5) it can be observed that nine voltage levels are created. Furthermore, as the DC link voltage for this project was chosen to be 600 V, those nine levels are $\pm 400, \pm 300, \pm 200, \pm 100, 0$.

To produce AC voltage waveforms with multiple levels, the diode – clamped multilevel inverter employs clamping diodes and cascade DC capacitors. In high power, the configuration used most often is three level neutral point clamped inverter. The most important characteristic of the NPC inverter, in comparison with two level inverters is that in AC output voltage dv/dt and THD is reduced [**19**].

Figure 2-3 presents the layout of a three level NPC inverter. Each inverter leg is composed of four switches with anti-parallel diodes. In real life these diodes are comprised inside the switching device module, if they are IGBTs. A zero DC voltage point is present dividing the DC link in two, which ensures the switching of each phase output to one of three level voltages. The most important benefit of this configuration is that every switching device needs to block only one half of the DC link voltage, but the main problem emphasis that DC link created by the two series capacitors needs to be balanced. A steady-state unbalance at the neutral point can appear due to non-idealities, nonlinearities and transients. For this problem there are two solutions presented [**20**]:

- Connect each capacitor to its own isolated DC source
- Balance of the midpoint by feedback control

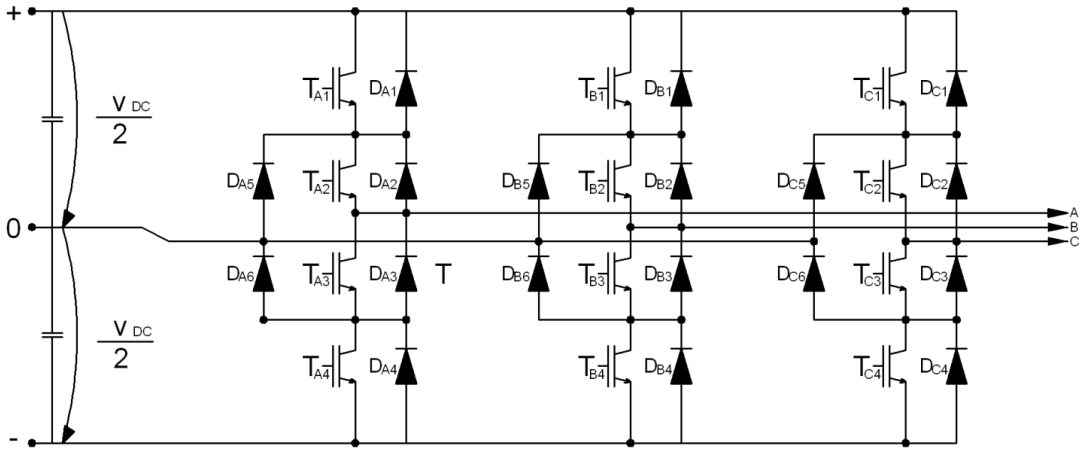
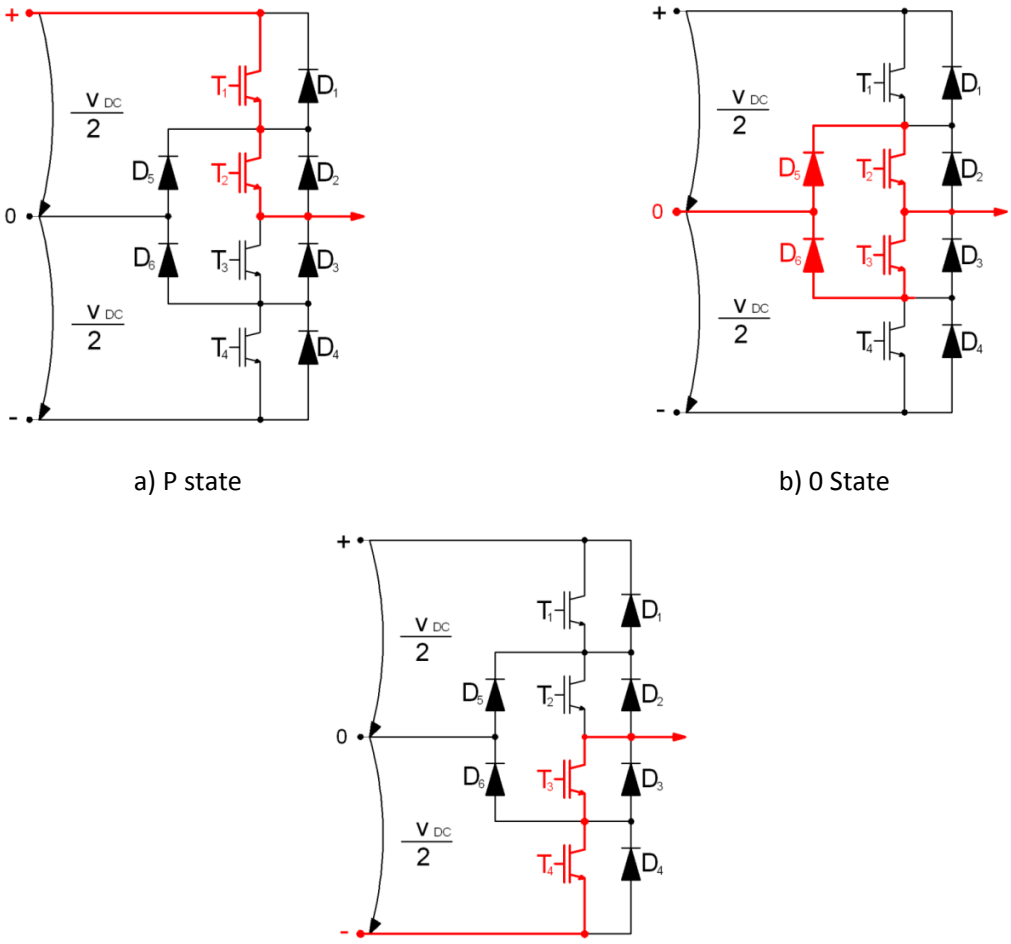


Figure 2-3 – Neutral Point Clamped Inverter Topology

The clamping diodes D_{A5}, D_{A6}, D_{B5}, D_{B6}, D_{C5}, D_{C6} are connected to neutral point. When the switches T_{A1} and T_{A3} are switched on, the inverter output terminal A is connected to the neutral point through one of the clamping diodes D_{A5} and D_{A6}. For a better analysis, one inverter leg is presented in Figure 2-4, representing the inverter states: P, N, 0.

In the switching state P (Figure 2-4a) the upper two switching devices are on and the resulting inverter leg voltage is $+\frac{V_{DC}}{2}$, while in N switching state (Figure 2-4c) the lower two switching devices are on and inverter leg voltage is $-\frac{V_{DC}}{2}$. When the inner two switches T_2 and T_3 are on the inverter leg voltage is 0, hence the switching state 0 (Figure 2-4b). The switches $T_1 - T_3$ and $T_2 - T_4$ operate in a complementary mode [**21**].



a) P state

b) 0 State

c) N State

Figure 2-4 – Switching Paths for NPC Inverter

Considering that the load current i_A is constant during commutation due to inductive load, the DC link capacitors are large enough and that all the switching devices are ideal, the commutation can be analysed [**19**]:

- <u>Commutation when $i_A > 0$</u>

In switching state 0, switches T_1 and T_4 are off and voltage across each one is $\frac{V_{DC}}{2}$. The devices T_2 and T_3 are on and the voltage across them is 0. Furthermore, the clamping diode D_5 is turned on by phase A current, i_A. During dead time δ, T_3 is turned off and load current path remains the same. When T_3 is completely off, the voltage across T_3 and T_4 becomes $\frac{V_{DC}}{4}$.

In switching state P, the first transistor T_1 is on and the clamping diode D_5 is turned off. The load current i_A is commutated from D_5 to T_1. Since T_3 and T_4 were off, the voltage across each one is $\frac{V_{DC}}{2}$.

- Commutation when $i_A < 0$

In switching state 0, the transistors T_2 and T_3 are on and the clamping diode D_6 is turned on by the phase A current, i_A. The voltage across T_1 and T_4 is $\frac{V_{DC}}{2}$. Furthermore, during dead time interval δ, T_3 is turned off. Diodes D_1 and D_2 are turned on and the voltage across T_1 and T_2 is 0 because i_A cannot change direction instantly. The phase A current, i_A, is then commutated from T_3 to the diodes. While T_3 is turned off, the voltage across T_4 will have a maximum of $\frac{V_{DC}}{2}$ due to the diode D_5. Hence, the voltage across T_3 increases from 0 to $\frac{V_{DC}}{2}$ while voltage across T_4 is $\frac{V_{DC}}{2}$.

In switching state P, the first two transistors, T_1 and T_2, are turned on and not affect the operation of the circuit. Even if T_1 and T_2 are on, they do not carry load current due to D_1 and D_2 conduction. The conclusion is that all switching devices sustain half of the DC link voltage during switching P-0, 0-P, N-0, 0-N. Switching P-N is denied because it involves all four switches commutated and the switching losses will be doubled.

Table 2-2 describes the switching states of the NPC inverter leg presented in Figure 2-4. The positive state denotes that the two upper switches are on and the voltage across the output terminal is $\frac{+V_{DC}}{2}$. This voltage is determined with respect to the neutral point 0. The negative state denotes that the two lower switches are turned on with respect to neutral point 0 and the output voltage is $\frac{-V_{DC}}{2}$.

Table 2-2 – NPC Switching States

	T1	**T2**	**T3**	**T4**	**Output phase Voltage**
State P	1	1	0	0	$\frac{+V_{DC}}{2}$
State N	0	0	1	1	$\frac{-V_{DC}}{2}$
State 0	0	1	1	0	0

Some of the most important advantages of diode-clamped multilevel VSI can be summarised as [**17**]:

- If the inverter level increases, the size and weight of harmonic filter decreases and thus, the need for harmonic filter decreases
- High efficiency
- Simple control for a back-to-back system

Electrostatic couplings between the rotor and stator windings produce shaft voltages and voltages between the rotor and the motor frame. These voltages will generate flashovers when the voltage exceeds the dielectric strength of the grease in the bearing [**22**].

One of the most important problems in the control of multilevel converters is the determination of switching angle so that the converter produces the required fundamental voltage and does not generate lower order dominant harmonics.

The main problems in the NPC can be summarised as [**23**]:

- Increased switching frequency in the converters can generate EMI.
- The common mode voltage is generated between the neutral point of the load and the NP of the inverter by means of PWM in the three phase inverter.
- Due to parasitic capacitances in the machine structure, the CMV creates problems such as shaft voltage and bearing currents.

In multilevel inverters CMV can be reduced or eliminated. These types of inverters have a high number of switching states; therefore the output voltage is stepped in small increments. The switching losses are reduced by the mitigation of the harmonics at low frequencies, thus the leakage current is reduced by a lower dv/dt [**2**]. A feasible solution is to eliminate the CMV by PWM techniques

2.2. Classical Modulation Strategies

2.2.1. Background

In the early stages of Voltage Source Inverters (VSI), the operation mode was square wave. Using this type of operation mode the inverter phase and phase – to – phase output voltage has a square wave shape. An important drawback of this operation mode is that the output voltage of the inverter has low order harmonics, such as 5^{th} and 7^{th}, with large magnitude. Regardless of this drawback this operation mode was preferred due to low number of switchings, as the switching devices used in the first inverters had long turn – on and turn – off time, thus the switching losses were high. Utilization of these switches made the switching at high frequency impossible, therefore the square wave operation was preferred [**1**].

Due to increasing development in the semiconductor technology faster switching devices have been developed. In VSI the most used power semiconductors are the IGBTs. These devices have low turn – on and turn – off times, thus reducing switching losses and making switching at high frequency possible. Nowadays, the PWM methods are preferred in three – phase motors due to superior characteristics. In this operation mode low current harmonics are not present, only at inverter switching frequency, and further on current damped by the motor windings [**1**].

In the carrier based PWM method, the power switches are turned on and off according to a carrier period in an appropriate manner in order to generate switch pulse patterns. There are three categories of modulation and control strategies for three level inverters [**5**]:

- Carrier based PWM – is a method based on the comparison of a fundamental sinusoidal waveform with two carrier signals
- Space Vector Modulation (SVM) – is defined by the switching states of the commutation devices
- Selective Harmonic Elimination (SHE) – in this method the commutation devices operate at a very low frequency in order to reduce the losses. The strategy is to control the fundamental frequency and to eliminate the harmonics five and seven.

Recently, more and more modulation strategies are implemented into Digital Signal Processors (DSP). PWM signals have to be calculated in real time, thus significant time is required for computation. When using SVM, the process for calculation is simplified. Therefore the computation time is reduced and better performance can be achieved.

It is known [**24**] that for each carrier-based there is an equivalent SVM and vice-versa. In [**24**] [**25**] [**26**] is concluded that by common-mode injections, an equivalent SVM of carrier-based modulation can be obtained. By selection of proper dwell times for the redundant states, the SVM can provide an equivalent for the carrier-based modulation. The authors choose for this project the Space Vector Modulation.

The SVM determines each switching state of the inverter in the complex $(\alpha\beta)$ space. The phasor rotating at the fundamental frequency is sampled and the three inverter switching states (nearest) are selected with the duty cycles calculated so that the same volt-second average is obtained as in the sampled reference frame. There is a vast research based on modulation strategies as SVM, which became a standard in the industry for the power converters. Park and Kron were the first ones to represent three phase systems in vectorial form [**27**]. Active and zero space vectors represent active and zero switching states. A typical space vector diagram is formed in the SVM hexagon with six equal sectors. Each sector can be divided into four equilateral triangles. This can be seen in Figure 2-5. The centre of the hexagon is represented by the zero vector $\overrightarrow{V_0}$ [**19**].

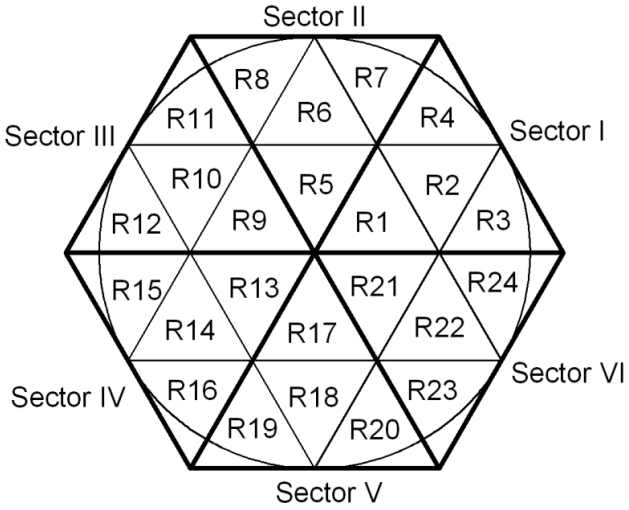


Figure 2-5 – Space Vector Diagram - Sectors and Regions [**19**]

A three phase system defined by $a_x(t), a_y(t)$ and $a_z(t)$ can be represented by a rotating vector $\overrightarrow{a_S}$ from equation (2-6):

$$\overrightarrow{a_s} = \frac{2}{3}\left[a_x(t) + \underline{a}a_y(t) + \underline{a^2}a_z(t)\right] \tag{2-6}$$

$$\underline{a} = e^{j\frac{2\pi}{3}} \tag{2-7}$$

The vectorial form can be obtained after Clarke transformation represented in equations (2-8) and (2-9):

$$\begin{bmatrix} A_\alpha \\ A_\beta \end{bmatrix} = T \begin{bmatrix} a_x \\ a_y \\ a_z \end{bmatrix} \tag{2-8}$$

$$T = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{2-9}$$

The coefficient $\frac{2}{3}$ is used so that the magnitude of the two phase voltages after transformation will have the same magnitude as the three phase voltages [**19**]. Inverse transformation can be obtained as in equation (2-10):

$$\begin{bmatrix} a_x \\ a_y \\ a_z \end{bmatrix} = T^{-1} \begin{bmatrix} A_\alpha \\ A_\beta \end{bmatrix} \tag{2-10}$$

A_α and A_β form a orthogonal two phase system. Furthermore, $\overrightarrow{a_s}$ can be written as in equation (2-11):

$$\overrightarrow{a_s} = a_\alpha + j a_\beta \tag{2-11}$$

Now there is a correspondence between the three phase system and the space vector in the three phase plane, hence some advantages appear:

- The three phase system can be analysed as a whole.
- Properties of a vectorial system can be used. When rotating with ωt the analysis can be made in DC

The voltage space vector in the complex $\alpha\beta$ can be written as in equation (2-12). Furthermore, the voltage phasor is expressed like in equation (2-13).

$$\overrightarrow{v(t)} = v_\alpha(t) + j v_\alpha(t) \tag{2-12}$$

$$\overrightarrow{v(t)} = \frac{2}{3}[v_{A0}(t)(1 + j0) + v_{BO}(t)\left(-0.5 + j\frac{\sqrt{3}}{2}\right) + v_{CO}(t)(-0.5 - j\frac{\sqrt{3}}{2})] \tag{2-13}$$

The exponential form can be written as in equation (2-14).

$$\overrightarrow{v(t)} = \frac{2}{3}[v_{A0}(t)e^{j0} + v_{BO}(t)e^{j\frac{2\pi}{3}} + v_{CO}(t)e^{j\frac{4\pi}{3}}] \tag{2-14}$$

From equation (2-14) the size for each type of vector can be calculated, equations (2-15) – (2-18).

- Zero vector:

$$\overrightarrow{v_{zero}} = \overrightarrow{v_{000}} = \frac{2}{3}\left[0e^{j0} + 0e^{j\frac{2\pi}{3}} + 0e^{j\frac{4\pi}{3}}\right] = 0 \tag{2-15}$$

- Small vector:

$$\overrightarrow{v_{small}} = \overrightarrow{v_{PN0}} = \frac{2}{3}\left[\frac{V_{DC}}{2}e^{j0} + 0e^{j\frac{2\pi}{3}} + 0e^{j\frac{4\pi}{3}}\right] = \frac{1}{3}V_{DC} \quad (2\text{-}16)$$

- Medium vector:

$$\overrightarrow{v_{medium}} = \overrightarrow{v_{P0N}} = \frac{2}{3}\left[\frac{V_{DC}}{2}e^{j0} + 0e^{j\frac{2\pi}{3}} - \frac{V_{DC}}{2}e^{j\frac{4\pi}{3}}\right] = \frac{\sqrt{3}}{3}V_{DC} \quad (2\text{-}17)$$

- Large vector:

$$\overrightarrow{v_{laorge}} = \overrightarrow{v_{PPN}} = \frac{2}{3}\left[\frac{V_{DC}}{2}e^{j0} + \frac{V_{DC}}{2}ee^{j\frac{2\pi}{3}} - \frac{V_{DC}}{2}e^{j\frac{4\pi}{3}}\right] = \frac{2}{3}V_{DC} \quad (2\text{-}18)$$

Space vector modulation is performed in real time and is used to determine the correct duty cycles for the corresponding switching sequences [**18**].

There is a total number of 24 active vectors which can be split in three categories: large, medium and small vectors. There are 6 large vectors, 6 medium vectors, 12 small vectors and 3 additional zero vectors. The midpoint charge is related to the switching vectors [**28**]. Figure 2-6 presents the vectors and their switching states.

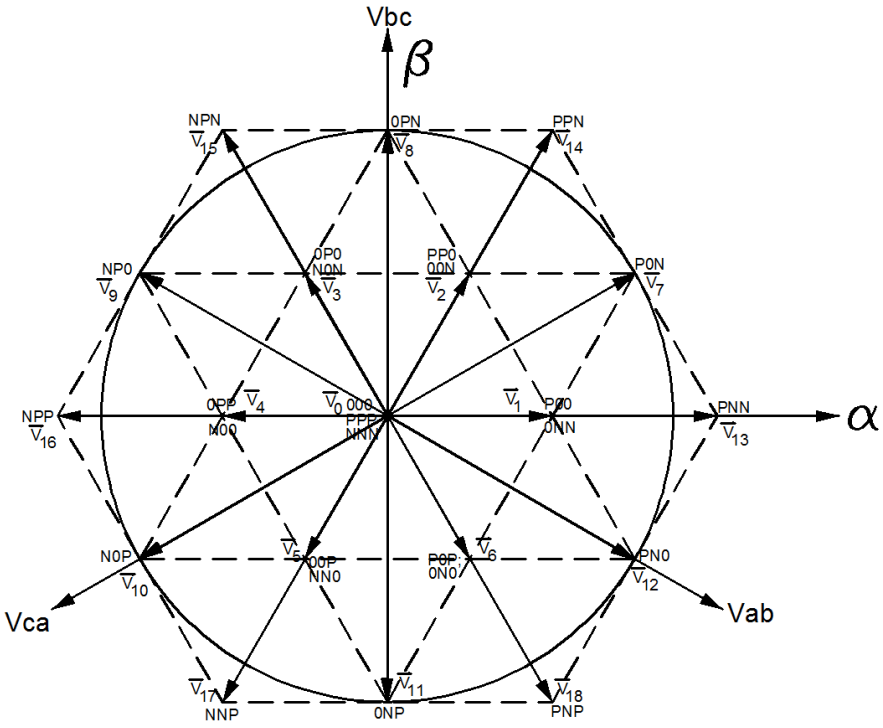


Figure 2-6 – NPC Vectors and Switching States [**28**]

Active and zero vectors are called stationary vectors due to the fact that they do not move in space. The reference vector $\overrightarrow{V_{ref}}$ rotates with the angular speed ω which is proportional with the fundamental frequency f_1 of the inverter, equation (2-19):

$$\omega = 2\pi f_1 \tag{2-19}$$

In $\alpha\beta$ plane the angle between V_{ref} and α axis is, equation (2-20):

$$\theta(t) = \int_0^t \omega(t)dt + \theta(0) \tag{2-20}$$

The twelve small vectors can be split in six sets of two types: N and P. The six sets have same direction and magnitude according to switching combination and will connected to one of the output lines through the upper or lower capacitor. Each set of vectors draw current in the opposite directions from the neutral point. By correct selection of small vectors for the reference vector, the balance can be set.

The medium vectors have one definition per current direction. One of the three output lines is permanently connected to the midpoint. When the reference vector is synthetized with the medium vector the line current flows through the midpoint. If the charge cannot be compensated with small vectors, the compensation is given to the next medium vector because it could have opposite current direction [**28**]. Further, the large vectors does not have direct connection to the neutral point, hence they do not influence it.

Table 2-3 – Space Vectors and Switching States

Vector Magnitude	Vector Type	Space Vector	Switching State	
			P Type	N Type
$\frac{1}{3}V_{DC}$	Small Vector	$\overline{v_1}$	P00	0NN
		$\overline{v_2}$	PP0	00N
		$\overline{v_3}$	0P0	N0N
		$\overline{v_4}$	0PP	N00
		$\overline{v_5}$	00P	NN0
		$\overline{v_6}$	P0P	0N0
$\frac{\sqrt{3}}{3}V_{DC}$	Medium Vector	$\overline{v_7}$	P0N	
		$\overline{v_8}$	0PN	
		$\overline{v_9}$	NP0	
		$\overline{v_{10}}$	N0P	
		$\overline{v_{11}}$	0NP	
		$\overline{v_{12}}$	PN0	
$\frac{2}{3}V_{DC}$	Large Vector	$\overline{v_{13}}$	PNN	
		$\overline{v_{14}}$	PPN	
		$\overline{v_{15}}$	NPN	
		$\overline{v_{16}}$	NPP	
		$\overline{v_{17}}$	NNP	
		$\overline{v_{18}}$	PNP	
0	Zero Vector	$\overline{v_0}$	000	PPP / NNN

A switching state, for example 0NP means that the inverter leg A is connected to the neutral point (0), leg B is connected to negative side (- or N) and the third leg C is connected to the positive side (+ or P).

These methods are based on load currents and the midpoint balance is kept to zero with a small variance, depending on the size of the capacitors. The efficiency of these methods is limited. This problem appears because the midpoint is used as power source. The midpoint problem increases with the level of the converter. The voltage vectors and the switching states are summarized in the Table 2-3:

The reference vector is built based on three stationary vectors. Each of the stationary vectors is applied for a specific time, the dwell time. The dwell time is defined as the duty cycle time of the switches during the modulation sampling period. The volt per second balancing principle is used in order to calculate the dwell times [**19**]. The principle is shown in equation (2-21):

$$\int_0^{T_s} \overrightarrow{V_{ref}} dt = \int_0^{T_a} \vec{V}_{\mathrm{x}} dt + \int_{T_a}^{T_b} \vec{V}_{\mathrm{y}} dt + \int_{T_b}^{T_c} \vec{V}_{\mathrm{z}} dt \quad (2\text{-}21)$$

$$T_s = T_a + T_b + T_c \quad (2\text{-}22)$$

Where:

- T_s is the sampling period
- $\overrightarrow{V_x}$, $\overrightarrow{V_y}$ and $\overrightarrow{V_z}$ are the nearest three vectors from arbitrary sector and region
- T_a, T_b and T_c are the dwell times for the three chosen vectors.

The volt – second balancing principle states that the product of the reference vector with the sampling period equals the sum of the products between the stationary vectors and their corresponding dwell times. This is shown in equation (2-23):

$$\overrightarrow{V_{ref}} T_s = \vec{V}_{\mathrm{x}} T_a + \vec{V}_{\mathrm{y}} T_b + \vec{V}_{\mathrm{z}} T_c \quad (2\text{-}23)$$

Voltage space vectors can also be expressed as:

$$\vec{V} = k V_{DC} e^{j\theta} \quad (2\text{-}24)$$

Where:

- θ is the angle displacement
- k a constant dependent on the vector type

The fundamental output voltage of the inverter is controlled by amplitude modulation index m_a which is defined as in equation (2-25):

$$m_a = \sqrt{3} \frac{V_{ref}}{V_{DC}} \quad (2\text{-}25)$$

The maximum magnitude of V_{ref} is the radius of the largest circle that can be inscribed in the SVM hexagon. Medium vectors have the same length as the maximum V_{ref}.

$$V_{ref,max} = \frac{2}{3} V_{DC} \frac{\sqrt{3}}{2} = \frac{\sqrt{3} V_{DC}}{3} \quad (2\text{-}26)$$

Based on equations (2-25) and (2-26), the maximum modulation index can be calculated:

$$m_{a,max} = \sqrt{3}\frac{V_{ref,max}}{V_{DC}} = 1 \quad (2\text{-}27)$$

The range of modulation index in SVM is in interval [0, 1] if over-modulation is not considered. The maximum phase-to-phase voltage obtained by means of SVM is calculated in equation (2-28):

$$V_{max,SVM} = \sqrt{3}\left(\frac{V_{ref,max}}{\sqrt{2}}\right) = 0.707V_{DC} \quad (2\text{-}28)$$

Where: $\frac{V_{ref,max}}{\sqrt{2}}$ is the maximum RMS value of the fundamental phase voltage.

2.2.2. Nearest Three Vectors with Even Harmonic Elimination

The Nearest Three Vectors with Even Harmonic Elimination (NTV-EHE) method was introduced by D. W. Feng and B. Wu in 2004 [**29**] for compliance with harmonic standards, like IEEE 519-1992, when the converter is used in rectifier mode. The generation of even order harmonics is due to fact that the waveform generated by SVM is not half – wave symmetrical [**29**]. Alternative switching sequences: one starting with N – type vector and the other with P – type vector needs to be used in order to obtain half – wave symmetrical voltage at the output.

The reference vector is synthetized by three stationary space vectors. The stationary vectors are chosen as the nearest three vectors from the region in which the reference vector is found. An example is considered where the reference vector falls in sector I, region 4, as seen in Figure 2-7. The reference vector will be synthetized by $\overrightarrow{V_2}$, $\overrightarrow{V_7}$ and $\overrightarrow{V_{14}}$.

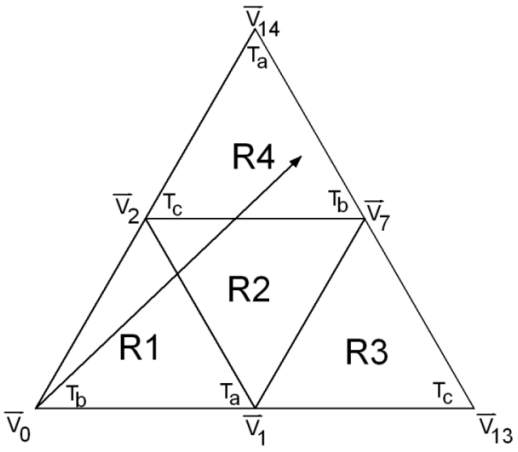


Figure 2-7 – NTV – Stationary and Reference Vectors with Corresponding Dwell Times for Sector I, Region 4

Using volt – second principle and assuming that during T_s the reference vector V_{ref} is constant equation (2-29) can be written.

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_{14}}T_a + \overrightarrow{V_7}T_b + \overrightarrow{V_2}T_c \tag{2-29}$$

The stationary vectors can be summarized as in equation (2-30).

$$\overrightarrow{V_{14}} = \frac{2}{3}V_{DC}e^{j\frac{\pi}{3}} \qquad \overrightarrow{V_7} = \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}} \qquad \overrightarrow{V_2} = \frac{1}{3}V_{DC}e^{j\frac{\pi}{3}} \qquad \overrightarrow{V_{\text{ref}}} = V_{ref}e^{j\theta} \tag{2-30}$$

The dwell times can be calculated by introducing equation (2-30) in (2-29). The result can be seen in equation (2-31).

$$V_{ref}e^{j\theta}T_s = \frac{2}{3}V_{DC}e^{j\frac{\pi}{3}}T_a + \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}}T_b + \frac{1}{3}V_{DC}e^{j\frac{\pi}{3}}T_c \tag{2-31}$$

Equation (2-32) is obtained by transformation of equation (2-31) in polar coordinates.

$$V_{ref}T_s(cos\theta + jsin\theta) = \frac{2}{3}V_{DC}T_a\left(cos\frac{\pi}{3} + jsin\frac{\pi}{3}\right) + \frac{\sqrt{3}}{3}V_{DC}T_b\left(cos\frac{\pi}{6} + jsin\frac{\pi}{6}\right) + \\ + \frac{1}{3}V_{DC}T_c\left(cos\frac{\pi}{3} + jsin\frac{\pi}{3}\right) \tag{2-32}$$

In order to calculate the dwell times, equation (2-32) is divided into real and imaginary part. Together with the switching period, the equation system (2-33) is obtained:

$$\begin{cases} V_{ref}T_scos\theta = \frac{\sqrt{3}}{3}V_{DC}T_a + \frac{\sqrt{3}}{6}V_{DC}T_b + \frac{\sqrt{3}}{6}V_{DC}T_c \\ V_{ref}T_ssin\theta = \frac{1}{3}V_{DC}T_a + \frac{1}{2}V_{DC}T_b + \frac{1}{6}V_{DC}T_c \\ T_s = T_a + T_b + T_c \end{cases} \tag{2-33}$$

By solving equation system (2-33) the dwell times will result as in equation (2-34):

$$\begin{cases} T_a = T_s\left(2\sqrt{3}\frac{V_{ref}}{V_{DC}}sin\theta - 1\right) \\ T_b = T_s\left(2\sqrt{3}\frac{V_{ref}}{V_{DC}}sin\left(\frac{\pi}{3} - \theta\right)\right) \\ T_c = T_s\left(2 - 2\sqrt{3}\frac{V_{ref}}{V_{DC}}sin\left(\frac{\pi}{3} + \theta\right)\right) \end{cases} \tag{2-34}$$

Observing equation (2-34) it can be noticed that $\sqrt{3}\frac{V_{ref}}{V_{DC}}$ is the modulation index, m_a. Using the above calculations the dwell times for the first sector are obtained in Table 2-4 [**19**]:

Table 2-4 – Dwell Times for Reference Voltage in Sector I [**19**]

Region	T_a		T_b		T_c	
1	$\overrightarrow{V_1}$	$T_s\left(2m_a sin\left(\frac{\pi}{3}-\theta\right)\right)$	$\overrightarrow{V_0}$	$T_s\left(1-2m_a sin\left(\frac{\pi}{3}+\theta\right)\right)$	$\overrightarrow{V_2}$	$T_s(2m_a sin\theta)$
2	$\overrightarrow{V_1}$	$T_s(1-2m_a sin\theta)$	$\overrightarrow{V_7}$	$T_s\left(2m_a sin\left(\frac{\pi}{3}+\theta\right)-1\right)$	$\overrightarrow{V_2}$	$T_s\left(1-2m_a sin\left(\frac{\pi}{3}-\theta\right)\right)$
3	$\overrightarrow{V_1}$	$T_s\left(2-2m_a sin\left(\frac{\pi}{3}+\theta\right)\right)$	$\overrightarrow{V_7}$	$T_s(2m_a sin\theta)$	$\overrightarrow{V_{13}}$	$T_s\left(2m_a sin\left(\frac{\pi}{3}-\theta\right)-1\right)$
4	$\overrightarrow{V_{14}}$	$T_s(2m_a sin\theta-1)$	$\overrightarrow{V_7}$	$T_s\left(2m_a sin\left(\frac{\pi}{3}-\theta\right)\right)$	$\overrightarrow{V_2}$	$T_s\left(2-2m_a sin\left(\frac{\pi}{3}+\theta\right)\right)$

The dwell times for each sector can be determined based on Table 2-4 by modifying the angular displacement θ. When calculating the dwell times for other sectors, the angle has to be adjusted so that it falls in the interval $\left[0,\frac{\pi}{3}\right]$. This can be done by extracting a multiple of $\pi/3$ from the actual angle and it is presented in equation (2-35):

$$\theta_n = \theta - \frac{\pi}{3}(n-1) \tag{2-35}$$

Where:

- θ_n is the angle reduced to sector I
- θ is the actual angle
- n is the sector number

The overall requirements for switching sequence design of a three level inverter are [**19**]:

- In one inverter leg, when moving from one switching state to another, only two switches can be used in complementary mode
- When moving from one sector to another there should be a minimum number of switchings
- Neutral point voltage deviation should be minimum

The dwell time between two opposite small vectors can be equally distributed in order to minimise the neutral point voltage deviation. There are two cases that need to be investigated regarding the position of the reference vector inside a sector:

- One small vector in the nearest three vectors – case 1
- Two small vectors in the nearest three vectors – case 2

Case 1 - the reference vector in sector I can be in region 3 or 4, as shown in Figure 2-8:

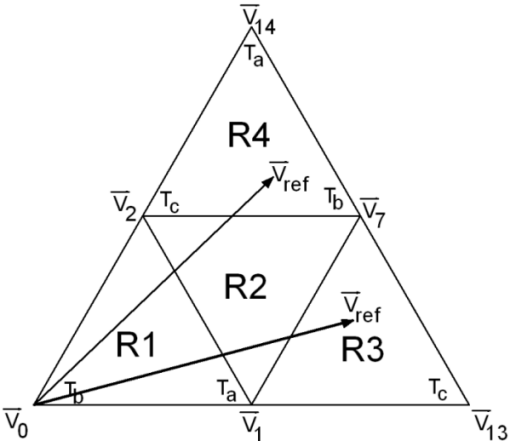


Figure 2-8 – Feasible Regions for Case 1

In order to minimize the NP voltage deviation, the dwell time for the small vector should be equally distributed between P and N type states [**19**]. A typical seven segment switching sequence is shown in Figure 2-9. From the switching sequence the following conclusions can be drawn:

- The sampling period equals the sum of all dwell times
- Only two switches are used in complementary mode
- Dwell time T_c for $\overrightarrow{V_2}$ is equally distributed between P and N type states, thus minimizing the NP voltage influence
- The device switching frequency is half of the sampling frequency due to the fact that in each inverter leg there are only two switchings on each sampling period.

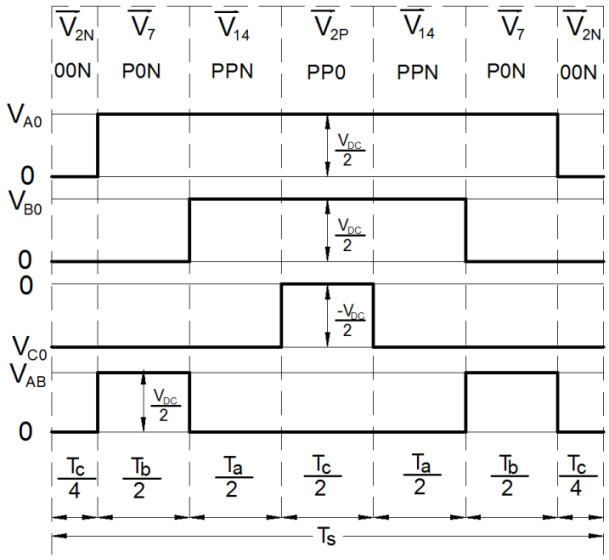


Figure 2-9 – Seven Segment Switching Sequence for $\overrightarrow{V_{ref}}$ in Sector I, Region 4 [**19**]

Case 2 – the reference vector in sector I can be in region 1 or 2. The region in which the reference vector is found is split in two sub-regions. Depending on which sub-region the reference vector is found, it will be

closer to one of the two small vectors. This will be the dominant small vector as it has the highest effect in the NP voltage. The dominant vectors dwell time is distributed equally between its N and P type states. An example can be seen in Figure 2-10:

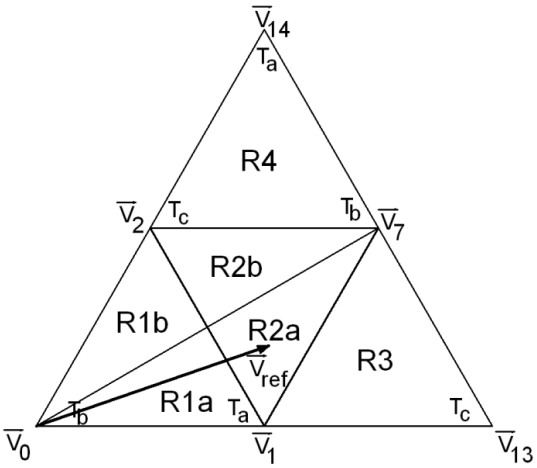
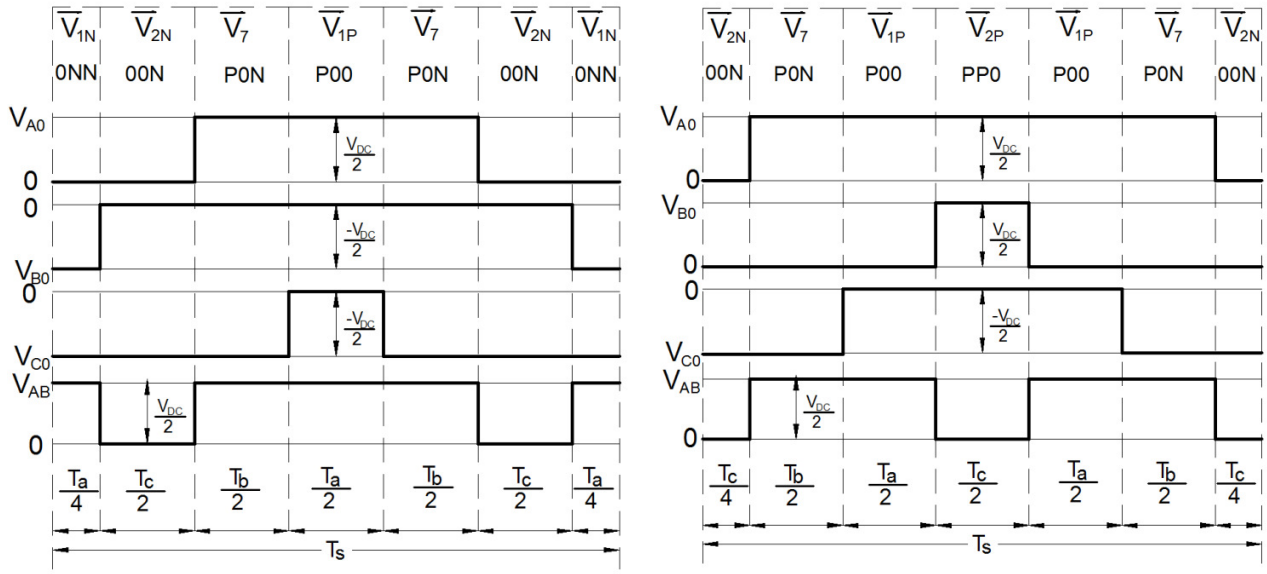


Figure 2-10 – Division of Region 2 in Sector I for Minimization of NP Voltage Deviation

Based on Figure 2-10 observations can be made:

- Transition between the two sub-regions implies an extra switching
- The average switching frequency is increased because of six extra switches in each fundamental switching period. The extra switching requires only two devices

The seven switching sequence for region 2a and 2b are shown in Figure 2-11:



$\overrightarrow{V_{ref}}$ in Region 2a

$\overrightarrow{V_{ref}}$ in Region 2b

Figure 2-11 – Seven Segment Switching Sequences for $\overrightarrow{V_{ref}}$ in Sector 1, Region 2a and 2b

Most standards, such as IEEE 519-1992, are very restrictive regarding THD in even harmonics. The NTV switching sequences can be altered in order to cancel phase-to-phase even harmonics from the voltage waveform.

Switching sequences can be split in two categories:

- Type A – the sequence starts with N type small vector
- Type B – the sequence starts with P type small vector

In classical SVM, only A type sequences are used. In order to force the phase-to-phase even harmonics to cancel, A and B types of switching sequences have to be alternated as shown in Figure 2-12.

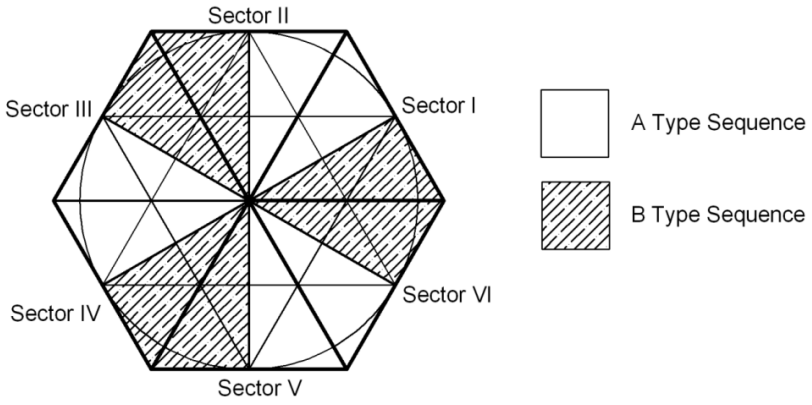
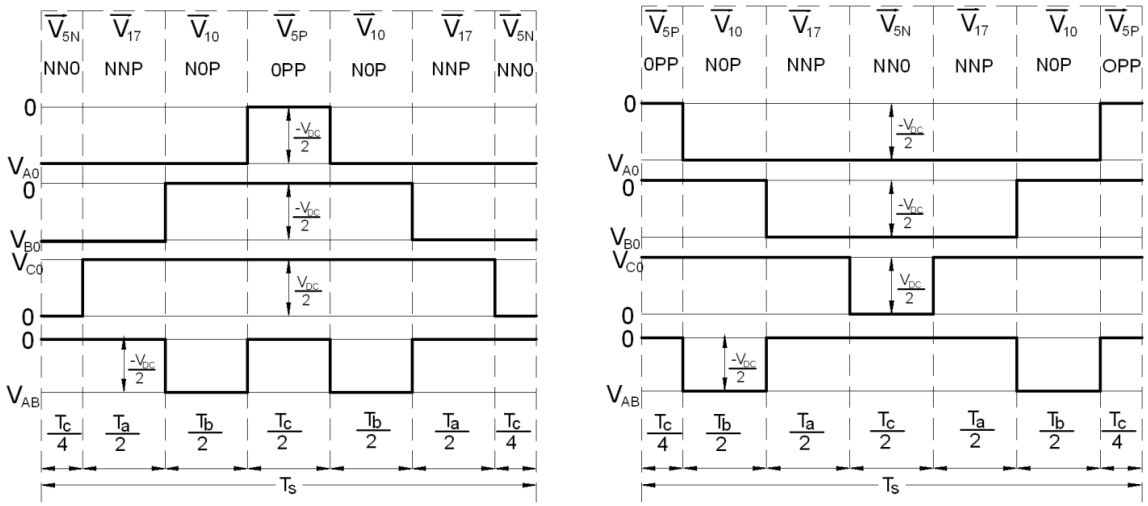


Figure 2-12 – Alternation of A and B Switching Sequences for Even Harmonic Elimination [**29**]

The requirement for even harmonic elimination is that the phase-to-phase voltage waveform is half wave symmetrical. Consider that the reference voltage vector is situated in sector I, region 4, as in Figure 2-9. The opposite half wave is reached when the reference vectors is situated in sector IV, region 4, as seen in Figure 2-13a.



a) Default A Type Switching Sequence b) Modified B Type Switching Sequence

Figure 2-13 – Switching Sequence when $\overrightarrow{V_{ref}}$ is situated in Sector IV, Region 4.

In order to gain symmetry, the switching sequence in sector IV, region 4 has to start with a P type small vector. The modified sequence can be seen in Figure 2-13b. The phase voltages appear to be different in Figure 2-13, the only difference is an offset of $\frac{T_s}{2}$ between the a) and b) variants of the switching sequence.

It can be observed that $V_{AB}(\omega t)$ from Figure 2-13a equals$-V_{AB}(\omega t + \pi)$ from Figure 2-13b, as the sequences are 180 degree apart. A minor increase in the switching frequency can be observed compared with conventional NTV method [**19**]. The increase is due to extra switching required to alternate between A and B type sequences.

In order to validate the theory presented here and to develop new modulation strategies a base model was built using Matlab/Simulink R2011b and Plecs. The inverter model was divided into two main parts: the electronic part, consisting in switching devices, and the control one. In order to facilitate the DSP implementation, the modulation strategy was developed in Matlab code. The switching devices were modelled using Plecs toolbox. The general structure is presented in Figure 2-14. For a better control of the modulation strategy few input parameters have been chosen:

- Reference voltage, V_{ref}
- Simulation time
- Output frequency, f
- Switching time, T_s
- Deadtime, dt

The outputs of the Control block are the gate signals. These signals are fed to the Inverter block through the dead time generator, together with the DC link voltage.

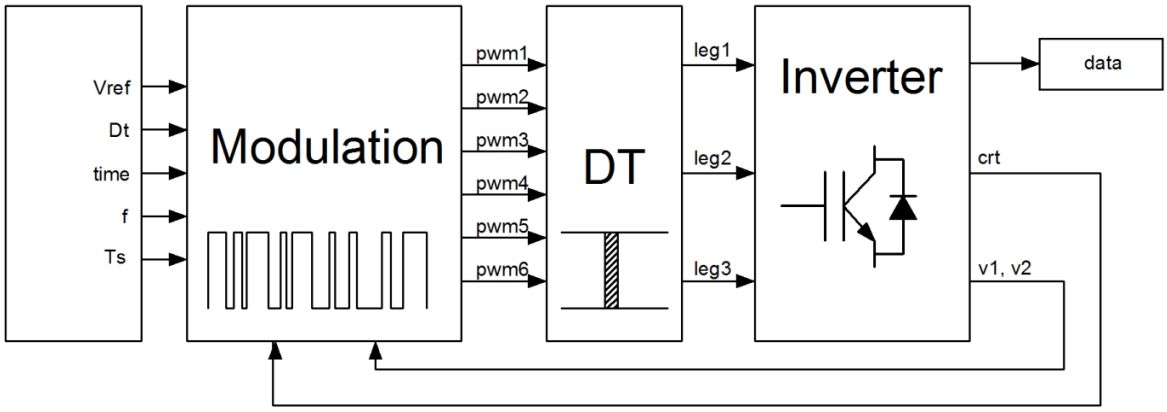


Figure 2-14 – General Structure of NPC Converter Developed in Matlab/Simulink and Plecs

In order to analyse the modulation strategy the following parameters were saved:

- DC link voltage
- DC link current
- CMV
- Inverter leg voltages (V_{a0}, V_{b0}, V_{c0})
- Inverter phase voltages (V_{an}, V_{bn}, V_{cn})

- Inverter phase – to – phase voltages (V_{ab}, V_{bc}, V_{ca})
- Inverter currents (I_a, I_b, I_c)

The main conditions in which the simulations were performed are:

- DC link voltage of 600 V
- Switching frequency of 4 kHz
- Fundamental frequency of 50 Hz
- Dead time of 2 µs
- Six DC link capacitors with the configuration presented in chapter 4.2
- Load of 7.5 kW modelled as in chapter 4.2

The general structure for the developed modulation strategies is presented in Figure 2-15. First the input parameters have to be set, followed by the definition of the stationary vectors and switching table. Next a decision has to be done regarding neutral point balancing. If the method has the ability to balance the neutral point, and it is needed, the switching sequence for balancing is chosen otherwise the default one. If the method does not have NP balancing and it is needed a fault will be triggered, otherwise the default is selected. After choosing the output switching sequence the dwell times are calculated and the PWM signals are generated.

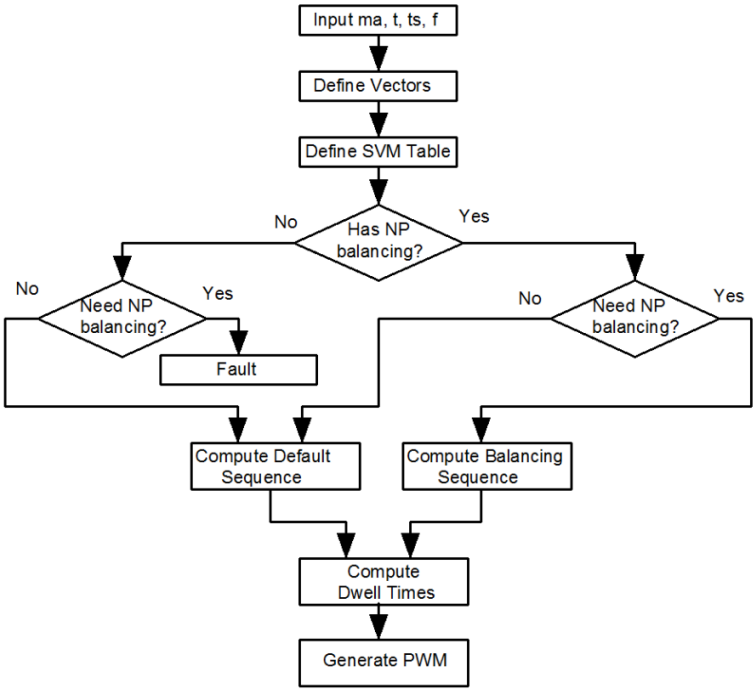


Figure 2-15 - Modulation Strategy Structure for Simulation Model

In order to validate the proposed simulation model, the results of NTV-EHE implementation are analysed. Simulations at maximum modulation index were performed. Figure 2-16 presents the output currents in steady state. The RMS value of current on a phase is 12.11 A.

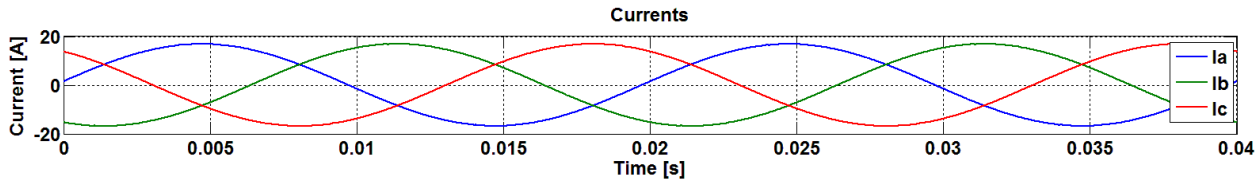


Figure 2-16 – Output Current for NTV-EHE at $m_a = 1$ – Simulation

The leg voltage is defined as the voltage drop between one leg and the neutral point of the inverter, Figure 2-17. This voltage can have only three levels: $\frac{V_{DC}}{2}, 0, -\frac{V_{DC}}{2}$, due to the direct connection to the positive, negative or midpoint of the DC link. Hence, the limits for the leg voltage are +300 V, -300 V and 0 V.

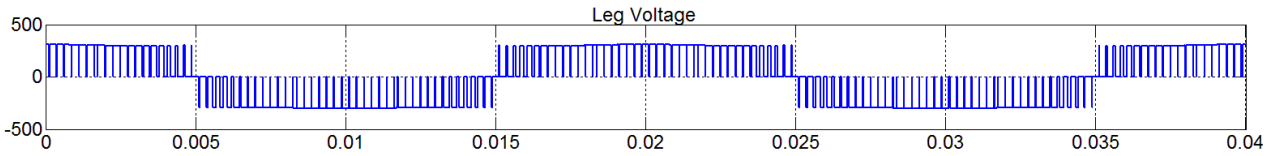


Figure 2-17 – Leg Voltage for NTV-EHE at $m_a = 1$ – Simulation

Figure 2-18 presents two fundamental periods of phase voltage, phase-to phase voltage, CMV and DC link voltages. The first waveform from Figure 2-18 presents the phase voltage, defined as the voltage drop between one inverter leg and neutral point of the load with wye connection, V_{an}. As can be seen this voltage is quasi-sinusoidal and has nine voltage levels $\pm 400, \pm 300, \pm 200, \pm 100, 0$. The second waveform from Figure 2-18 represents the phase-to-phase voltage, which has five voltage levels $\pm 600, \pm 300, 0$. The total harmonic distortion in this voltage is 26.73 [%]. Furthermore, the CMV for this method is presented in the third waveform from Figure 2-18 and it is defined as the voltage drop between the neutral point of the wye connected load and the neutral point of the DC link. As can be seen there are three voltage levels $\pm 200, \pm 100, 0$ with a fundamental period of 150 Hz. An analysis of this voltage will be performed in subchapter 5.9.

When referring to DC link voltage there has to be mentioned that this method has the ability of natural balancing. The voltage on the upper capacitor fluctuates between approximately 294 V and 308 V as for the lower capacitor the voltage is between 291 V and 306V at maximum modulation index.

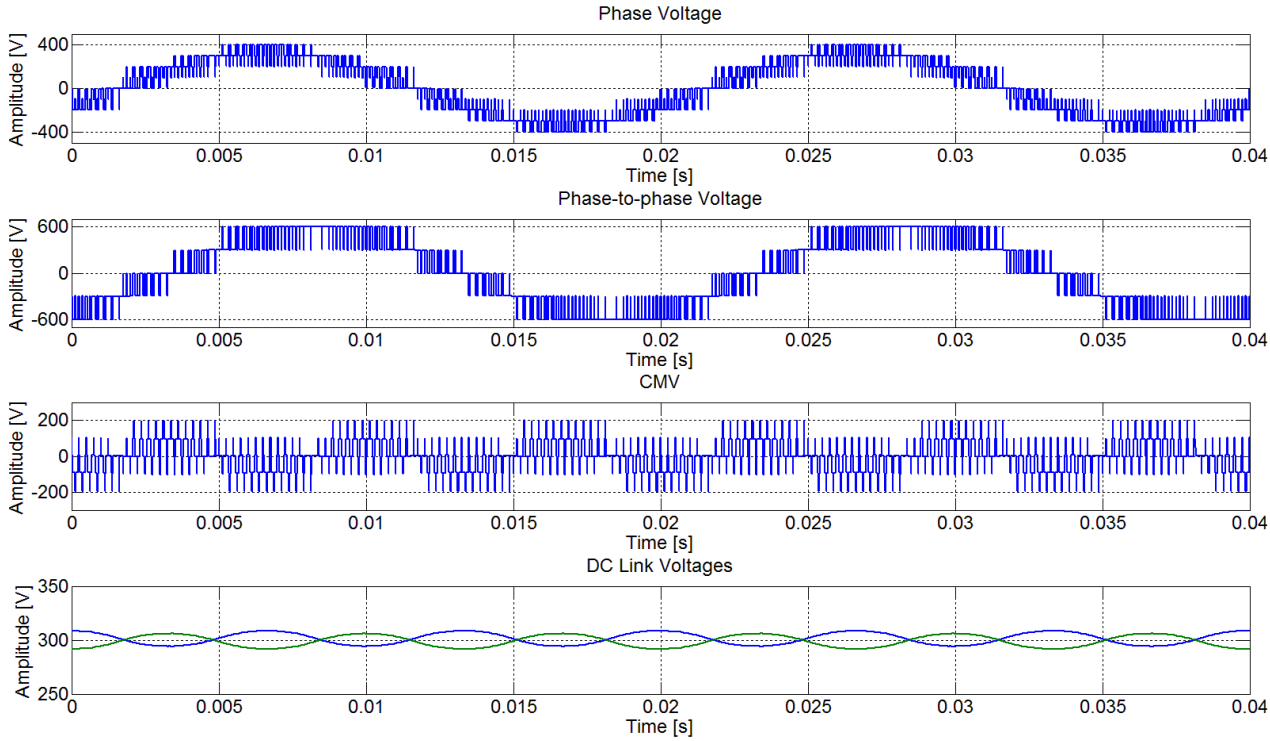


Figure 2-18 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for NTV-EHE at $m_a = 1$ - Simulation

The active switching frequency per device is different than the sampling frequency. If D_{sw} is the number of devices which perform a commutation, D_{Total} is the total number of switches, f_s is the sampling frequency, f_1 is the fundamental frequency and $S_{on,off}$ is the number of on/off and off/on switchings. The average active device switching frequency for NTV can be calculated as:

$$\frac{D_{sw1}}{D_{Total}} f_s + \frac{D_{sw2}}{D_{TOTAL}} \frac{S_{on,off}}{2} S_{ext} f_1 = 2.025\ kHz \tag{2-36}$$

Only six of the twelve transistors switch on and off per sampling frequency. Ignoring extra switching, for a 4 kHz sampling frequency there would result a 2 kHz active device frequency, due to the fact that when passing from region 1a to 1b or 2a to 2b, there is an extra switching, the 2 kHz is slightly increased. Per each fundamental period, there are six extra switchings which involve four devices out of twelve. The switching involves only on/off or off/on transition, hence the number of switches is divided by 2. The resulting frequency of 2.025 kHz is the average active switching frequency per IGBT.

2.2.3. Zero Common Mode Method

The Zero Common Mode Method (ZCM) was first introduced by Haoran Zhang and Annette von Jouanne in 2000 [**30**]. This method uses the six active middle vectors and one zero vector due to their ability to create zero common mode voltage as long as the DC link is balanced. These vectors can be seen in Figure 2-19.

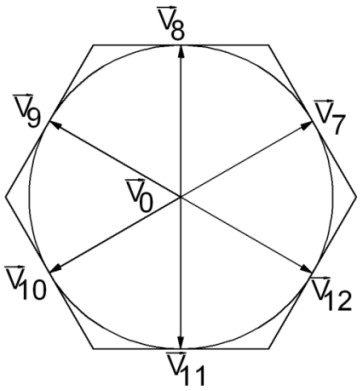


Figure 2-19 Switching Vectors for Zero Common Mode Method

As can be seen in Figure 2-19 the sectors need to be redefined compared with NTV-EHE, therefore the first sector is between $\overrightarrow{V_7}$ and $\overrightarrow{V_{12}}$. Based on this rearrangement and together with volt-second principle the dwell times for the first sector can be calculated, (2-37):

$$\overrightarrow{V_{ref}} \cdot T_s = \overrightarrow{V_{12}} \cdot T_a + \overrightarrow{V_7} \cdot T_b + \overrightarrow{V_0} \cdot T_c \tag{2-37}$$

Where:

- T_a – dwell time for vector $\overrightarrow{V_{12}}$
- T_b – dwell time for vector $\overrightarrow{V_7}$
- T_c – dwell time for vector $\overrightarrow{V_0}$

The stationary vectors for this method can be summarised as in equation (2-38)

$$\overrightarrow{V_{12}} = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{11\pi}{6}} \qquad \overrightarrow{V_7} = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} \qquad \overrightarrow{V_0} = 0 \tag{2-38}$$

Introducing equation (2-38) in (2-37) it will result into equation (2-39).

$$V_{ref} e^{j\theta} T_s = \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{11\pi}{6}} T_a + \frac{\sqrt{3}}{3} V_{DC} e^{j\frac{\pi}{6}} T_b \tag{2-39}$$

Dividing equation (2-39) into real and imaginary part and transforming it into polar coordinates the system of equations (2-40) will be obtained:

$$\begin{cases} V_{ref}T_s cos\theta = \frac{1}{2}V_{DC}T_a + \frac{1}{2}V_{DC}T_b \\ V_{ref}T_s sin\theta = -\frac{\sqrt{3}}{6}V_{DC}T_a + \frac{\sqrt{3}}{6}V_{DC}T_b \\ T_s = T_a + T_b + T_c \end{cases} \quad (2\text{-}40)$$

By solving (2-40) the dwell times are obtained as in (2-41):

$$\begin{cases} T_a = 2T_s \frac{V_{ref}}{V_{DC}} sin\left(\frac{\pi}{3} - \theta\right) \\ T_b = 2T_s \frac{V_{ref}}{V_{DC}} sin\theta \\ T_c = T_s - T_a - T_b \end{cases} \quad (2\text{-}41)$$

If the angular displacement is modified in such a manner that falls into the first sector the dwell times are valid for the other sectors. By the use of zero and medium vectors the modulation index will be decreased [**29**]. The maximum amplitude for the reference voltage is described in equation (2-42):

$$V_{ref,max} = \frac{\sqrt{3}}{3}V_{DC}\frac{\sqrt{3}}{2} = \frac{V_{DC}}{2} \quad (2\text{-}42)$$

The maximum modulation index for this method is presented in (2-43):

$$m_{a,max} = \sqrt{3}\frac{V_{ref,max}}{V_{DC}} = \sqrt{3}\frac{\frac{V_{DC}}{2}}{V_{DC}} = \frac{\sqrt{3}}{2} = 0.866 \quad (2\text{-}43)$$

Due to the fact that in this method there are no redundant states and the transition between two adjacent states involves two inverter legs, the harmonic content is increases [**31**]. This method does not follow the rule regarding the transition between two switching states. Figure 2-20 presents the switching sequences for the first sector in the ZCM method.

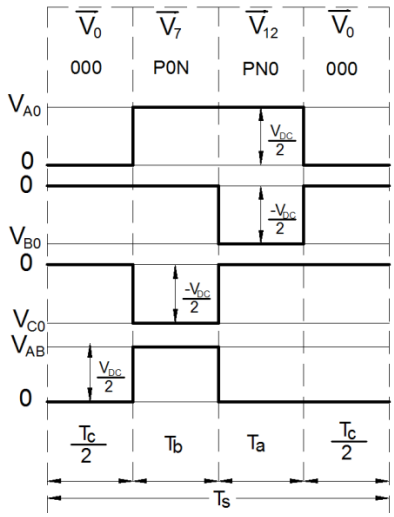


Figure 2-20 – Switching Sequence for the First Sector in ZCM Method

In order to test this modulation strategy, simulations were performed. The simulation structure presented in Chapter 2.2.2 was used. Simulations at its maximum modulation index, $m_a = 0.866$, were done.

Figure 2-21 presents two fundamental periods from phase voltage, phase-to phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, V_{an}. As can be seen this voltage is very similar with the output of a two level voltage source inverter, due to the fact that this strategy does not use all the vectors. Hence, the phase voltage levels are $\pm 300, 0$. The second waveform from Figure 2-21 is the phase-to-phase voltage, which has five voltage levels $\pm 600, \pm 300, 0$ as NTV-EHE. The total harmonic distortion in this voltage is $52.23\ [\%]$. Furthermore, the CMV for this method is presented in the third waveform. As it can be seen CMV has three voltage levels $\pm 100, 0$ (when deadtime is introduced) with a fundamental period of 150 Hz. As at NTV-EHE, a more specific analysis will be performed in subchapter 5.9.

By the use only of medium and zero vectors this method has the ability to self-balance. In steady state the voltage on the upper capacitor varies between approximately 296 V and 309 V as for the lower capacitor the voltage is between 292 V and 304V, at maximum modulation, $m_a = 0.866$.

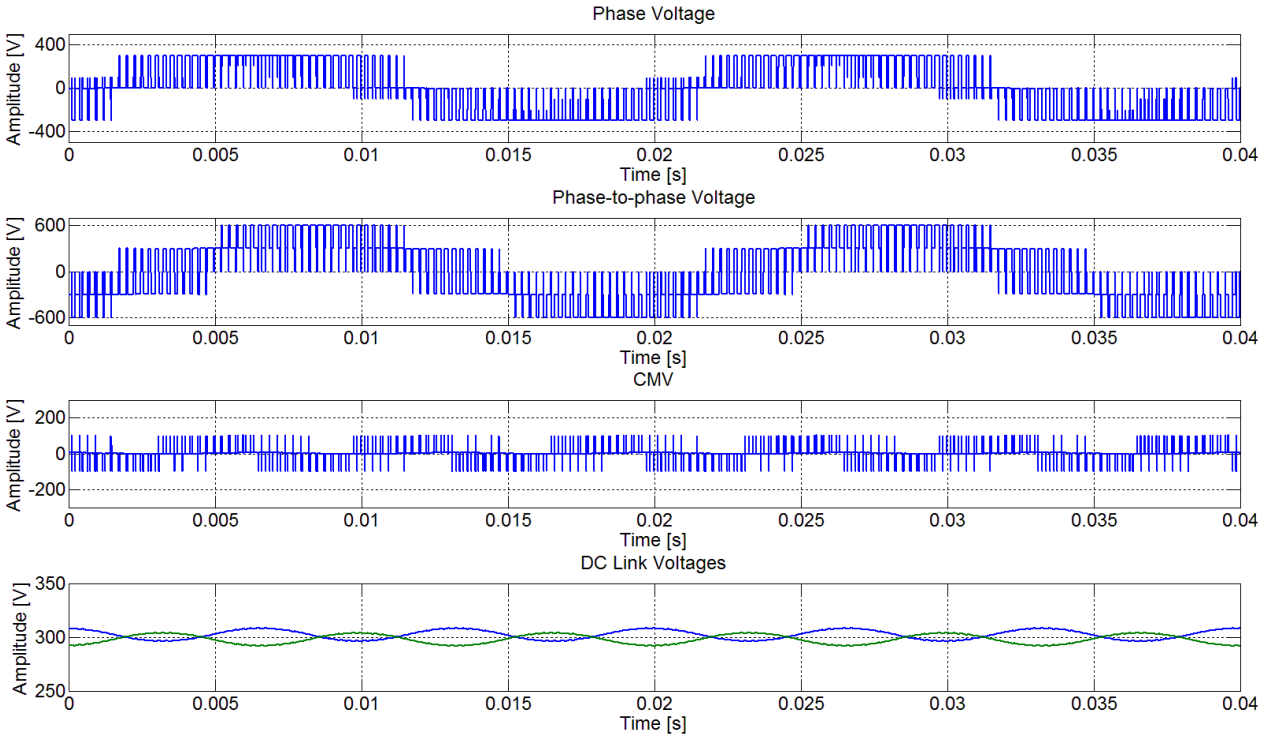


Figure 2-21 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for ZCM at $m_a = 0.866$ - Simulation

As described at NTV-EHE the active switching frequency per device can be calculated. For this method this frequency is 2 kHz, due to the fact that there are no extra switchings.

2.3. DC Link Balancing

The voltage deviation problem is inherent to all three level NPC converters [**32**]. Neutral point voltage deviation implies that any current flowing through the NP of a three level inverter would cause the charging of one of the capacitors and the discharging of the other. The effect is that the output voltage becomes asymmetric. The unbalance problem does not appear in two level inverters or in three level inverters with separate DC sources [**18**].

From the total of 27 vector combination, 18 produce neutral point voltage deviation [**32**]. The zero and the large vectors have no influence on the neutral point. Aside from this, the voltage deviation can have more causes [**18**]:

- The capacitors have different parameters
- DC link capacitor failure
- Switching devices have different parameters
- Non-linear and unbalanced loads

By not taking care of the DC link voltage deviation the following problems can occur [**18**]:

- Premature failure of the switching devices because the voltage increases above $\frac{V_{DC}}{2}$
- THD increase due to asymmetric supply
- The terminal with lower voltage will limit the modulation ratio
- The inverter will become unable of synthetizing the output voltage in case of a major DC link voltage deviation

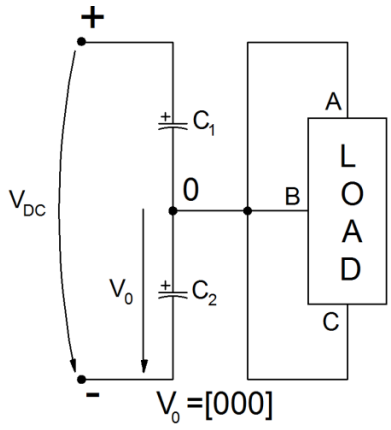
The effect of some switching states determines the AC currents to flow in and out the NP. These currents will generate a ripple in the NP voltage and low order harmonics. Without caring about the NP balancing, the DC link capacitors and the switching devices are prone to destruction [**32**].

The DC current ripple is important for the size determination of the DC link capacitors as they suppress the PWM current ripple. For the analysis of the DC link current ripple performance, K_{DC} factor is defined which is the squared ratio of DC link ripple RMS over the output phase current RMS [**1**]. This can be seen on equations (2-44) and (2-45):

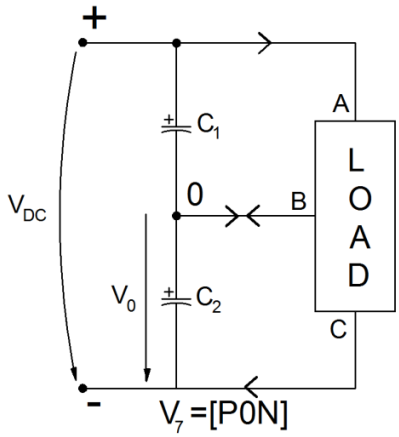
$$K_{DC} = \left(\frac{I_{DCR-RMS}}{I_{PH-RMS}}\right)^2 \tag{2-44}$$

$$I_{DCR-RMS}{}^2 = I_{DC-RMS}^2 - I_{DC-MEAN}^2 \tag{2-45}$$

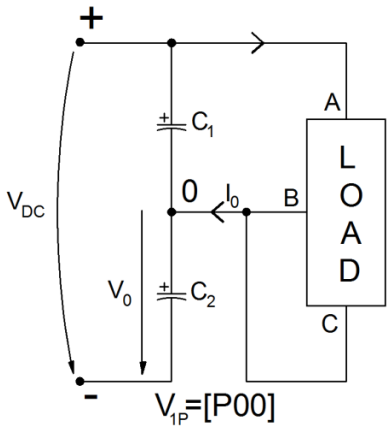
For a longer capacitor life and smaller size requirements, the K_{DC} variable has to be small. When the ASD runs at full load at rated current, the K_{DC} will be small. At no load and small currents the DC link current ripple, K_{DC}, will have higher values. The influence of each type of vector can be seen in Figure 2-22.



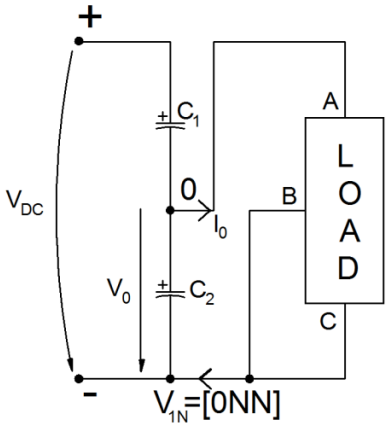
a) Zero Vector



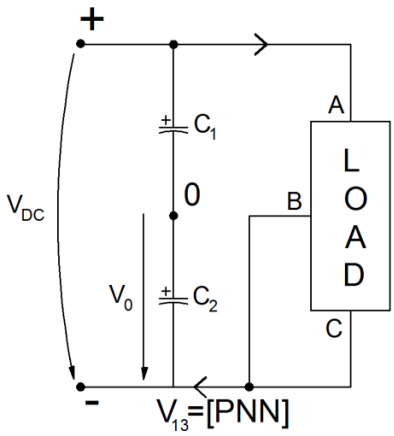
b) Medium Vector



c) P Type Small Vector



d) N Type Small Vector



e) Large Vector

Figure 2-22 – Space Vectors Influence on the NP Current

When the inverter uses the zero vector with 000 configuration, all three inverter legs are connected to the midpoint of the DC link, Figure 2-22a, thus the switching states do not affect V_0. Figure 2-22b describes how the medium vector influences the neutral point. For a better understanding one medium vector was chosen, V_7. As can be seen in Figure 2-22b each of the inverter legs are connected to one of the load terminals: the positive side of the DC link is connected to the A terminal, the neutral point is connected to B terminal and negative side of the DC link is connected to C terminal. The voltage across the lower capacitor may increase or decrease depending on the operating conditions of the inverter [**19**].

The small vectors have an important influence on the neutral point. The P type vector causes an increase in the voltage across one capacitor and the N type vector a decrease. This is due to the fact that for P type vectors, one of the load terminals is connected to the positive DC link, respectively negative DC link for N type vectors. As an example the V_1 small vector was chosen. Its influence can be seen in Figure 2-22c for P type small vector, and Figure 2-22d for N type small vector [**19**].

When talking about large vectors it can be noticed that each of the load terminals are connected to the positive or negative DC link, never at the neutral point. Hence, these types of vectors do not influence the neutral point. Figure 2-22e presents the V_{13} large vector. As it can be seen the A terminal of the load is connected to the positive DC link and B and C terminals to the negative DC link [**19**].

2.4. Common Mode Voltage

2.4.1. Common Mode Voltage in Adjustable Speed Drives

Electric machines are an important part of the industry. Most motors are controlled by variable frequency drives. These drives generate high frequency noise in current and voltage. This noise can follow the paths [**33**]:

- To the load
- To the supply
- Shaft through the motor bearings

When applying PWM to a three phase inverter a voltage is generated between neutral point of the wye connected load and NP of the inverter. This voltage is known as common mode voltage and acts like a source for many unwanted problems in motor drives such as shaft voltage and bearing currents due to parasitic capacitances that exists in the motor structure [**23**] [**34**].

The switching operation of the inverter generates common mode voltages. From this point of view the common mode voltages are defined as being the zero – sequence voltages overlapped with noise generated by switching. If the magnitude is not reduced the motor phase – to – ground voltage can be substantially increased, thus leading to premature failure of motor winding insulation. As a result, the life of the motor is shortened. In medium voltage, motors need to be protected against common mode voltages, if they are not,

the cost of the damaged motor will increase the cost of production [**19**]. The CMV path can be seen in Figure 2-23.

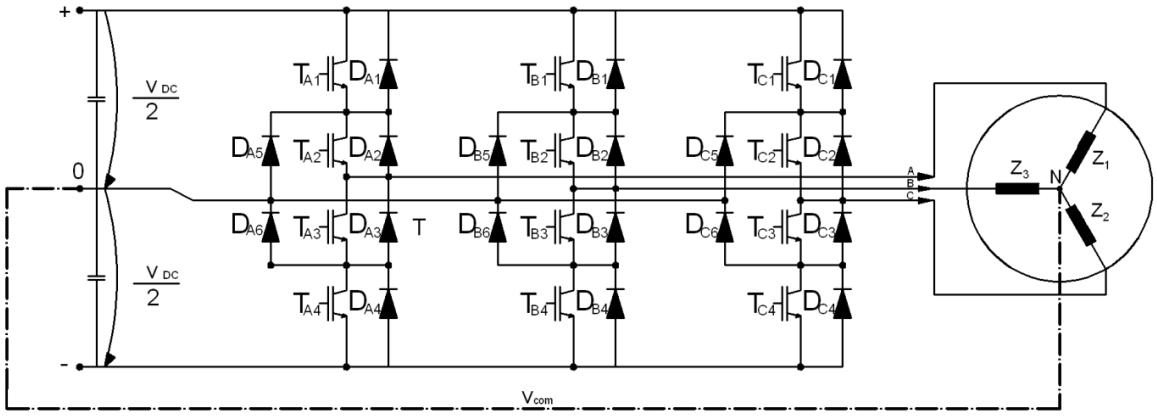


Figure 2-23 – Common Mode Voltage Path

The parasitic capacitance between the stator winding and the rotor can be changed by changing the design parameters while other capacitances cannot be changed that easily. Also, shaft voltage will be higher on an increased stator slot tooth [**6**].

The parasitic capacitances between the stator winding, rotor and motor frame is presented in Figure 2-24. The capacitances are:

- C_{wf} – equivalent capacitance between motor windings and motor frame
- C_{wr} – capacitance between the stator windings and rotor
- C_{rf} – capacitance between rotor and motor frame
- C_b – bearing capacitance

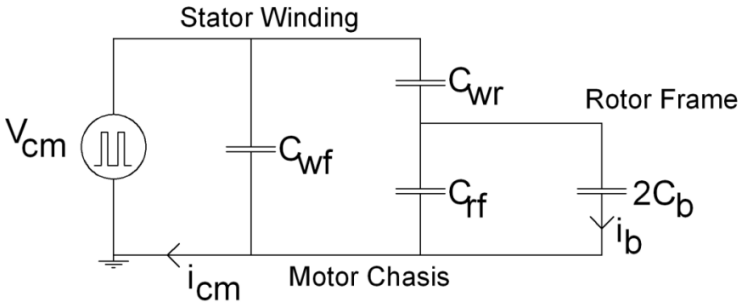


Figure 2-24 – Parasitic Capacitances [**1**]

In Figure 2-24 I_{cm} describes the overall leakage current flowing from the motor frame to ground and i_b is the bearing current. In practice the bearing currents are a small part of the overall leakage currents [**1**].

Three phase inverters have leg voltages (V_{a0}, V_{b0}, V_{c0}), phase voltages (V_{an}, V_{bn}, V_{cn}) and phase-to-phase voltages (V_{ab}, V_{bc}, V_{ca}). As can be seen from Figure 2-23 the leg voltages can be calculated as in equations (2-46), (2-47) and (2-48):

$$V_{a0}(t) = V_{an}(t) + V_{n0}(t) \quad (2\text{-}46)$$

$$V_{b0}(t) = V_{bn}(t) + V_{n0}(t) \quad (2\text{-}47)$$

$$V_{c0}(t) = V_{cn}(t) + V_{n0}(t) \quad (2\text{-}48)$$

If equations (2-46), (2-47) and (2-48) are summed equation (2-49) is obtained:

$$V_{a0}(t) + V_{b0}(t) + V_{c0}(t) = V_{an}(t) + V_{bn}(t) + V_{cn}(t) + 3 * V_{n0}(t) \quad (2\text{-}49)$$

As well known, the sum of a three phase voltages into a balanced system is equal to zero, thus the CMV at the motor terminals can be described as in equation (2-50) and defined as the load star point to the centre of the DC bus of the VSI [**35**].

$$V_{n0}(t) = \frac{V_{a0}(t) + V_{b0}(t) + V_{c0}(t)}{3} \quad (2\text{-}50)$$

The CMV magnitude depends on the switching sequence. Leakage currents (common mode currents) flow from motor to ground and from cables to ground due to high dv/dt and magnitude of CMV. The most important consequences of the Common Mode Current (CMC) are the bearing currents, electromagnetic interference and inverter unwanted trips [**1**].

A. Shaft Voltage

On rotating shafts stray voltages occur with magnitudes from micro – volts to hundreds of volts. This voltage may be produced in two ways: by rotation of the shaft (and produced into the magnetic field of the earth) and electromagnetic communication signal induction. The stray voltage induced by electromagnetic signal can be produced by shaft rotation that links to the asymmetrical magnetism of electrical machine, through the residual magnetism present in the shaft or in adjacent stationary members and by induction from power electronics devices, exciters or current – carrying brushes [**36**].

Shaft voltages are produced by CMV through capacitive couplings between rotor and stator windings (C_{rs}) and between rotor and frame (C_{rf}). The structure of a simplified high frequency model of motor is described in Figure 2-24. Based on this figure the shaft voltage can be calculated as:

$$V_{shaft} = \frac{C_{rs}}{C_b + C_{rs} + C_{rf}} * V_{CMV} \quad (2\text{-}51)$$

Shaft voltages can help and harm the system. They can warn about problems regarding development at an early stage, but at the same time they can generate circulating currents, reduce the efficiency of the unit, and generate flashovers that can damage the bearings, seals, gears and couplings. The potential for damage can be reduced by controlling the shaft voltages. There are two methods for controlling the shaft voltage: passive and active. The active method refers to injecting counteracting current signals in the rotor and the passive method is by simply placing grounding brushes [**36**].

B. Shaft Current

According to the generating mechanism there can be multiple types of bearing currents. The inverter – induced bearing currents classification can be found in Figure 2-25 .

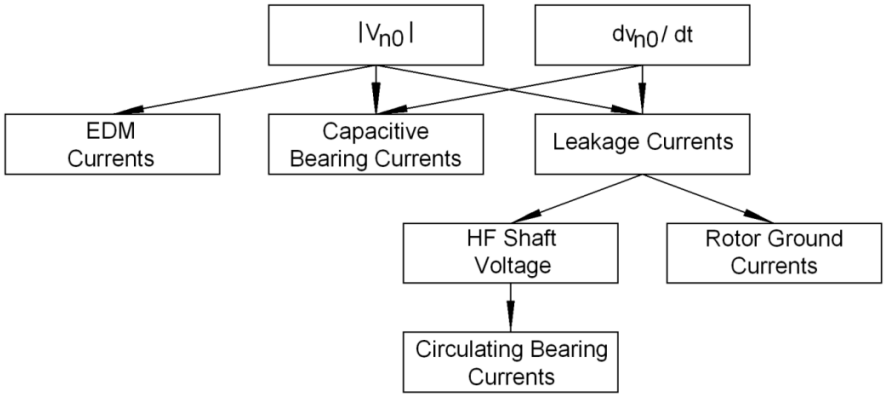


Figure 2-25 – Inverter – Induced Bearing Currents Classification

The common mode voltage can result in capacitive bearings currents, Electric Discharge Machine (EDM) and leakage currents. High frequency shaft voltage is induced by leakage ground currents originated from high dv/dt, therefore resulting in a source of high frequency circulating bearing currents. From all types of currents, the capacitive currents have the smallest magnitude and do not harm the motor. The most important common mode currents are EDM and High Frequency (HF) circulating bearing currents [**1**]. This can be seen in Figure 2-25.

The bearing currents appear when the shaft voltage exceeds the breakdown limit of the insulating grease thin film [**3**].

2.4.2. Switching Sequence Influence on CMV

Stationary vectors produce CMV, thus every vector influence in different manners [**31**]. Based on equations (2-46), (2-47), (2-48) and (2-50) the influence of every switching state on CMV can be calculated. As an example the sector I, region 4 from NTV-EHE was chosen. Each of the leg voltages has been drawn, as well as the resultant CMV for the case in which the DC link is balanced, presented in Figure 2-26.

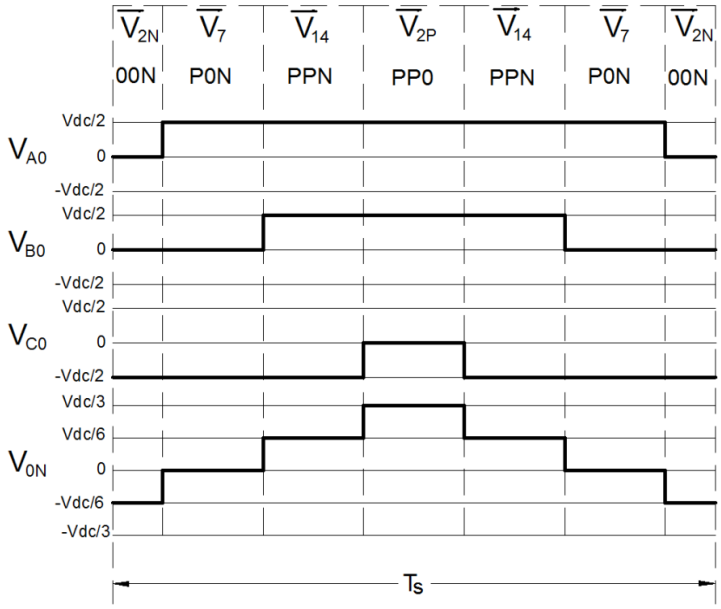


Figure 2-26 – NTV-EHE Sector I, Region 4 - Leg Voltages and their Resultant CMV

Furthermore the influence of each space vector on the CMV can be calculated. This can be seen in Table 2-5: first column represents the switching state, column two the vector type, column three describes the CMV when the neutral potential is zero and column four when it is different from zero.

Table 2-5 – Influence of Space Vectors on CMV [**31**]

State	Vector Type	Common Mode Voltage ($V_0 = 0$)	Common Mode Voltage ($V_0 \neq 0$)
000	Zero	0	V_0
NNN	Zero	$-\frac{1}{2}V_{DC}$	$-\frac{1}{2}V_{DC}$
PPP	Zero	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
NOO	Small	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
ONO	Small	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
OON	Small	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
POO	Small	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
OPO	Small	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
OOP	Small	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
NNO	Small	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
NON	Small	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
ONN	Small	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$

PPO	Small	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
POP	Small	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
OPP	Small	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
PON	Medium	0	$\frac{1}{3}V_0$
OPN	Medium	0	$\frac{1}{3}V_0$
NPO	Medium	0	$\frac{1}{3}V_0$
NOP	Medium	0	$\frac{1}{3}V_0$
ONP	Medium	0	$\frac{1}{3}V_0$
PN0	Medium	0	$\frac{1}{3}V_0$
NNP	Large	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}$
NPN	Large	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}$
PNN	Large	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}$
PPN	Large	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$
PNP	Large	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$
NPP	Large	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$

2.5. Method of Measuring EMI and CMV

2.5.1. Method of Measuring EMI

One of the most important problems in electric motor drives is the electromagnetic interference. This phenomenon produces undesirable effects on electronic devices. The top requirements in markets are increasing power density and decreasing cost and size of a system. When designing or optimising an electric machine drive: switching losses, harmonics and electromagnetic interference should be taken into account [**37**].

The operation of switching in power electronics, that feed one motor, creates electromagnetic noise in the drive system. EMI is generated by electromagnetic disturbances and can be classified as noise, impulses and transients. This noise goes into close circuits by inductive and capacitive couplings. This type of disturbance can be divided into [**38**]:

- Conducted EMI

- Radiated EMI

The most problematic frequency range that Electromagnetic Compatibility (EMC) standards address for conducted disturbances is 0.15 – 30 MHz [**39**]. There are four methods developed for mitigation of Common Mode (CM) EMI:

- Passive CM current cancellation [**40**]
- Active noise cancellation [**41**]
- CMV source reduction through modified PWM strategies [**42**]
- Filters [**43**] [**44**]

Conducted EMI is defined as undesired electromagnetic energy coming from an emitter or entering into a receptor through cables or wires. This type of electromagnetic energy causes interference in electronic system due to the fact that power distribution is represented as a large antenna. In order to measure it the CISPR 16 standard needs to be taken into account. This international standard specifies the tests for compliance with conducted emissions limits and utilises the Line Impedance Stabilization Network (LISN), a passive filter, for measurements. This can be seen in Figure 2-27:

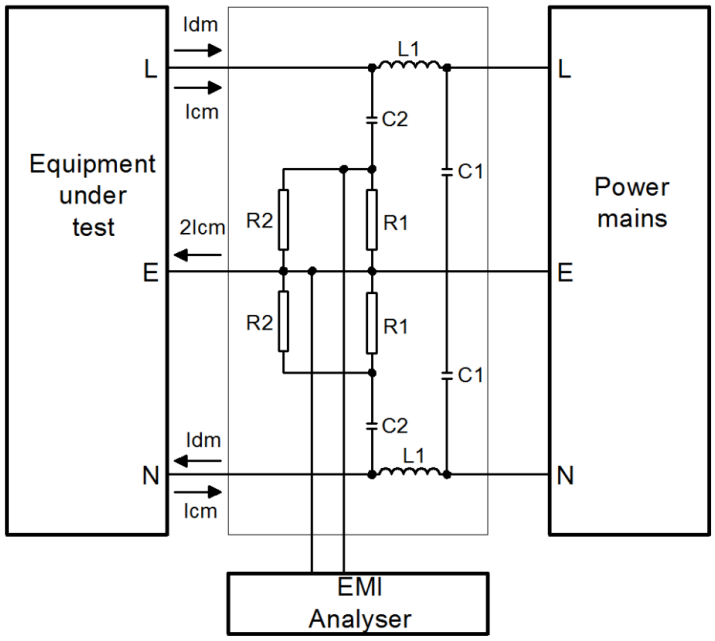


Figure 2-27 Test Setup for EMI Measurement

The current created by noise has two components:

- Common mode noise current, I_{cm}, that flows out from line and neutral and returns through the earth wire
- Differential mode noise current, I_{dm}, which flows from line and returns through neutral.

The test set-up presented in Figure 2-27 measures the total common and differential mode current in the line or neutral. These are measured across the 50 Ohm LISN resistor (R2).

This thesis proposes the reduction of the CM EMI by reducing the CMV through improved PWM strategies.

2.5.2. Method of Measuring CMV

For measuring CMV and CMC the setup from Figure 2-28 can be used. The setup is isolated from the network through the isolation transformer. The motor is mounted on an insulated plate (wood) for a good galvanic separation from the ground. The CMV is measured between the neutral point of the motor and the zero point of the DC link. The CMC must be measured via a high bandwidth current transducer and the CMV via a high bandwidth voltage probe [**1**].

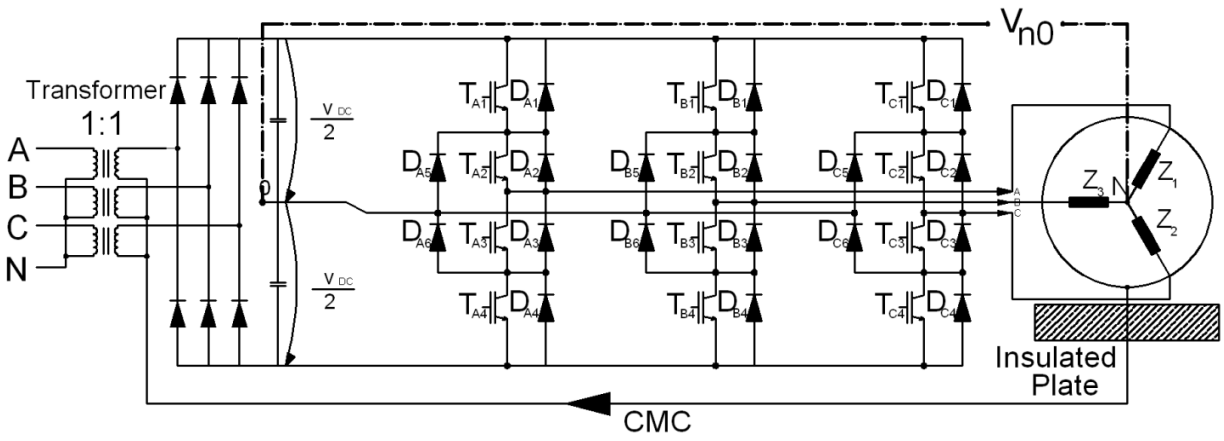


Figure 2-28 – Test Setup for Measuring the CMV and CMC

3. Improved Modulation Strategies

This chapter introduces four improved modulation strategies developed based on the space vector table and theory presented in chapter 2. Each of this modulation strategies are validated through simulation results. This chapter ends with a comparative performance evaluation consisting of comparison at maximum modulation index as well as an analysis of THD in the phase-to-phase voltage throughout entire modulation index range.

3.1. One Small One Medium Vector

Analysing Table 2-5 from Chapter 2.4.2 it can be noticed that small vectors have the ability to natural balance the neutral point by proper switching from N – type to P – type vectors. In order to create this modulation strategy the space vector diagram is divided in twelve sectors with a 30° angle between small vectors and medium vectors. The appropriate vectors for this method, regarding sector one and two, are presented in Figure 3-1.

a) Space Vectors for Creation of Reference Voltage in the First Sector

b) Space Vectors for Creation of Reference Voltage in the Second Sector

Figure 3-1 – One Small One Medium Vector Method

Considering the first sector, the reference vector is created from the stationary vectors $\overrightarrow{V_0}$, $\overrightarrow{V_1}$, $\overrightarrow{V_7}$. In order to calculate the dwell times for this sector the volt – second principle together with the assumption that during $T_s$the reference voltage $V_{ref}$is constant are used. This can be seen in equation (3-1).

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_1}T_a + \overrightarrow{V_7}T_b + \overrightarrow{V_0}T_c \quad (3\text{-}1)$$

The stationary vectors that form the reference voltage as well as the reference vector are summarized in equation (3-2).

$$\overrightarrow{V_1} = \frac{1}{3}V_{DC}e^{j0} \qquad \overrightarrow{V_7} = \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}} \qquad \overrightarrow{V_0} = 0 \qquad \overrightarrow{V_{\text{ref}}} = V_{ref}e^{j\theta} \tag{3-2}$$

Introducing (3-2) in (3-1) the dwell times can be calculated. The result can be seen in equation (3-3).

$$V_{ref}e^{j\theta}T_s = \frac{1}{3}V_{DC}e^{j0}T_a + \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}}T_b \tag{3-3}$$

Equation (3-4) is obtained by transforming equation (3-3) into polar coordinates.

$$V_{ref}T_s(cos\theta + jsin\theta) = \frac{1}{3}V_{DC}T_a(cos\ 0 + jsin\ 0) + \frac{\sqrt{3}}{3}V_{DC}T_b\left(cos\frac{\pi}{6} + jsin\frac{\pi}{6}\right) \tag{3-4}$$

In order to calculate the dwell times, equation (3-4) is divided into real and imaginary part. Equation system (3-5) is obtained for a switching period:

$$\begin{cases} V_{ref}T_s cos\theta = \frac{1}{3}V_{DC}T_a + \frac{1}{2}V_{DC}T_b \\ V_{ref}T_s sin\theta = \frac{\sqrt{3}}{6}V_{DC}T_b \\ T_s = T_a + T_b + T_c \end{cases} \tag{3-5}$$

Solving equation (3-5), dwell times will result as in equation (3-6):

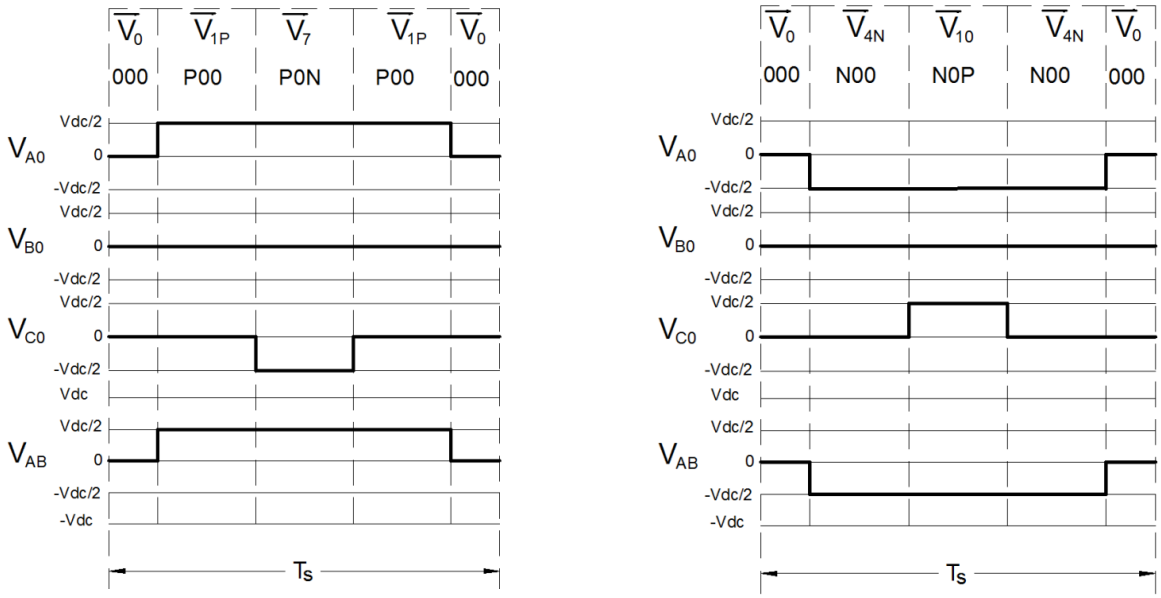
$$\begin{cases} T_a = 6T_s\frac{V_{ref}}{V_{DC}}\sin\left(\frac{\pi}{6} - \theta\right) \\ T_b = 2\sqrt{3}T_s\frac{V_{ref}}{V_{DC}}sin\theta \\ T_c = T_s - T_a - T_b \end{cases} \tag{3-6}$$

The dwell times for odd sectors are determined based on equation (3-6) by adjusting the angular displacement so that it can fall in the interval $\left[0, \frac{\pi}{6}\right]$. For even sectors the dwell times are determined in the same manner.

In order to cancel the phase-to-phase even harmonics from the voltage waveform the switching sequences are divided in:

- Odd sector – the sequence is predominant by P type small vector
- Even sector – the sequence is predominant by N type small vector

The requirement for even harmonic elimination is that the phase-to-phase voltage waveform is half wave symmetrical. By alternating the N and P type small vectors these harmonics are forced to cancel. This can be seen in Figure 3-2.



$\overrightarrow{V_{ref}}$ in Region 1 $\overrightarrow{V_{ref}}$ in Region 7

Figure 3-2 – Five Segment Switching Sequences for $\overrightarrow{V_{ref}}$ in Sector I and VII

When referring to modulation index it is needed to be mentioned that, for this method, the magnitude for the reference vector is limited to the inscribed circle in the hexagon created by the small vectors. The maximum reference vector is presented in equation (3-7):

$$V_{ref,max} = \frac{1}{3} V_{DC} \frac{\sqrt{3}}{2} = \frac{\sqrt{3} V_{DC}}{6} \tag{3-7}$$

The maximum modulation index is presented in equation (3-8):

$$m_{a,max} = \sqrt{3} \frac{V_{ref,max}}{V_{DC}} = \sqrt{3} \frac{\frac{\sqrt{3} V_{DC}}{6}}{V_{DC}} = \frac{1}{2} = 0.5 \tag{3-8}$$

It can be mentioned that in comparison with ZCM, this method has the advantages:

- Redundant states
- Transition between two adjacent states does not involve two inverter legs

In order to test this modulation strategy simulations at its maximum modulation index, $m_a = 0.5$, were performed. The simulation structure presented in Chapter 2.2.2 was used. Figure 3-3 presents two fundamental periods of phase voltage, phase-to phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, V_{an}. This voltage has five levels $\pm 300, \pm 100, 0$, due to the fact that only small, medium and zero vectors are used. The second waveform from the same figure represents the phase-to-phase voltage, which has five voltage levels $\pm 600, \pm 300, 0$ as the classical methods. The total harmonic distortion in this voltage is 78.52 [%]. Furthermore, the CMV is presented in

the third waveform. As it can be seen CMV has three voltage levels $\pm 100, 0$, with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in Chapter 5.8.

By the use of small, medium and zero vectors this method has the ability to self-balance, through a proper switching between P and N type small vectors. The DC link voltage is presented in last waveform from Figure 3-3. In steady state the voltage on the upper capacitor varies between approximately 299 V and 304 V as for the lower capacitor the voltage is between 296 V and 301 V at maximum modulation, $m_a = 0.5$.

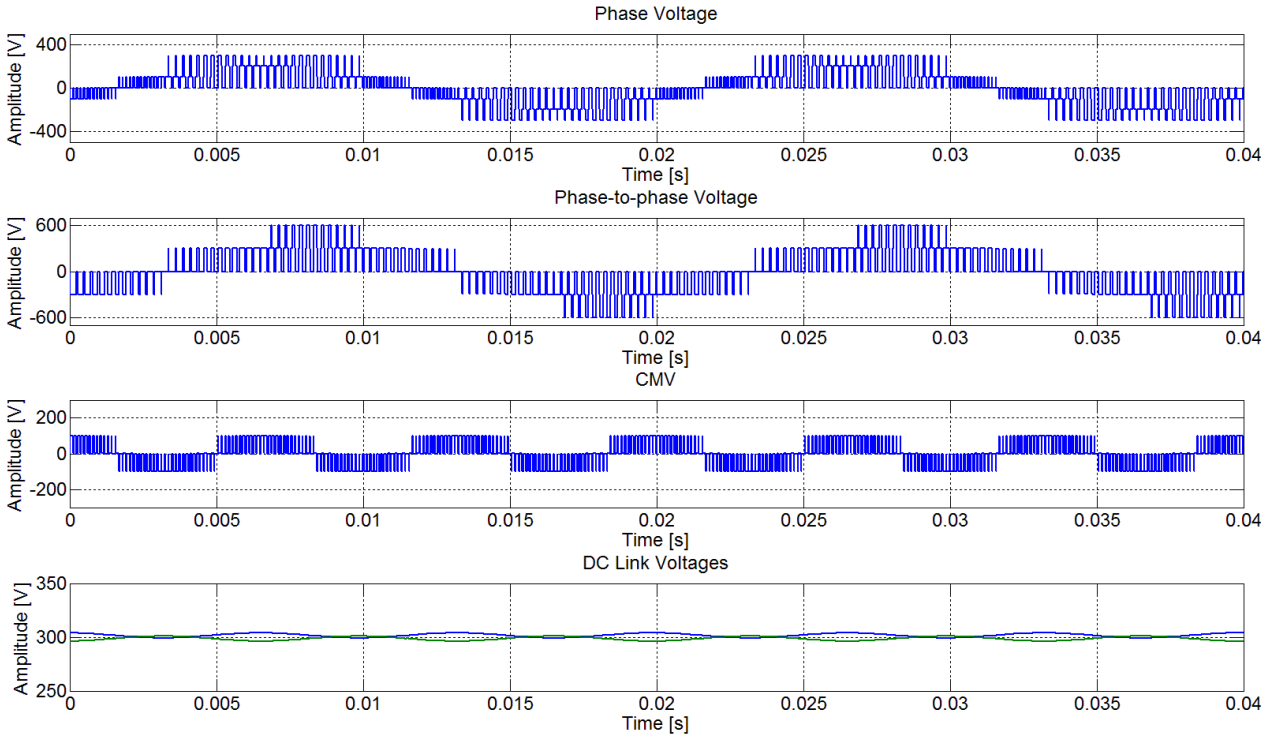
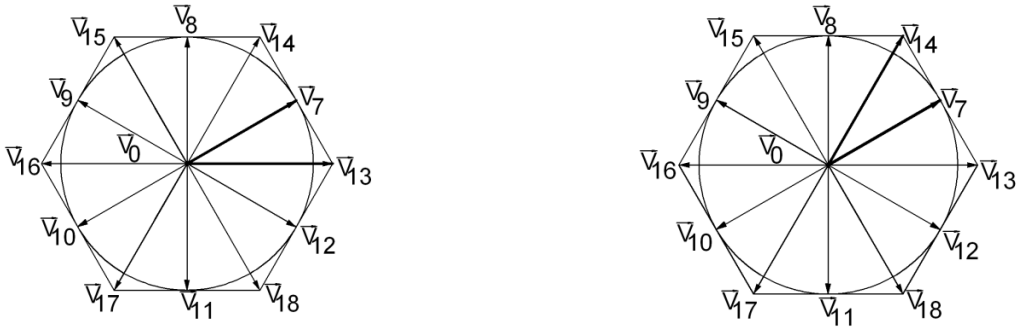


Figure 3-3 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for OSOM at $m_a = 0.5$ - Simulation

As described at NTV-EHE the active switching frequency can be calculated and results as 1.33 kHz, due to the fact that only four transistors from a total of twelve perform a full commutation on each sampling period.

3.2. One Large One Medium Vector

In order to increase the modulation index and to better use the bus bar, one large and one medium vectors are used to define the reference vector. The space vector diagram is divided into twelve sectors with 30° angle between medium and large vectors as shown in Figure 3-4.



a) Space Vectors for Creation of Reference Voltage in the First Sector

b) Space Vectors for Creation of Reference Voltage in the Second Sector

Figure 3-4 – One Large One Medium Vector Method

In order to calculate the dwell times, for this method, the first sector is taken into account. The reference vector is created by $\overrightarrow{V_0}$, $\overrightarrow{V_{13}}$, $\overrightarrow{V_7}$. Using volt – second principle together with the assumption that during T_s the reference voltage is constant, equation (3-9) is obtained.

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_{13}}T_a + \overrightarrow{V_7}T_b + \overrightarrow{V_0}T_c \tag{3-9}$$

The stationary vectors that form the reference voltage are summarized in equation (3-10).

$$\overrightarrow{V_{13}} = \frac{2}{3}V_{DC}e^{j0} \qquad \overrightarrow{V_7} = \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}} \qquad \overrightarrow{V_0} = 0 \tag{3-10}$$

The dwell times can be calculated by introducing (3-10) in (3-9). The result can be seen in equation (3-11).

$$V_{ref}e^{j\theta}T_s = \frac{2}{3}V_{DC}e^{j0}T_a + \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}}T_b \tag{3-11}$$

By transforming equation (3-11) into polar coordinates equation (3-12) is obtained.

$$V_{ref}T_s(cos\theta + jsin\theta) = \frac{2}{3}V_{DC}T_a(\cos 0 + jsin\ 0) + \frac{\sqrt{3}}{3}V_{DC}T_b\left(cos\frac{\pi}{6} + jsin\frac{\pi}{6}\right) \tag{3-12}$$

Equation (3-12) is divided into real and imaginary part, thus obtaining the system of equations (3-13) for a switching period:

$$\begin{cases} V_{ref}T_s cos\theta = \frac{2}{3}V_{DC}T_a + \frac{1}{2}V_{DC}T_b \\ V_{ref}T_s sin\theta = \frac{\sqrt{3}}{6}V_{DC}T_b \\ T_s = T_a + T_b + T_c \end{cases} \quad (3\text{-}13)$$

Solving equation (3-13) the dwell times will result as in equation (3-14):

$$\begin{cases} T_a = 3T_s \frac{V_{ref}}{V_{DC}} \sin\left(\frac{\pi}{6} - \theta\right) \\ T_b = 2\sqrt{3}T_s \frac{V_{ref}}{V_{DC}} sin\theta \\ T_c = T_s - T_a - T_b \end{cases} \quad (3\text{-}14)$$

The dwell times for all odd sectors are determined based on equation (3-14) by adjusting the angular displacement in such a manner that it can fall in the interval $\left[0, \frac{\pi}{6}\right]$. Furthermore, for even sectors the dwell times are determined in the same manner.

For a better understanding of the proposed modulation strategy the switching sequence for sector I is presented in Figure 3-5.

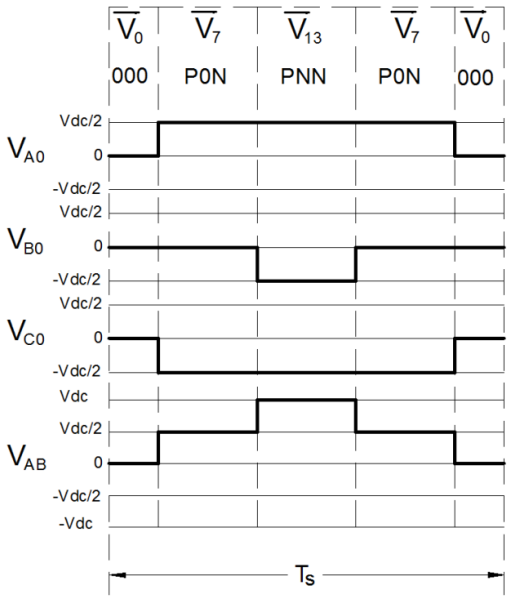


Figure 3-5 – Five Segment Switching Sequences for $\overrightarrow{V_{ref}}$ in Sector I

The modulation index for this method is determined by the inscribed circle in the hexagon created by large vectors. The maximum reference vector is presented in equation (3-15):

$$V_{ref,max} = \frac{2}{3}V_{DC}\frac{\sqrt{3}}{2} = \frac{\sqrt{3}\,V_{DC}}{3} \quad (3\text{-}15)$$

The maximum modulation index is calculated in (3-16):

$$m_{a,max} = \sqrt{3}\frac{V_{ref,max}}{V_{DC}} = \sqrt{3}\frac{\frac{\sqrt{3}\,V_{DC}}{3}}{V_{DC}} = 1 \tag{3-16}$$

In order to test this modulation strategy simulations at maximum modulation index, $m_a = 1$, were performed. The simulation structure presented in subchapter 2.2.2 was used. Figure 3-6 presents two fundamental periods of phase voltage, phase-to phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, V_{an}. This voltage has seven levels $\pm 400, \pm 300, \pm 200, 0$, due to the fact that only large, medium and zero vectors are used. The second waveform from the same figure represents the phase-to-phase voltage, which has five voltage levels $\pm 600, \pm 300, 0$ as expected. The total harmonic distortion in this voltage is $31.81\,[\%]$. Furthermore, the CMV is presented in the third waveform. As it can be seen CMV has three voltage levels $\pm 100, 0$, with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in subchapter 5.9.

By the use of only of large, medium and zero vectors this method has the ability to self-balance. The DC link voltage is presented in last waveform from Figure 3-6. In steady state the voltage on the upper capacitor varies between approximately 294 V and 308 V as for the lower capacitor the voltage is between 292 V and 306 V at maximum modulation index, $m_a = 1$.

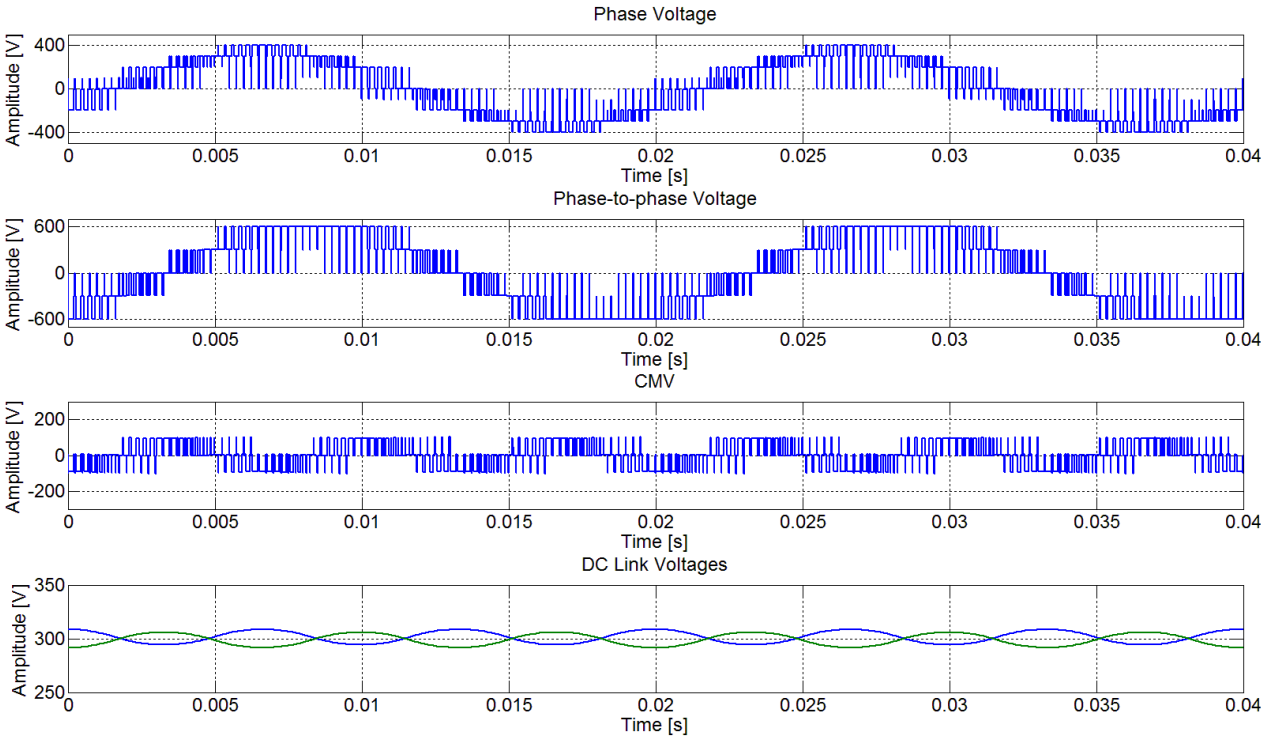
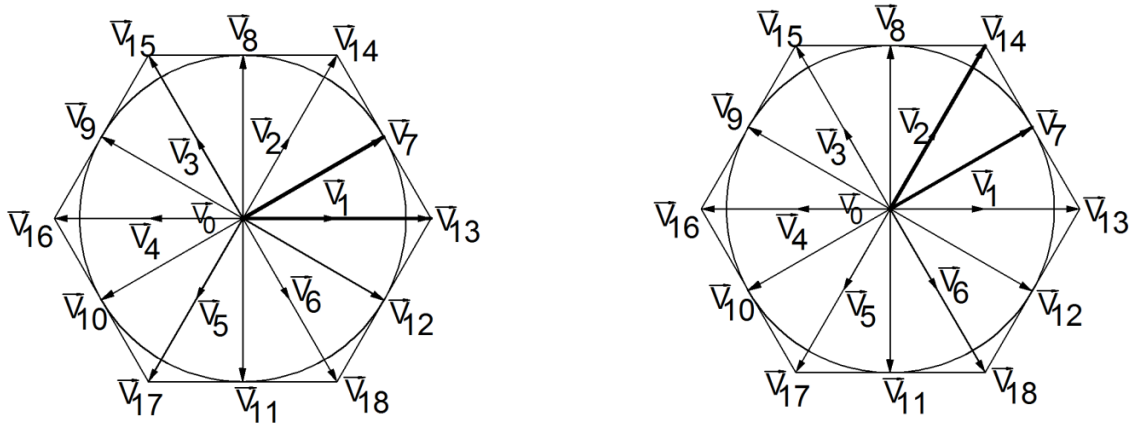


Figure 3-6 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for OLOM at $m_a = 1$ - Simulation

As described for the classical modulation strategy NTV-EHE the active switching frequency on each device can be calculated. For this method the active switching frequency is 2 kHz.

3.3. Zero Small Medium Large Method

Taken into consideration Table 2-5 and theory presented at NTV, another method can be proposed. The idea behind this method is to use all four vectors in order to maintain the THD low, while choosing the small vectors in such a manner that the CMV levels are half compared to NTV. The space vector diagram is divided into six sectors each of them having two regions. This configuration can be seen in Figure 3-7. First region lasts between $\left[0,\frac{\pi}{6}\right]$ and the second one between $\left[\frac{\pi}{6},\frac{\pi}{3}\right]$.



a) Space Vectors for Sector I, Region 1

b) Space Vectors for Sector I, Region 2

Figure 3-7 – Space Vector Diagram for Zero Small Medium Method in Sector I

In order to calculate the dwell times the volt-second principle is used, together with the assumption that during switching time the reference vector is constant. As an example the reference vector from sector I, region 1 is presented in equation (3-20) and its stationary vectors in equation (3-18).

$$\overrightarrow{V_{ref}}T_s = \overrightarrow{V_1}T_a + \overrightarrow{V_7}T_b + \overrightarrow{V_{13}}T_c + \overrightarrow{V_0}T_d \tag{3-17}$$

$$\overrightarrow{V_{13}} = \frac{2}{3}V_{DC}e^{j0} \qquad \overrightarrow{V_7} = \frac{\sqrt{3}}{3}V_{DC}e^{j\frac{\pi}{6}} \qquad \overrightarrow{V_1} = \frac{1}{3}V_{DC}e^{j0} \qquad \overrightarrow{V_0} = 0 \tag{3-18}$$

The dwell times are calculated differently for each half-sector. A factor k1 is inserted in the equations in order to make possible the division of the dwell times between the four vectors. This factor has been defined as the ratio between the reference voltage and maximum reference voltage, equation (3-19). Furthermore, when the amplitude of the reference voltage is maximum only small, medium and large vectors will form it.

$$k1 = \frac{V_{ref}}{V_{ref,max}} \tag{3-19}$$

When calculating the dwell times, the displacement angle needs to be taken into account. Hence when the displacement angle is in region 1 the dwell times have the form presented in equation (3-20) and when is in region 2 they have the form presented in equation (3-21).

$$\begin{cases} T_{aa} = T_s \dfrac{-3 * V_{ref} * \cos\theta + 2 * k1 * V_{DC} - \sqrt{3} * V_{ref} * sin\theta}{k1 * V_{DC}} \\ T_{bb} = 2\sqrt{3} * T_s * \dfrac{V_{ref} * sin\theta}{k1 * V_{DC}} \\ T_{cc} = T_s * \dfrac{3 * V_{ref} * \cos\theta - 3\sqrt{3} * V_{ref} * sin\theta - k1 * V_{DC} + 2\sqrt{3} * V_{ref} * sin\theta}{k1 * V_{DC}} \end{cases} \quad (3\text{-}20)$$

$$\begin{cases} T_{aa} = T_s \dfrac{-3 * V_{ref} * \cos\theta + 2 * k1 * V_{DC} - \sqrt{3} * V_{ref} * sin\theta}{k1 * V_{DC}} \\ T_{bb} = T_s * \dfrac{3 * V_{ref} * \cos\theta - \sqrt{3} * \sin\theta}{k1 * V_{DC}} \\ T_{cc} = T_s * \dfrac{2\sqrt{3} * V_{ref} * sin\theta - k1 * V_{DC}}{k1 * V_{DC}} \end{cases} \quad (3\text{-}21)$$

Based on equations (3-20) and (3-21), the dwell times are presented in equation (3-22) :

$$\begin{cases} T_a = k1 * T_{aa} \\ T_b = k1 * T_{bb} \\ T_c = k1 * T_{cc} \\ T_d = (1 - k1) * T_s \end{cases} \quad (3\text{-}22)$$

This method is able to balance the DC link, in a case of an external event, by proper use of the small vectors. When is in balancing mode, the CMV levels are same as NTV. As all the vectors are used, the largest vector that can be inscribed in the hexagon is the large vector, thus the modulation index is 1, as at the classical method, NTV-EHE. For a better understanding of this method a typical switching sequence is presented in Figure 3-8:

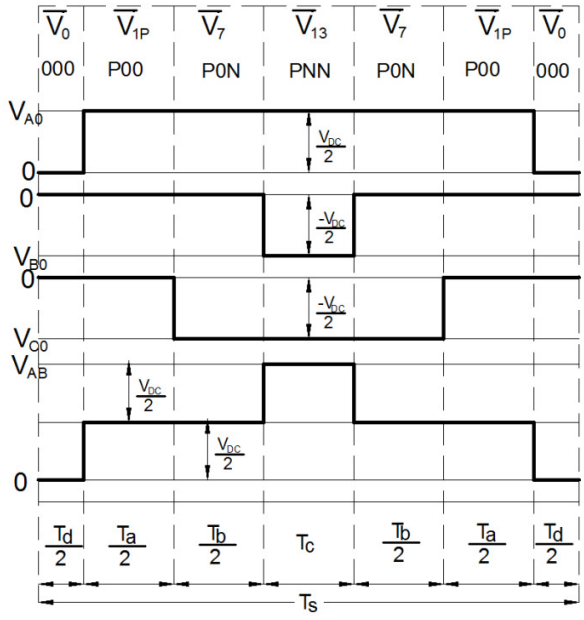


Figure 3-8 – Switching Sequence for ZSML in Sector I, Region 1

In order to test this modulation strategy, simulations at maximum modulation index, $m_a = 1$, were performed based on the simulation structure presented in subchapter 2.2.2. Figure 3-9 presents two fundamental periods of phase voltage, phase-to phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, V_{an}. This voltage has a quasi – sinusoidal shape and nine levels $\pm 400, \pm 300, \pm 200, \pm 100, 0$, because all the stationary vectors are used in order to form the reference voltage vector. The second waveform from this figure represents the phase-to-phase voltage, which has five voltage levels $\pm 600, \pm 300, 0$ as expected. The total harmonic distortion in the line voltage is $27.13\ [\%]$. Furthermore, the CMV is presented in the third waveform. As it can be seen CMV has three voltage levels $\pm 100, 0$, with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in subchapter 5.9.

By the use of stationary vectors this method has the ability to self-balance and balance the DC link in case of an external disturbance. The voltage on the DC link capacitors under natural balancing conditions is presented in last waveform from Figure 3-9. In steady state the voltage on the upper capacitor varies between approximately 295 V and 309 V as for the lower capacitor the voltage is between 291 V and 305 V at maximum modulation index, $m_a = 1$.

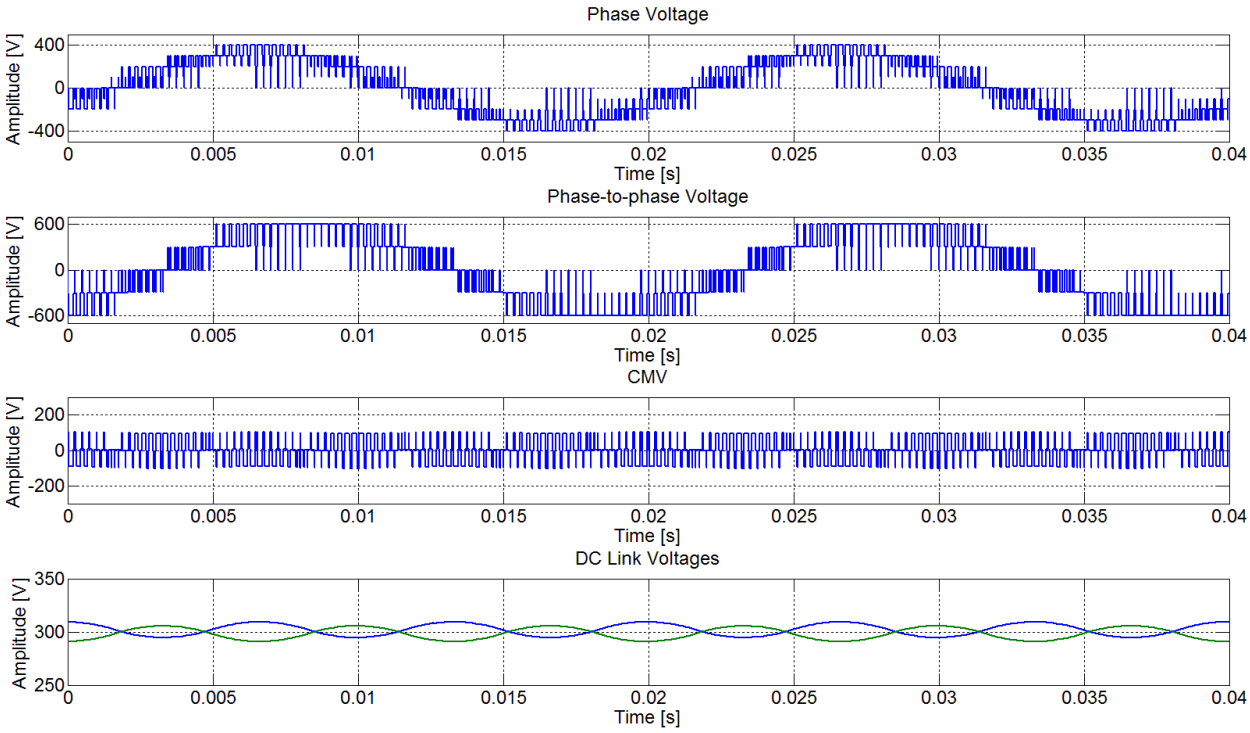


Figure 3-9 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for ZSML Method at ma=1 - Simulation

As presented at NTV-EHE the active switching frequency on each device can be calculated. For this method this frequency is 2 kHz as only six of the twelve transistors are commutated in each sampling period.

3.4. Random Sequence of 3 Vectors with Neutral Point Balancing Method

The idea of randomization is not new to inverters modulation, but its purpose and utilization is quite different from the idea implemented in Random Sequence of 3 Vectors with Neutral Point Balancing (RS3N). Some methods used are SVM with variable switching frequency others are deterministic [**45**] because of the fixed switching frequency. The methods try to maintain the average switching frequency low while reducing acoustic noise [**46**]. Lead-lag modulation (RLL) aligns the pulse position with the beginning or the end of the switching interval. Random displacement of pulse centre (RCD) aligns the centre of pulses from each phase. Random distribution of zero vector (RZD) is based on the idea that zero vector time is randomly divided between PPP and 000 state [**46**]. The RLL, RCD and RZD are fixed frequency random modulation strategies for two level inverters.

Random pulse width modulation is known to be proposed for reduction of current harmonics, torque ripple and acoustic noise [**45**]. Because using a variable switching frequency is microcontroller intensive, the methods based on fixed switching frequency are preferred.

The proposed method is based on the idea that each switching sequence can have the vector order changed, having an impact in the CMV due to the reduction of voltage levels at high frequencies. Eliminating the repetition of the CMV distribution between each switching sequence should have a big impact on the frequencies which are a multiple of the switching frequency. These assumptions are confirmed in both the simulation and the experimental results.

The idea behind the RS3N modulation strategy is to improve spectral performance on CMV while reducing it in the time domain to half of NTV. To obtain this, the switching sequence for each combination of nearest three vectors is done in a sequence of three vectors. Using a pseudo-random number generator, this switching sequence is randomized up to 80 times on each period of the output frequency. The maximum randomization value is obtained as in equation (3-23).

$$r = \frac{f_{sw}}{f_{out}} = \frac{4000}{50} = 80 \tag{3-23}$$

Where:

- r – is the randomization factor
- f_{sw} – is the switching frequency
- f_{out} – is the output frequency

By having the switching sequence randomized, the resultant CMV levels on each sequence will not be repeated anymore, thus reducing the CMV levels which are multiple of switching frequency, in the frequency domain. An example of the effect of randomization can be seen in Figure 3-10, the CMV output does not repeat from one sequence to another.

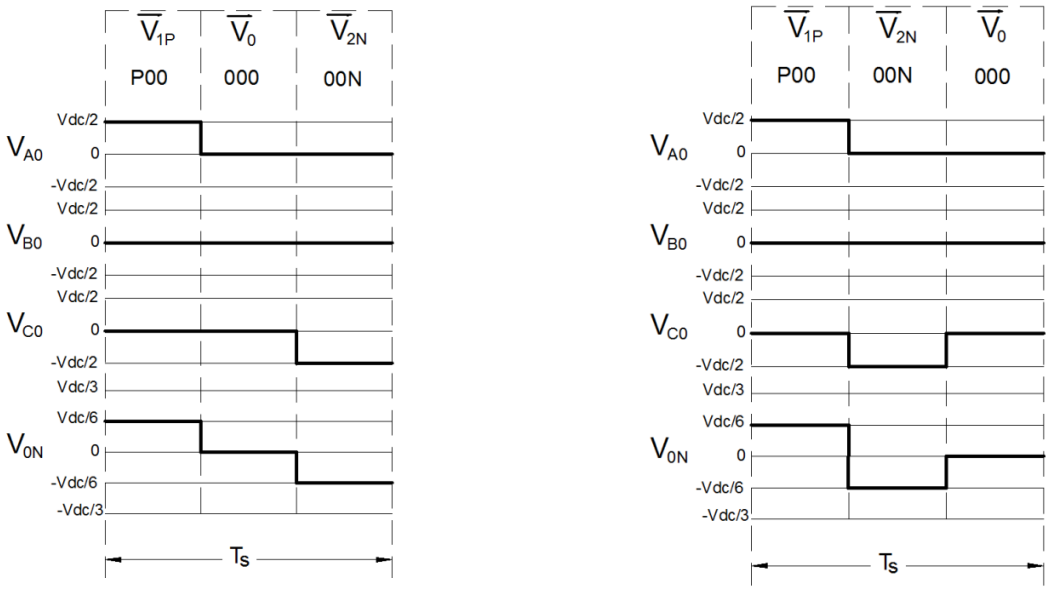


Figure 3-10 – Randomization Effect on CMV on RS3N Modulation Strategy in Sector I, Region 1

For this method, the space vector diagram is divided in 6 sectors, as the NTV-EHE. The difference between these two is that there are only four regions in each sector, and the behaviour of the modulation in these regions is different. As it is well known that some of the small vectors produce less CMV [**31**], these vectors are preferred in each region. By choosing these vectors, the CMV levels in the time domain are half of NTV for any modulation index. The division between sectors and regions can be seen in Figure 3-11. The THD should follow the behaviour of the NTV-EHE method due to the fact that it relies on the choice of the nearest three vectors.

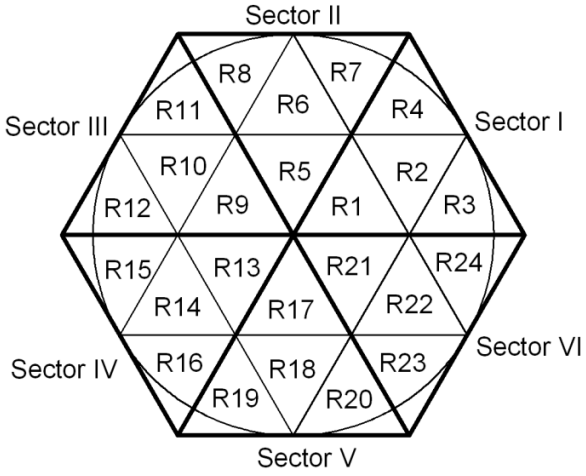


Figure 3-11 – Space Vector Diagram of RS3N Modulation Strategy

As this method uses the same principle as NTV, the dwell times will have the same form as well as the modulation index.

The method is able to balance the DC link voltage, in a case of an external event, by proper use of the P and N type small vectors. During balancing mode, in case on an external event, the CMV level in time domains are same to NTV, however there is an improvement in the frequency domain due to switching sequence randomization.

In order for this method to function adequately, two filters were implemented. The first filter ensures that there is no N-P or P-N switching between two consecutive sequences and the second one that the combination P-O-P is avoided, in order to make the DSP implementation possible. These two filters follow the principle: if one of the two events is detected, another random number is chosen and the switching sequence is randomized again. If the new combination passes the two filters, is sent to the output. For the DSP implementation, this method uses asymmetrical up-count mode for the enhanced Pulse Width Modulator (ePWM) modules.

As the other methods, this one has been tested on the structure presented in subchapter 2.2.2. Figure 3-12 presents two fundamental periods of phase voltage, phase-to phase voltage, CMV and DC link voltages in steady state. The first waveform describes the phase voltage, V_{an}. This voltage has a quasi – sinusoidal shape and nine levels $\pm 400, \pm 300, \pm 200, \pm 100, 0$, as NTV. The second waveform from this figure represents the phase-to-phase voltage, which has five voltage levels $\pm 600, \pm 300, 0$ as expected. The total harmonic distortion in the line voltage is $26.73\ [\%]$. Furthermore, the CMV is presented in the third waveform. As it can be seen it has three voltage levels $\pm 100, 0$, with a fundamental period of 150 Hz. As the classical modulation strategies a more specific analysis will be performed in subchapter 5.9.

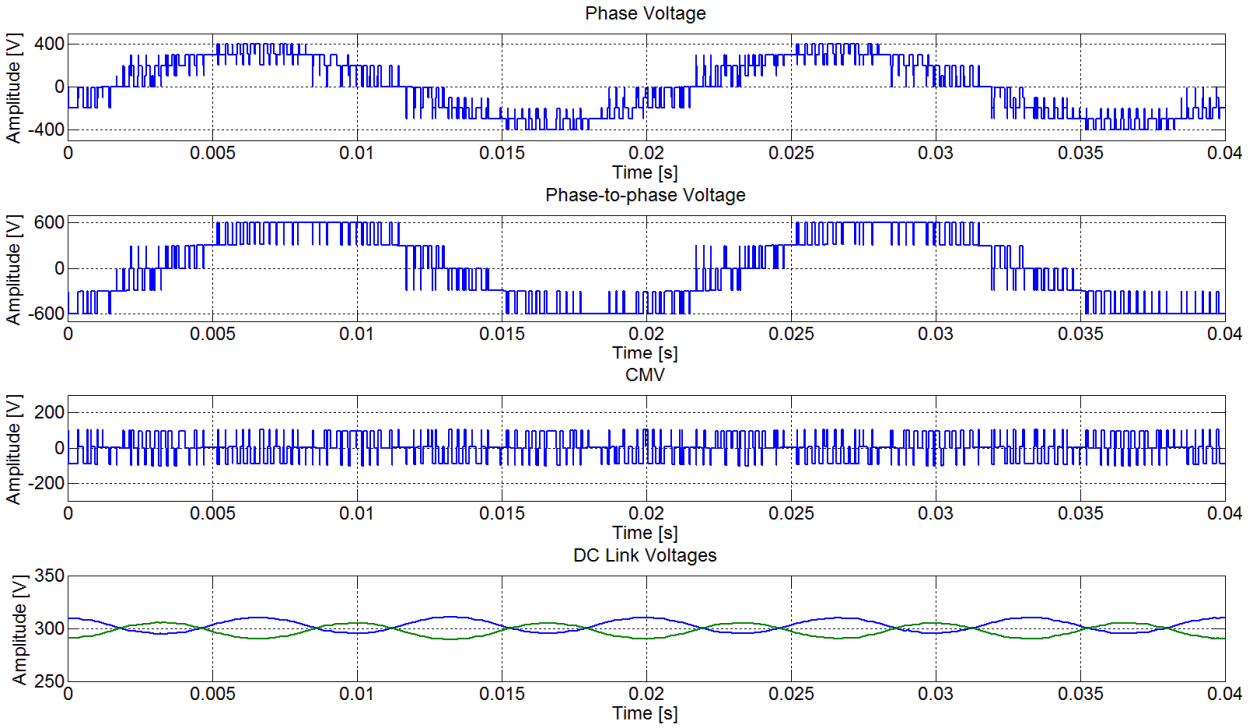


Figure 3-12 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for RS3N at $m_a = 1$ - Simulation

This method has the ability to self-balance and balance the DC link in case of an external disturbance. The fourth waveform from Figure 3-12 presents the DC link voltage in natural balancing mode. The voltage on the DC link capacitors is presented in last waveform from Figure 3-9. In steady state the voltage on the upper capacitor varies between approximately 295 V and 310 V as for the lower capacitor the voltage is between 290 V and 305 V at maximum modulation index, $m_a = 1$.

The active switching frequency on each device is 2 kHz as only six transistors from a total of twelve perform a full commutation on each sampling period.

3.5. Performance Evaluation of Improved Modulation Strategies

Based on the theory and simulations results presented in this chapter, a comparative analysis has been performed between the developed modulation strategies and the classical ones.

Two of the developed modulations, ZSML and RS3N, have nine levels on the phase voltage as NTV-EHE, while OLOM has seven and OSOM five. Hence, for ZSML and RS3N the output filter requirements are as for NTV, while at OLOM and OSOM the filter needs to be increased. For a better understanding of the output filter requirements, in order to reduce the cost of the drive, the current and phase-to-phase voltage THD have been calculated. OLOM and ZSML have the current THD very similar with NTV, while ZSML present similarities with ZCM. OSOM has the largest distortion in the phase current and phase-to-phase voltage, but the modulation index is half of the other ones. ZSML and RS3N have similar harmonic distortion with NTV, at maximum modulation index, while at OLOM is slightly increased.

For a good utilization of the bus bar the modulation index needs to be taken into account as this is proportional with the DC link voltage. From this point of view OLOM, ZSML and RS3N have the best perspective, while OSOM can use only half of it.

In case of an external event that will unbalance the DC link, the modulation strategy needs to be able to counteract it as to maintain the balance. The RS3N and ZSML have this ability, while the other methods have only the ability to self-balance. Furthermore, the CMV needs to be analysed. From this point of view all the developed methods present a better performance in time domain, half of the NTV amplitude.

Table 3-1 – Comparative Analysis between Modulation Strategies

Modulation Strategy	Output phase to neutral voltage levels [V]	Modulation Index	DC link balancing	CMV Levels [V]	THD_i	Phase to phase THD_v
NTV	$\pm 400, \pm 300, \pm 200, \pm 100, 0$	1	Natural balancing	$\pm 200, \pm 100, 0$	0.23%	27.93%
ZCM	$\pm 300, 0$	0.866	Natural balancing	$\pm 100, 0$	0.56%	52.23%
OLOM	$\pm 400, \pm 300, \pm 200, 0$	1	Natural balancing	$\pm 100, 0$	0.30%	31.81%
ZSML	$\pm 400, \pm 300, \pm 200, \pm 100, 0$	1	Natural balancing and balancing	$\pm 100, 0$	0.28%	27.13%
OSOM	$\pm 300, \pm 100, 0$	0.5	Natural balancing	$\pm 100, 0$	0.88%	78.52%
RS3N	$\pm 400, \pm 300, \pm 200, \pm 100, 0$	1	Natural balancing and balancing	$\pm 100, 0$	0.56%	26.73%

For a better understanding of how each modulation strategy acts at different reference voltages a chart has been developed, Figure 3-13. This figure presents the THD on phase-to-phase voltage as a function of modulation index. From the developed strategies only OLOM, ZSML and RS3N have a proper utilization of the DC link.

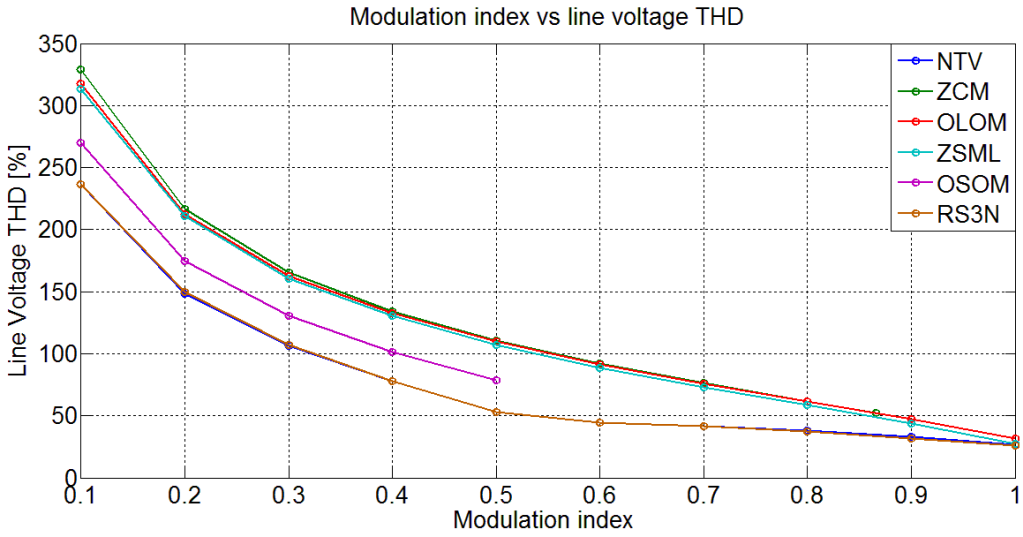


Figure 3-13 – Modulation Index vs. Line Voltage THD of Classic and Developed Modulation Strategies based on Developed Simulation

As it can be seen from Figure 3-13 RS3N has the THD exactly the same as NTV-EHE. OSOM presents a good performance in the entire range, less than half of the distance between NTV and ZCM. At maximum modulation index ZSML and OLOM present similar performance with NTV, but when the modulation index decreases the similarity is closer to ZCM.

4. Hardware Design of three-level NPC Inverter

This chapter presents the design of the 7.5 kW NPC inverter that was built featuring newly introduced NPC leg modules from Semikron, four layer PCB for noise reduction and full protections against over temperature, overcurrent or out of range voltages on the DC link capacitors. The embedded DSP design together with a CPLD for deadtime and protection management make the inverter very customisable through software. Advanced gate drivers with extra protection add to the design performance.

4.1. System Overview

The three level NPC inverter was modelled based on the simplified hardware schematic from Figure 4-1 and has the following main features:

- Embedded TMS320F28335 DSP design.
- 4 layer Printed Circuit Board (PCB) with stacked DC link layout, ground and power planes.
- Design based on NPC leg IGBT modules.
- Adjustable over temperature, overcurrent and overvoltage protection.
- Xilinx XC9572XL CPLD based dead time and protection management.
- Real time PWM Signal analysis and protection.
- DC Link up to 1kV.
- Shielded Analog to Digital Converter (ADC) and PWM signals.
- RS-232, RS-485 and Controller Area Network (CAN) communication.
- Optocoupler galvanic isolated gate driver with active Miller clamping.
- Desaturation detection.
- JTAG interface for DSP and CPLD.
- Hall effect current sensors.
- Mixed analog and digital design.
- Reduced size.

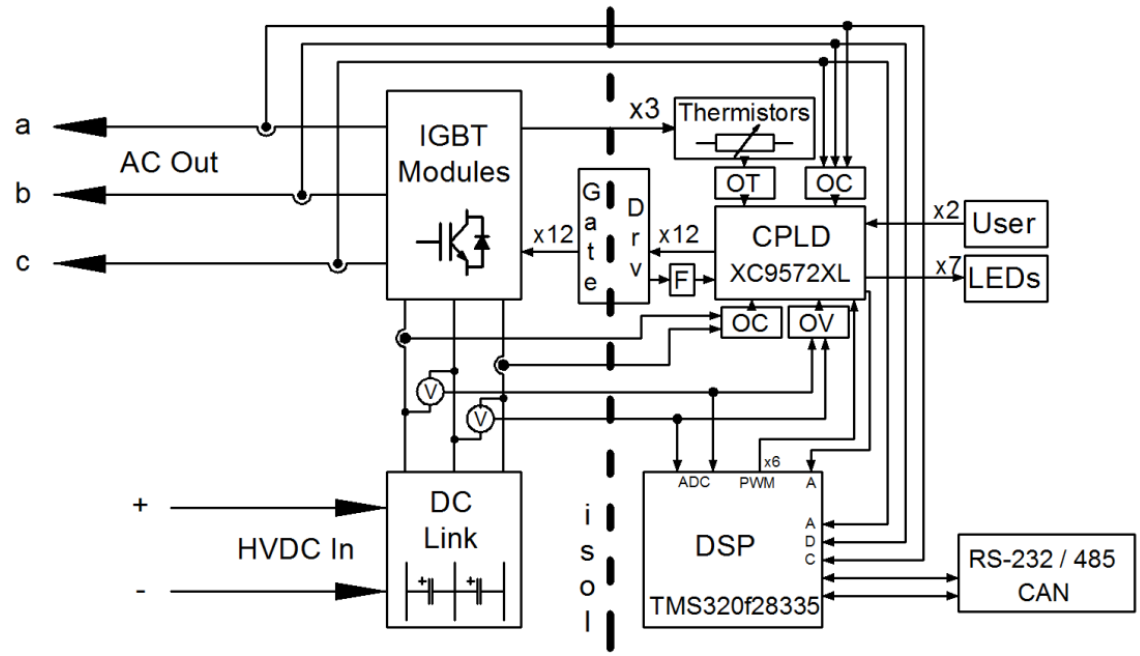


Figure 4-1 – Simplified Schematic of Hardware Platform

The developed schematic is based on two stages – control and power – which are electrically isolated from each other. In the low power, low voltage stage, the DSP supplies the six PWM signals which are a result of the implemented modulation algorithms. The PWM signals from the DSP are transmitted to the CPLD, which manages the insertion of deadtime and PWM signal multiplication. The twelve PWM signals outputs of the CPLD are used by the gate drivers in order to control the three IGBT modules that supply the three phase AC voltage to the desired load. The power input for the modules is the DC Link, a high voltage DC which is supplied with an external DC source and the bulk capacitors form the DC link.

As feedback, the three phase currents are acquired via Hall Effect sensors. Each sensor transmits the analogue signal to the DSP through the ADC. The same signals are used in order to detect an overcurrent event. The upper "OC" block, manages the phase overcurrent / short-circuit situations. The OC block consists of three window comparators that generate an active high fault signal which is transmitted to the CPLD through an AND gate (not shown).

From the DC link, using the same Hall effect sensors, two signals are acquired and used in order to detect a DC Link overcurrent or shortcircuit. The signals are processed through the lower "OC" block. The CPLD is interfaced via an AND logic gate.

The DC link voltages, corresponding to the superior and the inferior halves of the DC link, are acquired using a differential operational amplifier from Linear Technology, LT1366. The signals are fed back to the DSP via its ADC. The same signals are used in "OV" block in order to detect a DC link overvoltage or voltage out of range. The detected overvoltage is processed through an AND gate and fed to the CPLD.

Overtemperature detection is also implemented. Three thermistors are used in order to monitor the temperature on each IGBT module. For each module, the comparators detect two temperature levels. The

six resulted signals are passed thorough and AND logic gate which outputs two signals, one for each level. The two signals are passed to the CPLD. The overtemperature management is included in "OT" block.

Each gate driver outputs an active high fault signal. The twelve signals are tied on a logical AND configuration indicated by the "F" block. The resulting signal is passed to the CPLD. Another two inputs for the CPLD come from the user via two buttons, one for reset / trip and one for initialisation of modulation (not shown). The XC9572 outputs a communication signal for the DSP, marked by the letter "A". Also, seven Light-Emitting Diodes (LED) are controlled by the CPLD in order to show current circuit state.

The DSP receives five analogue signals which are converted in numerical form by the internal ADCs. Furthermore, the six PWM signals are sent to the CPLD. The begging and ending of the modulation is controlled through the "A" pin. The RS-232 / 485 and CAN protocols for communication with other devices are also implemented.

The dotted line which passes through the gate driver block represents the electrical isolation which separates high power circuitry from the low power control stage.

4.2. DC Link Capacitors and Load

The DC link capacitors are used mainly to decouple the effects of the inductance from the DC voltage source. They provide a low impedance path for the ripple currents that are associated with the switching devices of the inverter. There are three main factors that influence the ripple currents: the output inductance of the load, the bus voltage and the PWM frequency of the inverter. These ripple currents are the most important in sizing the electrolytic DC link capacitors [**47**]. Figure 4-2 presents the structure of the DC link capacitors as developed on the experimental board.

Figure 4-2 – DC Link Capacitors from the Developed Experimental Board

These capacitors have to reduce the leakage inductance of the power bridge. The leakage inductances produces inefficiencies throughout voltage spikes when the semiconductors are switched on and off with a high $\frac{dI}{dt}$. If this inductance has a large value the switching time of the semiconductors needs to be increased in order to protect the switching devices from voltage spikes. If this solution is implemented the losses

during turn on and off increase, thus more heat is dissipated through the switching devices, hence the impedance of the DC link has to be low.

When calculating the value of the DC link capacitors the amount DC link capacitance needs to be taken into account as required for the inverter design. There are two important limitations when talking about electrolytic capacitors in the DC link: the ripple current and the voltage that these capacitors can sustain [**47**].

It has been highlighted that the impedance of the load influences the ripple currents in the DC link, thus for the inverter designed a $7.5\ [kW]$ induction motor was chosen as a load. The motor has the following parameters according to [**48**]:

- Power: $7.5\ [kW]$
- Voltage: 220 V
- Poles: 6
- Type: squirrel – cage induction motor
- Stator resistance: $R_s = 0.288\ \left[\frac{\Omega}{phase}\right]$
- Stator inductance: $L_s = 0.0425\ \left[\frac{\mathrm{H}}{phase}\right]$
- Rotor inductance: $L_r = 0.0418\ \left[\frac{\mathrm{H}}{phase}\right]$
- Rotor resistance: $R_r = 0.158\ \left[\frac{\Omega}{phase}\right]$
- Mutual inductance: $L_m = 0.0412\ \left[\frac{\mathrm{H}}{phase}\right]$
- Inertia: $J = 0.4[kg * m^2]$

Taking this information into account the equivalent resistance and inductance per phase can be obtained as: $R_e = 1.57\ [\Omega]$ and $L_e = 64.1\ [mH]$. These calculations were made based on the equivalent schematic of the induction motor.

Based on equivalent impedance per phase, the peak phase current can be written as in equation (4-1).

$$I_{phase} = \left|\frac{V_{ref}}{R_e + j\omega L_e}\right| = 17.15\ [A] \tag{4-1}$$

The three phase currents can be further modelled as in (4-2).

$$\begin{cases} I_a = 17.15\sin(\theta) \\ I_b = 17.15\sin(\theta - \frac{2\pi}{3}) \\ I_c = 17.15\sin(\theta + \frac{2\pi}{3}) \end{cases} \tag{4-2}$$

The only influence in the neutral point is due to small and medium vectors. For maximum modulation index, the reference vector lies in region 3 or 4. If the reference vector lies in region 3, the dwell times for chosen vectors are the one in Table 2-4. Given that only the small and medium vector influences the neutral point, and that in the region 3, the dwell times of small vectors is equally split between N and P state, the RMS value of the NP current for half sector is:

$$I_{np} = \sqrt{\frac{6}{\pi}\int_0^{\frac{\pi}{6}} \left| I_b \sqrt{\frac{T_b}{T_s}} \right|^2 d\theta} = \sqrt{\frac{6}{\pi}\int_0^{\frac{\pi}{6}} \left| 17.15\sin(\theta - \frac{2\pi}{3})\sqrt{2m_a sin\Theta} \right|^2 d\theta} = 12\ [A] \quad (4\text{-}3)$$

Given the neutral point current, the capacitor current can be written as:

$$I_c = C\frac{dU_c}{dt} \quad (4\text{-}4)$$

The total DC link capacitance results as:

$$C_{total} = \frac{I_c dt}{dU_c} \quad (4\text{-}5)$$

For a maximum voltage change of 2 V at 4 kHz switching frequency, the needed capacitance results as 1.5 mF. Given the neutral point current ripple and the needed capacitance, the DC link was modelled using 6 capacitors of 330 µF, each supporting up to 3 A rms current ripple at 450 V. The Panasonic capacitor chosen feature reduced size and 85 °C endurance. Each half of the DC link consists of 3 parallel connected capacitors as seen in Figure 4-3. The total supported current ripple is $18\ A_{rms}$ and the equivalent capacitance is 1.98 mF.

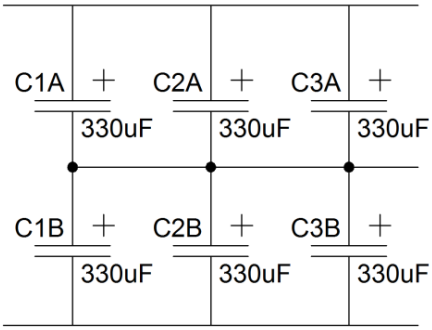


Figure 4-3 – DC Link Configuration Used

4.3. Switching

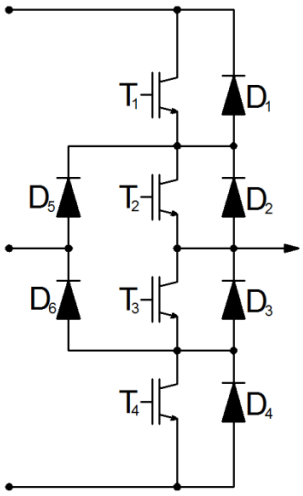
As mentioned earlier, for switching, three NPC IGBT leg modules from Semikron were chosen. The Semitop 3 series module, Figure 4-4, SK50MLI065 features the following [**49**]:

- 600 V / 54 A per IGBT
- Compact design
- One screw mounting
- Snubberless design
- Heat transfer and isolation through Direct Copper Bonded aluminium oxide ceramic (DCB)
- Ultra-fast Non Punch Through (NPT) IGBT technology
- Controlled Axial Lifetime (CAL) technology for freewheeling diodes [**50**]

Figure 4-4 – One NPC Leg IGBT Module [**49**]

The advantage of using modules is that they are designed with special consideration for the commutation paths [**51**]. Large commutation paths would make the circuit prone to high stray inductance. The chosen Semikron modules are designed to minimise the stray inductance problem [**51**].

The CAL technology used for the freewheeling diodes is able to provide 30% more current compared with previous generations. The technology features high power density and high thermal stability and reliability [**50**]. The IGBT leg configuration is shown in Figure 4-5:



- 4 N-channel IGBTs: $T_1 - T_4$
- 4 freewheeling diodes: $D_1 - D_4$
- 2 clamping diodes: $D_5 - D_6$

Figure 4-5 – Internal NPC Module Schematic

The gate switching times as a function of gate resistor R_G, extracted from IGBTs datasheet, is shown in Figure 4-26. Based on this characteristic, in order to have a fall time of 20 ns and a rise time of 25 ns, the value for R_G was chosen to be 20.1 Ω. The switch on delay results as 60 ns and the switch off delay as 300 ns. The switch off delay is the main reason for the chosen value.

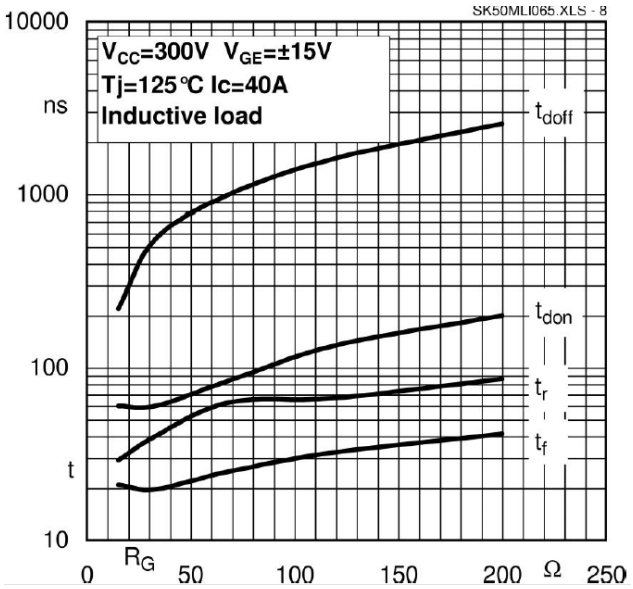


Figure 4-6 – R_G as a Function of Switching Times [**49**]

Given a dead time of 1.5 μs, the switching frequency has to be chose so that the dead time represents only a small fraction of the switching period (calculated in subchapter 4.7). Considering maximum 1% deadtime [**52**], the maximum switching frequency preferred is:

$$\frac{1}{100dt} = \frac{1}{100 \cdot 1.5 \cdot 10^{-6}} = 6.67\ kHz \tag{4-6}$$

Given that the DSP main code run time for the NTV modulation is approximately 0.1 μs and considering that the whole code should run at least twice after each interrupt, the preferred frequency considering the update of the main code inside the 150 MHz DSP of 2.5 times is:

$$\frac{1}{0.1 \cdot 10^{-6} \cdot 2.5} = 4\ kHz \tag{4-7}$$

Based on this, the 4 kHz frequency was used both in the simulations and experiments.

4.4. Gate Drivers and Protections

4.4.1. Gate Drivers

When choosing a gate driver, high interest was focused on a solution which would integrate both optocoupler isolation and protection on a single Integrated Circuit (IC). Avago ACPL-332j, Figure 4-7, was chosen due to its features such as [**53**]:

- Desaturation detection
- Active Miller Clamping
- Isolated Fault feedback
- "Soft" IGBT turn-off
- Under Voltage Lock-Out
- Small package – Small Outline Integrated Circuit SOIC-16
- 50 $kV/\mu s$ Common Mode Rejection (CMR) at VCM = 1500 V
- 2.5 A output current

Figure 4-7 – Avago ACPL-332j Gate Driver [**54**]

The gate driver has an optically isolated power stage capable of driving IGBTs with up to 150 A and 1200 V [**53**] . Under normal operation, the output voltage at pin 11 is controlled by the input LED PWM signals. At the same time, the V_{CE} voltage is monitored. The fault output is active high.

When the voltage on the desaturation pin 14 exceeds 6.5 V while the switching devices are on, the output voltage is "softly" turned off in order to avoid large di/dt voltages [**53**]. At the same time, the fault output is brought low. During "soft" turn-off, all input signal are ignored and the output is shut down for at least 5 μs. The output of the gate driver is a combination of LED PWM input, Under Voltage Lock-Out (UVLO) and desaturation detection.

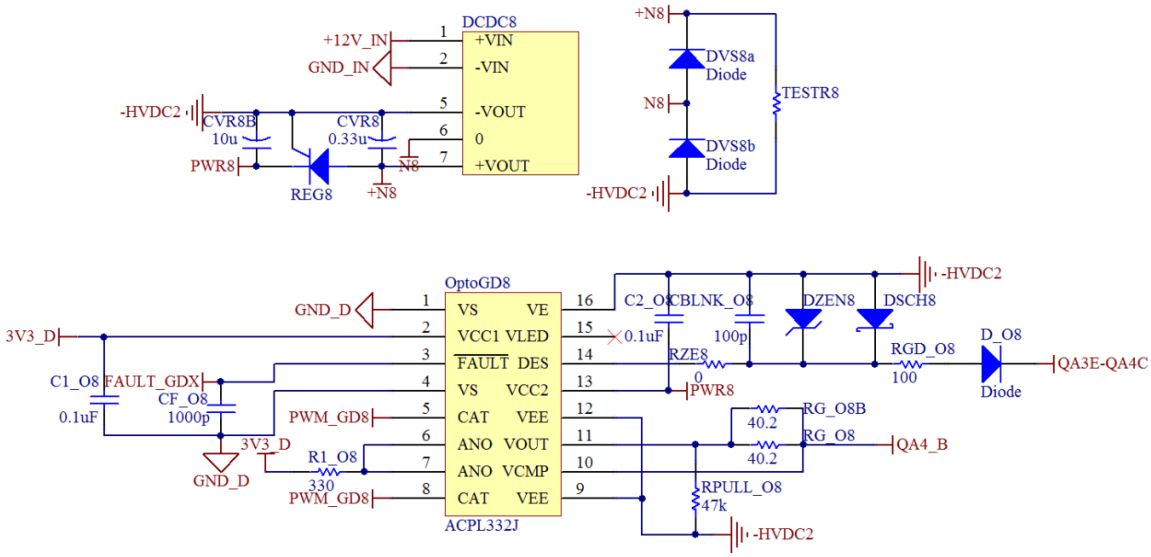


Figure 4-8 – ACPL-332j Circuit Application

The gate driver is used based on the recommended application circuit from Avago datasheet. The implementation for driving the third transistor from leg A is shown in Figure 4-8.

The circuit is powered through the floating isolated dual DC-DC converter DCDC8 from Murata (NMK1212SC). The converter is floating with respect to IGBT emitter voltage. The input voltage is +12 V_{DC} between pin 1 and 2. The output voltage between pin 5 an 7 is 24 V_{DC}. This 2 Watt converter was chosen for the physical form, being rectangular instead of a square, as the other single output 24 V_{DC} DC-DC converters were. The physical form helps in designing a reduced size inverter. Also, if features 3 kV isolation. Two Schottky diodes, B0530W from Taiwan Semiconductor are tied between pins 5-6 and 6-7. The two diodes are used in order to prevent converter damage from reverse current [**55**].

For obtaining the required 18 V for supplying the power part of the gate driver, the L78S18CV voltage regulator from ST Microelectronics is used. The regulator features 2 A current capability, thermal overload protection and shortcircuit protection [**56**]. The 0.33 μF electrolytic capacitor is used for input filtering and the 10 μF electrolytic capacitor is used for improving regulator transient response [**56**] and for supplying high currents needed during transient switching for the IGBT. The TESTR8 resistor is used for debugging purposes.

The Avago ACPL-332j gate driver is formed by two circuits optically separated. The primary input voltage is 3.3 V_{DC} and the secondary input voltage is 18 V_{DC}. The 3.3 V_{DC} is supplied to the pins 2, 6 and 7. Because the signal coming from the CPLD is passed through an inverting buffer, the PWM signal is connected to pin 5 and 8 (cathode) while the anode (pins 6-7) is kept a 3.3 V_{DC} potential. The 330 Ω resistor used limits the input LED current to recommended 10 mA. The low power ground is connected to pins 1 and 4.

The fault signal is transmitted through a LED (pins 5-8). A 0.471 $k\Omega$ pull-up resistor (not shown) is used after the logical AND connection of the twelve fault signals. The 1000 pF capacitor on each fault output is used for filtering. C1_08, a 0.1 μF capacitor is used for bypassing and circuit decouplings. The values chosen are the ones recommended by the datasheet.

In the secondary part of the gate driver circuit, 18 V_{DC} is supplied to pin 13. The power ground (which is the IGBT emitter) is connected to pins 9, 12 and 16. Another 0.1 μF capacitor is used for decoupling. CBLNK_08, D_08, 35 ns diode from Taiwan Semiconductor and the 100 Ω resistor, are required for fault detection. The 0 Ω resistor is used as a simple jumper. The parallel connection of the 10 V_{DC} Zener diode and the 0.5 A Schottky (On Semiconductor) diodes to pins 14 and 16, is used for improving desaturation detection by avoiding false triggering which could happen when the gate driver substrate diode is forward biased. This can happen when the negative voltage spikes due to freewheeling IGBT diode bring the desaturation pin below ground. The Schottky prevents the substrate diode from being forward biased and the Zenner diode prevents positive transient voltage to affect the desaturation pin.

The fast recovery, 35 ns diode is used in order to deny reverse recovery spikes on forwarding the gate driver substrate diode which would lead to false fault detection. The 100 Ω resistor is used to limit the current which could appear due to a negative voltage spike on the desaturation, pin 14. The negative voltage spike can happen when the IGBT anti-parallel diode has a large instantaneous voltage transient [**57**].

The parallel 40.2 Ω resistors from Te Connectivity are 0.1% precision, 0.5 W power devices used as IGBT gate resistors with an equivalent resistance of 20.1 Ω. The resistor limits the gate charge and collector rise and fall times. The value is chosen based on IGBTs characteristics [**49**] from Figure 4-6. The 47 $k\Omega$ resistor is used for pull-down in order to benefit a predictable high level output voltage.

Power dissipation in the gate resistors needs to be checked. Based on [**58**] the peak power dissipation in the gate resistor can be calculated using (4-8) resulting as 16.119 W.

$$P_{peak} = I_{peak}^2 R_G \tag{4-8}$$

The RMS current is the value that needs to be considered. Based on (4-8), the power dissipation in the gate resistor for a 4 kHz switching frequency is 1.07 [mW]:

$$P_g = 2Ig_{RMS}^2 R_G \tag{4-9}$$

The RMS gate current is obtained considering a triangle pulse derivation during turn-on time:

$$Ig_{RMS} = Ig_{peak}\sqrt{\frac{t_p f_{sw}}{3}} \tag{4-10}$$

Under Voltage Lockout [**53**]

The under voltage lockout prevents the application of insufficient voltage in the gate of the IGBT by forcing the output of the gate driver to be low by clamping it. When the V_{CC2} (pin 13) goes above V_{UVLO+} (positive threshold) the UVLO clamp is released and the gate driver will respond to input PWM signals. During the increase of V_{CC2} from 0 V, the first function which becomes active is the desaturation function. UVLO has an integrated hysteresis for improved noise immunity [**57**].

Active Miller Clamping [**59**]

A serious problem when driving IGBTs is the parasitic turn-on. This arises due to the Miller capacitor between gate and collector. During turn-off, a high dv/dt transient could induce a parasitic turn-on which could destroy the power converter. A current flowing through the parasitic Miller capacitor, gate resistor and gate driver internal resistor can create a voltage drop on the gate resistor. If the voltage drop is higher than the IGBT threshold, the parasitic turn-on will occur. Also, gate threshold is reduced by chip temperature increase.

The Miller current can be derived as:

$$I_{CG} = C_{CG}\frac{dV_{CE}}{dt} \tag{4-11}$$

In equation (4-11), the C_{CG} is the Miller capacitor, I_{CG} is the Miller current and V_{CE} is the IGBT collector-emitter voltage. This effect can be seen of both switching devices of a half – bridge configuration. The Miller capacitance can be seen in Figure 4-9.

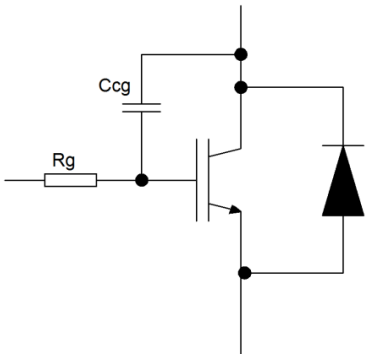


Figure 4-9 – Miller Capacitor

The classical solution for dealing with Miller capacitor is the use of an additional gate-emitter capacitor to shunt the Miller current or the use of a negative power supply in order to increase the threshold voltage for the IGBT. First method suffers from efficiency loss and the second from the increased cost by the use of a negative power supply.

Another solution would be the shorting of gate-emitter path through the help of an additional transistor between gate and emitter. The currents across Miller capacitance are shunted by this transistor and will not flow through the output gate driver pin 11. The gate clamp is activated when, during turn-off, the gate voltage goes below 2 V.

“Soft” Turn-off Feature [**60**]

When short-circuit or overcurrent events occur, the soft turn-off feature helps by improving the designed application reliability. Soft turn-off means that the gate driver output voltage is brought low softly in order to reduce overvoltage spikes caused by lead wire inductances.

This feature is a process which occurs in two stages. The ACPL-332j features two pull-down devices, a weak one (Doubled Diffused Metal Oxide Semiconductor – DMOS) and a larger (fifty times) DMOS transistor. In the first stage, the weak pull-down device will slowly discharge the IGBT. During turn-off the large DMOS remains off until the gate voltage output goes below $V_{EE} + 2$ V. This is the time the large DMOS will clamp the gate voltage to V_{EE}.

Desaturation Detection [**57**]

Desaturation detection and protection are used to ensure the safety operation of IGBTs in short-circuit condition. Desaturation can also occur due to other reasons such as driver supply voltage problems or insufficient driver gate signal. Human error and supply rail short-circuits can cause high power dissipation in the switching devices which lead to device destruction by overheat. The desaturation protection works by monitoring the collector-emitter voltage, V_{CE}. When a high current of a shorcircuit occurs, the voltage will rise. The gate driver detects and triggers a fault when the collector-emitter voltage rises above the internal gate driver desaturation voltage threshold, 6.5 V. When the fault is triggered, the IGBT is “softly” turned off and the fault output is brought low.

While the IGBT is in off state, the fault detection is disabled in order to prevent false triggering. Also, the desaturation fault detection has to be disabled for a small amount of time after the IGBT is turned on in order to allow the V_{CE} voltage to fall below the internal desaturation threshold. The blanking time is controlled by the internal desaturation charge current of 250 μA, the desaturation threshold and the external blanking capacitor. The blanking time is calculated using equation (4-12):

$$t_{blnk} = \frac{C_{blnk} V_{desat}}{I_{chg}} \quad (4\text{-}12)$$

With the recommended 100 pF capacitor, the resulting blanking time is 2.6 μs.

Gate driver fault management, as a combination of LED current I_F, UVLO and desaturation function is shown in Table 4-1:

Table 4-1 – Fault Management [**53**]

I_F	UVLO ($V_{CC2} - V_E$)	DESAT Function	FAULT Output	V_{OUT}
On	Active	Inactive	High	Low
On	Inactive	Active (desaturation fault)	Low (fault)	Low
On	Inactive	Active (no fault)	High (no fault)	High
Off	Active	Inactive	High	Low
Off	Inactive	Inactive	High	Low

4.4.2. Signal Acquisition

To assure that the inverter is working in its safe operating area and that in case of a fault, no hardware destruction occur, different types of hardware protection must be considered. The protections implemented for the proposed design are:

- Phase overcurrent / short-circuit protection
- DC Link overcurrent / short-circuit protection
- DC Link overvoltage / out of range protection and detection
- Over temperature protection
- Integrated gate driver protection

In order to implement these protections, essential measurements have to be made. The phase currents and the DC link currents are measured with Allegro ACS756 Hall Effect based current sensor. The DC link voltages are measured by means of Linear Technology LT1366 differential amplifier. Temperatures are measured using AVX NJ28 Negative Temperature Coefficient (NTC) thermistor.

Currents and voltages have been passed through the TLC372 voltage comparators used in a window configuration. The temperature signals are compared with two levels. All signals are passed through AND gates and then supplied to the CPLD. The CPLD will further stop the modulation in case of a fault and output the fault condition through LEDs. All fault management is performed through the CPLD.

Current Signal Acquisition

Allegro ACS756 Hall Effect IC sensor is a precise and economical solution for current sensing in AC and DC. The low-offset linear Hall circuit converts the current flowing though the conductive path and generates proportional magnetic field which is then converted into a voltage signal. The obtained voltage is precise due to low-offset chopper stabilised IC. The Allegro ACS756, shown in Figure 4-10, benefits from the following features [**61**]:

- Industry-leading noise performance
- Total output error 0.8%
- Monolithic Hall IC
- Ultra-low power loss: 130 $\mu\Omega$ conductor resistance
- 3 kV RMS minimum isolation
- Nearly zero magnetic hysteresis
- Small package size
- Measurement of ±50 A
- Chopper stabilisation technique

Figure 4-10 – Allegro ACS756 Hall Current Sensor

The current sensors are used in the configuration shown in Figure 4-11 for both phase current acquisition and DC link current acquisition. The shown example from Figure 4-11 is for phase A. The 0.1 μF capacitor is used for bypassing and the 100 pF capacitor is recommended for filtering [**61**]. The current path is through pins 4 and 5. The 5 V_{DC} analogue supply voltage is connected to pins 1-2. The output voltage signal is yielded at pin 3. Tbe SNS_CRTx (where x=1:3) signal outputs have a value of 2.5 V_{DC} for 0 A and $\pm 40\ mV/A$ characteristic.

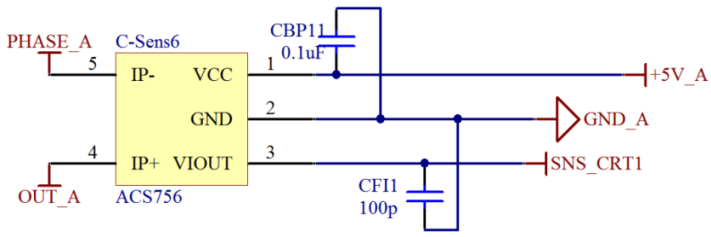


Figure 4-11 – ACS756 Current Acquisition

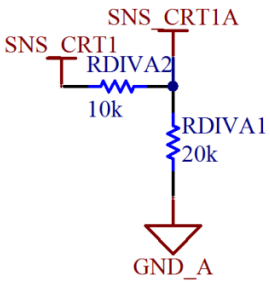


Figure 4-12 – Phase Signal Divider

For a correct ADC interface, the 2.5 V_{DC} for 0 A has to be brought to about 1.5 V_{DC}. This is performed through a divider on each SNS_CRTx signal (where x=1:3), like in Figure 4-12. The resulting signal, SNS_CRTxA (where x=1:3) has a value of:

$$SNS\_CRTxA = \frac{RDIVA1 \cdot SNS\_CRTx}{RDIVA1 + RDIVA2} = \frac{20 \cdot 10^3 \cdot SNS_{CRTx}}{30 \cdot 10^3} = 0.6666 \cdot SNS\_CRTx \quad (4\text{-}13)$$

The SNS_CRTxA signal could be written as a function of measured current, equation (4-15).

$$SNS\_CRTxA = k_{cs} I_{SNS} \tag{4-14}$$

Where k_{cs} is defined as in equation (4-15).

$$k_{cs} = \frac{RDIVA1 \cdot (40 \cdot 10^{-3} \cdot I_{meas} + 2.5)}{RDIVA1 + RDIVA2} \tag{4-15}$$

For a current of 0 A through the sensor, SNS_CRTxA will have a value of 1.666 V_{DC}. The $\pm 40\, mV/A$ characteristic is also changed by the divider based on equation (4-13) to $\pm 26.666\, mV/A$. The SNS_CRTx signals are passed to the window comparators and the SNS_CRTxA signals are supplied to the ADC through voltage followers (buffers).

Voltage Signal Acquisition

An effective and economical solution for acquirement of voltage signals is the use of a differential operational amplifier connected to the DC Link through high value resistors. The resistor network used is composed of four High Voltage Direct Current (HVDC) connections through three series resistors (470k+470k+560k). The series connection of the resistors ensures that the connection to the DC link will not fail, as the current is small compared to resistors current capability.

The operational amplifier chosen is Linear Technology LT1366. The application of LT1366 is shown in Figure 4-13. The choice was made for to the features that this amplifier benefits of:

- Input common mode range includes both rails
- Output swing rail-to-rail
- Low offset voltage
- High Common Mode Rejection Ratio – 90dB
- Power Supply Rejection Ration – 105 dB
- Low input bias current – 10nA
- Low supply current
- 400 kHz gain bandwidth

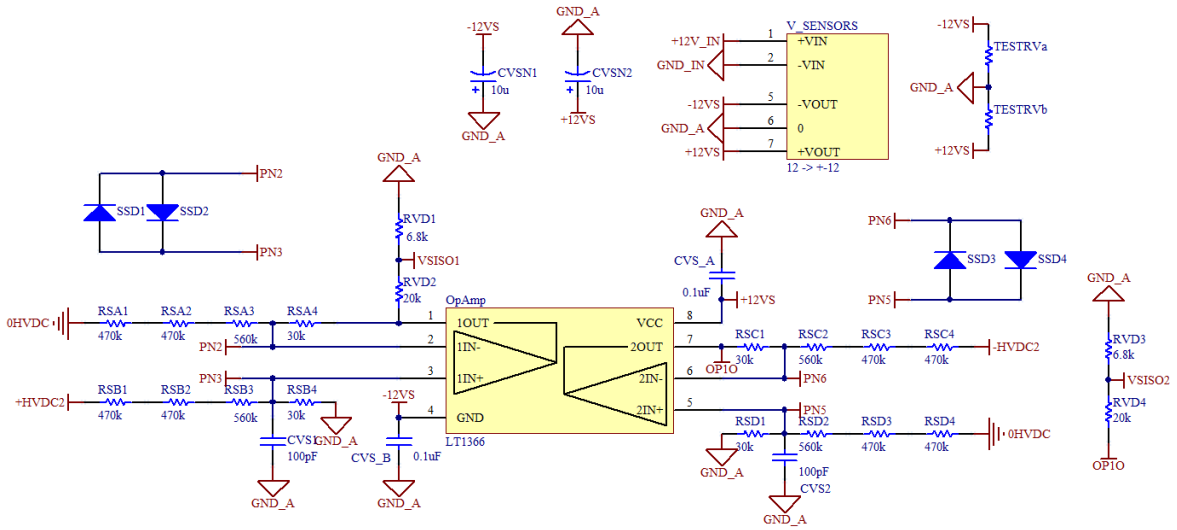


Figure 4-13 – LT1366 Voltage Acquisition

The LT1366 is a dual operational amplifier supplied by a dual $\pm 12\, V_{DC}$ isolated DC-DC converter (NMK1212SC from Murata). A voltage of +12 V_{DC} is supplied at pin 8 and -12 V_{DC} at pin 4. Both pins are bypassed by a 0.1 μF capacitor. The DC-DC converter is bypassed by two 10 μF electrolytic capacitors, one between pins 5-6 and the other between pins 6-7. Resistors TESTRVa and TESTRVb are for debugging purposes.

The inputs of each comparator are protected from DC link voltage transients through a pair of antiparallel small signal diodes (TS148 from Taiwan Semiconductor). As said earlier, the high voltage signal is passed through four series of three resistors with an equivalent resistance of 1.5 $M\Omega$. The 100 pF capacitor on both non-inverting inputs forms with the resistors a low-pass filter. The cut-off filter frequency results as in (4-16) where R=1.5 $M\Omega$ and C=100 pF.

$$f_c = \frac{1}{2\pi RC} = \frac{1}{2\pi 1.5 \cdot 10^6 \cdot 100 \cdot 10^{-12}} = 1.06\, kHz \tag{4-16}$$

The transfer function of each operational amplifier, configured as a differential amplifier, is derived as an example for first amplifier as in equation (4-17). In the normal operating condition, +HVDC=300 V, 0HDVC=0 V and –HVDC=-300 V. The second output can be calculated in the same manner, equation (4-18).

$$V_{1OUT} = \frac{RSA4}{RSA1 + RSA2 + RSA3}(+HVDC2 - 0HVDC) = \frac{30 \cdot 10^3}{1.5 \cdot 10^6}(300 - 0) = 6\, V_{DC} \tag{4-17}$$

$$V_{1OUT} = \frac{RSC1}{RSC2 + RSC3 + RSC4}(0HVDC - -HVDC) = \frac{30 \cdot 10^3}{1.5 \cdot 10^6}(0 - -300) = 6\, V_{DC} \tag{4-18}$$

Both 6 V_{DC} outputs are passed through a voltage divider in order to obtain $\sim 1.5\, V_{DC}$. The VSISO1 and VSISO2 voltages will have for 300 V_{DC} an output of:

$$VSISO1 = VSISO2 = \frac{RVD1}{RVD1 + RVD2}6 = \frac{RVD3}{RVD3 + RVD4}6 = \frac{6.8 \cdot 10^3}{26.8 \cdot 10^3}6 = 1.522\ V_{DC} \quad (4\text{-}19)$$

Combining (4-17), (4-18) and (4-19), the VSISOx (where x=1,2) could be written as:

$$VSISOx = k_{VS} \cdot HVDC2 \quad (4\text{-}20)$$

Where:

$$k_{VS} = \frac{RSA4 \cdot RVD1}{(RSA1 + RSA2 + RSA3)(RVD1 + RVD2)} = 0.0050733 \quad (4\text{-}21)$$

The VSISOx signals are passed through the window comparators and then to the ADC through operational amplifier voltage followers (buffers).

Temperature Signal Acquisition

The temperature is acquired using NJ28 high accuracy thermistors from AVX. The thermistors have a resistance of 100 $k\Omega$ at 25 °C, which decreases with the temperature increase – thus having a NTC characteristic. Temperature acquirement setup is shown in Figure 4-14:

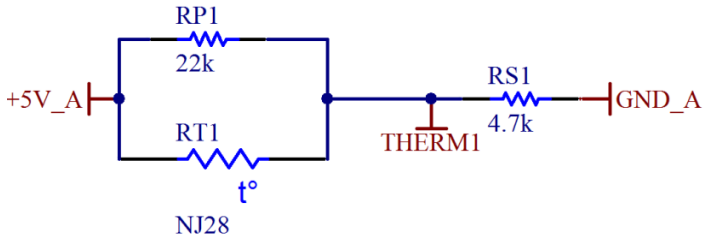


Figure 4-14 – NJ28 Temperature Acquisition

Each thermistor, RTx (x=1:3) is connected in parallel with a 22 $k\Omega$ resistor and the resulted value signal is passed through a voltage divider in order to modify the NJ28 characteristic. They are supplied with 5 V_{DC}.

The output voltage of the thermistors becomes (example shown for RT1), equation (4-22):

$$THERM1 = \frac{RS1 \cdot 5}{RS1 + (\frac{RP1 \cdot RT1}{RP1 + RT1})} \quad (4\text{-}22)$$

THERM1 values for important temperatures are shown in Table 4-2, calculated using (4-22).

Table 4-2 – Output Signal from Thermistor Acquisition

Degree Celsius	RT1 Value $k\Omega$ [**62**]	THERM1 Output V_{DC}
25	100	1.0337
70	14.83	1.4994
75	12.28	1.6106
80	10.22	1.7332
85	8.537	1.8679

The THERMx signals are compared with two pre-settable values and the result is passed to the CPLD through logical AND gates.

Signal Processing Through Windows Comparators

The TLC372 from Texas Instruments was chose due to following features [**63**]:

- Fast response time: 200 ns typical
- Low supply current drain: 150 μA at 5 V_{DC}
- High input impedance: 10^{12} Ω

The voltage signals corresponding to phase currents, DC link currents and DC link voltages are passed through windows comparators with an active high output [**64**] when the signal is in the window limits. The TLC372 [**63**] voltage comparator from Texas Instruments features two comparator per each IC, which are connected in a window configuration as shown in Figure 4-15 (example for phase A current):

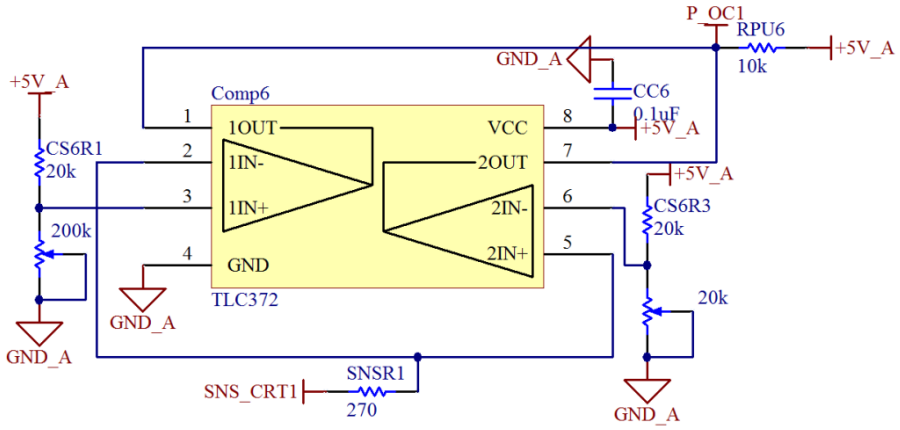


Figure 4-15 – Window Comparator Configuration

The comparator IC is supplied with 5 V_{DC} at pin 8 and bypassed with a 0.1 μF capacitor. The signal to be compared is fed to pin 2 (inverting input for first comparator) and pin 5 (non-inverting input for the second comparator). The "window" is formed by the reference voltages supplied at pins 3 and 6. The high reference is supplied at the non-inverting input pin 3 and the low reference to the inverting pin 6. The high reference is always greater than the low reference voltage. Each voltage reference is obtained by means of a voltage divider between a potentiometer, configured as a variable resistor and a fixed 20 $k\Omega$ resistor. The output signal is the union of first comparator output from pin 1 and the second comparator output from pin 7. The signal is pulled up through a 10 $k\Omega$ resistor. Signals should not go above the maximum common mode input voltage of 3.5 V_{DC}.

When the input signal voltage is between the two references, the output will be high and low when the input signal is out of the voltage window from Figure 4-16 . The output signal is the thick dashed line and the input is the thin arrow-ended line.

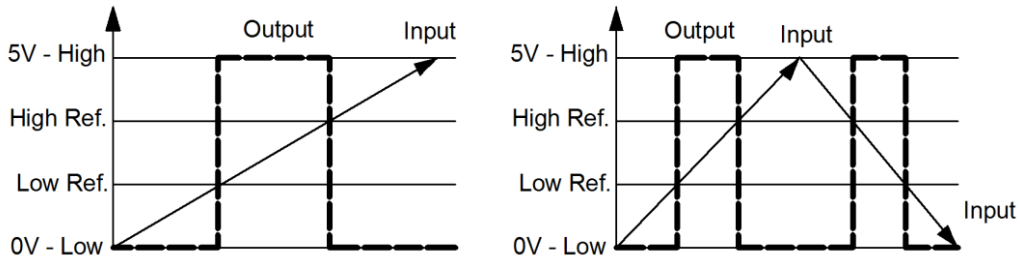


Figure 4-16 – Window Comparator Operation

4.4.3. Protection Adjustment

The phase overcurrent and DC link overcurrent protection should be adjustable in $\pm 50\ A$ range. The input signal for the window comparators is 1.666 V_{DC} for 0 A and the sensitivity is $\pm 26.666\ mV/A$. The output voltage, using (4-14), will be 2.9993 V_{DC} at +50 A and 0.3327 V_{DC} at -50 A. Based on these values, the potentiometers for high reference voltage and the one for low reference voltage can be chosen. For the low reference value a potentiometer of 20 $k\Omega$ was chosen, and for the high reference value a potentiometer of 200 $k\Omega$. The choice is viable for both phase overcurrent protection as for DC link overcurrent protection.

The over temperature protection should have two pre-settable levels. First level should be settable up to 70°C and the second level should be settable up to 80°C. For both levels one potentiometer with the value of 100 $k\Omega$ was chosen.

The DC link voltages should be settable to deviate up to $\pm 10\%$ of the DC link voltage. At 300 V_{DC}, the output of the voltage sensing is 1.522 V_{DC}. For 330 V_{DC}, the output signal will be 1.674 V_{DC} and for 270 V_{DC} will be 1.37 V_{DC}. For the low voltage reference a 10 $k\Omega$ potentiometer is chosen and a 20 $k\Omega$ potentiometer for the high voltage reference.

For management and further fault notification, two SN75F21D AND logical gates from Texas Instruments are used. Each IC contains three AND logical gates with three input each. The choice was made due to 3.2 ns fast switching times [**65**]. Each gate is decoupled by a 0.1 μF capacitor. Through these gates, the outputs of the three window comparator for phase overcurrent detection are merged into a single signal informing about a fault condition regarding the current on one of the phases. The operation is logical AND because the fault signals are active high. Furthermore, the signal is supplied to the CPLD.

The output of the six comparators used for over temperature detection are merged through the AND gates in order to have two fault signals – one representing the first temperature level threshold and another representing the second temperature threshold. These two signals are also supplied to the CPLD.

The two outputs regarding DC link overvoltage are also merged through the AND gates into a single signal. The DC link overcurrent conditions are performed in the same manner. The gate drivers fault signals are tied in a wired AND connection. The final fault signals supplied to the CPLD are:

- OT_A - which will switch low when one of the temperature of the IGBT modules will go above first threshold level
- OT_B - which will switch low when IGBTs temperature goes above second threshold level
- DC_OV - will switch low when there is an overvoltage on one of the DC link halves
- DC_OC - will switch low if there is an overcurrent condition on the two DC link halves
- OCR - which switches low if a overcurrent condition occurs on any of the three phases
- FAULT_GDX - which will be low if any of the twelve gate drivers encounters a fault

The three phase currents and the two DC link voltages are transmitted to the ADC block of the DSP. The interfacing is made through five operational amplifiers configured as voltage followers. The chosen amplifier is also recommended by Texas Instruments – OPA234, the manufacturer of the DSP. These are chosen due to features such as rail-to-rail input/output, low noise and low quiescent current [**66**]. The voltage follower configuration is shown in Figure 4-17 for the signals corresponding to the currents on two phases. The configuration used is the same for the other signals.

Each OPA2343 IC contains two operational amplifiers. The IC is supplied with 3.3 V_{DC} from the analog supply. The 0.1 μF capacitor on pin 8 is used for bypassing. The 100 Ω resistor and the 0.1 uF capacitor on the outputs of each operational amplifier are used as a low-pass filter for ADC input. Other scope of the two components is to be used as a flywheel for the currents pulses created by the ADC's input circuitry [**67**] . The resulted filter cut-off frequency is 15.91 kHz, calculated using (4-16).

The buffer input signals and the ADC input signals are protected from going over 3.3 V_{DC} or below ground potential using a pair of dual series small signal Schottky diodes (BAT54S) from ST Microelectronics, Figure 4-17. The chosen solution is made due to low conduction and reverse losses, low forward and reverse recovery times, low capacitance and extreme fast switching (8 ns) [**68**].

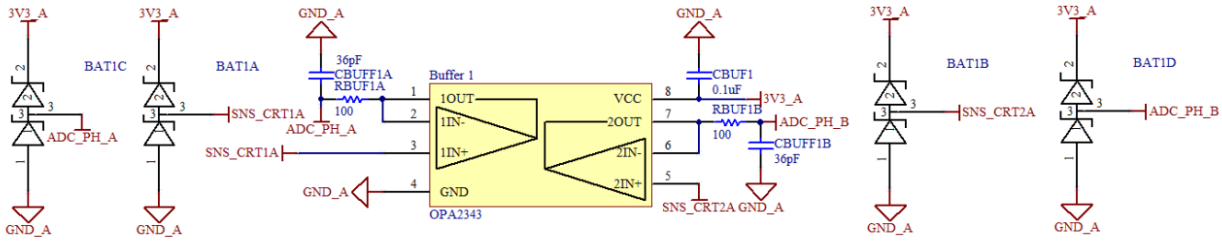


Figure 4-17 – OPA2343 Buffer Solution

4.4.4. Voltage Supply and Regulators

The developed PCB is divided in two main areas: HVDC area and low voltage – control area. The HVDC is supplied through an external power supply. For the control area, a 12 V_{DC} also must be supplied externally.

The low voltage area has three parts: analog, digital and isolated communications area. For this purpose, three isolated DC-DC converters from Traco Power (TEL3-1211) are used. These converters feature high

efficiency, 1.5 kV isolation, and short-circuit protection and regulated 5 V_{DC} output. Power supplied is up to 3 W [**69**]. The output of each DC-DC converter is decoupled by a 33 μF capacitor.

In order to obtain 3.3 V_{DC}, the Texas Instruments TPS79533 regulator was chosen due to its features:

- 500 mA low dropout regulator
- Ultralow noise
- 50 μs start-up
- Very low dropout voltage, 110 mV at full load
- High Power Supply Rejection Ration (PSRR)
- Internal current limiting and thermal protection

The application of TPS79533 is show in Figure 4-18 . The datasheet [**70**] recommends a 2.2 μF filtering capacitor near the input of the regulator – pins 1 and 2. The output capacitor, used to stabilize the internal control loop is chosen to be 2.2 μF and connected between pin 4 and 6. The 0.01 μF capacitor is user for bypassing the NR pin. Together with the internal 250 $k\Omega$ resistor, a low pass filter is created for the internal voltage reference.

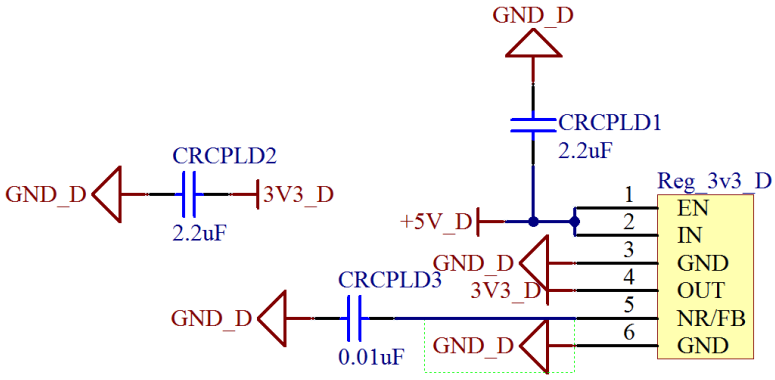


Figure 4-18 – TPS79533, 3.3 Vdc Voltage Regulator

Three 3.3 V_{DC} regulators are used on the board design. The given example, Figure 4-18, is for obtaining desired voltage level for powering digital circuitry. The other two regulators supply 3.3 V_{DC} to analog circuitry and isolated communication circuitry. Their usage is the same as give in Figure 4-18 .

In Table 4-3 the low voltage sequencing is shown. Each voltage type has its own ground and power planes. The analogue and digital grounds meet near the DSP.

Table 4-3 – Voltage Type and Levels used on the Experimental Board

Type	Voltage Levels [V_{DC}]			
Input	12			
Isolated	3.3		5	
Analog	-12	3.3	5	12
Digital	3.3		5	
Floating	-12	12	18	24

4.4.5. Communication

The DSP can communicate with external CPUs through the CAN or RS-232 / 485 protocols. Hardware implementation for CAN and RS-232 / 485 is shown in Figure 4-26. Through the D_Isolator1, signals needed for RS-485 communication are isolated. Furthermore, the CAN signal isolation is obtained through the D_Isolator2. The digital isolator chosen is the ISO7221 from Texas Instruments, featuring up to 150 Mbps signalling rate, low Pulse Width Distortion (PWD), low jitter (1 ns), 4 kV isolation and high electromagnetic immunity [**71**].

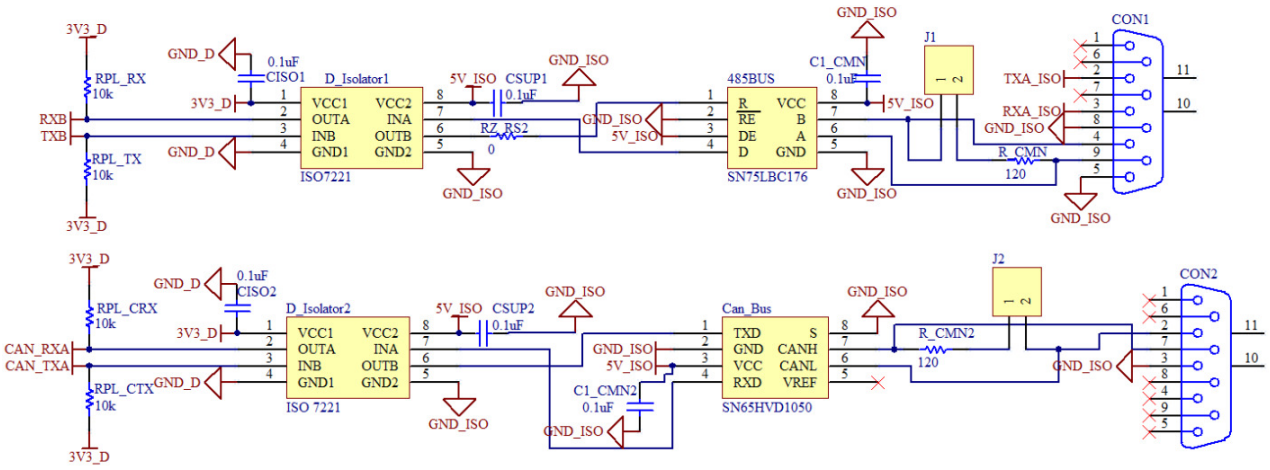


Figure 4-19 – CAN and RS-232 / 485 Communication

The digital isolators are powered with 3.3 V_{DC} from the digital supply on the PCB side and with 5 V_{DC} from isolated supply for the output side. Both are decoupled by a 0.1 μf capacitor. The 0 Ω resistor on pin 6 of the D_Isolator1 is to be soldered only if RS-485 is going to be used. The input of the D_Isolator1 is formed by RXB and TXB signals coming from the DSP. The D_isolator2 input is composed of CAN_RXA and CAN_TXA also coming from the DSP. All digital isolator input signals are pulled-up with a 10 $k\Omega$ resistor.

The signals for RS-485 communication are passed through SN75LBC176 differential bus transceiver from Texas Instruments, featuring bidirectional transmission, high speed, low skew, current limiting and thermal shutdown protection [**72**]. The IC is supplied with 5 V_{DC} from the isolated supply and bypassed with 0.1 μF capacitor. The driver and the receiver enable pins 2 and 3, RE and DE, connected to the 5 V_{DC} supply (DE pin) and ground (RE pin). A and B are the driver outputs and R is the receiver output. The jumper J1 is used to enable or disable the 120 Ω termination resistor.

The output of the transceiver together with the RXA_ISO and TXA_ISO are received from the DSP and are interfaced through a serial DE-9 connector. RXA_ISO and TXA_ISO are connector to pins 2 and 3 of the RS-232 communication. Pins 4-8 and 5-9 are used for RS-485 communication [**73**].

The CAN signals are passed through SN65HVD1050 CAN transceiver from Texas Instruments. It features high electromagnetic immunity, low electromagnetic emissions and bus fault protection [**74**]. The IC is supplied with isolated 5 V_{DC} and bypassed with 0.1 μF capacitor. The J2 jumper is used to enable or disable the 120 Ω

resistor termination. The output signals are transmitted to the outside world through another DE-9 connector, that has pins 2 and 7 used for data [**75**].

4.5. Power Tracks Sizing

The current carrying capability of the PCB has to be calculated prior to the board manufacture. The maximum current is proportional to the cross-sectional area of the tracks. The copper thickness is 70 µm. Given the minimum width of the DC link track as 6.73 mm and of the phase track as 10.5 mm, the maximum current [**76**] can be calculated as in equation (4-23).

$$I = k\Delta T^{0.44} A^{0.725} \tag{4-23}$$

Where I is the current in amperes, A is the cross section in square mills and ΔT is the temperature rise in Celsius degree between ambient temperature and the safe operating temperature of the PCB [**76**]. The constant k is defined as k=0.048 for outer layers and k=0.024 for inner layers. Knowing that 1 mil = 0.0254 mm, the equation (4-23) can be modified to be used with the metric units, thus resulting equation (4-24).

$$I = k\Delta T^{0.44} \left(\frac{A}{0.0254^2}\right)^{0.725} \tag{4-24}$$

Using equation (4-24), the current carrying capability of the DC link, for a temperature rise of 55 °C, results as 33 A for outer layers and 17 A for inner layers. For the same temperature rise, the phase current for inner layers results as 23 A for inner layers and 46 A for outer layers. The above calculation is validated through thermal imaging in subchapter 4.8.

4.6. Cooling

An important role is hold by maximum electrical ratings and thermal limitations of semiconductor devices. There needs to be taken into account that the operating junction temperature of all devices does not exceed the limits under all specified conditions [**77**]. The Semikron modules have high thermal performance and integrate latest silicon technology, thus the result has high efficiency and cost effectiveness. These modules are used for PCB soldering, Figure 4-20. A single mounting screw and the copper baseplate are used in order to ensure thermal performance [**78**].

Figure 4-20 – NPC Leg Module – Copper Baseplate

The inverter designed in this thesis has a power rating of 8 $[kW]$ at a frequency of 4$[kHz]$. Semikron offers an application note for loss calculation [**51**]. The analytical method presented in this application note is based on [**79**]. The cross – sectional view of a typical Semikron IGBT package can be seen in Figure 4-21.

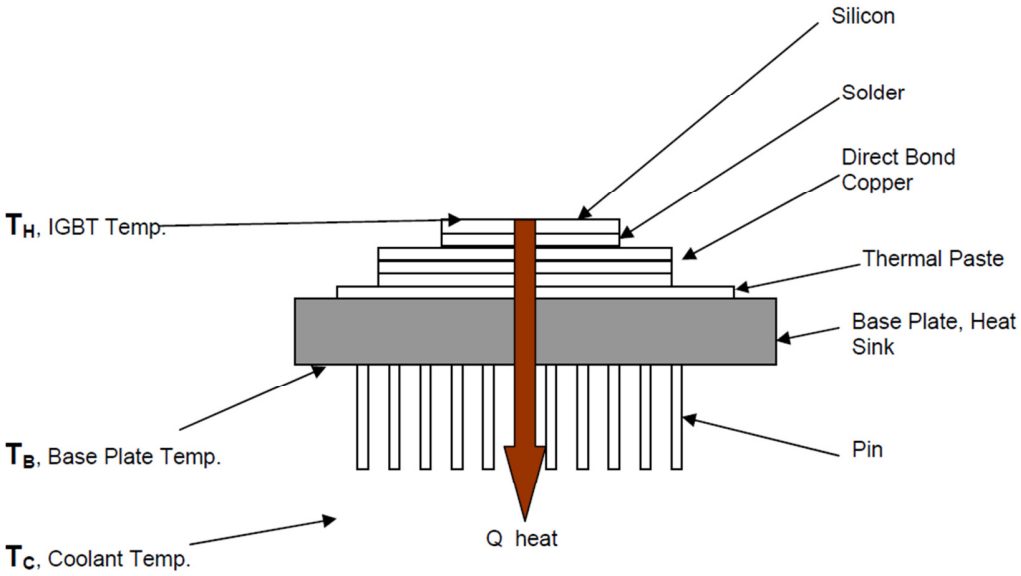


Figure 4-21 Typical IGBT Structure – Layers and Heat Flow Path [**80**]

On the three level NPC configuration presented in **Chapter 2** the conduction losses for transistors T1 and T4 can be calculated in the same manner. This is presented in (4-25).

$$P_{cond} = \frac{M\hat{I}}{12\pi}\{3V_{ce0}[(\pi - \varphi)\cos\varphi + \sin\varphi] + 2r_{ce}\hat{I}[1 + \cos\varphi]^2\} \quad (4\text{-}25)$$

Where:

- M – Modulation index
- $\hat{I}$ – Peak value of current
- V_{ce0} – IGBT forward threshold voltage
- φ – conduction angle
- r_{ce} – IGBT on – state slope resistance

For a proper calculation regarding the thermal resistance of the heatsink NTV-EHE modulation strategy was taken into account. As a load, for thermal calculations, an induction motor with the power rating of 8 $[kW]$, peak current of 19.2 $[A]$, power factor of 0.85 and a voltage of 400 $[V]$ was considered. Considering these informations the conduction angle was calculated and it has a value of 0.554.

The switching losses for transistors T1 and T4 are calculated as in equation (4-26).

$$P_{sw} = f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_l}\left(\frac{V_{cc}}{V_{ref}}\right)^{K_v}\left(\frac{1}{2\pi}[1+\cos\varphi]\right)^{1-K_l}G_l \tag{4-26}$$

Where:

- f_{sw} – Switching frequency
- E_{sw} – Sum of energy dissipation during turn – on and turn – off time
- K_l – Exponent for the current dependency of the switching losses
- I_{ref} – Reference current value of the switching loss measurement
- K_v – Exponent for the voltage dependency of the switching losses
- V_{cc} – Collector – emitter supply voltage
- V_{ref} – Reference voltage value of the switching loss measurement
- G_l – Adaptation factor for the non – linear semiconductor characteristics

Conduction losses for transistors T2 and T3 are calculated based on (4-27).

$$P_{cond} = \frac{\hat{I}}{12\pi}\{V_{ce0}[12+3M(\varphi\cos\varphi-\sin\varphi)]+r_{ce}\hat{I}[3\pi-2M(1-\cos\varphi)^2]\} \tag{4-27}$$

In order to calculate the switching losses for transistors T2 and T3 formula (4-28) is used.

$$P_{sw} = f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_l}\left(\frac{V_{cc}}{V_{ref}}\right)^{K_v}\left(\frac{1}{2\pi}[1-\cos\varphi]\right)^{1-K_l}G_l \tag{4-28}$$

The formula for conduction losses on the clamping diodes D5 and D6 is presented in (4-29).

$$P_{cond} = \frac{\hat{I}}{12\pi}\{V_{f0}\big[12+3M[(2\varphi-\pi)\cos\varphi-2\sin\varphi]\big]+r_f\hat{I}[3\pi-4M(1+\cos^2\varphi)]\} \tag{4-29}$$

Where:

- V_{f0} – Diode collector – emitter threshold voltage
- r_f – Diode on – state slope resistance

In order to calculate the switching losses for the clamping diodes D5 and D6 formula (4-30) is used.

$$P_{sw} = f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_l}\left(\frac{V_{cc}}{V_{ref}}\right)^{K_v}\left(\frac{1}{2\pi}[1+\cos\varphi]\right)^{1-K_l}G_l \tag{4-30}$$

Conduction losses for reverse recovery diodes D1 and D4 are calculated as (4-31):

$$P_{cond} = \frac{M\hat{I}}{12\pi}\{3V_{f0}[-\varphi\cos\varphi + \sin\varphi] + 2r_f\hat{I}[1-\cos\varphi]^2\} \quad (4\text{-}31)$$

Based on equation (4-32) the switching losses for reverse recovery diodes D1 and D4 are calculated.

$$P_{sw} = f_{sw}E_{sw}\left(\frac{\hat{I}}{I_{ref}}\right)^{K_l}\left(\frac{V_{cc}}{V_{ref}}\right)^{K_v}\left(\frac{1}{2\pi}[1-\cos\varphi]\right)^{1-K_l}G_l \quad (4\text{-}32)$$

The formula for conduction losses on reverse recovery diodes D2 and D3 are presented in (4-33).

$$P_{cond} = \frac{M\hat{I}}{12\pi}\{3V_{f0}[-\varphi\cos\varphi + \sin\varphi] + 2r_f\hat{I}[1-\cos\varphi]^2\} \quad (4\text{-}33)$$

Switching losses for reverse recovery diodes D2 and D3 are presented in (4-34).

$$P_{sw} = 0 \quad (4\text{-}34)$$

The typical values for K_v, K_l, and G_l are found on the Semikron modules datasheet for three level NPC and three level Type Neutral Point Clamped (TNPC). They are presented in Table 4-4.

Table 4-4 – Typical K_v, K_l, and G_l for Semikron Modules [**51**]

	IGBT	Diode
K_v	1.4	0.6
K_l	1	0.6
G_l	1	1.15

In order to calculate the thermal resistance of the heat sink the total losses in the NPC leg need to be calculated. The absolute maximum ratings described in (NPC leg datasheet) are used. The other parameters are selected based on the NTV modulation strategy. The most important ratings are:

- $V_{cc} = 300\ [V]$
- $V_{ref} = 600\ [V]$
- $V_{ce0} = 2.2\ [V]$
- $r_{ce} = 22\ [m\Omega]$
- $f_{sw} = 4000\ [Hz]$
- $E_{sw} = 1.83\ [mJ]$ – for each IGBT
- $E_{sw} = 1[mJ]$ – for each diode
- $V_{f0} = 0.85\ [V]$
- $r_f = 11\ [m\Omega]$ – freewheeling diode
- $r_f = 22\ [m\Omega]$ – antiparallel diode
- $T_s = 80$ [°C]

The ambient temperature was considered to be $T_a = 25$ [°C]. By solving the equations presented above conduction losses on each device are obtained and presented in Figure 4-22.

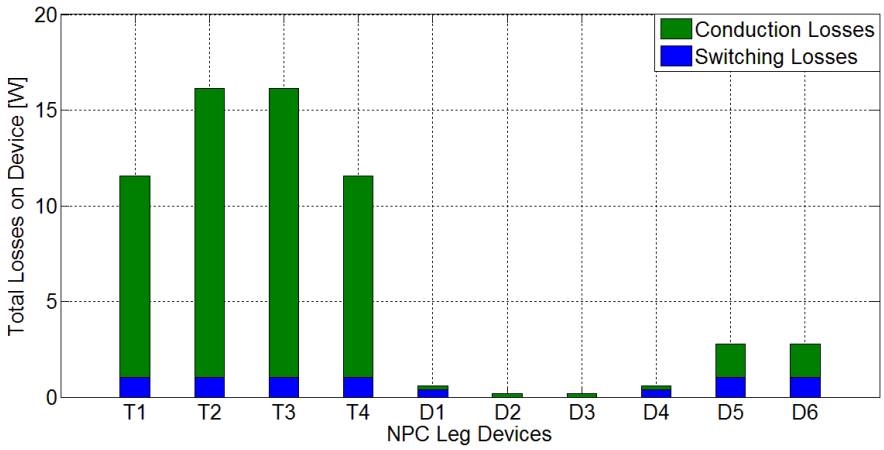


Figure 4-22 – Losses on Each Component in the NPC Leg

Taking all the calculated losses into account the equivalent thermal model for the NPC converter can be drawn. The equivalent model of the thermal behaviour can be seen in Figure 4-23. This represents the Semikron Semitop3 Module with the structure presented in the beginning of this chapter (Figure 4-4). From the thermal point of view the NPC leg has been considered to be built of ten parallel heat sources, correspondent into electrical terms as current sources. The model presented in Figure 4-23 describes each device from the NPC converter leg. The temperature difference between each nod is considered to be a voltage drop on the equivalent thermal resistance. There are three types of thermal resistances that are generally considered: junction – to – case resistance $R_{th\ jc}$, case – to – heat sink resistance $R_{th\ cs}$, sink – to – ambient resistance $R_{th\ sa}$. The junction – to – case resistance and case – to – heat sink resistance are offered by the producer in the datasheet. Semikron gives in [**49**].the thermal resistance between junction and heat sink for each device:

- $R_{th\ js} = 0.85\ \frac{K}{W}$ per IGBT.
- $R_{th\ js} = 1.7\ \frac{K}{W}$ per antiparallel diode
- $R_{th\ js} = 1.1\ \frac{K}{W}$ per freewheeling diode.

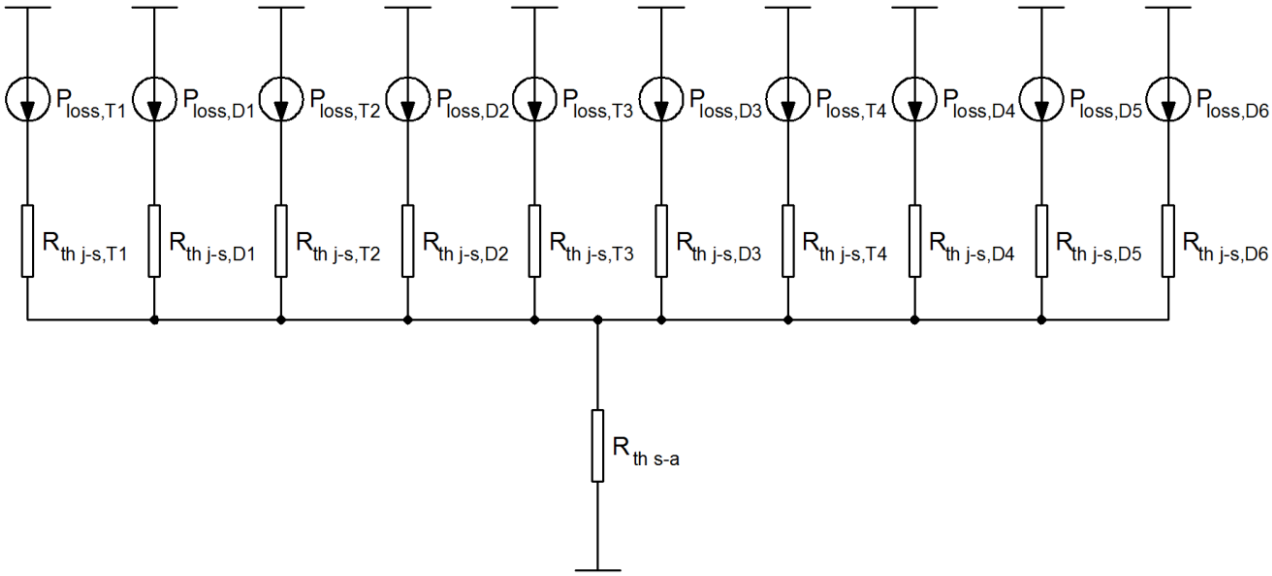


Figure 4-23 Thermal Model of Semikron SEMITOP Module (NPC Leg)

When talking about the heat sink all devices that produce heat has to be taken into account. One of the important components that need cooling is the voltage regulator that supplies the gate driver. There are 12 gate drivers, thus 12 voltage regulators need to be used. These voltage regulators are supplied with $24\ [V]$ and have $18\ [V]$ at the output. The power dissipation on these devices has been calculated based on [**81**] [**82**]. This is presented in equation (4-35).

$$P_D = [(V_{in} - V_{out})I_{load}] + (V_{in}I_{gnd}) \tag{4-35}$$

Where:

- P_D – Power dissipation
- V_{in} – Input voltage supplied to the regulator
- V_{out} – regulator output voltage
- I_{out} – regulator output current
- I_{gnd} – Regulator biasing currents

In general, when talking about thermal considerations the worst case scenario needs to be used. The output current of the voltage regulator is decided by the gate driver, thus $I_{load} = 8.33\ [mA]$ at $18\ [V]$ output voltage. The regulator biasing current is zero. In conclusion, the power dissipated on a voltage regulator is $P_D = 49.98\ [mW]$, therefore all the voltage regulators dissipates $599.76\ [mW]$. The base plates of the voltage regulators have different potential, thus in order to avoid short circuit the thermo – conducting insulating layers have to be used. The thermal resistance of the pads is $R_{th\,cs} = 0.24\ \frac{K}{W}$.

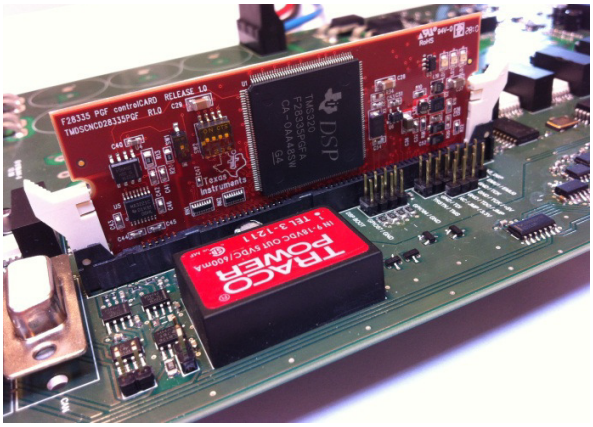
Taking into account the voltage regulators and NPC legs the total power dissipated on the inverter is $188.16\ [W]$. The thermal resistance was calculated based on [**83**] and is presented in (4-36).

$$R_{th} = \frac{\Delta T}{P_D} = \frac{T_s - T_a}{P_D} = \frac{80 - 25}{188.1632} = 0.2923 \left[\frac{°C}{W}\right] \quad (4\text{-}36)$$

Considering the value of the thermal resistance a heat sink with the thermal resistance of $0.29 \left[\frac{°C}{W}\right]$ from H S Marston has been chosen.

4.7. CPLD and DSP Control

The space vector modulation strategies were implemented on a TMS320F28335 DSP based Control Card from Texas Instruments. Deadtime and protection management is performed through Complex Programmable Logic Device (CPLD) XC9572XL. The use of the Control Card represents a fully embedded design solution, Figure 4-24, providing features as:



ControlCard Features

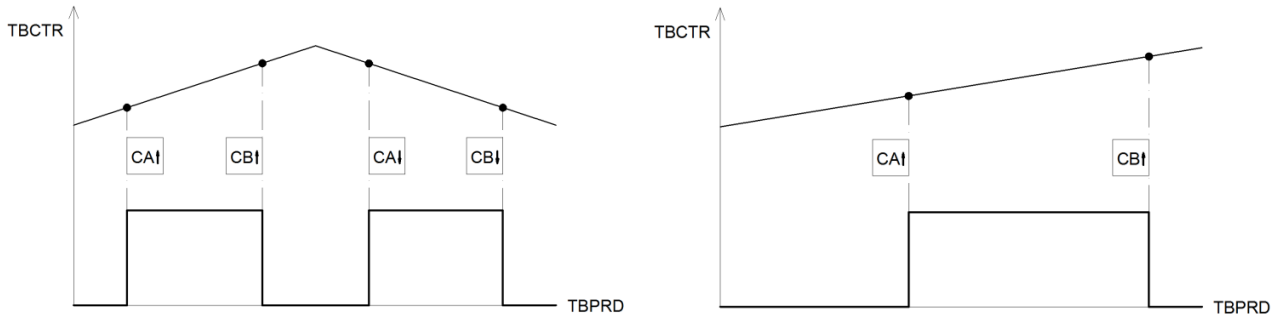
- Small Form Factor
- Standard 100 pin DIMM
- Analog and Digital Input/ Output (I/O)
- JTAG Interface
- Isolated RS-232 Interface
- 5v Supply

CPU Features

- 150 mhz, 32 bit Floating Point
- 256k x 16 Flash, 34k x 16 Single Access Random Access Memory (SARAM)
- Up to 18 PWM Outputs
- 12 Bit ADC With 16 Channels
- 80 ns ADC Conversion Rate
- 88 General Purpose Input/ Output (GPIO)
- CAN, RS-232

Figure 4-24 – Control card Integration into the Designed Inverter

Different modulation strategies are implemented on the DSP based on the code developed in the simulation model. The PWM is executed by six ePWM modules. Analogue signals, as three phase currents and DC link voltages are acquired on 5 ADC channels. Pin number 95 is reserved for communication with the CPLD. The ePWM modules are set to work based on modified Up-Down-Count mode with Dual Edge Asymmetric Waveform [**84**]. The schematic of how the ePWM module configuration works can be seen in Figure 4-25:



a) Symetrical Up – Down Count Mode

b) Asymetrical Up Count Mode

Figure 4-25 – DSP Counter Modes

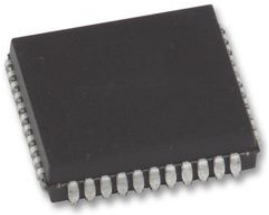
There are two counters active for each ePWM module, CA and CB. When the Time Based Counter (TBCTR) reaches CA on Up Count, or CB on Down Count, the output is set high. When TBCTR reaches CB on Up Count, CA on Down Count, equals zero or period, the output is switched low. This mode of operation permits better use of the ePWM module, retaining 0-100% duty cycle. All modulation strategies use the symmetrical up-down count mode, except for RS3N and ZCM which use the asymmetrical up count mode.

An interrupt takes place on the beginning of each period that is acknowledged in an Interrupt Service Routine (ISR). During the ISR, the dwell times calculated on the main function are assigned to the ePWM module counters. Also, ePWM1A sends the Start-Of-Conversion signal to all ADCs. The ePWM module uses the shadow registers which act as time buffers. On the beginning of each period, the values of the counters are updated on the shadow register after the register has assigned the values to the active counters.

From the ADC module [**85**], 5 channels are used. The sampling frequency is set to 12.5 MHz. The three phase currents and the two DC link voltages are acquired on each Start-Of-Conversion signal received from the ePWM module. In order to save time, the values are read into 5 global variables on the ISR used for PWM.

Pin 95 on the control card makes possible communication with the CPLD. The signal received from the CPLD stops the modulation or starts the V/f control when needed. One of the LEDs on the Control Card is used to show operation of the DSP and it flashes with the system frequency of 50 Hz or the frequency used to start in V/f control. The LED is off while the modulation is not running. In order to benefit from the full speed while embedded, the DSP has been programmed to load the entire code from flash memory to the Random Access Memory (RAM) memory at power-up. Then, the programs run fully from the RAM memory.

The Xilinx XC9572XL, Figure 4-26, CPLD used benefits from the following features:



- 72 Macrocells
- 100 MHz frequency
- 1600 usable logic gates
- 34 User I/O
- 3.3/5v Tolerant

Figure 4-26 – CPLD used for Deadtime and Protection Management

The tasks performed by the CPLD are:

- Deadtime management for each pair of complementary switches.
- Stop the modulation and disable the buffers in case of a fault.
- Signal fault status.
- Manages PWM procedures specific to NPC topology.

When IGBTs are used the deadtime or interlock delay time needs to be taken into account. This time is used to first turn off one IGBT and turn on another. Furthermore, bridge shoot through caused by unsymmetrical turn on and off times are avoided [**86**]. The dead time was calculated based on equation (4-37).

$$t_{dead} = \left[\left(t_{d\_off\_max} - t_{d\_on\_min}\right) + \left(t_{pdd\_max} - t_{pdd\_min}\right)\right] * 1.2 \quad (4\text{-}37)$$

Where:

- $t_{d\_off\_max}$ – is the maximum turn off delay time
- $t_{d\_on\_min}$ – the minimum turn on delay time
- t_{pdd_max} – the maximum propagation delay of driver
- t_{pdd_min} - the minimum propagation delay of driver

By the use of gate driver [**53**] and Semikron module datasheets [**49**] the dead time can be calculated. The maximum turn off delay time is $300\,ns$, the minimum turn on delay time is $60\,ns$, the maximum propagation delay of the driver is $500\,ns$ and the minimum propagation delay of the driver is $200\,ns$. Hence, the dead time according to equation (4-37) is $6.48 * 10^{-7}\,s$. As the developed board is a test one and the dead time is generated through the CPLD, dead time can be modified through software, for safety reasons a dead time of $1.5\,us$ was chosen. Aside from deadtime insertion, the algorithm has to assure that certain gate signal combinations are avoided. On a three level inverter using IGBT leg modules, the following switching states are possible [**51**], Table 4-5.

Table 4-5 – NPC Switching States

T1	0	0	0	1	0	0	1	0	1	1	0	1	1	1	0	1
T2	0	1	0	1	1	0	0	0	0	0	1	1	1	0	1	1
T3	0	0	1	0	1	1	0	0	0	1	0	1	0	1	1	1
T4	0	0	0	0	0	1	0	1	1	0	1	0	1	1	1	1
state	Allowed States						Dangerous States					Destructive States				

All the destructive states are avoided by insertion of deadtime by means of shift registers because switch pairs T1-T3 and T2-T4 cannot be high at the same time. By means of a simple filter on the PWM inputs, the rest of the dangerous states are avoided.

Also, in the case of an emergency shutdown, the switches have to be turned off in a certain manner. In order to avoid voltage breakdown, outer switches (T1 and T4) have to be switched off first [**51**]. Also, in a desaturation event, there is a window of 10 us for complete switch-off [**51**]. The shutdown procedure ensures that any switching sequence is overridden with state “O” after proper deadtime. After reach of state “O” the inverter is completely shut down by disabling the external PWM buffers. The shutdown procedure is applied whenever there is a fault or the inverter is manually tripped.

In case of a desaturation event, the gate drivers will latch in fault state. In order to be able to further use the inverter, a gate driver reset procedure is performed. The reset procedure disables the PWM from the DSP and sends the command sequence O-N-O-P-O to the inverter. This way each gate driver receives a short reset pulse used to release the latch (in case the fault is cleared).

The LED enable procedure sends the multiplexed LED signals to a demultiplexer through PWM. Seven LEDs, two green and five red provide information about the inverter state.

Table 4-6 – Fault Warning

LED1 Green	LED2 Green	LED3 Red	LED4 Red	LED5 Red	LED6 Red	LED7 Red
Power On	SVM On	Gate driver	DC Overcurrent	DC Voltage Range	Phase Overcurrent	Overtemperature

The start/end of PWM is transmitted to the DSP in order to stop the ePWM modules or to start the V/f control.

4.8. Hardware Validation

The three level NPC inverter design presented in this chapter has been built and tested in the laboratory. Furthermore, the protections together with dead time and turn on and off procedures are validated through experimental results.

Deadtime Insertion

Before powering up the inverter at full power a few tests have to be performed. The dead time between two complementary IGBTs has to be tested. The experimental result can be seen in Figure 4-27. The purple signal is the command for transistor T1 and the blue signal is the command for transistor T3. A proper 1.5 us dead time is inserted between any two complementary IGBTs.

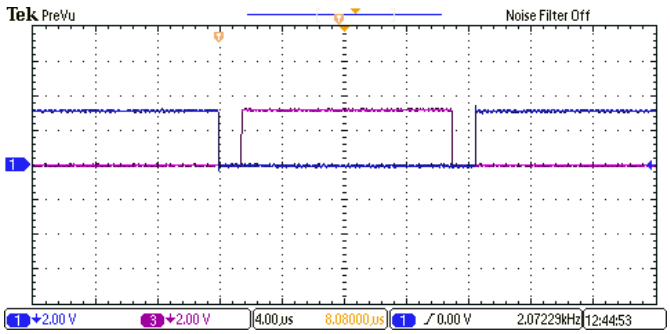


Figure 4-27 – Deadtime between Two Complementary IGBTs – Experimental Result

Turn On and Off Procedures

As stated before, in chapter 4.7, each IGBT leg of the inverter has to be turned on and off in a certain way. When the inverter is shut down, the outer transistors have to be turned off first followed by the inner transistors after proper deadtime.

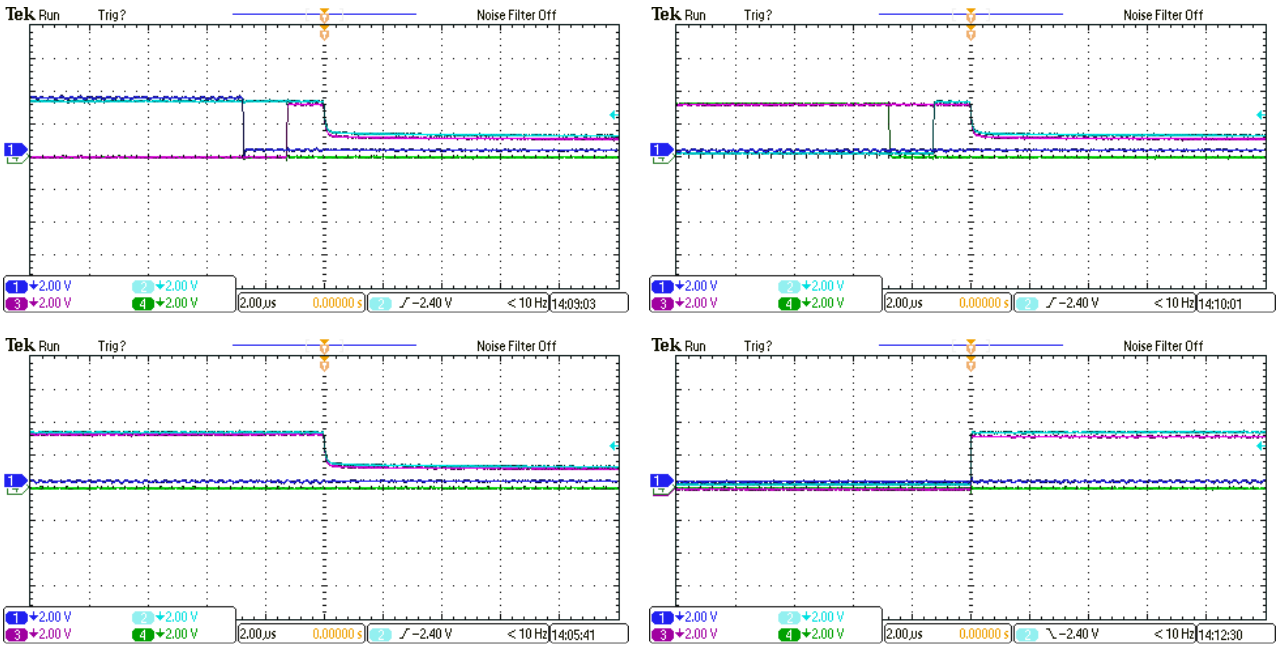


Figure 4-28 – Turn On and Off Procedures of the Semikron IGBT Module – Experimental Results

The turn on and turn off procedures can be seen in Figure 4-28. The procedures are applied in parallel for all three inverter legs. Each of the inverter legs can be in a different state (0, N or P). Figure 4-28 presents one inverter leg. For all waveforms, the blue represents signal for transistor T1, light blue signal for transistor T2, purple represent signal for transistor T3 and the green signal represents transistor T4. As seen in the first waveform, the inverter is in N state. After deadtime, the inverter is switched to state 0 and after 1.5 us, the octal buffers are disabled, switching the inverter off completely. Second waveform represents the shut down from an N state and the third waveform shows turn off from a 0 state. The fourth waveform represents the turn on procedure. Every time, every leg starts in the 0 state, after which the modulation is started.

Reset Procedure

In the case that one of the gate drivers encounters a fault, a reset procedure has to be followed in order to release all gate drivers latch and restart modulation. Signal colours are the same as in Figure 4-28. The reset procedure can be seen in Figure 4-29.

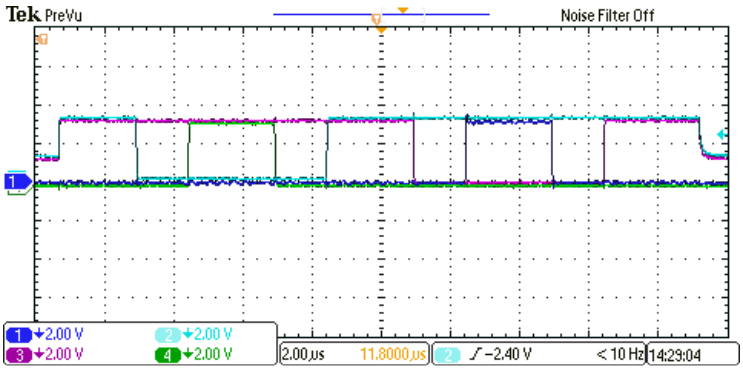


Figure 4-29 – Reset Procedure for Restarting the Modulation – Experimental Result

The reset procedure works together with the turn on and the turn off procedures. Hence, the start and end of the reset procedure is the state "0" (0110), meaning that the inner transistors are switch first at the beginning and end of procedure. As each gate driver has to receive a short pulse in order to release the latch, the gate driver reset procedure ensures that the entire inverter is reset using zero states. As it can be seen in Figure 4-29, each inverter leg goes through states O-N-O-P-0. Because the procedure is applied at the same time for all legs, the inverter will switch through all zero vectors: 000, NNN and PPP thus ensuring that each gate driver receives a short signal in order to release the fault latch, while the voltage applied to the load is 0 V.

DC Link Voltage Range Protection

The DC link voltage has to be maintained between certain limits. The protection is set to shut down the inverter if each capacitor voltages voltage drops or increases with 10%. This means a $\pm 30\ V$ band for each of the capacitors. For this test, the DC link was connected to a three phase power switch in order to be able to connect a 5 kΩ resistor to upper or lower side. In Figure 4-30, the green signals serves as overvoltage reference, set at 330V. The light blue signal serves as undervoltage reference equal to 270 V. The blue signal is the capacitor bank voltage for upper half of the DC link (left) and lower half (right). The purple signal represents the protection response. As it can be seen in Figure 4-30, when the capacitor voltage is outside the two references, the protection triggers a fault, shutting down the inverter. The capacitor voltage in each case was raised from below the lower reference to above the upper reference and back.

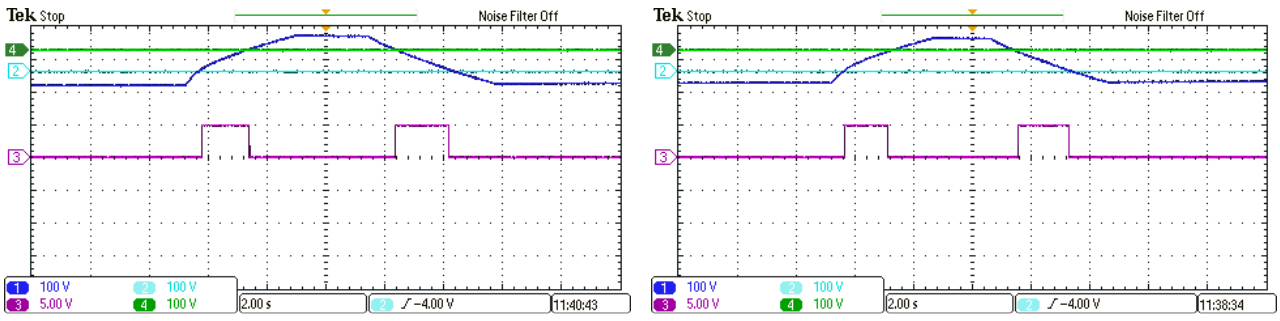


Figure 4-30 – DC Link Voltage Range Protection – Experimental Results

DC Link and Phase Overcurrent Protection

An overcurrent event on the DC link or one of the phases also triggers the inverter. The phase overcurrent response can be seen in Figure 4-31. For this test the DC link was set at 15V and two of the output phases have been connected together. The pink signals serves as the reference and it is set to 25 A. The green signal is the short circuit current for phase overcurrent protection (left) and for DC link overcurrent protection (right). The blue signal is the protection response in each case. At the encounter of a high current the inverter trips in both cases.

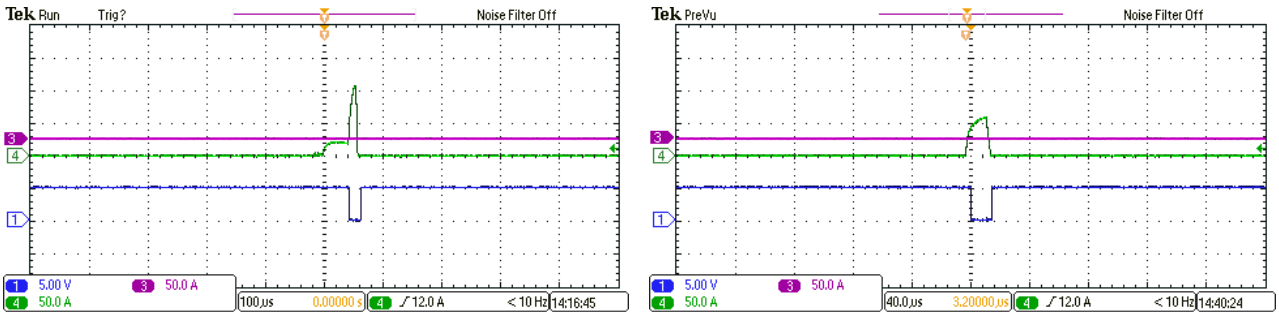


Figure 4-31 – Overcurrent Protection – Experimental Result

Overtemperature Protection

The overtemperature protection has to trip the inverter if any of the three modules surface reaches 80°C. The protection response can be seen in Figure 4-32. For this test, the thermistors were removed from their sockets and external resistors were used to trigger the protection. Each of the signals represents one of the IGBT thermal protection responses.

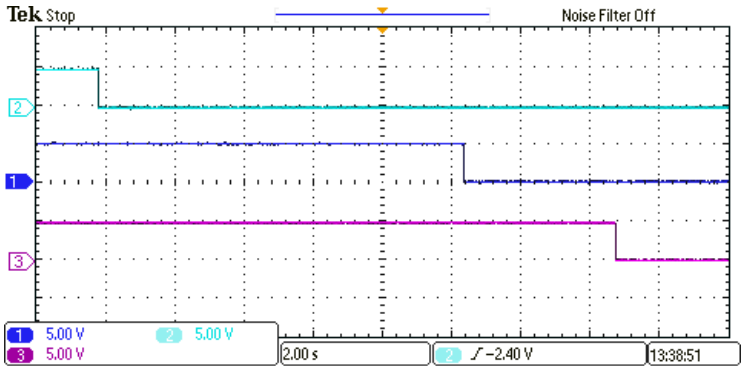


Figure 4-32 – Overtemperature Protection – Experimental Result

Three 9.09 kΩ resistors corresponding to a temperature of 82 degree Celsius has been inserted at different times in the socket of each thermistor in order to trigger the protection. The protection triggers a fault immediately as the resistors are inserted.

Thermal Design Validation

Furthermore, the thermal design needs to be validated through experimental results. The setup from Figure 4-33 was used. The inverter had an R-L load with equivalent of 6 kVA. Temperature was verified each ten minutes using a thermal camera. The inverter reached thermal steady state after 40 minutes. In order to have a confidence in the measurement the test was carried another 20 minutes. The temperature did not increase in this interval.

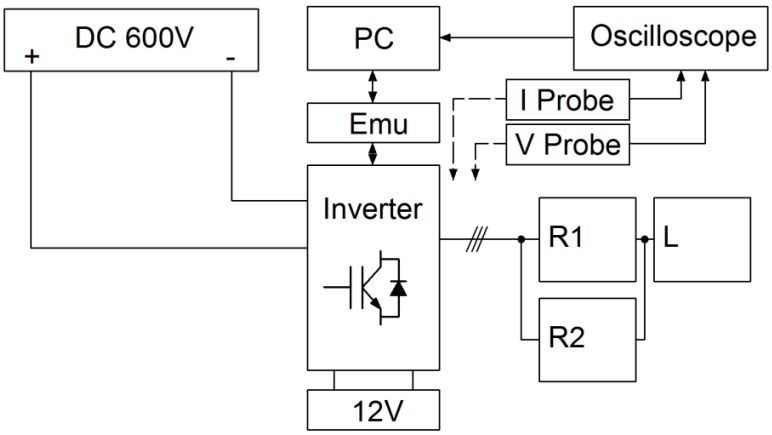


Figure 4-33 – Experimental Setup for Thermal Validation

The infrared picture from Figure 4-34 was taken after one hour. As it can be seen the temperature in the DC link capacitors was approximately 30°C, which is below the 85°C limit of the Panasonic capacitor chosen. The temperature from the modules area was 50°C, which is below the maximum surface temperature of 80°C allowed for the IGBT modules. The hottest part of the inverter was at 56°C on the gate drivers and their DC-DC converters. The board shows thermal symmetry with the hot area in the middle being surrounded by colder areas, presenting good heat dissipation. Hence, the thermal design was validated.

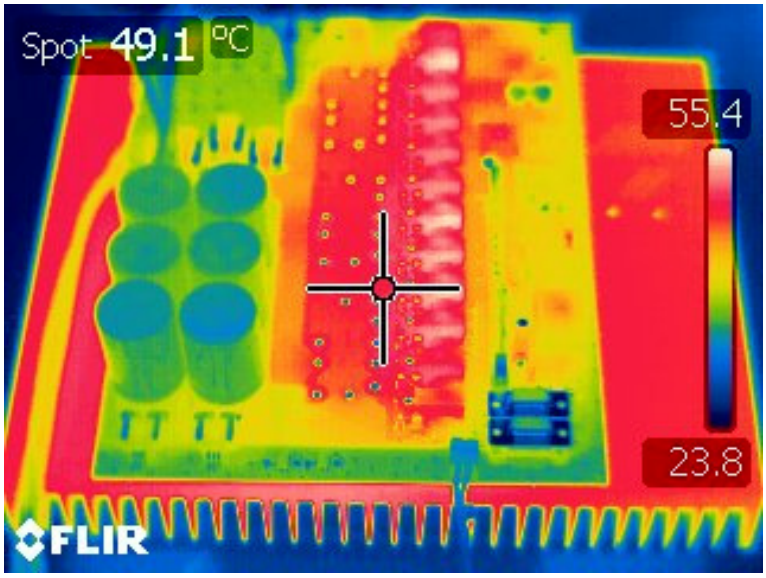


Figure 4-34 – Thermal Picture of the Inverter at $6\ [kW]$ After One Hour

5. Experimental Validation and Analysis of the Developed Modulation Strategies

Four modulation strategies were developed and rigorously tested through simulation before implemented on the designed inverter. The comparison between the four new strategies was made against classical NTV and ZCM. All offer reduced spectra for CMV compared to NTV. Although all offer natural NP balancing, only two provide extra balancing capability of up to 35%. One of the strategies developed, RS3N exhibits very strong advantages: the CMV is similar to ZCM method while maintaining the maximum modulation index of the NTV modulation. It also offers better EMI performance in high frequency range and the ability to balance the DC link in the event of external factors.

5.1. Experimental Setup

For validation of the theory and simulations, regarding the developed modulation strategies, experiments have been performed on the developed board described in Chapter 4. All experiments were performed in the same manner and with the same settings at its maximum modulation index. The control of the inverter was supplied from an external source, GwInstek GPS-4303. The DC link voltage was provided by 2 power supplies of 300 V each, SM 300-5. A 1.5 kW three phase induction motor was used as a load connected to a DC motor and power resistor. In order to see how the modulation strategy influences the CMV and EMI, no output filters were used. All voltage measurements were acquired using differential probes and visualised on the Tektronix oscilloscope. The experimental setup used to validate the developed modulation strategies is presented in Figure 5-1.

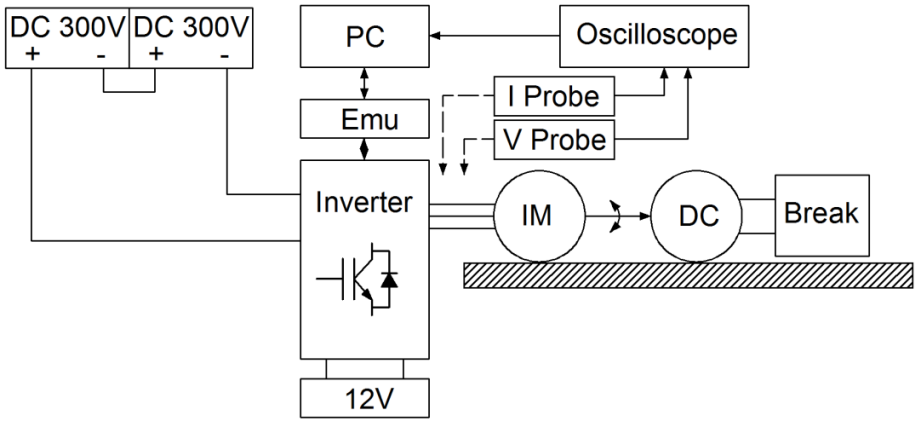


Figure 5-1 – Experimental Setup for Testing the Developed Modulation Strategies

5.2. Nearest Three Vectors with Even Harmonic Elimination Method

Figure 5-2 presents the experimental results regarding the phase, phase-to-phase, common mode and DC link voltages for NTV-EHE. The experiment was performed at maximum modulation index, $m_a = 1$. As expected, this voltage has a quasi-sinusoidal shape and nine voltage levels. The line voltage features five levels and the CMV has the maximum amplitude of +-$\pm 200\,V$. The DC link maintains balance proving the natural balancing mode. The voltage variation on the DC link capacitors is under 5V. The results are in concordance with the theoretical basics and with the simulations. The results regarding the performance of the following methods will be compared to this method.

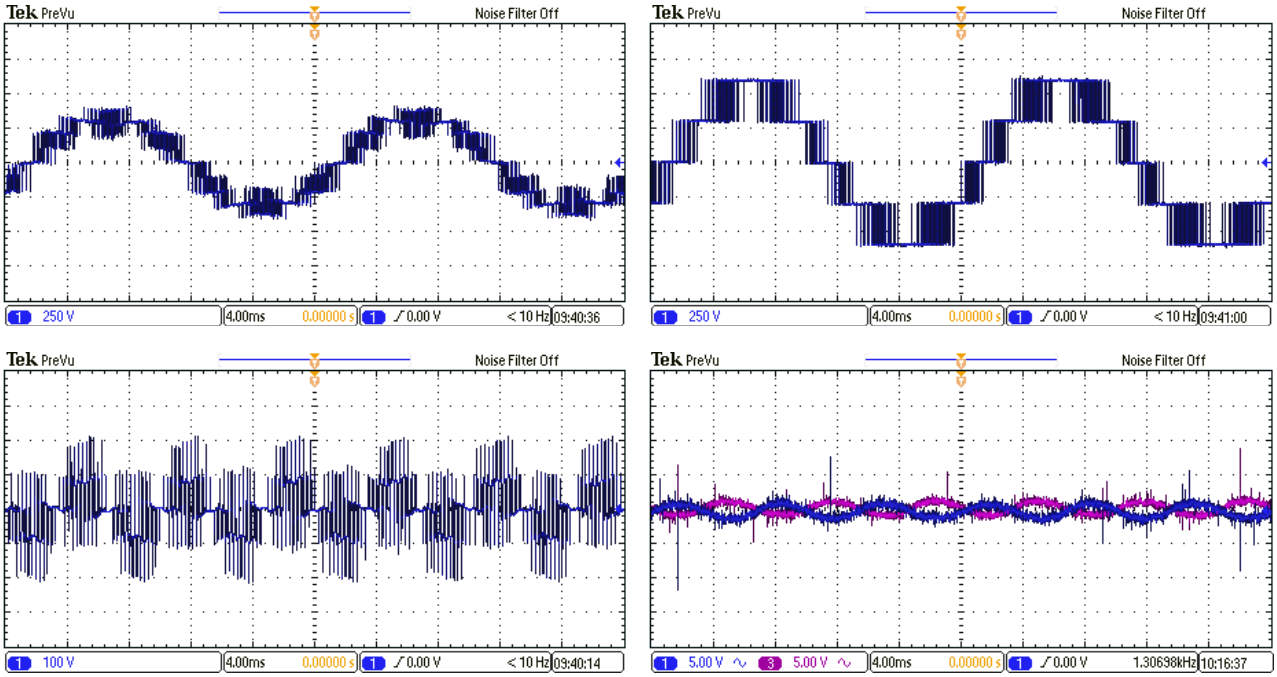


Figure 5-2 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for NTV-EHE - Experimental Results

5.3. Zero Common Mode Method

The waveforms for ZCM are also in concordance with theory and the results from simulation. The level on the phase and on the line voltages are the same with the simulation. The effect of dead time is seen in the presence of CMV, Figure 5-3. The amount is to be analysed on chapter 5.9. Considering that the reference vector lies in sector 1 the switching sequence is $[V_0\ V_7\ V_{12}\ V_0]$. The IGBT modules will receive the command from Table 5-1. In the ideal case, the switching between vectors does not have any dead time inserted, thus resulting in no CMV. This can be seen in the first line of Table 5-1. In the presence of dead time, the intermediate states appear when switching between certain vectors, as seen in the second line of Table 5-1. For example, the crossing between PON and PNO vectors has an intermediate state for which both second

leg and third leg are in zero state, hence P00. The length of this state is the dead time interval. Known from Table 2-5 in chapter 2.4.2, the POO intermediate state generates a CMV of $+\frac{1}{6}V_{DC}$. Similarly happens in the rest of the sectors, resulting in a CMV of $\pm\frac{1}{6}V_{DC}$, but on a very short period of time, compared to the applied vectors.

The performance of the proposed modulation strategies is going to be analysed in comparison with the ZCM and NTV.

Table 5-1 – Influence of dead time on the switching sequence

000		P0N		PN0		000	
000	000	000	PON	P00	PNO	000	000

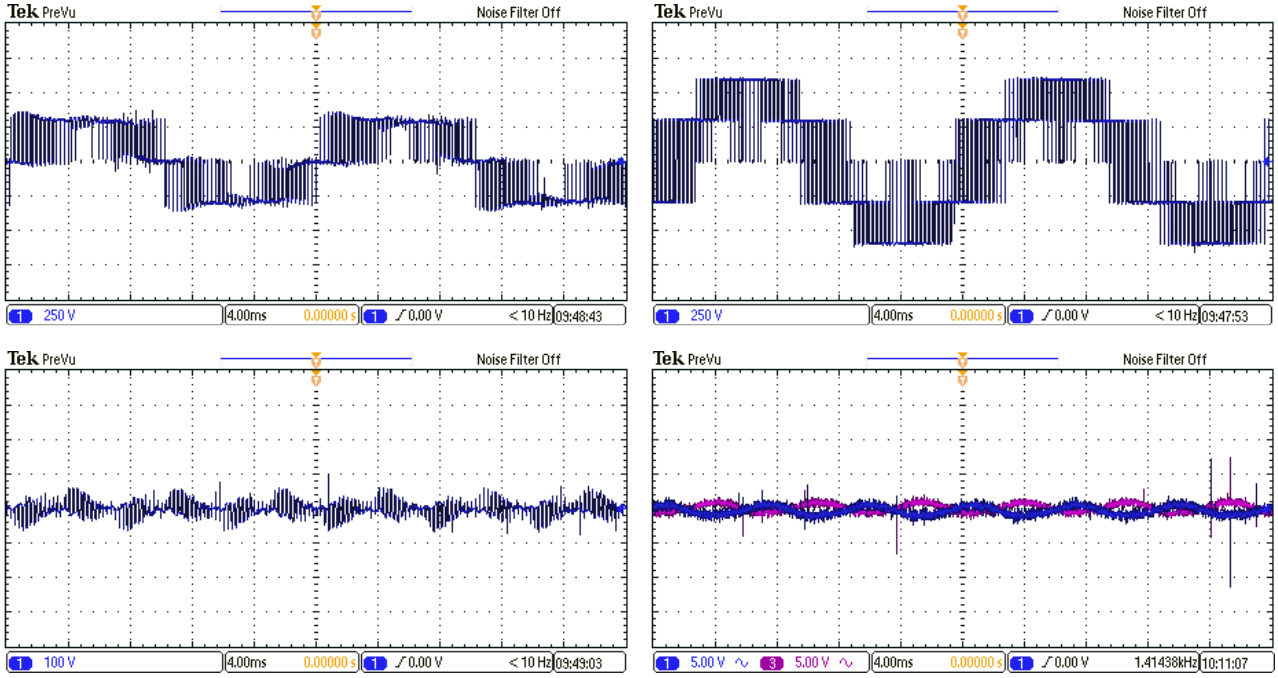


Figure 5-3 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for ZCM - Experimental Results

5.4. One Large One Medium Method

Experimental results for OLOM validate the simulation model proposed before. The experiment, Figure 5-4, shows the same number levels in the phase voltage, phase-to-phase voltage and CMV. The DC link benefits the natural balancing mode, with the capacitor voltage having a ripple under 5V. The CMV has a fundamental of 150 Hz, easily visible. The performance regarding CMV is going to be analysed in chapter 5.9.

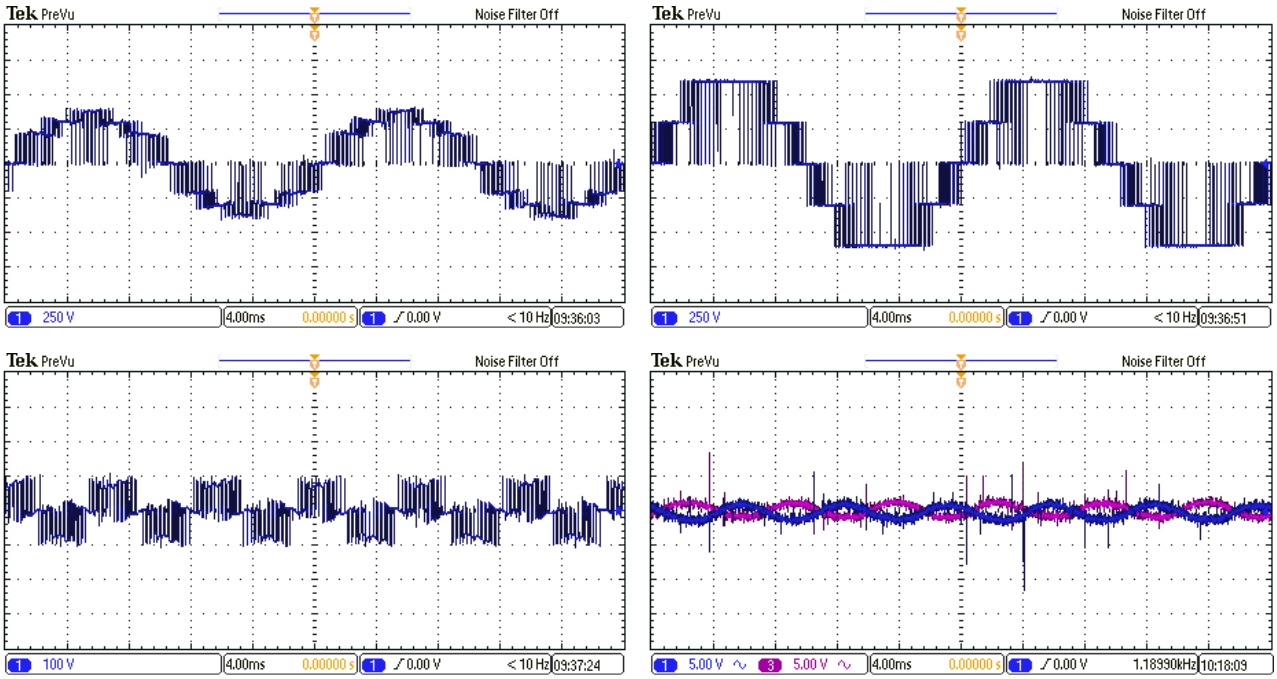


Figure 5-4 –Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for OLOM - Experimental Results

5.5. Zero Small Medium Large Method

The results of the ZSML, Figure 5-5, seem to be similar with NTV modulation. This occurs only at maximum modulation index, due to the fact that the zero vector is not applied. This can be seen from equation (5-1).

$$T_{zero} = \left(1 - \frac{V_{ref}}{V_{ref,max}}\right) T_s \tag{5-1}$$

As the reference voltage is increased, the time for zero vector is decreased. Hence, the dwell time for the zero vector becomes zero when $V_{ref} = V_{ref,max}$. This particularity makes the phase and phase-to-phase voltages to look identical with NTV-EHE. The difference can be clearly seen in the CMV levels, which are maxim $\pm 100\,V$ compared with $\pm 200\,V$ for NTV. The method is tested in natural balancing mode, but there is the possibility of balancing in the case of an external neutral point unbalance. The balancing capability curve is presented in chapter 5.8.

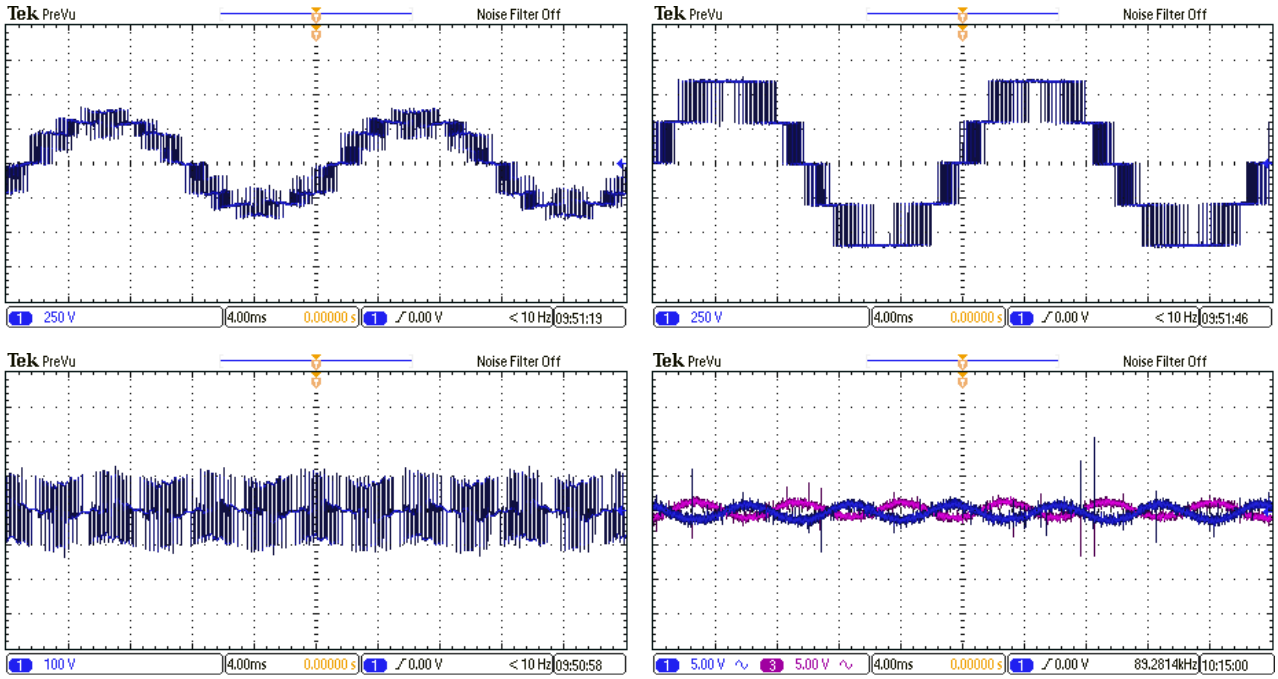


Figure 5-5 –Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltage for ZSML - Experimental Results

5.6. One Small One Medium Method

The good concordance between theory, simulation and experiment is also maintained for OSOM, Figure 5-6. The ripple on the capacitor voltages is smaller when compared with the rest of the modulations, being under 2.5 V. As in the OLOM modulation, the CMV fundamental frequency of 150 Hz can also be clearly seen.

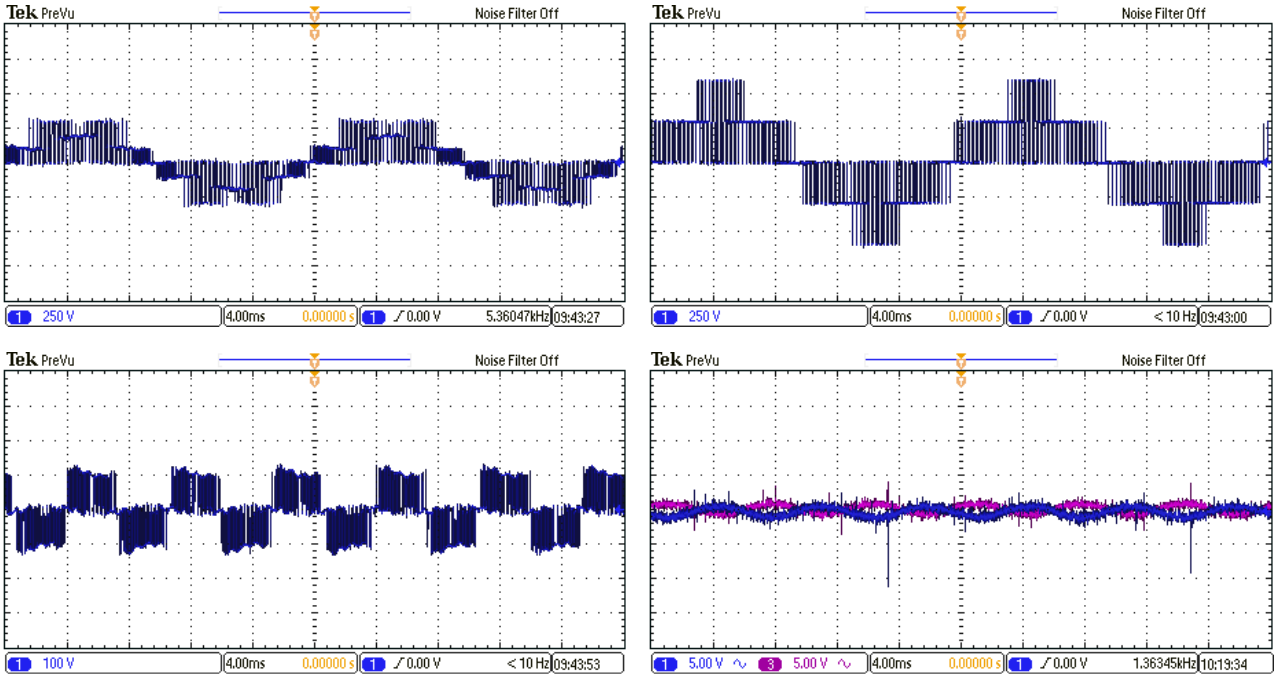


Figure 5-6 – Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for OSOM - Experimental Results

5.7. Random Sequence of 3 with Neutral Point Balancing Method

RS3N modulation follows the same pattern of good concordance between simulation, theory and experimental results as seen in Figure 5-7. Although the similarity with the NTV modulation is very high, this method has some clear differences compared to NTV. The line voltage and phase voltage are similar to NTV but the randomization of the vectors inside each switching sequence can be clearly seen. Another difference is the level of $\pm 100\ V$ in the CMV voltage, which is half of NTV. Again, the random component can also be seen clearly in the CMV which is expected to reduce the amplitudes at high frequencies.

The voltage on the capacitors features a variation under 5 V. The waveforms were acquired for natural balancing mode. Another method of differentiating it from NTV is by the fact that this modulation will recover natural point balance if the neutral point potential slides towards negative or positive voltages. The balancing capability curve is presented in chapter 5.8.

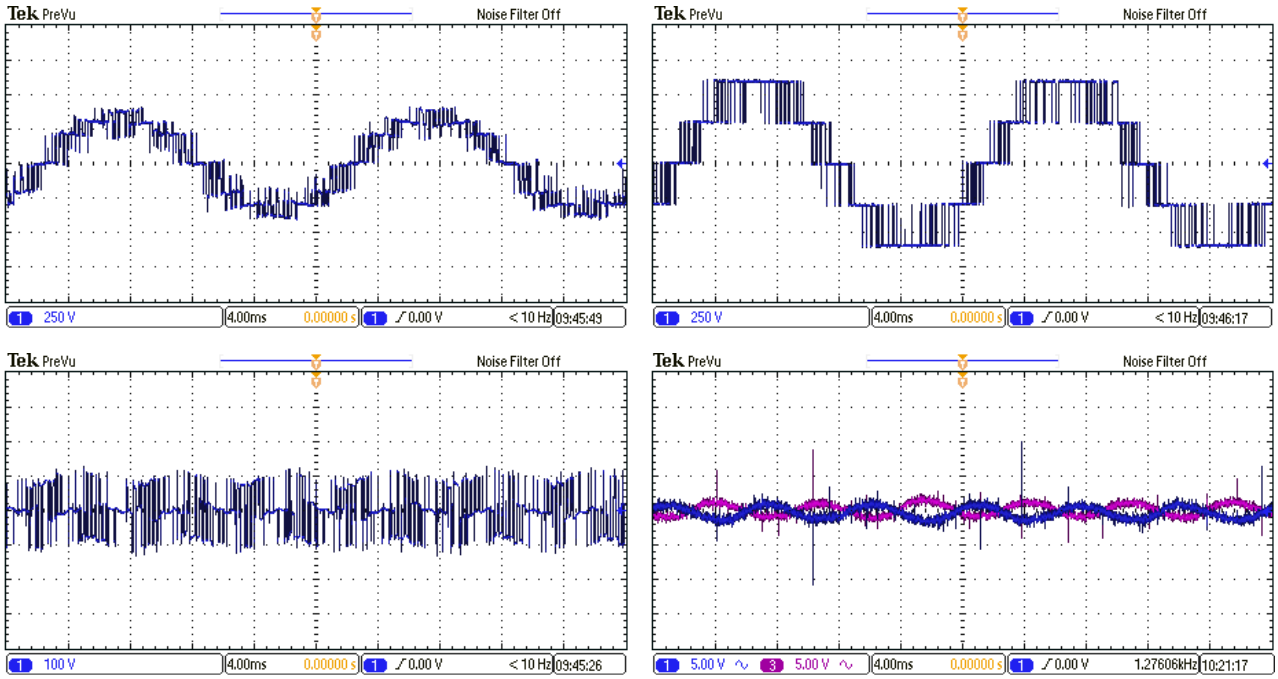


Figure 5-7 –Phase Voltage, Phase-to-Phase Voltage, CMV and DC Link Voltages for RS3N - Experimental Results

5.8. DC Link Balancing Capability

All developed modulation strategies have the ability to self-balance, but only ZSML and RS3N can balance the DC link in case of an external event. The balancing capability can be determined based on theory presented at DC link capacitors, chapter 4.2 – equation (4-3). According to [**32**] it can be determined which phase is connected to the neutral point. Furthermore, the balancing capability is calculated as a function of phase current, equation (4-15).

$$B_c = \frac{I_{bal}}{I_{ph}} 100\ [\%] \tag{5-2}$$

When the modulation index is maxim and the displacement angle is between 0 and $\frac{\pi}{6}$ the balancing current can be calculated as in equation (5-3) for both ZSML and RS3N.

$$I_{bal} = \sqrt{\frac{6}{\pi}\int_0^{\frac{\pi}{6}} \left| -I_a \sqrt{\frac{T_a}{T_s}} \right|^2 d\theta} \tag{5-3}$$

Starting from minimum modulation index until at half of it, both modulation use two small vectors for balancing. Hence, their balancing capability can be calculated. As an example, the equation for balancing capability at $m_a = 0.5$ is presented in (5-4).

$$I_{bal} = \sqrt{\frac{3}{\pi}\int_0^{\frac{\pi}{3}} \left| -I_a\sqrt{\frac{T_a}{T_s}} + I_c\sqrt{\frac{T_c}{T_s}} \right|^2 d\theta} \tag{5-4}$$

In order to validate this theory experiments at different modulation indexes have been performed on the two methods, ZSML and RS3N. The setup shown in Figure 5-8 was used. A variable power resistor was connected through a three position switch to the neutral point of the inverter, enabling the connection to the upper or lower halves of the DC link. When the switch is in neutral position the resistor has no effect (natural balancing mode).

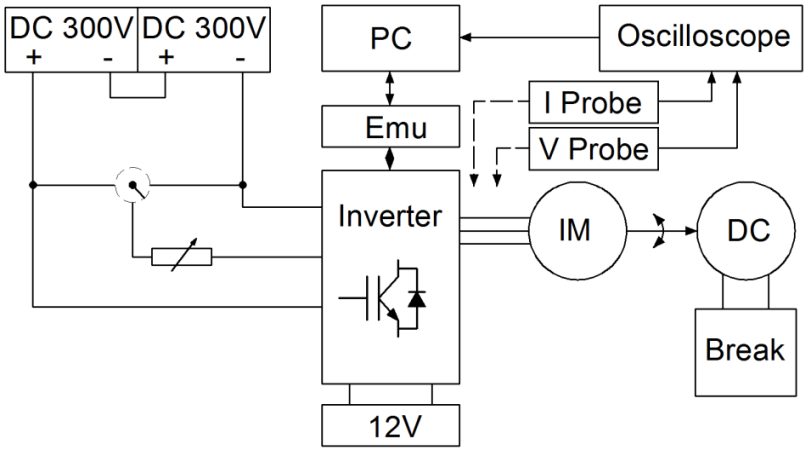


Figure 5-8 – Experimental Setup Used for DC Link Balancing Capability Assessment

Based on the performed experiments Figure 5-9 was obtained. As it can be observed RS3N has better capabilities of balancing than ZSML. The RS3N has the maximum balancing capability at $m_a = 0.6$, while ZSML at $m_a = 1$. The ability to balance the DC link at maximum modulation index is similar.

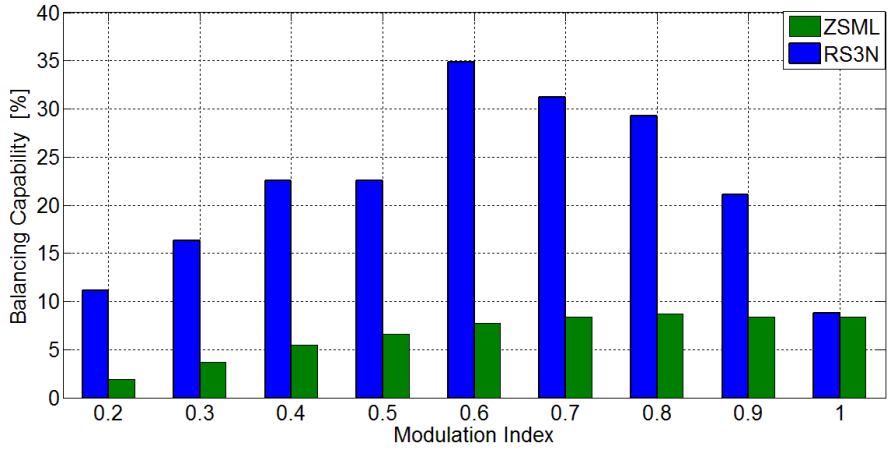


Figure 5-9 – Capability Curve Function of Phase Current vs. Modulation Index Determined Experimentally

5.9. CMV Analysis

The general theory regarding CMV has been presented in subchapter 2.4 and the theory of developed modulation strategies chapter in 3. For a better understanding, experiments have been performed with the measurement setup described in chapter 2.5.2. The CMV has been measured at the maximum modulation index of each modulation strategy and performed the Fast Fourier Transformation (FFT) on it, Figure 5-10. As it can be seen, all modulation strategies decrease in amplitude while increasing in frequency. As the parasitic coupling inside the motor are mainly capacitive, this characteristic is preferred. The amplitude at very low frequency, as 150 Hz has little effect as the current generated is small. This can be observed from the formula (5-5). As the frequency of the capacitance decreases, the current decreases.

$$I_p = \left| \frac{U}{R + j\frac{1}{2\pi f C}} \right| \tag{5-5}$$

The fundamental frequency for all modulation strategies is 150 Hz. The NTV-EHE modulation has 53.7 V on the fundamental frequency. Around the switching frequency, 4 kHz, the CMV amplitude is 44.3 V. At the rest of the frequency range, the NTV-EHE modulation has amplitudes under 14.8 V. The CMV is present up to 100 kHz. The ZCM modulation should have zero CMV, if it was ideal, but in real life applications deadtime has an influence resulting in the low CMV, Figure 5-10. The fundamental for ZCM is at 8.24 V; while at switching frequency is 16.5 V. The CMV vanishes before reaching 50 kHz.

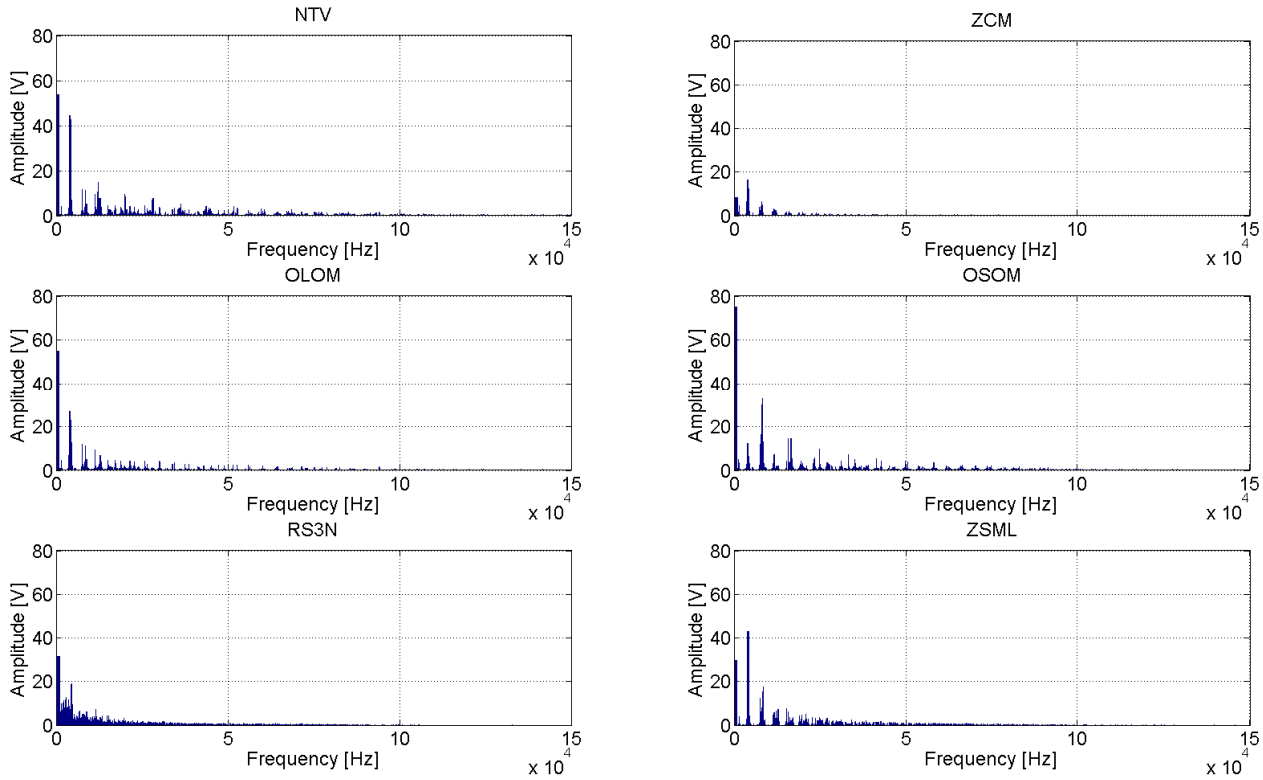


Figure 5-10 – FFT on CMV for Classic and Developed Modulation Strategies – Experimental Results [103]

Further on, the proposed modulation strategies are to be compared with the classical ones. OLOM shares the same 100 kHz frequency range as NTV while having only 27 V CMV around the switching frequency. The rest of the spectrum remains below 11.8V. OSOM has higher amplitude on fundamental frequency 74.7 V, and low amplitude, 12.3 V, around the switching frequency. The disadvantage would be the 32.7 V at the double of the switching frequency. The spectrum remains below 100 kHz with amplitudes below 14.7V.

ZSML has 43 V on CMV around the switching frequency, but the spectrum is only until 50 kHz with amplitudes under 17.7V. An interesting result is provided by the RS3N modulation strategy. By randomizing its vectors inside the switching sequence, the CMV frequencies are moved towards lower frequency range. The CMV around the switching frequency for RS3N is 19.1 V. The rest of the spectrum, which is until 50 kHz, features amplitudes below 7.5 V.

In an overall comparison, ZSML maintains the level of CMV around the switching frequency, compared with NTV, while having half its spectrum. OLOM has almost twice as low CMV at switching, retaining amplitudes under NTV throughout the entire spectrum. OSOM seems to move the amplitudes, seen at other strategies, to double of switching frequency, while the rest of the spectrum is comparable with NTV-EHE. The RS3N modulation has superior results to NTV-EHE for entire spectrum. Around switching frequency, it features half of the CMV, compared to NTV-EHE, and almost the same level compared to ZCM. The performance of RS3N is comparable with ZCM modulation in terms of spectrum length and CMV levels throughout the entire frequency range.

5.10. Comparison of Conductive EMI produced by Modulation Strategies

The theoretical part regarding EMI is described in chapter 2.5.1. An experimental setup has been built in order to observe the influence of modulation strategy over the EMI. Due to limited resources an alternative solution has been adopted. This solution is based on [**87**] and uses a clamp-on current probe for measuring the common mode current. The current probe used can measure currents with frequencies up to 20 MHz. Figure 5-11 presents the adopted solution. The probe will add the currents in the same direction and subtract the one with opposite directions, hence only the common mode current will be measured.

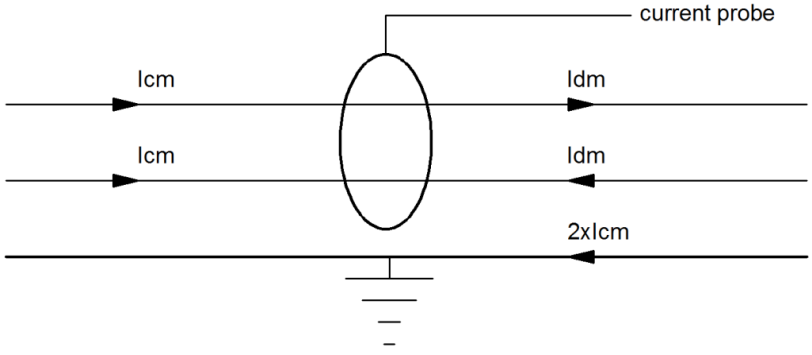


Figure 5-11 – Common Mode Current Measurement [**87**]

Based on this solution experiments were performed on each modulation strategy at its maximum modulation index. Figure 5-12 presents the conducted EMI, between the inverter and load, in decibels on a logarithmic scale. All six modulation strategies seem to develop the same EMI, but at a closer look, there are some differences. The four developed modulation strategies are compared against the classical ones, ZCM and NTV. The ZCM method has 7 dB less at lower frequencies, compared to NTV, which is constant at 60 dB up to 1 MHz. After this frequency the difference between these two decreases to 2 dB. The peak for all strategies is at 2 Mhz. NTV has a peak of 79 dB, while ZCM has 70 dB. Both strategies remain at 50 dB on the high frequency range, between 3 MHz and 20 MHz.

The proposed strategies have similar results in the low frequency range, amplitude of 57 dB. The peak for al strategies is around 75-77 dB at 2 MHz, being situated between ZCM and NTV. In the high frequency range, OLOM, OSOM and ZSML remain at 50 dB. RS3N has lower amplitude between 3 MHz and 20 MHz, 43 dB, being 7 dB lower than the rest of the modulation strategies.

Comparing all the EMI results it can be seen that OSOM, OLOM and ZSML seem to be situated between ZCM and NTV. RS3N is situated between ZCM and NTV at low frequency range, while at high frequency range seem to offer improvements over both.

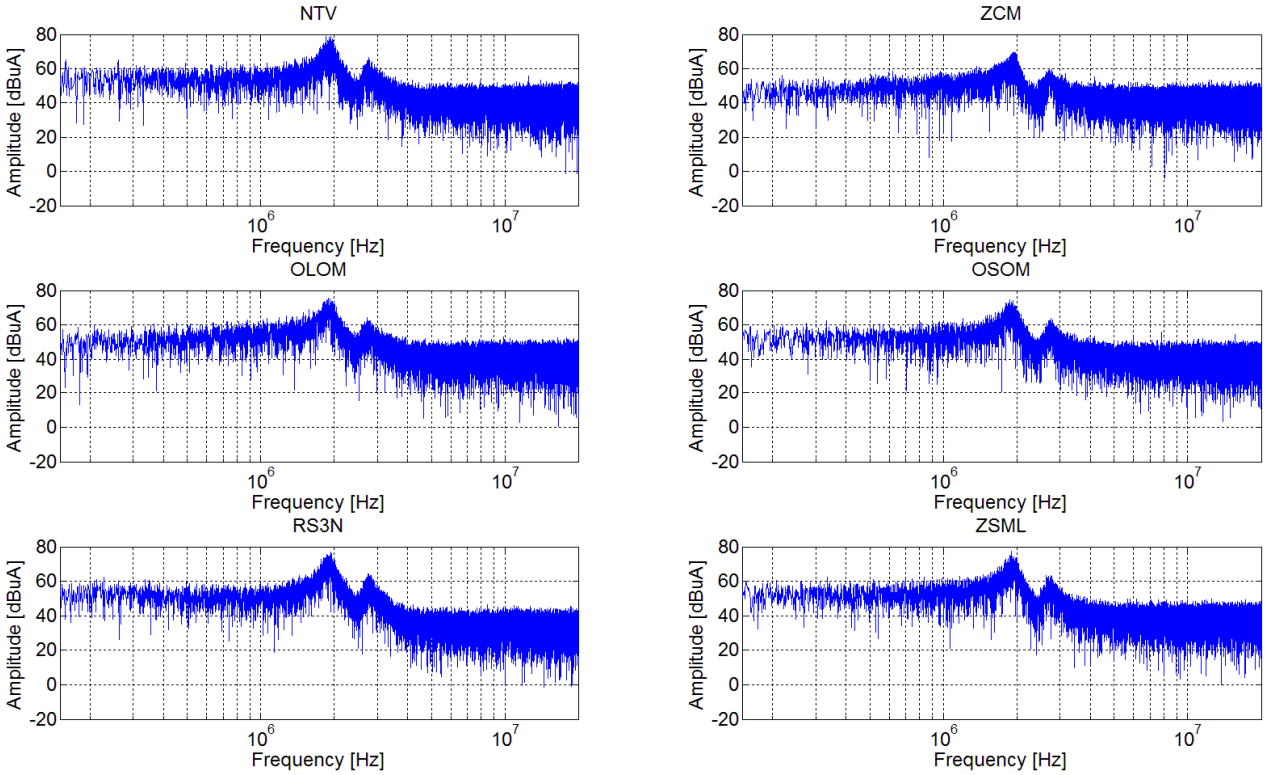


Figure 5-12 – Conductive EMI Currents Produced by Modulation Strategies

6. Conclusions and Future Work

This chapter presents the conclusions regarding the two main objectives: development of modulation strategies that address DC link balancing and CMV reduction and the hardware design of the three-level NPC inverter. Further on, future work is stated.

6.1. Conclusions Regarding the Development of Modulation Strategies that Address DC Link Balancing and CMV Reduction

Solutions to reduce the common mode voltage and to balance the DC link through modulation strategies regarding three-level NPC inverter were studied. Throughout the master thesis four modulation strategies have been developed that address these problems:

- OLOM – uses one large, one medium and one zero vector in order to create the reference voltage vector over each 30° displacement angle.
- ZSML – the reference vector comprises all types of stationary vectors. At maximum modulation index only small, medium and large vectors are used. The zero vector is applied at smaller modulation indexes and its time is dependent on the amplitude of the reference voltage.
- OSOM – on each 30° displacement angle one small, one medium and one zero vector are used to build the reference vector.
- RS3N – uses the nearest three vectors to create the reference vector. The difference from NTV is that has the switching sequence of three and it is randomized.

All of the developed modulations have the ability to self-balance, but only two can balance the DC link voltage in case of external event. The balancing capability has been determined as a function of phase current. At maximum modulation index both ZSML and RS3N have similar capabilities for balancing the neutral point, but RS3N offers more at smaller modulation indexes than ZSML.

The methods were developed targeting an improved CMV response over the classical modulation strategies. All methods offer reduced CMV spectrum. Their performance is between ZCM and NTV. Good results are obtained by RS3N, which offers performance similar to ZCM while preserving the modulation index of NTV and offering up to 35% balancing capability.

Furthermore, each of these methods was analysed regarding electromagnetic interference. Conductive EMI has been measured and the results show that OSOM, OLOM and ZSML are situated between NTV and ZCM. RS3N is as well situated between NTV and ZCM at low frequencies, until 3 MHz, while at high frequency, over 3 MHz, offers better performance.

By the use of small and medium vectors OSOM can only go at half of the maximum modulation index. The other three methods have a better utilisation of the bus bar, modulation index equal to one.

All of the developed modulations were validated through simulations and experimental results. All experimental analysis has been performed on the designed three-level NPC prototype. Based on the analysis performed on each of them it can be affirmed that all of them offers reduction of the CMV. From the spectral and CMV analysis it can be affirmed that the best performance is offered by RS3N.

6.2. Conclusions Regarding Hardware Design of the Three-Level NPC Inverter

The three-level NPC inverter PCB was design in Altium. The PCB manufacturing had to be done by an external company based on the source files provided due to the fact that it has four layers and only PCBs with two layers can be done in AAU laboratories. The assembly, test and all experiments were performed in AAU laboratories. The PCB features integrated DC link and galvanic isolation between power and control stage together with mixed analog and digital design. All ADC and PWM signals are shielded against noise by being buried into the PCB and having ground layers on top and bottom.

The new specialized NPC leg IGBT modules reduce the commutation paths; therefore the high voltage spikes and noise are reduced. By using these modules the inverter has no overvoltage snubbers and permits an overall enhanced design.

Furthermore, special attention was paid when sizing the DC link capacitors. They have reduced size, 30%, and are configured in a bank having a thermally optimal position.

The use of optocoupler based gate drivers with advanced features such as undervoltage lock-out, desaturation detection and active Miller clamping contribute even more to the reduced size, featuring the need only for single power supply because the turn-off is performed by the gate driver through the active Miller clamping. The possibility of current up to 2.5 A together with soft turn-off and isolated fault feedback make these drivers well suited for this application.

The inverter reduced size is also a consequence of the embedded DSP design in combination with the CPLD used for management of dead-time and protections. This combination offers flexibility and safety. The chosen DSP benefits of small form factor, DIMM100 connector, as well as integrated FLASH and RAM memory with CPU speed up to 150 MHz. The ADC modules have fast sampling, 80ns, and run independently of the CPU as the ePWM units. Having this property the ePWM gain extra degrees of freedom. Furthermore, the CPLD features a 100 MHz running frequency and full flexibility in configuring the I/O and extra clocks. The 3.3V/5V tolerance makes the CPLD a very good choice as it permits a mixed voltage design.

Protections regarding DC link overcurrent, phase overcurrent, DC link voltage out of range, overtemperature and protection against desaturation events make the design bullet proof. The protections are all fully

adjustable thus providing a flexible hardware platform. The protections were tested and resulted in full validation of the design. As a feature this protections have an optical fault feedback system through LEDs.

Furthermore, special attention was given to the specifics of the three-level topology such as semiconductor turn-on and turn-off order. For this concern, turn-off, turn-on and reset procedures are implemented on the CPLD and validated though experiments as well as the PWM filters. These filters prevent the shoot-through of the entire inverter and N-P or P-N switching sequence combinations. The start-up behavior of the inverter was also carefully managing ensuring no destructive device states occur.

Other features such as use of Hall-effect current sensors and RS-232 and CAN communications provide an enhanced design. The JTAG interfaces for both CPLD and DSP were implemented, thus making the debugging and onboard programming processes easy.

The code inside the DSP is designed to automatically transfer itself from flash memory into RAM at each power-up, and run from there in order to optimize the computing speed and algorithm performance.

Conduction losses as well as the switching ones were calculated using a methodology offered by Semikron. Furthermore, the thermal influence of the voltage regulators, need for gate drivers, were taken into account. Based on these calculations the thermal resistance was calculated. This design was experimentally validated through thermal imaging.

6.3. Future Work

Future work might include:

- Standard measurement of Conducted EMI
- Measurements and Analysis of Radiated EMI

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Appendix 1: Project Proposal

#16 Student Project

Project Title

Modulation of three-level inverter with common-mode voltage elimination and DC-link balancing

Target Group

M.Sc.E.E. or B.Sc.E.E. graduate students

Background

Conventional two-level voltage source inverters (VSI) generate common-mode voltage within the motor windings, which may cause motor failures due to bearing currents. Further, due to the capacitive coupling between the stator winding and the grounded motor frame, a common mode leakage current will flow, resulting in significant common-mode EMI. By use of a three-level inverter, c.f. Fig 1. and by use of only six of the active switch vectors, the common-mode voltage can be eliminated. (The common-mode voltage elimination is achieved at the expense of a reduction in the voltage transfer ratio, which becomes 0.866.) This modulation scheme was proposed by [1] where the voltage levels within the three-level inverter were achieved from independent DC-sources. However, in three-level converter structures, where the voltage levels are obtained by series connected capacitors, a DC-link voltage problem might occur by which an excessive high voltage might be applied to the switching devices (only for the topology in Fig. 1a). Further, the three-level converter might be unable to synthesize the reference voltage if too large voltage unbalance occurs. Hence, besides avoiding the common mode voltage, the modulation of the three-level converter also has to address the voltage unbalance between the upper and the lower switches.

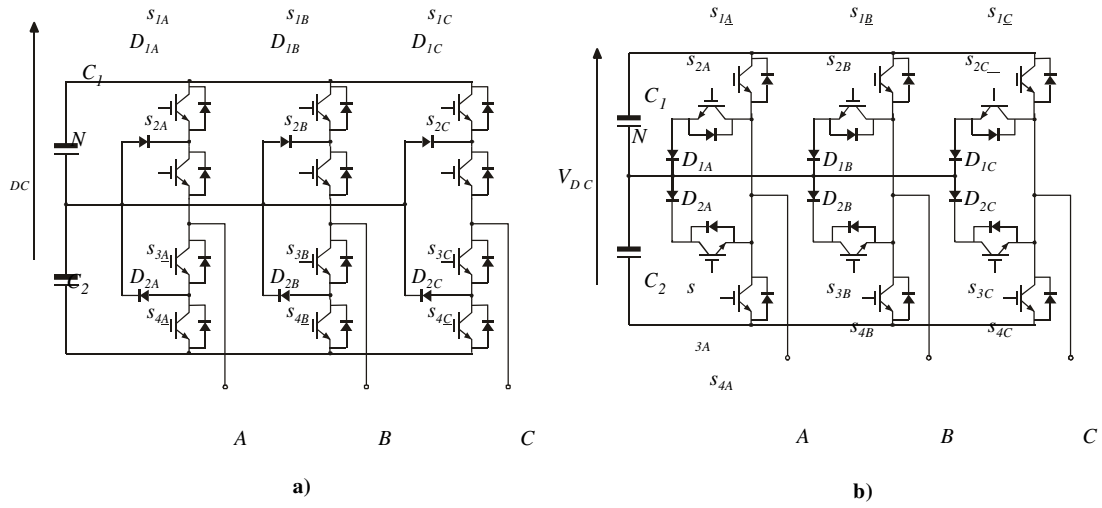

Fig. 1. Three-level neutral point clamped inverters. ***a)*** *Conventional topology.* ***b)*** *Modified topology.*

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Problem Statement:

Based on the problems listed above, the problem statement for this project becomes:

> Development of a modulation scheme that addresses both common-mode voltage elimination and DC-link balancing.

Project Content

Besides paying attention to the stated problem, the project could/should include the following issues:

- Hardware design of the three-level inverter
- Development of a simulation model to test different modulation strategies before implementation.
- d-SPACE or DSP implementation of the modulation/control of the three-level converter.
- Comparison of the emitted common-mode EMI from conventional modulation schemes and the developed modulation scheme.

Analysis of the DC-link unbalance problem.

Appendix 2: Switching Tables for All Methods

In this appendix the switching table from each modulation strategy is presented. The first implemented method was the classical NTV –EHE for comparison with the developed ones. The switching table for NTV-EHE is presented below.

Sector I												
Region 1a		Region 1b		Region 2a		Region 2b		Region 3		Region 4		
$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{2N}}$	OON	
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_7}$	PON	$\overrightarrow{V_7}$	PON	$\overrightarrow{V_7}$	PON	$\overrightarrow{V_7}$	PON	
$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{13}}$	PNN	$\overrightarrow{V_{14}}$	PPN	
$\overrightarrow{V_{1N}}$	ONN	$\overrightarrow{V_{2P}}$	PPO	$\overrightarrow{V_{1N}}$	ONN	$\overrightarrow{V_{2N}}$	PPO	$\overrightarrow{V_{1P}}$	ONN	$\overrightarrow{V_{2P}}$	PPO	
$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{13}}$	PNN	$\overrightarrow{V_{14}}$	PNN	
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_7}$	PON	$\overrightarrow{V_7}$	PON	$\overrightarrow{V_7}$	PON	$\overrightarrow{V_7}$	PON	
$\overrightarrow{V_{1p}}$	POO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{2N}}$	OON	
Sector II												
Region 1a		Region 1b		Region 2a		Region 2b		Region 3		Region 4		
$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{2N}}$	OPO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{3P}}$	OPO	
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_8}$	OPN	$\overrightarrow{V_8}$	OPN	$\overrightarrow{V_8}$	OPN	$\overrightarrow{V_8}$	OPN	
$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{1N}}$	OON	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{14}}$	PPN	$\overrightarrow{V_{15}}$	NPN	
$\overrightarrow{V_{2P}}$	PPO	$\overrightarrow{V_{3N}}$	NON	$\overrightarrow{V_{2P}}$	PPO	$\overrightarrow{V_{3N}}$	NON	$\overrightarrow{V_{2P}}$	PPO	$\overrightarrow{V_{3N}}$	NON	
$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{1N}}$	OON	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{14}}$	PPN	$\overrightarrow{V_{15}}$	NPN	
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_8}$	OPN	$\overrightarrow{V_8}$	OPN	$\overrightarrow{V_8}$	OPN	$\overrightarrow{V_7}$	OPN	
$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{2N}}$	OPO	$\overrightarrow{V_{2N}}$	OON	$\overrightarrow{V_{3P}}$	OPO	
Sector III												
Region 1a		Region 1b		Region 2a		Region 2b		Region 3		Region 4		
$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_9}$	NPO	$\overrightarrow{V_9}$	NPO	$\overrightarrow{V_9}$	NPO	$\overrightarrow{V_9}$	NPO	
$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{15}}$	NPN	$\overrightarrow{V_{16}}$	NPP	
$\overrightarrow{V_{3N}}$	NON	$\overrightarrow{V_{4P}}$	OPP	$\overrightarrow{V_{3N}}$	NON	$\overrightarrow{V_{4P}}$	OPP	$\overrightarrow{V_{3N}}$	NON	$\overrightarrow{V_{4P}}$	OPP	
$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{15}}$	NPN	$\overrightarrow{V_{14}}$	NPP	
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_9}$	NPO	$\overrightarrow{V_9}$	NPO	$\overrightarrow{V_9}$	NPO	$\overrightarrow{V_9}$	NPO	
$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{3P}}$	OPO	$\overrightarrow{V_{4N}}$	NOO	
Sector IV												

Appendix 2 – Switching Tables

Region 1a		Region 1b		Region 2a		Region 2b		Region 3		Region 4	
$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	OOP
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_{10}}$	NOP	$\overrightarrow{V_{10}}$	NOP	$\overrightarrow{V_{10}}$	NOP	$\overrightarrow{V_{10}}$	NOP
$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{16}}$	NPP	$\overrightarrow{V_{17}}$	NNP
$\overrightarrow{V_{4P}}$	OPP	$\overrightarrow{V_{5N}}$	NNO	$\overrightarrow{V_{4P}}$	OPP	$\overrightarrow{V_{5N}}$	NNO	$\overrightarrow{V_{4P}}$	OPP	$\overrightarrow{V_{5N}}$	NNO
$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{16}}$	NPP	$\overrightarrow{V_{17}}$	NNP
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_{10}}$	NOP	$\overrightarrow{V_{10}}$	NOP	$\overrightarrow{V_{10}}$	NOP	$\overrightarrow{V_{10}}$	NOP
$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	00P	$\overrightarrow{V_{4N}}$	NOO	$\overrightarrow{V_{5P}}$	OOP
Sector V											
Region 1a		Region 1b		Region 2a		Region 2b		Region 3		Region 4	
$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_{11}}$	ONP	$\overrightarrow{V_{11}}$	ONP	$\overrightarrow{V_{11}}$	ONP	$\overrightarrow{V_{11}}$	ONP
$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{17}}$	NNP	$\overrightarrow{V_{18}}$	PNP
$\overrightarrow{V_{5N}}$	NNO	$\overrightarrow{V_{6P}}$	POP	$\overrightarrow{V_{5N}}$	NNO	$\overrightarrow{V_{6P}}$	POP	$\overrightarrow{V_{5N}}$	NNO	$\overrightarrow{V_{6P}}$	POP
$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{17}}$	NNP	$\overrightarrow{V_{18}}$	PNP
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_{11}}$	ONP	$\overrightarrow{V_{11}}$	ONP	$\overrightarrow{V_{11}}$	ONP	$\overrightarrow{V_{11}}$	ONP
$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{5P}}$	OOP	$\overrightarrow{V_{6N}}$	ONO
Sector VI											
Region 1a		Region 1b		Region 2a		Region 2b		Region 3		Region 4	
$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_{12}}$	PNO	$\overrightarrow{V_{12}}$	PNO	$\overrightarrow{V_{12}}$	PNO	$\overrightarrow{V_{12}}$	PNO
$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{18}}$	PNP	$\overrightarrow{V_{13}}$	PNN
$\overrightarrow{V_{6P}}$	POP	$\overrightarrow{V_{1N}}$	ONN	$\overrightarrow{V_{6P}}$	POP	$\overrightarrow{V_{1N}}$	ONN	$\overrightarrow{V_{6P}}$	POP	$\overrightarrow{V_{1N}}$	ONN
$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{18}}$	PNP	$\overrightarrow{V_{13}}$	PNN
$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_0}$	OOO	$\overrightarrow{V_{12}}$	PNO	$\overrightarrow{V_{12}}$	PNO	$\overrightarrow{V_{12}}$	PNO	$\overrightarrow{V_{12}}$	PNO
$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO	$\overrightarrow{V_{6N}}$	ONO	$\overrightarrow{V_{1P}}$	POO

Furthermore, another classical method was implemented for its ability to reduce the CMV. The switching table is presented below.

ZCM switching sequence					
Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6
$V_0\ V_7\ V_{12}\ V_0$	$V_0\ V_8\ V_7\ V_0$	$V_0\ V_9\ V_8\ V_0$	$V_0\ V_{10}\ V_9\ V_0$	$V_0\ V_{11}\ V_{10}\ V_0$	$V_0\ V_{12}\ V_{11}\ V_0$

Appendix 2 – Switching Tables

The first method developed modulation strategy is OLOM. This method is divided into 12 sectors with a displacement angle of 30°. The switching table is presented below.

OLOM Switching table	
Sector 1	$V_0\ V_7\ V_{13}\ V_7\ V_0$
Sector 2	$V_0\ V_7\ V_{14}\ V_7\ V_0$
Sector 3	$V_0\ V_8\ V_{14}\ V_8\ V_0$
Sector 4	$V_0\ V_8\ V_{15}\ V_8\ V_0$
Sector 5	$V_0\ V_9\ V_{15}\ V_9\ V_0$
Sector 6	$V_0\ V_9\ V_{16}\ V_9\ V_0$
Sector 7	$V_0\ V_{10}\ V_{16}\ V_{10}\ V_0$
Sector 8	$V_0\ V_{11}\ V_{16}\ V_{11}\ V_0$
Sector 9	$V_0\ V_{11}\ V_{17}\ V_{11}\ V_0$
Sector 10	$V_0\ V_{11}\ V_{18}\ V_{11}\ V_0$
Sector 11	$V_0\ V_{12}\ V_{18}\ V_{12}\ V_0$
Sector 12	$V_0\ V_{12}\ V_{13}\ V_{12}\ V_0$

Next, another method arises, OSOM. This method is divided into 12 sectors as well as OLOM, but uses small, medium and zero vectors in order to crate the reference vector. Its table can be seen below.

OSOM switching sequence	
Sector 1	$V_0\ V_{1p}\ V_7\ V_{1p}\ V_0$
Sector 2	$V_0\ V_{2n}\ V_7\ V_{2n}\ V_0$
Sector 3	$V_0\ V_{2n}\ V_8\ V_{2n}\ V_0$
Sector 4	$V_0\ V_{3p}\ V_8\ V_{3p}\ V_0$
Sector 5	$V_0\ V_{3p}\ V_9\ V_{3p}\ V_0$
Sector 6	$V_0\ V_{4n}\ V_9\ V_{4n}\ V_0$
Sector 7	$V_0\ V_{4n}\ V_{10}\ V_{4n}\ V_0$
Sector 8	$V_0\ V_{5p}\ V_{10}\ V_{5p}\ V_0$
Sector 9	$V_0\ V_{5p}\ V_{11}\ V_{5p}\ V_0$
Sector 10	$V_0\ V_{6n}\ V_{11}\ V_{6n}\ V_0$
Sector 11	$V_0\ V_{6n}\ V_{12}\ V_{6n}\ V_0$
Sector 12	$V_0\ V_{1p}\ V_{12}\ V_{1p}\ V_0$

Theory states that if all stationary vectors are used the number of levels, in the phase voltage, is maximum. The switching table for ZSML, when in natural balancing, is presented below.

ZSML switching sequence for natural balancing		
	Region 1	Region 2
Sector 1	$V_0\ V_{1p}\ V_7\ V_{13}\ V_7\ V_{1p}\ V_0$	$V_0\ V_{2n}\ V_7\ V_{14}\ V_7\ V_{2n}\ V_0$
Sector 2	$V_0\ V_{2n}\ V_8\ V_{14}\ V_8\ V_{2n}\ V_0$	$V_0\ V_{3p}\ V_8\ V_{15}\ V_8\ V_{3p}\ V_0$
Sector 3	$V_0\ V_{3p}\ V_9\ V_{15}\ V_9\ V_{3p}\ V_0$	$V_0\ V_{4n}\ V_9\ V_{16}\ V_9\ V_{4n}\ V_0$

Sector 4	$V_0\ V_{4n}\ V_{10}\ V_{16}\ V_{10}\ V_{4n}\ V_0$	$V_0\ V_{5p}\ V_{10}\ V_{17}\ V_{10}\ V_{5p}\ V_0$
Sector 5	$V_0\ V_{5p}\ V_{11}\ V_{17}\ V_{11}\ V_{5p}\ V_0$	$V_0\ V_{6n}\ V_{11}\ V_{18}\ V_{11}\ V_{6n}\ V_0$
Sector 6	$V_0\ V_{6n}\ V_{12}\ V_{18}\ V_{12}\ V_{6n}\ V_0$	$V_0\ V_{1p}\ V_{12}\ V_{13}\ V_{12}\ V_{1p}\ V_0$

Furthermore, if the DC link is unbalanced due to an external event the next switching tables are going to be used until the perturbation is eliminated.

ZSML switching sequence in balancing mode – P and N type tables				
	Region 1 – P type	Region 2 – P type	Region 1 – N type	Region 2 – N type
Sector 1	$V_0\ V_{1p}\ V_7\ V_{13}\ V_7\ V_{1p}\ V_0$	$V_0\ V_{2p}\ V_{14}\ V_7\ V_{14}\ V_{2p}\ V_0$	$V_0\ V_7\ V_{13}\ V_{1n}V_{13}\ V_7\ V_0$	$V_0\ V_{2n}\ V_7\ V_{14}\ V_7\ V_{2n}\ V_0$
Sector 2	$V_0\ V_{2p}\ V_{14}\ V_8\ V_{14}\ V_{2p}\ V_0$	$V_0\ V_{3p}\ V_8\ V_{15}\ V_8\ V_{3p}\ V_0$	$V_0\ V_{2n}\ V_8\ V_{14}\ V_8\ V_{2n}\ V_0$	$V_0\ V_8\ V_{15}\ V_{3n}\ V_{15}\ V_8\ V_0$
Sector 3	$V_0\ V_{3p}\ V_9\ V_{15}\ V_9\ V_{3p}\ V_0$	$V_0\ V_{4p}\ V_{16}V_9\ V_{16}\ V_{4p}\ V_0$	$V_0\ V_9\ V_{15}\ V_{3n}\ V_{15}\ V_9\ V_0$	$V_0\ V_{4n}\ V_9\ V_{16}\ V_9\ V_{4n}\ V_0$
Sector 4	$V_0\ V_{4p}\ V_{16}V_{10}\ V_{16}\ V_{4p}\ V_0$	$V_0\ V_{5p}\ V_{10}\ V_{17}\ V_{10}\ V_{5p}\ V_0$	$V_0\ V_{4n}\ V_{10}V_{16}\ V_{10}\ V_{4n}\ V_0$	$V_0\ V_{10}\ V_{17}\ V_{5n}\ V_{17}\ V_{10}\ V_0$
Sector 5	$V_0\ V_{5p}\ V_{11}\ V_{17}\ V_{11}\ V_{5p}\ V_0$	$V_0\ V_{6p}\ V_{18}\ V_{11}\ V_{18}\ V_{6p}\ V_0$	$V_0\ V_{11}\ V_{17}\ V_{5n}\ V_{17}\ V_{11}\ V_0$	$V_0\ V_{6n}\ V_{11}\ V_{18}\ V_{11}\ V_{6n}\ V_0$
Sector 6	$V_0\ V_{6p}\ V_{18}\ V_8\ V_{18}\ V_{6p}\ V_0$	$V_0\ V_{1p}\ V_{12}\ V_{13}\ V_{12}\ V_{1p}\ V_0$	$V_0\ V_{6n}\ V_{12}\ V_{18}\ V_{12}\ V_{6n}\ V_0$	$V_0\ V_{12}\ V_{13}\ V_{1n}V_{13}\ V_{12}\ V_0$

Based on nearest three vectors idea, another method was developed. This method randomises the switching table in order to reduce the CMV. The switching sequence can be seen below. As ZSML, this method has the ability to balance the DC link in case of an external event.

RS3N switching sequence when in natural balancing mode						
	Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6
Region 1	$V_{1p}\ V_0\ V_{2n}$	$V_{2n}\ V_0\ V_{3p}$	$V_{3p}\ V_0\ V_{4n}$	$V_{4n}\ V_0\ V_{5p}$	$V_{5p}\ V_0\ V_{6n}$	$V_{6n}\ V_0\ V_{1p}$
Region 2	$V_{1p}\ V_7\ V_{2n}$	$V_{2n}\ V_8\ V_{3p}$	$V_{3p}\ V_9\ V_{4n}$	$V_{4n}\ V_{10}\ V_{5p}$	$V_{5p}\ V_{11}\ V_{6n}$	$V_{6n}\ V_{12}\ V_{1p}$
Region 3	$V_{1p}\ V_7\ V_{13}$	$V_{2n}\ V_8\ V_{14}$	$V_{3p}\ V_9\ V_{15}$	$V_{4n}\ V_{10}\ V_{16}$	$V_{5p}\ V_{11}\ V_{17}$	$V_{6n}\ V_{12}\ V_{18}$
Region 4	$V_{2n}\ V_7\ V_{14}$	$V_{3p}\ V_8\ V_{15}$	$V_{4n}\ V_9\ V_{16}$	$V_{5p}\ V_{10}\ V_{17}$	$V_{6n}\ V_{11}\ V_{18}$	$V_{1p}\ V_{12}\ V_{13}$

RS3N switching sequence when in balancing mode						
	Sector 1	Sector 2	Sector3	Sector 4	Sector 5	Sector 6
Region 1 – P Type	$V_{1p}\ V_0\ V_{2p}$	$V_{2p}\ V_0\ V_{3p}$	$V_{3p}\ V_0\ V_{4p}$	$V_{4p}\ V_0\ V_{5p}$	$V_{5p}\ V_0\ V_{6p}$	$V_{6p}\ V_0\ V_{1p}$
Region 2 – P Type	$V_{1p}\ V_7\ V_{2p}$	$V_{2p}\ V_8\ V_{3p}$	$V_{3p}\ V_9\ V_{4p}$	$V_{4p}\ V_{10}\ V_{5p}$	$V_{5p}\ V_{11}\ V_{6p}$	$V_{6p}\ V_{12}\ V_{1p}$
Region 3 – P Type	$V_{1p}\ V_7\ V_{13}$	$V_{2p}\ V_8\ V_{14}$	$V_{3p}\ V_9\ V_{15}$	$V_{4p}\ V_{10}\ V_{16}$	$V_{5p}\ V_{11}\ V_{17}$	$V_{6p}\ V_{12}\ V_{18}$
Region 4 – P Type	$V_{2p}\ V_7\ V_{14}$	$V_{3p}\ V_8\ V_{15}$	$V_{4p}\ V_9\ V_{16}$	$V_{5p}\ V_{10}\ V_{17}$	$V_{6p}\ V_{11}\ V_{18}$	$V_{1p}\ V_{12}\ V_{13}$
Region 1 – N Type	$V_{1n}\ V_0\ V_{2n}$	$V_{2n}\ V_0\ V_{3n}$	$V_{3n}\ V_0\ V_{4n}$	$V_{4n}\ V_0\ V_{5n}$	$V_{5n}\ V_0\ V_{6n}$	$V_{6n}\ V_0\ V_{1n}$
Region 2 – N Type	$V_{1n}\ V_7\ V_{2n}$	$V_{2n}\ V_8\ V_{3n}$	$V_{3n}\ V_9\ V_{4n}$	$V_{4n}\ V_{10}\ V_{5n}$	$V_{5n}\ V_{11}\ V_{6n}$	$V_{6n}\ V_{12}\ V_{1n}$
Region 3 – N Type	$V_{1n}\ V_7\ V_{13}$	$V_{2n}\ V_8\ V_{14}$	$V_{3n}\ V_9\ V_{15}$	$V_{4n}\ V_{10}\ V_{16}$	$V_{5n}\ V_{11}\ V_{17}$	$V_{6n}\ V_{12}\ V_{18}$
Region 4 – N Type	$V_{2n}\ V_7\ V_{14}$	$V_{3n}\ V_8\ V_{15}$	$V_{4n}\ V_9\ V_{16}$	$V_{5n}\ V_{10}\ V_{17}$	$V_{6n}\ V_{11}\ V_{18}$	$V_{1n}\ V_{12}\ V_{13}$

Appendix 3: Experimental Setup Data

When the experiments were performed the following devices were used as a part of the setup:

- 2x SM 300-5, 300V, 5A Power Supplies
- 1x SM 600-10, 600V, 10A Power Supply
- 1x GwInstek GPS-4303, 12v Power Supply
- 1x Tektronix DPO 2014 Digital Phosphor Oscilloscope
- 3x Tektronix P5200 High Voltage Differential Probe 130v / 1300v
- 1x Tektronix TCP0150 Current Probe, 150A, 20 MHz
- 1x Fluke 179 True RMS Multimeter
- 4x Tektronix P2221 Voltage Probe
- 1x Digilent HS1 JTAG Emulator for CPLD
- 1x Signum JTAGJET-C2000 JTAG Emulator for DSP
- 1x National Instruments NI cDAQ-9172 Acquisition System Chasis
- 1x NI 9227 Quad Current Sensor Module
- 2x ASEA Load Inductor, 3 kVAr
- 2x ASEA 5514 152-8, 220/95 V, 4000 ohm, Load Resistor, 4.5 / 2 kW,
- 1x Zentro Elektric Electronic Load, EL1000/800/20, Vi=230v, 50hz, 0.2A, V0=800v, 20A, 1000W.
- 2x Danotherm 23 E, 12.5 ohm, 13.6 A Variable Resistors
- 1x Danotherm 23 E, 2.5 ohm, 13.6 A Variable Resistor
- 1x Danotherm 23 E, 5000 ohm, 0.33 A Variable Resistor
- 1x Danotherm 23 D, 500 ohm, 0.96 A Variable Resistor
- 1x ABB Induction Motor, M2VA80C-2 3GVA081003-ASB, Wye Connection, 380-420V, 50hz, 2840 rpm, 1.5 kW, 3.4/5.7 A, cos(fi)=0.83
- 1x Transtecno DC Motor, EC350.240, 24V, 29.4A, 3000 rpm, 1.57 Nm, 0.5 kW
- 1x Forward Looking Infra-Red (FLIR) Camera – Thermal Camera
- Three Phase Switch, 72502E, AAU

Appendix 4: CPLD/DSP Pin Assignment

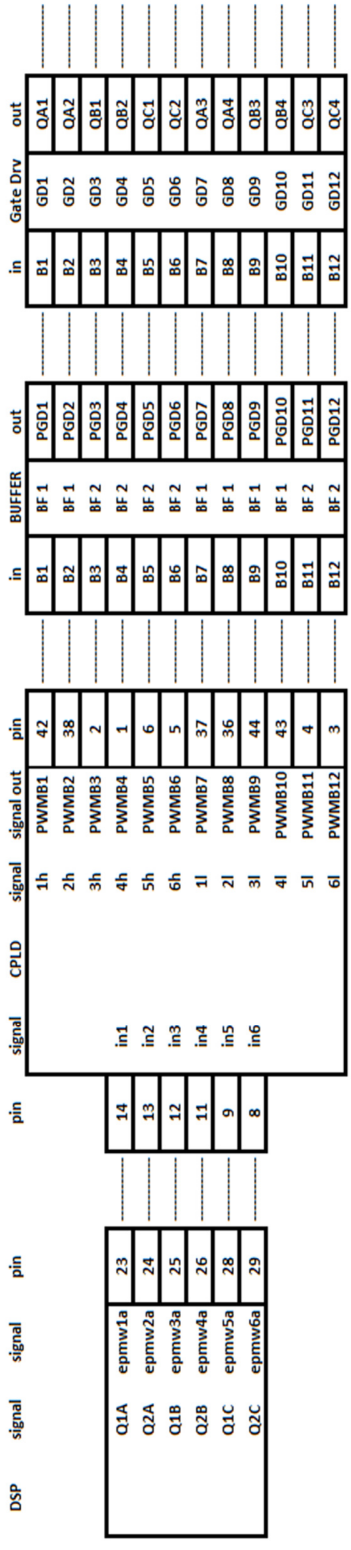
When the modulation strategies have been developed on the DSP, the pin assignment had to be performed. This was done accordingly to the DSP hardware design guidelines [**67**].

DSP Pin Assignment									
Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	3V3 ISO	21	GND A	41	NC	61	GND A	81	GPIO 85
2	RXA_ISO	22	NC	42	GPIO 87	62	GND A	82	5V D
3	NC	23	EPWM 1A	43	NC	63	GND A	83	NC
4	NC	24	EPWM 2A	44	CAN RXA	64	GND A	84	NC
5	NC	25	EPWM 3A	45	NC	65	GND A	85	NC
6	GND ISO	26	EPWM 4A	46	NC	66	GND A	86	NC
7	ADC PHASE A	27	GND D	47	GND D	67	GND A	87	5V D
8	GND A	28	EPWM 5A	48	TCK	68	NC	88	NC
9	ADC PHASE B	29	EPWM 6A	49	TMS	69	GND A	89	NC
10	GND A	30	NC	50	EMU1	70	NC	90	NC
11	ADC PHASE C	31	GPIO 84	51	3V3 ISO	71	GND A	91	NC
12	GND A	32	GPIO 86	52	TXA ISO	72	NC	92	5V D
13	ADC DC+	33	NC	53	NC	73	NC	93	NC
14	GND A	34	NC	54	NC	74	NC	94	CAN TXA
15	ADC DC-	35	NC	55	NC	75	NC	95	TO DSP
16	GND A	36	NC	56	GND ISO	76	NC	96	5V D
17	GND A	37	GND D	57	GND A	77	5V D	97	TDI
18	NC	38	NC	58	GND A	78	TXB	98	TDO
19	GND A	39	NC	59	GND A	79	RXB	99	TRSTn
20	NC	40	NC	60	GND A	80	NC	100	EMU0

The CPLD pin configuration can be seen in the following table.

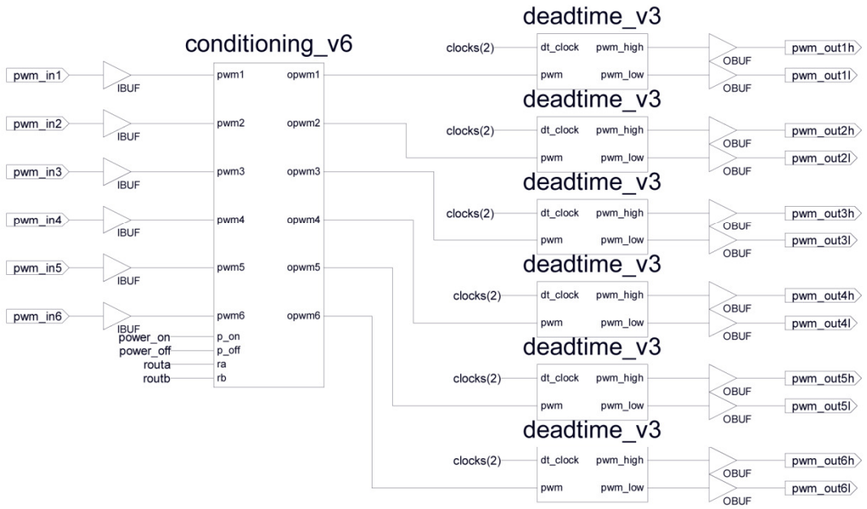
CPLD Pin Assignment							
Pin No.	Function	Pin No.	Function	Pin No.	Function	Pin No.	Function
1	PWM_out 4	12	PWM_in 3	23	GND	34	Over temp B
2	PWM_out 3	13	PWM_in 2	24	DC OV	35	Over temp A
3	PWM_out 12	14	PWM_in 1	25	DC OC	36	PWM_out 8
4	PWM_out 11	15	TDI	26	Demux C	37	PWM_out 7
5	PWM_out 6	16	TMS	27	Demux B	38	PWM_out 2
6	PWM_out 5	17	TCK	28	Demux A	39	GSR
7	GCK3	18	Buffer Enable	29	NC	40	GTS2
8	PWM_in 6	19	To DSP	30	TDO	41	Vcc +3V3
9	PWM_in 5	20	Fault Gate Driver	31	GND	42	PWM_out 1
10	GND	21	Vcc +3V3	32	Vcc +3V3	43	PWM_out 10
11	PWM_in 4	22	NC	33	Over current	44	PWM_out 9

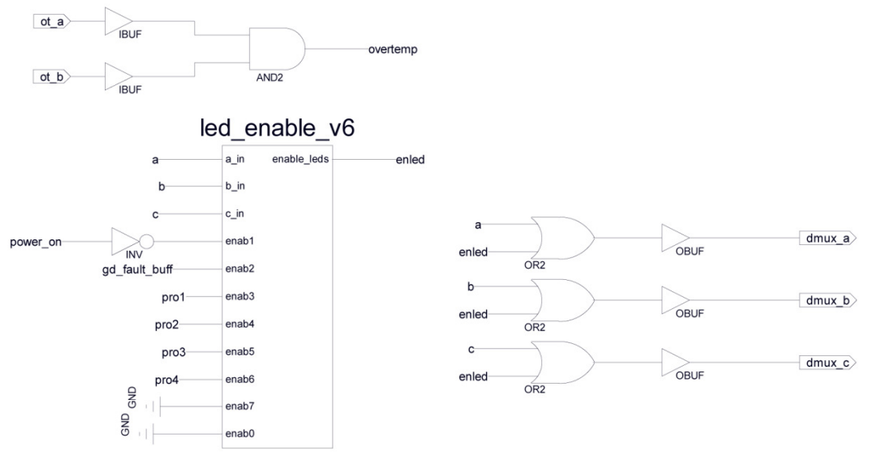
The following figure shows how the control signal path.

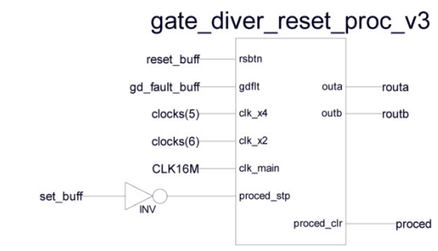


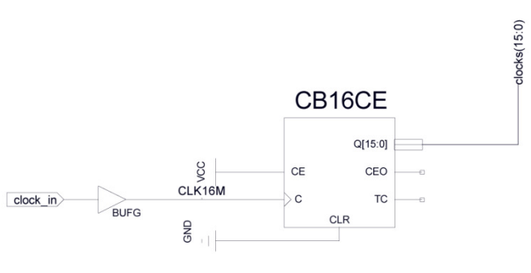
Signal Path from DSP to gate drives

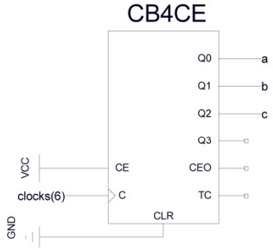
Appendix 5: CPLD Functional Schematic

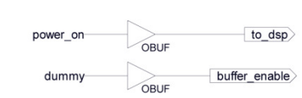


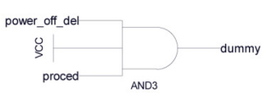


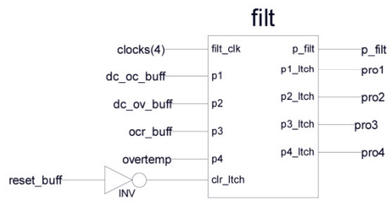


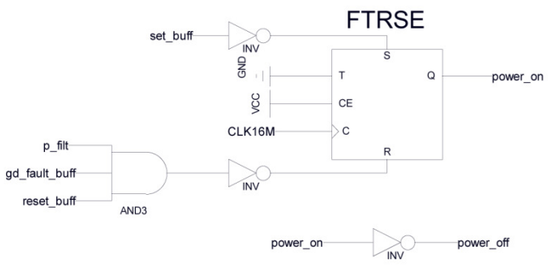


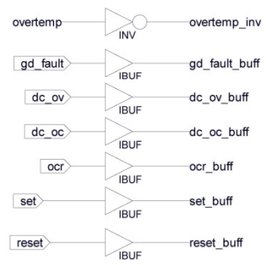








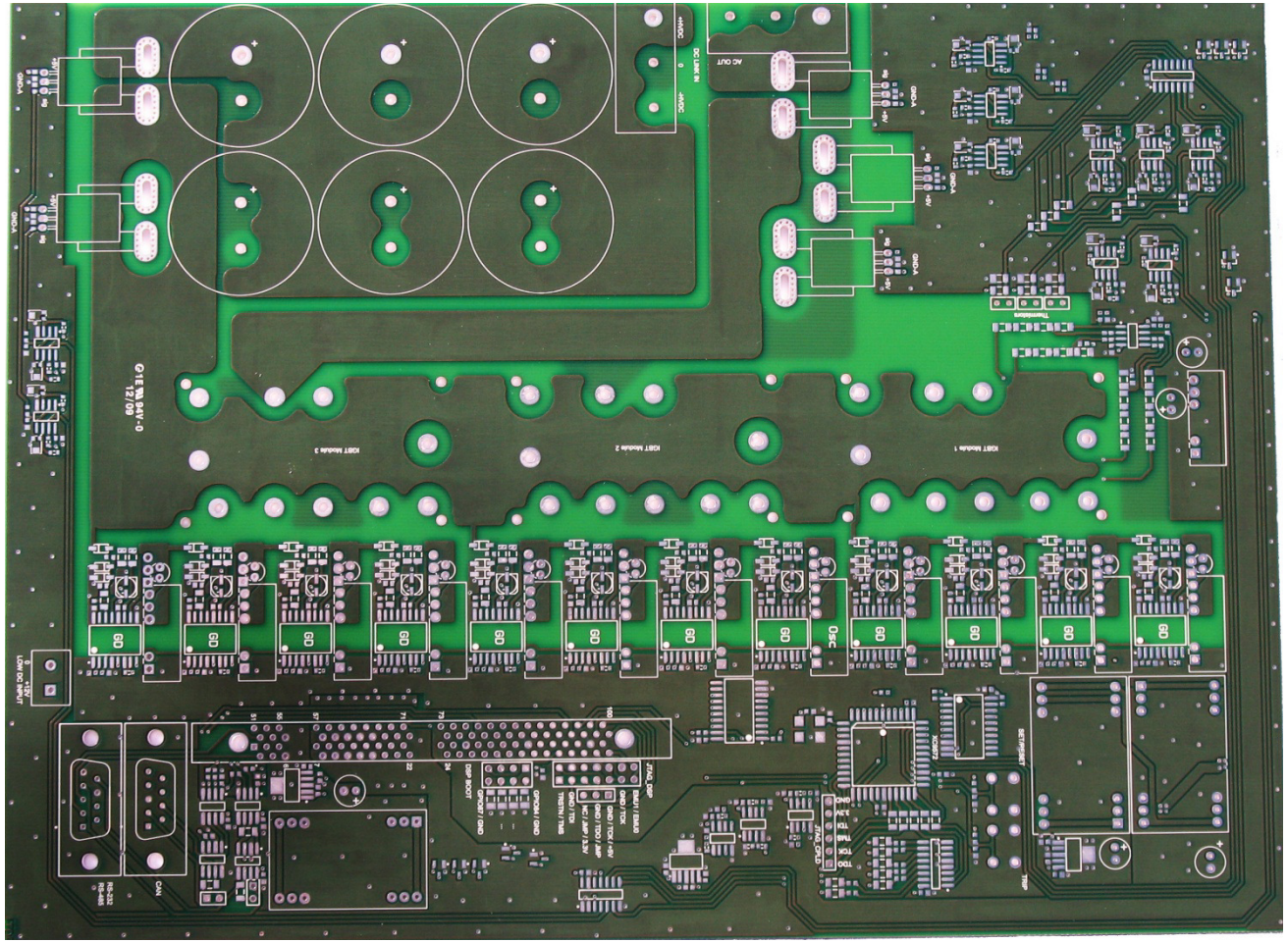


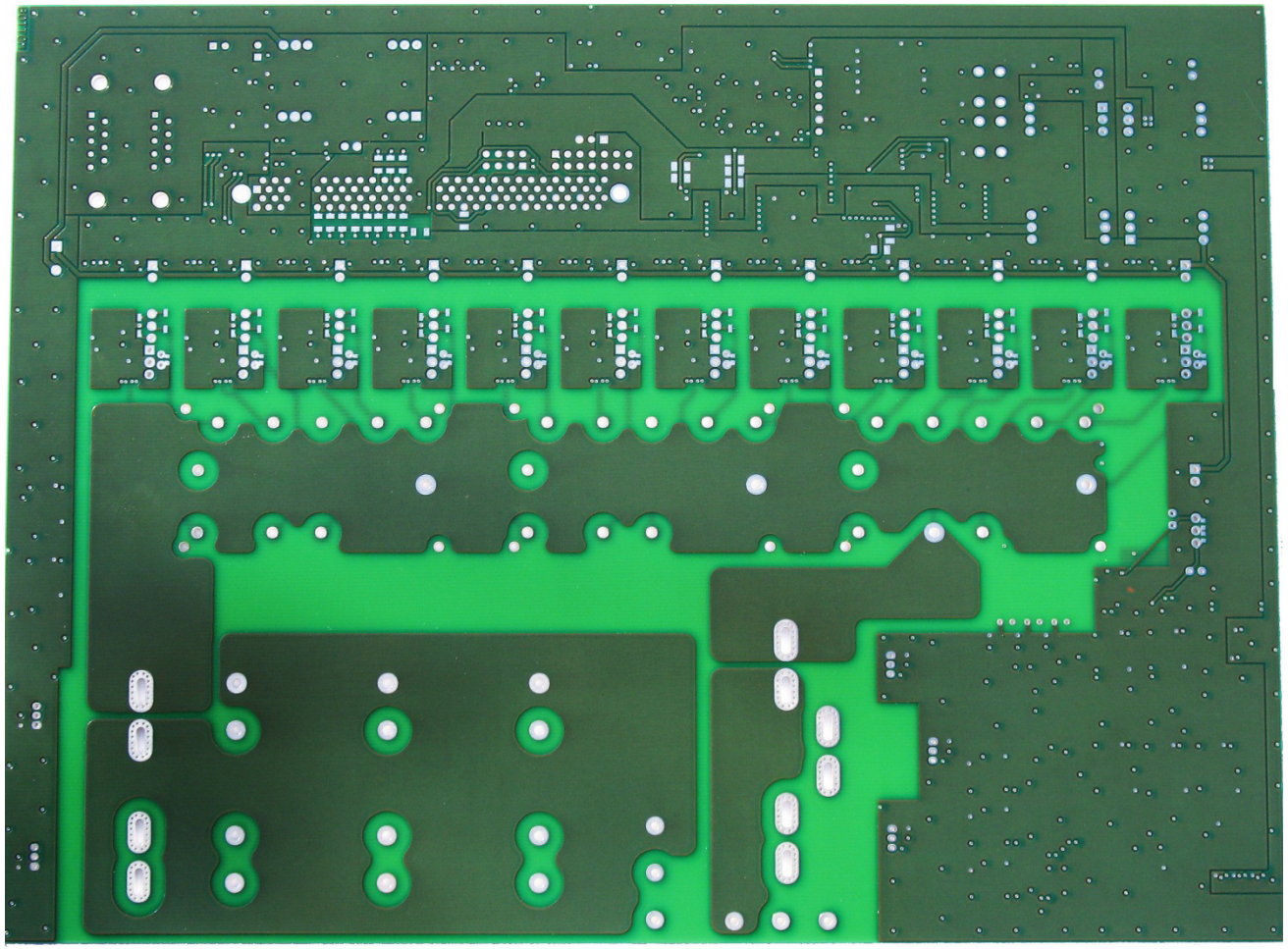


Title: Three Level NPC Inverter
Revision: 9
Date: 25.05.2012
Authors: Daniela B. and Ciprian B.

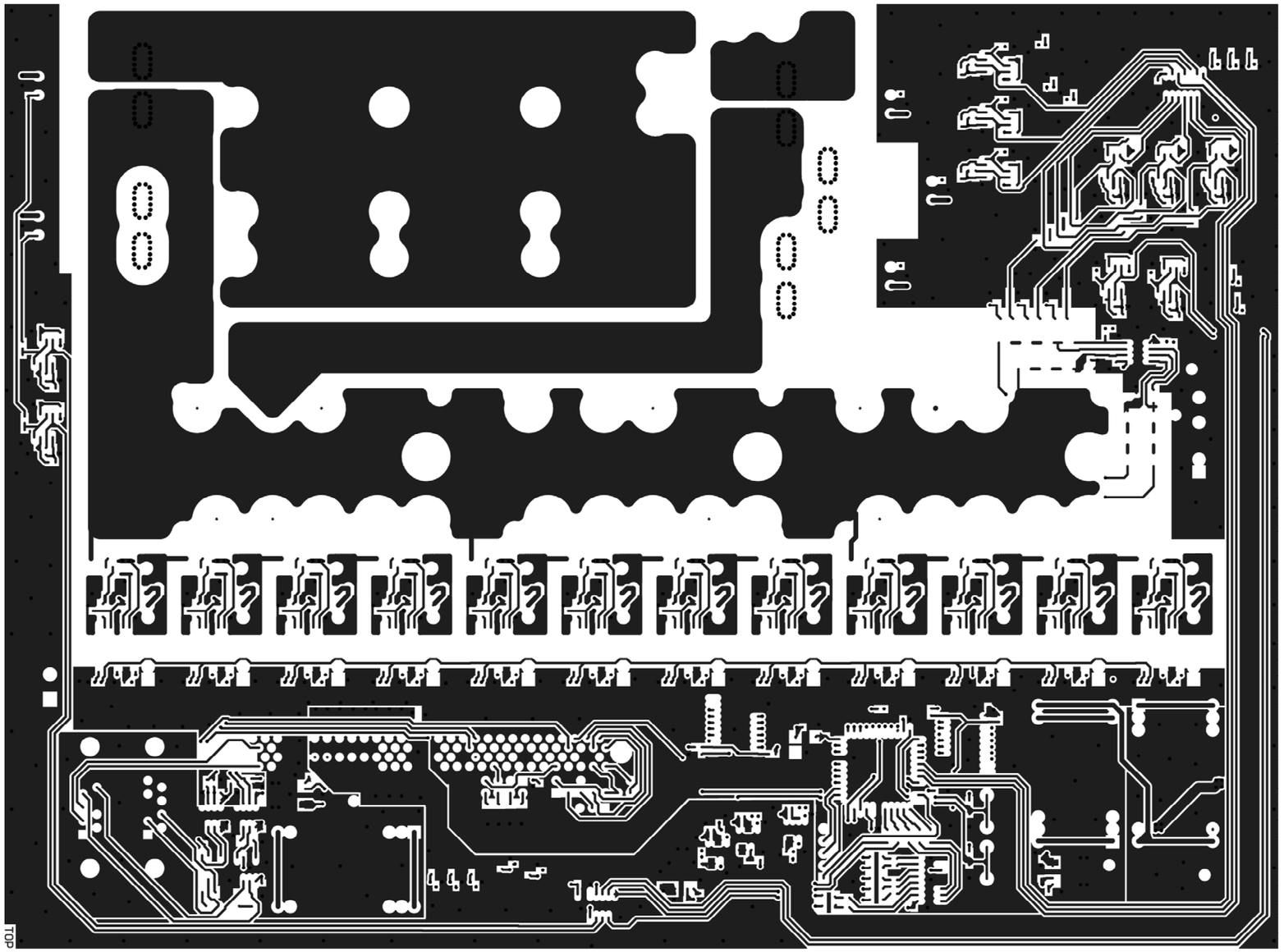
Appendix 5: CPLD Functional Schematic

Appendix 6: PCB Photos





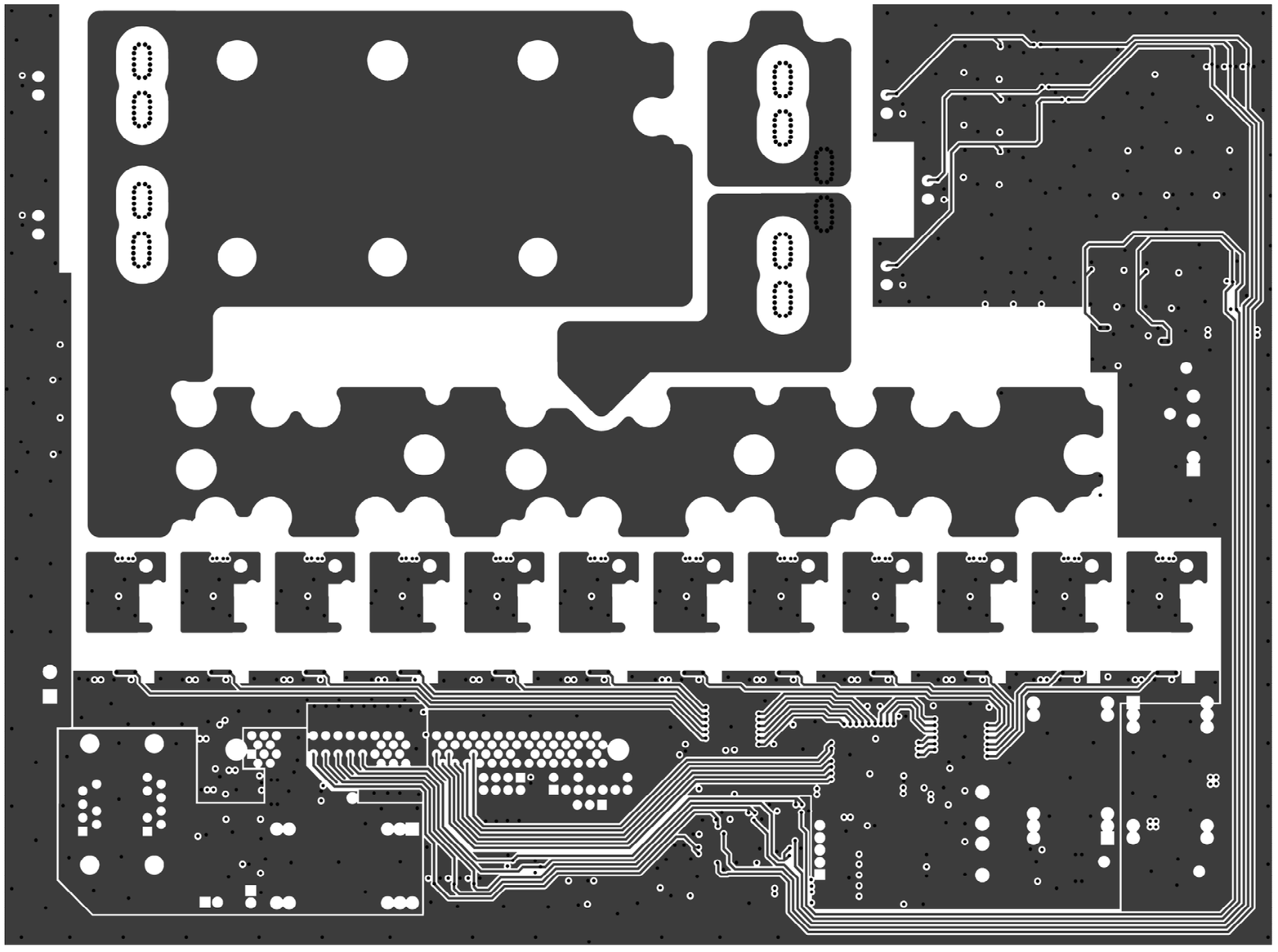
Appendix 7: PCB Layers



Layer 1

Appendix 7: PCB Layers

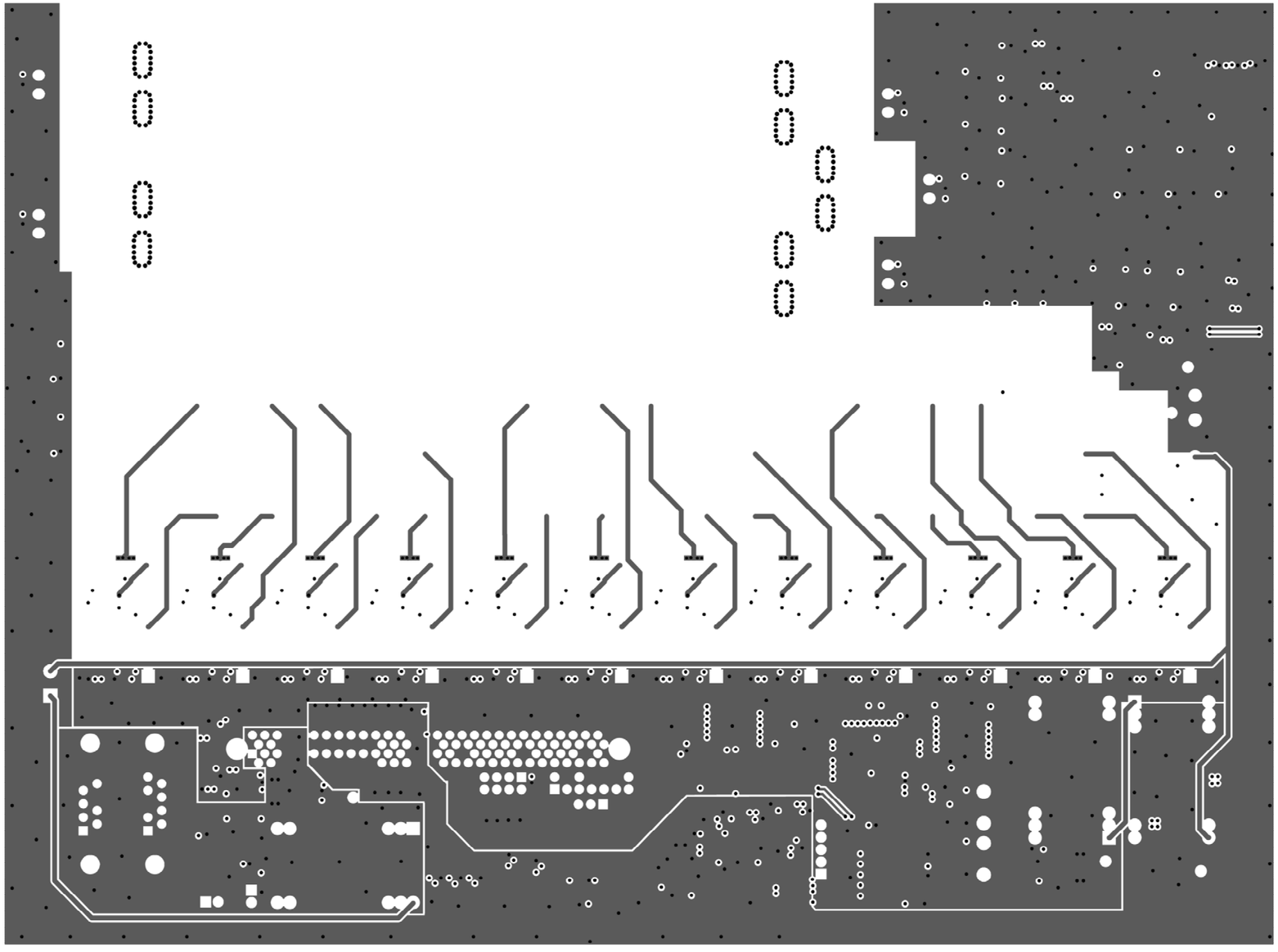
Layer 1



Layer 2

Appendix 7: PCB Layers

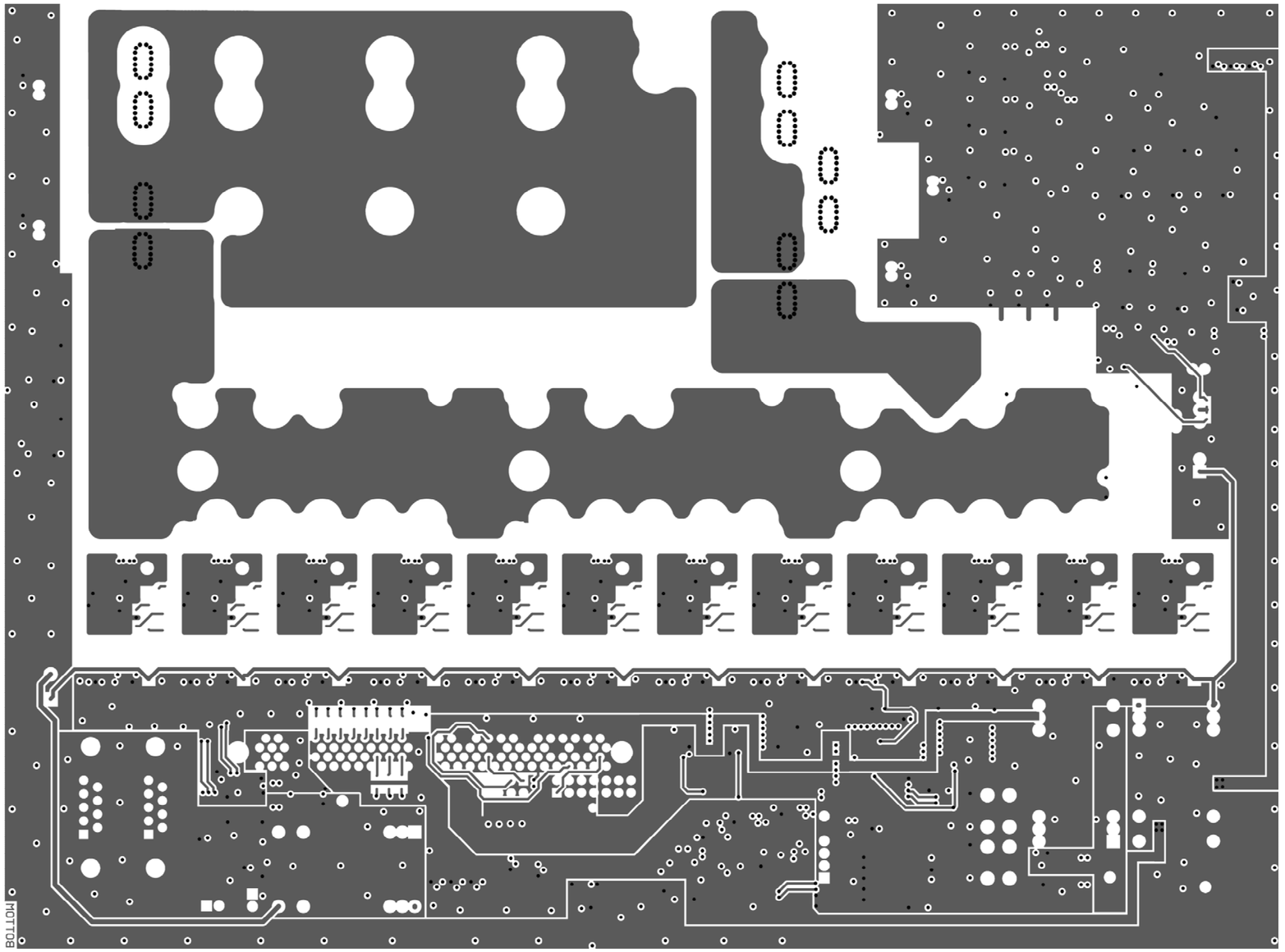
Layer 2



Layer 3

Appendix 7: PCB Layers

Layer 3

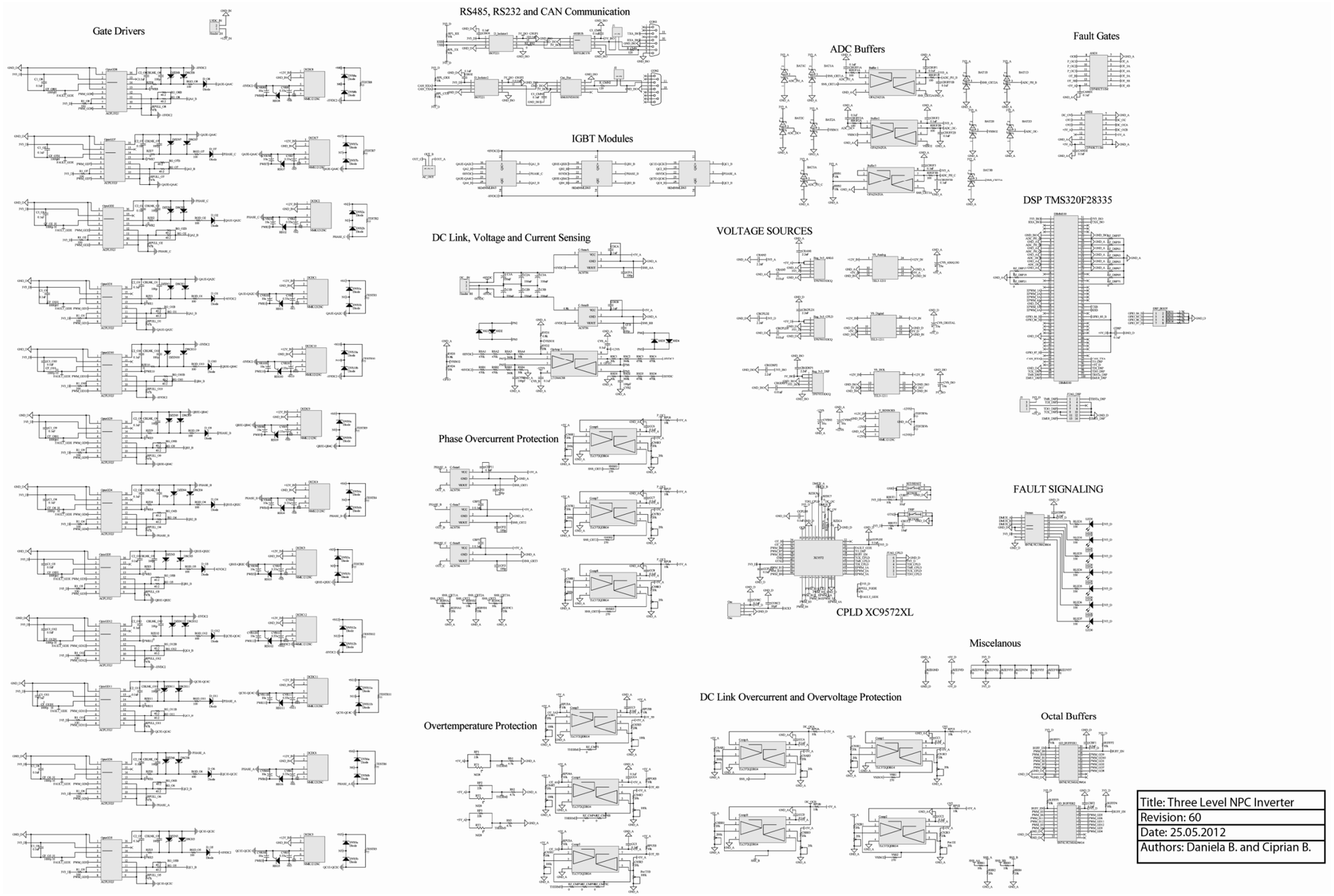


Layer 4

Appendix 7: PCB Layers

Layer 4

Appendix 8: Electrical Schematic



Title: Three Level NPC Inverter
Revision: 60
Date: 25.05.2012
Authors: Daniela B. and Ciprian B.

Appendix 8: Electrical Schematic

Appendix 9: Bill of Materials

NO.	Value	Order Code	Provider	Manufactured	Manufactured Code	Pieces
1	Capacitor 10pF	499110	farnell	AVX	06035A100JAT2A	1
2	Capacitor 100pF	1414603	farnell	Kemet	C0603C101J5GACTU	19
3	Capacitor 1000pF	1414605RL	farnell	Kemet	C0603C102J5GACTU	12
4	Capacitor 0.01uF	722236	farnell	Yageo	CC0603KRX7R9BB103	3
5	Capacitor 0.1uF	1759122RL	farnell	Multicorp	MCCA000255	65
6	Capacitor 0.33u	1870967	farnell	Multicorp	MCMR50V334M4X7	12
7	Capacitor 2.2uF	1845734	farnell	Murata	1845734	6
8	Capacitor 10uF	1458902	farnell	Yageo	CC0603MRX5R5BB106	15
9	Capacitor 10uF	1539492	farnell	Panasonic	EEEFPV100UAR	2
10	Capacitor 33uF	1870963	farnell	Multicomp	MCMR35V336M6.3X7	2
11	Capacitor 330uF	1198688	farnell	Panasonic	EETUQ2W331DA	6
12	Diode 35 ns	1559131	farnell	Taiwan Semi	ES1JL	12
13	Diode Schottjy 40V 0.5A	9556923	farnell	On Semi	MBR0540T1G	12
14	Diode Schottjy BAT54S	9801510	farnell	STMicroelectronics	BAT54SFILM	10
15	Diode Schottky 30V, 0.5A	1863142	farnell	TAIWAN SEMICONDUCTOR	B0530W	24
16	Diode Small Signal	8150192RL	farnell	Taiwan Semi	TS4148 RZG	4
17	Diode Zener 10V	1431280RL	farnell	On Semi	MMSZ5240BT1G	12
18	Connector DE9	x	x	x	x	2
19	Connector DIMM100	DIMM100	mouser	Molex	87630-1001	1
20	Connector 39 pin header	x	x	x	x	1
21	Connector Header 2H	425-8720	rs-online	Weidmuller	PM 5.08/2/90 3.5 SW	1
22	Connector Headere 3H	692-0553	rs-online	Amphenol	ESPM03200	2
23	IC CAN Transciever	1220984	farnell	Texas Instruments	SN65HVD1050D	1
24	IC Comparator	660-6783	rs-online	Texas Instruments	TLC372QDRG4	10
25	IC CPLD	1193232	farnell	xilinx	XC9572XL-10PCG44C	1
26	IC Current Sensor	1791390	farnell	Allegro	ACS756SCA-050B-PFF-T	5
27	IC Demultiplexer	662-8617	rs-online	Texas Instruments	SN74LVC138ADRG4	1
28	IC Digital Isolator	660-7679	rs-online	Texas Instruments	ISO7221BDG4	2
29	IC Gate Driver	1640541	farnell	Avago	ACPL-332J-000E	12
30	IC Octal Buffer	663-2899	rs-online	Texas Instruments	SN74LVC540ADWG4	2
31	IC OpAmp	461-8526	rs-online	Texas Instruments	OPA2343UA	3
32	IC OpAmp	9560483	farnell	Linear Technology	LT1366CS8#PBF	1
33	IC Quartz	478-8653	rs-online	IQD	LFSPXO018038	1
34	IC RS 485 Transciever	527-877	rs-online	Texas Instruments	SN75LBC176DRG4	1
35	IC Triple Input	1739952	farnell	Texas Instruments	CD74HCT11M	2

	AND Gate					
36	IC Voltage Regulator 18V	9756183	farnell	ST	L78S18CV	12
37	IC Voltage Regulator 3.3V	620-1899	rs-online	Texas Instruments	TPS79533DCQ	3
38	Resistor 0	1692540	farnell	Vishay	CRCW12060000ZSTA	44
39	Resistor 40.2	1501453RL	farnell	Te Conect.	RP73D2B40R2BTG	24
40	Resistor 100	9238360RL	farnell	Yageo	RC0603FR-07100RL	17
41	Resistor 120	223-2136	rs-online	TE Connectivity	CRG1206F120R	2
42	Resistor 270	1577598RL	farnell	Panasonic	ERA3AEB271V	5
43	Resistor 330	740-8931	rs-online	Bourns	CR0603-JW-331GLF	19
44	Resistor 470	9331239RL	farnell	Multicorp	MC 0.063W 0603 1% 470R	1
45	Resistor 2.7K	9337288RL	farnell	Multicomp	MC 0.125W 1206 5% 2K7	4
46	Resistor 4.7k	x	x	x	x	3
47	Resistor 6.8k	1717690RL	farnell	Panasonic	ERA3APB682P	2
48	Resistor 10k	1469748RL	farnell	Vishay	CRCW060310K0FKEA	44
49	Resistor 20k	1160374	farnell	Welwyn	PCF0603R 20KB.T1	27
50	Resistor 22k	x	x	x	x	3
51	Resistor 30k	1841783RL	farnell	Panasonic	ERA8AEB303V	4
52	Resistor 47k	1697398	farnell	Te	CPF0603B47KE1	12
53	Resistor 470k	1841811	farnell	Panasonic	ERA8AEB474V	8
54	Resistor 560k	1841813	farnell	Panasonic	ERA8AEB564V	4
55	Potentiometer 20k	691-2612	rs-online	Bourns	3302W-3-203E	9
56	Potentiometer 100k	729-9673	rs-online	Panasonic	EVM2WSX80B15	6
57	Potentiometer 200k	729-9676	rs-online	Panasonic	EVM2WSX80B25	5
58	Thermistor	697-4588	rs-online	AVX	NJ28RA0104F	3
59	LED Green	1466000	farnell	Dialight	5988270107F	2
60	LED Red	1465997	farnell	Dialight	5988210107F	5
61	Push Button - Green	1550259	farnell	Multicorp	TS0B26	1
62	Push Button - Red	1550258	farnell	Multicorp	TS0B23	1
63	DCDC 12 -> +-12	689-5236P	rs-online	Murata	NMK1212SC	13
64	DCDC 12 -> 5V	396-5146	rs-online	Traco	TEL 3-1211	3
65	IGBT Module	X	semikron	Semikron	SK50MLI065	3
66	ControlCard DSP	X	ti	Texas Instruments	x	1
67	Heatsink	148121	farnell	H S MARSTON	96CN-02500-A-200	1
68	PCB	X	printline	printline.dk	x	1

Appendix 10: Paper

Development of Modulation Strategies for NPC Converter Addressing DC Link Voltage Balancing and CMV Reduction

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Abstract—**Multilevel inverters are more popular due to their superior performance compared with two level inverters. One of the most optimal applications for multilevel inverter is the Adjustable Speed Drives (ASD). The industry reported numerous ASD failures due to high frequency PWM. Those failures consist in insulation breakdown and bearing failures. By the use of this type of converters, both Electromagnetic Interference (EMI) and harmonic distortions are improved.**

This paper proposes two modulation strategies for Three Level Neutral Point Clamped Converter (3L-NPC). The main focus of these modulation strategies is to reduce the Common Mode Voltage (CMV) and balance the DC Link Voltage.

Keywords- 3L-NPC Converter, Modulation Strategies, DC Link Balancing, CMV Reduction, Multilevel, SVM

I. INTRODUCTION

An important issue nowadays is saving energy. Electrical motors are widely used to generate motion from electrical energy [1]. Industrial and domestic applications use electric motors with a large variety of power ratings. In industrialized countries, electric motors use approximately 70% of the produced electric energy [2]. In the past, DC machines were used for their simplicity in speed control. Nevertheless, these types of machines have some disadvantages compared with AC machines. AC machines cannot be efficiently controlled with direct connection to the grid, thus adjustable speed drives (ASD) for control of the magnitude and frequency of the output voltage are required. These types of drives have a large scale of utilization in industrial applications. Due to the development of adjustable drives, the reliance in three phase AC motors has increased [1]. ASD are often used in industrial and household applications, like ventilation system, pumps and electric drives for machine tools. By the use of the ASD the output speed can be modified through magnitude and frequency of the output voltage by means of PWM [2].

When talking about three level Voltage Source Inverters (VSI), there has to be mentioned that since their invention they have been considered to be used in high capacity, high performance AC drives applications [3]. Common Mode Voltage (CMV) is defined as the voltage between the neutral point and ground and it is generated by the PWM strategies. This type of voltage creates important problems when talking of high switching frequencies. The techniques regarding attenuation of high frequency problems in AC motor drives systems have at base the reduction of CMV. This voltage has a very important influence over the shaft voltage [2]. One important solution for reducing the shaft voltage and leakage current is the reduction of CMV. This can be done by two methods:

- Attenuation of the shaft voltage through motor design
- CMV attenuation through PWM strategy

It has to be mentioned that there exists different capacitive couplings between the ASD system and motor. When talking about low frequency analysis in drives systems these capacitances can be neglected due to their small values, but their effects become important when the switching frequency of the converter is increased as the switching devices are improved. These capacitances offer a flow path for high frequency currents.

One important problem discovered in 3L-NPC converter is the balancing of the DC link Neutral Point (NP). This type of inverter is exposed to problems like fluctuations in the NP due to irregular and unpredictable charging and discharging of the upper and lower DC link capacitors. As it is defined in [3], there exists an unbalance regarding the charging and discharging in each capacitor, thus the voltage across the capacitor may rise or fall and the NP voltage will not be able to keep half of the DC link voltage. Due to this problem, a high voltage may be applied to the semiconductors or DC link capacitors causing damage. This can be solved through three methods:

- Separate DC sources [4].
- Voltage regulators for each level using an additional small leg [5].

- Modified PWM pattern and voltage vector selection [4] [6]

This paper presents improved modulation strategies that reduces CMV and/or balances the DC link voltage.

II. NPC Converter and Classical Modulation Strategies

Two classical modulation strategies will be shortly presented. These methods are presented for comparison with the developed modulation strategies.

A. NPC Converter Theory

In order to produce AC voltage waveforms with multiple levels, the diode – clamped multilevel inverter employs clamping diodes and cascade DC capacitors. This topology can have three, four or five levels. In high power, the configuration that is used most often is three level neutral point clamped inverter. The most important characteristic of the NPC inverter, in comparison with two level inverters is that in AC output voltage dv/dt and THD is reduced [7].

Figure II-1 presents a layout of a NPC inverter leg. This leg is composed of four switches (T1 to T4) with anti-parallel diodes (D1 to D4) and two clamping diodes (D5 and D6). In real life, forward diodes are comprised in the switching device module if they are IGBTs. A zero DC voltage point is present, which ensures the switching of each phase output to one of the three level voltages. The most important benefit of this configuration is that every switching device needs to block only half of the DC link voltage. But new problem is emphasized that DC link created by the two series capacitors needs to be balanced. For this problem there are two solutions [8]:

- Connect each capacitor to its own isolated DC source.
- Balance of the midpoint by feedback control.

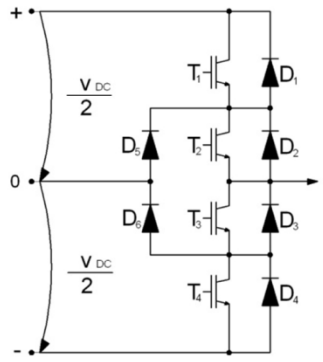


Figure II-1 NPC Leg

The midpoint charge is related to the switching vectors. There are a total number of 24 active vectors which can be split in three categories: large, medium and small vectors. There are 6 large vectors, 6 medium vectors and 12 small vectors. There are 3 additional zero vectors. The large vectors do not have connection to the midpoint so they are free from charge balance [9].

The influence of these vectors has been studied in [10] and can be seen in **Table II-1**.

Table II-1 – Influence of Space Vectors on CMV

State	Vector Type	CMV (V0=0)	CMV (V0≠0)
000	Zero	0	V_{DC}
NNN	Zero	$-\frac{1}{2}V_{DC}$	$-\frac{1}{2}V_{DC}$
PPP	Zero	$\frac{1}{2}V_{DC}$	$\frac{1}{2}V_{DC}$
NOO	Small	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
ONO	Small	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
OON	Small	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
POO	Small	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
OPO	Small	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
OOP	Small	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}+\frac{2}{3}V_0$
NNO	Small	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
NON	Small	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
ONN	Small	$-\frac{1}{3}V_{DC}$	$-\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
PPO	Small	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
POP	Small	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
OPP	Small	$\frac{1}{3}V_{DC}$	$\frac{1}{3}V_{DC}+\frac{1}{3}V_0$
PON	Medium	0	$\frac{1}{3}V_0$
OPN	Medium	0	$\frac{1}{3}V_0$
NPO	Medium	0	$\frac{1}{3}V_0$
NOP	Medium	0	$\frac{1}{3}V_0$
ONP	Medium	0	$\frac{1}{3}V_0$
PN0	Medium	0	$\frac{1}{3}V_0$
NNP	Large	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}$
NPN	Large	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}$
PNN	Large	$-\frac{1}{6}V_{DC}$	$-\frac{1}{6}V_{DC}$
PPN	Large	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$
PNP	Large	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$
NPP	Large	$\frac{1}{6}V_{DC}$	$\frac{1}{6}V_{DC}$

The 12 small vectors can be split in 6 sets of 2 vectors. The 6 sets have same direction and magnitude according to switching combination and will connect one or two output lines to the upper or lower capacitor. The vectors in each set draw currents opposite in direction from the capacitor bank. By correct selection of small vectors for the reference vector, the balance can be set.

The medium vectors have one vector per current direction. One of the three output lines is permanently connected to the

midpoint. When the reference vector is synthetized with the medium vector the line current flows through the midpoint. If the charge balance cannot be compensated with small vectors, the compensation is given to the next medium vector because it could have opposite current direction [9].

B. Nearest Three Vectors with Even Harmonic Elimination – NTV-EHE

The oldest topology of three level inverters was introduced by Nabae in 1981 [4]. The layout that he proposed is neutral point clamped topology. Compared with conventional voltage source inverters this topology has better spectral performance. The original topology with the neutral point clamped has been expanded to higher number of levels. Multilevel inverters reduce voltage stress on the devices. The required voltage blocking capability of the clamping diodes varies with the levels, thus multiple diodes at higher levels may be required [7].

NTV-EHE was introduced by D. W. Feng and B. Wu in 2004 [11] for compliance with harmonic standards, like IEEE 519-1992, when the converter is used in rectifier mode. The generation of these even order harmonics is due to fact that the waveform generated by SVM is not half – wave symmetrical [11]. In order to obtain half – wave symmetrical voltage at the output and to cancel the line-line even harmonics alternative switching sequences: one starting with N – type vector (A type) and the other with P – type vector (B type) need to be used. This can be seen in **Figure II-2**.

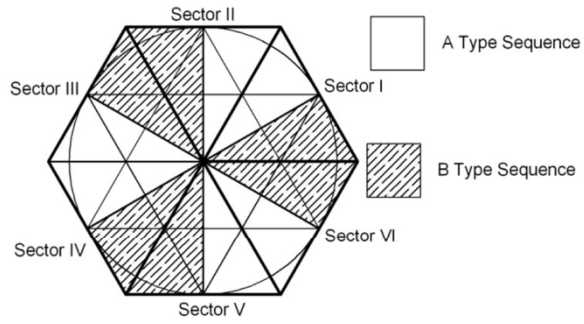


Figure II-2 Alternation of N and P type sequences in NTV

This method provides low harmonic distortion. The reference vector is synthetized by three stationary space vectors. The stationary vectors are chosen as the nearest three vectors from the region in which the reference vector is found.

C. ZeroCommon Mode - ZCM

The Zero Common Mode Method (ZCM) was first introduced by Haoran Zhang and Annette von Jouanne in 2000 [12]. This method uses the six active middle vectors and one zero vector due to their ability to create zero common mode voltage as long as the DC link is balanced. This can be seen in **Figure II-3**.

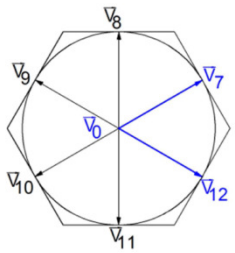


Figure II-3 Switching Vectors for ZCM

This method uses only medium vectors, thus the other type of vectors are going to be neglected. Taking this into account, it can be observed that the maximum vector that can be inscribed in the hexagon of space vectors is given by the medium vector, therefore the maximum utilization of the bus is 86.6% of the utilization the NTV-EHE modulation strategy [10]. Due to the fact that in this method there are no redundant states, the transition between two adjacent states involves two inverter legs that double the switching frequency and increase the harmonic content.

III. PROPOSED MODULATION STRATEGIES

The voltage deviation problem is inherent to all 3L-NPC converters [13]. Neutral point voltage deviation means that any current flowing through the neutral point of a three level inverter would cause the charging of one of the capacitors and the discharging of the other. The effect is that the output becomes asymmetric. The unbalance problem does not appear in two level inverters or in three level inverters with separate DC sources [14].

When applying PWM to a three phase inverter, a voltage between neutral point of the load and ground is generated. This voltage is known as common mode voltage and acts like a source for many unwanted problems in motor drives such as shaft voltage and bearing currents (due to parasitic capacitances that exists in the motor structure) [15].

Based on the influence of the space vectors described in **Table II-1** the improved modulation strategies have been developed.

A. One Large One Medium Vector - OLOM

For a proper utilisation of the bus bar, three vectors were chosen: one medium, one large and the zero vector. This method divides the space vector hexagon in 12 sectors with a displacement angle of 30°. Switching vectors for this method are presented in **Figure III-1**. As ZCM this method does not have the ability to balance the DC link voltage when a voltage drop occurs on one of the capacitors, but it has the ability of natural balancing.

As this method uses medium, large and the zero vectors the largest vector that can be inscribed in the space vector hexagon is the large vector, thus the modulation index is maximum as in NTV-EHE.

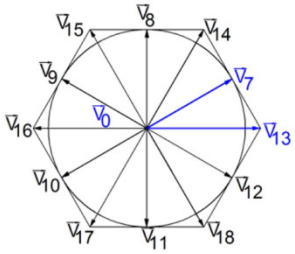


Figure III-1 Switching Vectors for OLOM Method in first sector

The reference vector for each sector is comprised by one large, one medium and the zero vector. Dwell times for each device are calculated using the volt-second principle together with the assumption that during switching time the reference voltage vector is constant.

Considering these space vectors and their influence, it can be stated that the influence of NP current is only given by medium vectors, as CMV is produced only by large vectors.

B. Zero Small Medium Large Vector - ZSML

The idea behind this method is to use all available levels of voltage in order to keep THD low while having the possibility to balance the DC link. In natural balancing mode the CMV levels are half of NTV-EHE. The switching vectors for first sector can be seen in **Figure IV-1**.

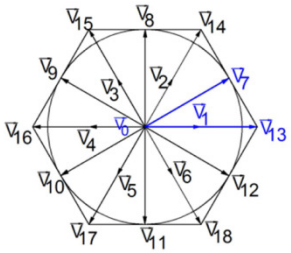


Figure III-2 Switching vectors for ZSML Method for first sector

The dwell times are calculated based on volt-second principle. Distinctive for this method is that the dwell time for zero vector is equal to $1 - \frac{V_{ref}}{V_{ref,max}}$.

In order to have natural balancing in odd sectors the N type small vector is used and P type small vector in even sectors.

IV. Proposed Modulation Strategies Validation through Simulation and Experimental Results

For a proper validation of the two proposed modulation strategies simulations and an experimental PCB were developed. The simulations were performed in Matlab/Simulik and Plecs.

The 3L-NPC inverter was modelled based on the simplified hardware schematic from **Figure IV-1**:

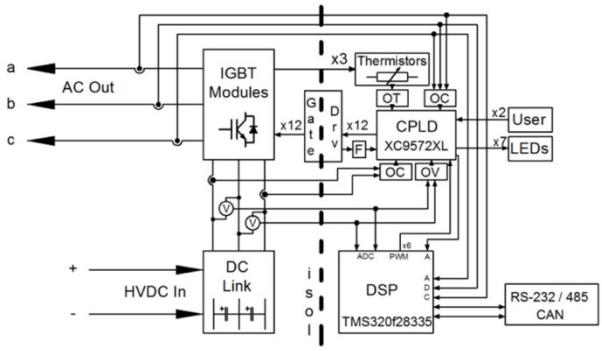


Figure IV-1 Simplified schematic of the designed NPC converter

This inverter has the following main features:

- Embedded TMS320F28335 DSP design.
- 4 layer PCB with stacked DC link layout, ground and power planes.
- Design based on NPC leg IGBT modules (Semikron SK50MLI065).
- Adjustable over temperature, overcurrent and overvoltage protection.
- Xilinx XC9572XL CPLD based dead time and protection management.
- Real time PWM signal analysis and protection.
- DC link up to 1kV.
- Shielded ADC and PWM signals.
- RS-232, RS-485 and CAN communication.
- Optocupler galvanic isolated gate driver with active Miller clamping.
- Desaturation detection.
- JTAG interface for DSP and CPLD.
- Hall effect current sensors.
- Mixed analogue and digital design.
- Reduced size.

This inverter can be seen in **Figure IV-2**.

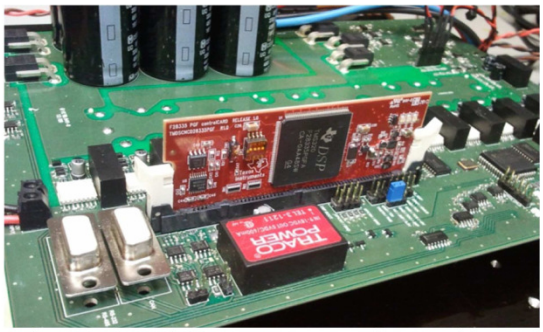


Figure IV-2 NPC Converter developed for experimental validation of proposed modulation strategies

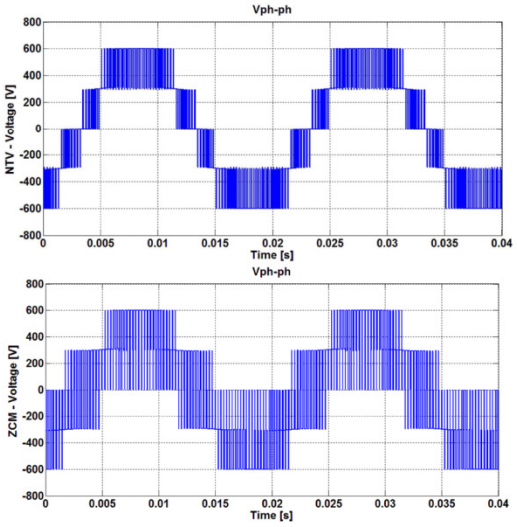
A. Validation through simulations

Extensive simulations have been developed in order to validate the proposed modulation strategies. **Figure IV-3** presents the simulation results regarding phase-to-phase voltage of the two classical methods and the two proposed methods.

The modulations were performed using the equivalent model of a 7.5 kW IM with star – neutral connection. The DC link is set at 600 V and equivalent capacitance of upper and lower capacitor is 0.99 µF. The waveforms are obtained when the motor reaches steady state. Switching frequency is set a 4 kHz with a 2µs deadtime.

Industry standard modulation strategy is NTV. A newer method, ZCM, benefits in a great reduction in the CMV with the disadvantage of THD increase. Using only the medium vectors, ZCM manages to keep the CMV very low in comparison with NTV while this benefits of lower THD due to use of 3 vector sizes. This is reflected in the number of voltage levels, which is 9 for NTV and 3 for ZCM. Also, the modulation index is lower for ZCM. The line voltages for NTV and ZCM are found in **Figure IV-3**.

The first proposed method, OLOM retains the maximum modulation of NTV while using only large, medium and zero vectors. The line voltage can be seen in **Figure IV-3**. The second proposed method, ZSML has the distinctive feature of using 4 vectors: zero, small, medium and large. The line voltage is comparable to the waveform for OLOM. Using 4 vectors sizes comes with a THD decrease of 1.38% over NTV and 24.96% lower than ZCM.



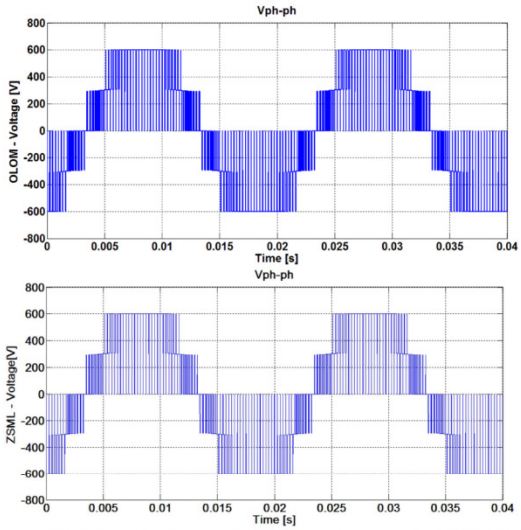
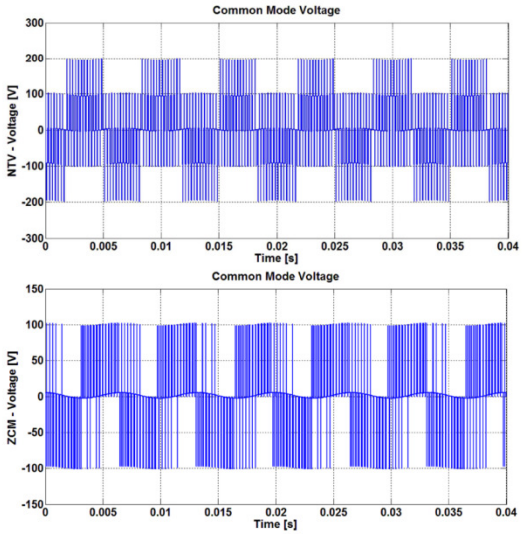


Figure IV-3 Simulation results in time domain for NTV-EHE, ZCM, OLOM and ZSML regarding phase to phase voltage

The CMV for NTV has a range of ±200 V. The ZCM has very low CMV, under 5V on all frequencies. The CMV present is due to the influence of dead time.

The CMV range for OLOM is little over half of NTV for a THD increase in the line voltage of 6.34% compared to NTV and 17.24% lower than ZCM. The increase is also for using 7 voltage levels compared with NTVs 9 levels. The CMV can be seen in **Figure IV-4**. As it can be seen in the FFT in **Figure IV-5**, OLOM has 60% lower amplitude at the switching frequency, compared to NTV. The CMV is lower on all frequency ranges.



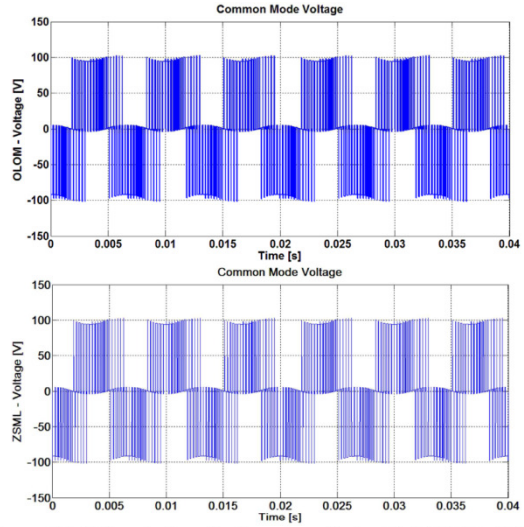
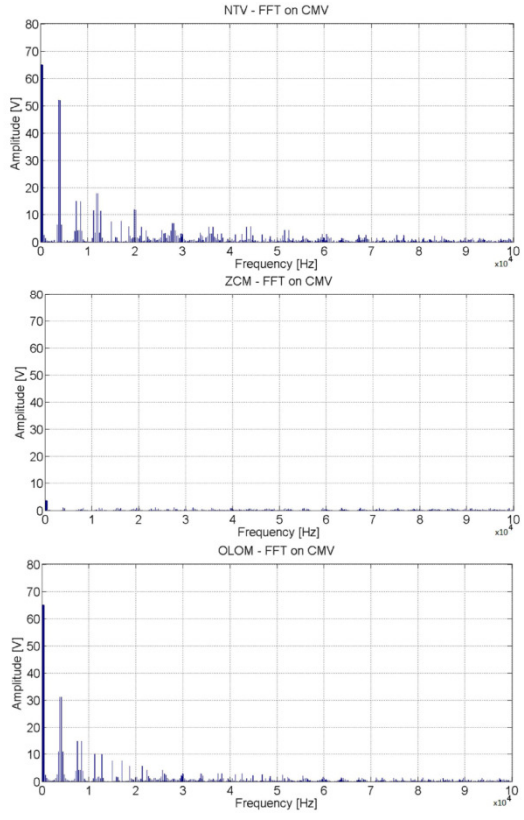


Figure IV-4 Simulations in time domain for NTV-EHE, ZCM, OLOM and ZSML regarding CMV

The CMV range for ZSML is also lower than half of the NTV as seen in **Figure IV-4**. The specific of this method is the extra ability to balance the DC link in the case of an external influence. The values shown are for steady state when in natural balancing mode.



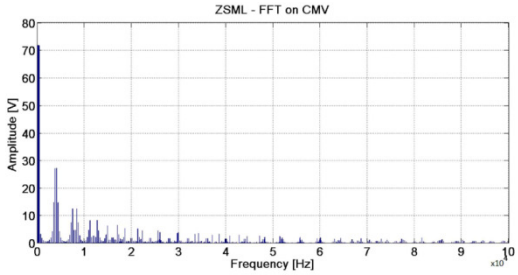


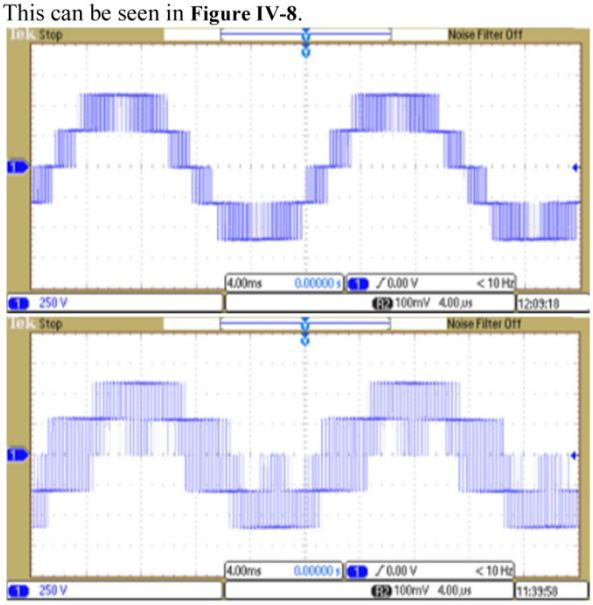
Figure IV-5 Simulations of frequency domain spectrum for NTV-EHE, ZCM, OLOM and ZSML regarding CMV

B. Validation through experimental work

The hardware presented at the beginning of this chapter was built in order to validate the proposed modulations strategies. As a load to this inverter a 1.5 kW IM has been used.

The experimental results of the phase-to-phase voltage in time domain regarding classical and proposed modulation strategies can be seen in **Figure IV-6**. It can be observed that the modulation strategies maintain the same characteristics as in simulations.

The CMV in time domain of these modulation strategies can be seen in **Figure IV-7**. Voltage levels discussed on simulation results are maintained, as well as spectral analysis. This can be seen in **Figure IV-8**.



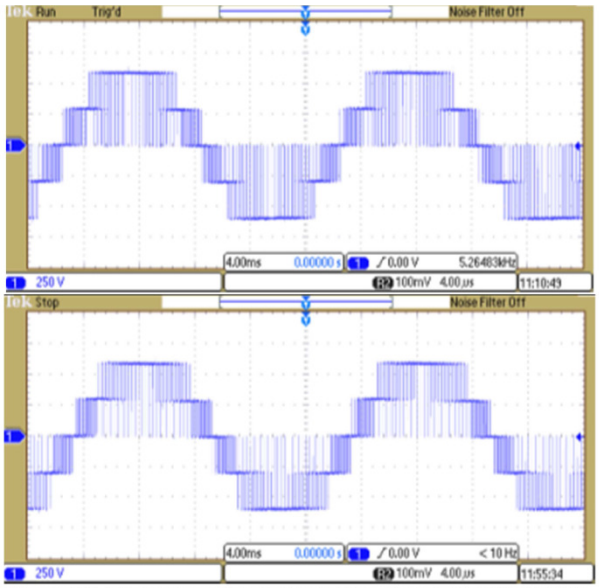
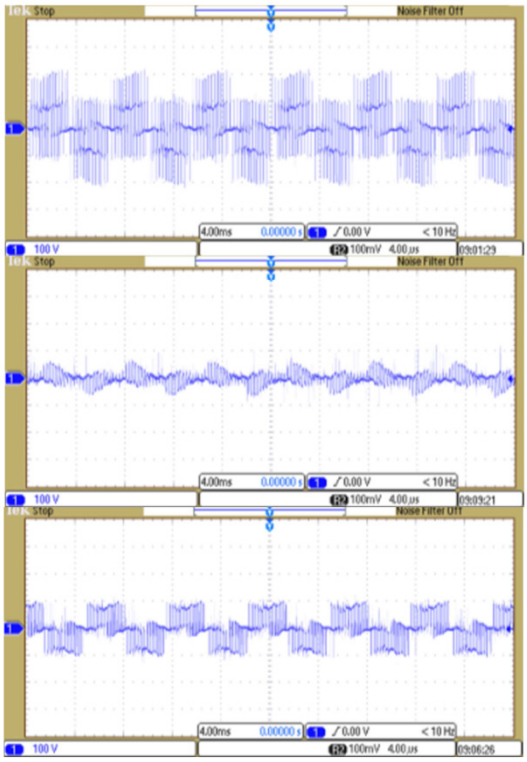


Figure IV-6 Experimental results in time domain for NTV-EHE, ZCM, OLOM and ZSML regarding phase to phase voltage



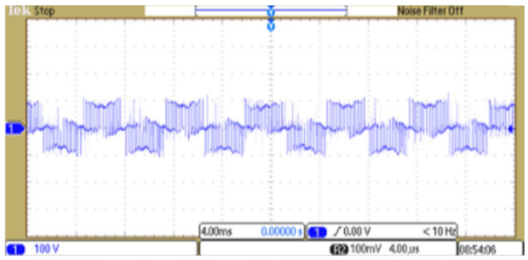
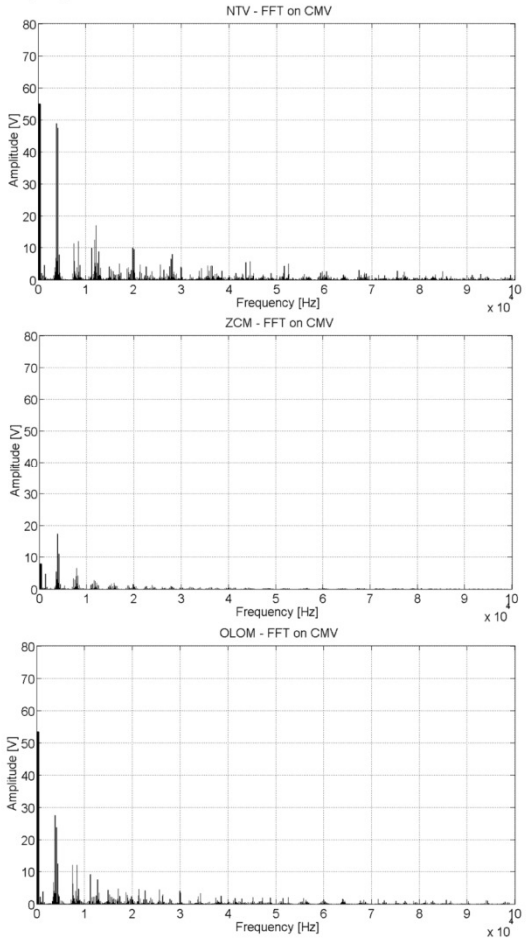


Figure IV-7 Experimental results in time domain for NTV-EHE, ZCM, OLOM and ZSML regarding CMV

THD in the line voltage for each method shows a good correspondence between simulation and experiments. In the experimental setup, the THD is higher with only 2-3%. The effect of this can be seen as a lower fundamental frequency in the CMV spectral analysis. The results confirm the feasibility of the proposed methods.



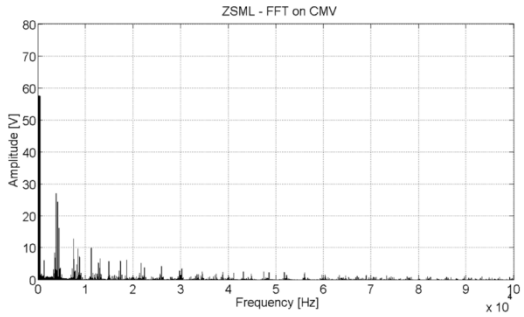


Figure IV-8 Experimental results of frequency domain spectrum for NTV-EHE, ZCM, OLOM and ZSML regarding CMV

V. ASSESMENT OF THE PROPOSED MODULATION STRATEGIES

For a better view on the proposed modulation strategies, a comparative analysis has been done. This can be seen in **Table V-1 – Comparative Analysis between Modulation StrategiesTable V-1**.

The two new proposed strategies seem prospective as they offer performance improvements. OLOM reduces the CMV on all frequencies while preserving modulation index compared to NTV. While having same amplitude of CMV at the low fundamental frequency of 150 hz, it has 40% lower amplitude at the switching frequency of 4 khz. It is also comparable with ZCM because it makes better use of the three level topology, preserving the maximum modulation index and lower THD.

Also, ZSML seems promising. The THD is lower than NTV and ZCM while the CMV distribution is more than half lower on all switching frequencies compared to NTV. While preserving the maximum modulation index, the method is able to balance the dc-link in the case of an external event, which is a great advantage. Both methods are comparable with ZCM in the high frequency range, where the effects of CMV are highest.

Table V-1 – Comparative Analysis between Modulation Strategies

	NTV	ZCM	OLOM	ZSML
Phase / Line Voltage Levels	9 / 5	3 / 5	7 / 5	9 / 5
Modulation Index	1	0.866	1	1
DC link balancing	Natural balancing	Natural balancing	Natural balancing	Natural balancing and balancing
CMV Levels [V]	$\pm 200, \pm 100$	$\pm 100, 0$	$\pm 100, 0$	±100,0
Simulation ph-ph THD_v	27.93%	51.51%	34.27%	26.55%
Experiment ph-ph THD_v	29.88%	55.03%	36.53%	28.45%

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Appendix 11: Contents of the CD

The CD will contain the following folders and documents:

- Report.
- CPLD Program ISE Design Suite: this folder contains the CPLD program that has integrated deadtime programming and protections.
- Developed Modulation Strategies – Matlab Simulation: this folder contains the simulations regarding classical and developed modulation strategies.
- Modulation Strategies – DSP Code Composer C++: this folder contains the C++ code implemented into DSP regarding the classical and developed modulation strategies,
- NPC Inverter Design – Altium: the PCB layout of the three level NPC converter designed in Altium.