AALBORG UNIVERSITY

MASTER THESIS PROJECT

Control of Multilevel HVDC based on Modular Multilevel Converter (MMC) during Faults

Department of Energy Technology

AALBORG UNIVERSITY
DENMARK

Author: Dimitrios Rizadis

Supervisors: Remus Teodorescu, Sanjay K. Chaudhary

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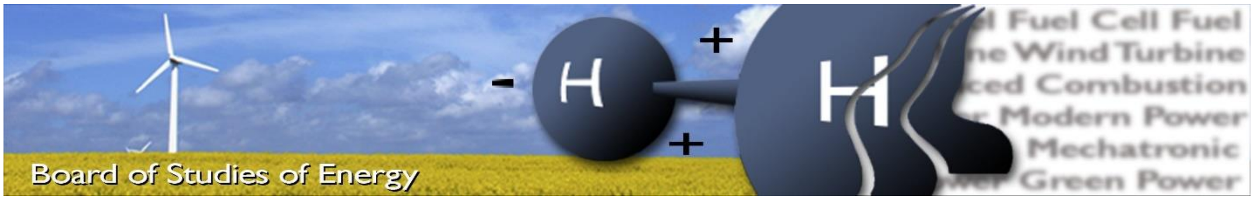

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SYNOPSIS:

MMC is a converter topology that acquires a significant and increasing role in a number of applications, such as HVDC. The current project thesis aims at enhancing the MMC Control for cases of AC Faults, with respect to the grid requirements for reactive current injection without violating the physical limitation of the converter. The following injection strategies are developed; Positive Sequence Injection, Mixed Sequence Injection with Balanced Power and Mixed Sequence Injection with Grid Compliance. The strategies show improvement in the support of the positive sequence voltage, decrease of the negative sequence and ripple minimization for active power. A current limitation method is furthermore developed, with priority to the reactive current injection for both positive and mixed sequence injection. These techniques are validated both in simulation and in experimental results, which are

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Preface

This report describes the work carried out for the long Master thesis project at the Department of Energy Technology, Aalborg University.

Aalborg, 6th October 2017

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Nomenclature and abbreviations

i_c	Circulating current
i_s	Output current
v_c	Voltage driving circulating current
v_s	Output Voltage
v_a	Grid Voltage
v_d	DC link voltage
R	Arm Resistance
L	Arm Inductance
C	Capacitance of one submodule
$v_{cu,l}^{\Sigma}$	Upper/Lower arm sum capacitor voltage
$i_{u,l}$	Upper/Lower arm current
i_d	DC Current
N	Number of arm submodules
W_{Σ}	Sum of arm energy
W_{Δ}	Difference between upper and lower arm energy
$W_{u,l}$	Upper/Lower arm energy
P_{Σ}	Sum of arm power
P_{Δ}	Difference between upper and lower arm power
$P_{u,l}$	Upper/Lower arm energy
Z_L	Load Impedance
$v_{du,l}$	Upper/Lower DC half voltage
$i_{u,l}^{k}$	k submodule current
$\overline{i_x}$	Mean value of X current
$\overline{v_x}$	Mean value of X voltage
M	Number of phases
$v_{u,l}$	Upper/Lower arm voltage
$v_s^{max,min}$	Maximum output voltage
$v_{cu,l}^{i}$	i submodule voltage
$n_{u,l}^{i}$	Number that indicates if submodule is inserted (1) or bypassed (0)
$n_{u,l}$	Upper/Lower arm insertion indice for the averaged model
v_x^*	Reference for X voltage
i_x^*	Reference for X current
$i_{(d,q)^{(+,-)}}$	Positive/Negative Sequence Active/Reactive Current
$\widehat{V}_s$	Sinusoidal Output Voltage Amplitude
ω_1	Fundamental Frequency
h	Harmonic Order
φ	Power angle
T_s	Sampling Period
T_c	Switching Delay
T_d	Total Delay
ω_s	Switching Frequency
φ_m	Phase Margin

LPF	Low Pass Filter
k_+	Droop Factor for grid requirements for positive sequence reactive power
k_-	Droop Factor for grid requirements for negative sequence reactive power
V_+	Positive Sequence Voltage component
V_-	Negative Sequence Voltage component
P	Active Power
$\tilde{p}$	Oscillating Power
p	Instantaneous Power
Q	Reactive Power
q	90 degrees lagging phase-shifting operator
$\mathbf{v}_{\perp}$	Orthogonal version of the grid voltage

1 Introduction

1.1 HVDC over AC transmission

During the last years, the well-established dominance of the AC transmission over DC is in question. Although the generated and delivered power is AC, the high voltage direct current (HVDC) transmission is receiving more attention. [1][2]

The AC transmission has been generally preferred for many years in the past, because of some benefits that it presents. However, some difficulties arise with the use of AC transmission, such as the inability of connecting together asynchronous systems, distance limitations and transmission capacity.

For these reasons, the HVDC is thought to be the emerging area of interest for the implementation of the transition towards a smart grid. This technology is used for subsea connection, connection of systems with different frequencies, long distance connections due to the fact that it presents lower losses than the AC transmission. The reason is that the losses in a transmission line are highly dependent on the frequency. That characteristic is also a reason for HVDC to be chosen for renewable energy sources power transmission, as long as the latter can be placed away from the point where the power is consumed (i.e. industrial and urban consumers). It is also deduced that the lower losses mean lower cost for a HVDC system, as long as a more environmentally friendly nature. The controllability of a HVDC system is also an advantage.

The HVDC system consists of the supply side, in which the power is converted from AC to DC in order to be transmitted, and the conversion again in AC at the point of delivery. Since around 2000, the converters used for these purposes are voltage source converters (VSC).

1.2 MMC-HVDC State of the Art

The Modular Multilevel Converter (MMC) is a configuration that has emerged the last years and has been seen as a topic of rising attention for a number of advantages in comparison with the conventional 2 level VSC:

- High efficiency
- Modular Design
- Scalability
- Low harmonic distortion

The MMC is considered to be a promising technology for many applications, including HVDC (MMC-HVDC). As a VSC application, it offers the ability of accurate active power control, with independent reactive power control.

An example of different uses of a HVDC system is depicted in Fig. 1, and the scheme of the internal structure of a HVDC system in Fig. 2.

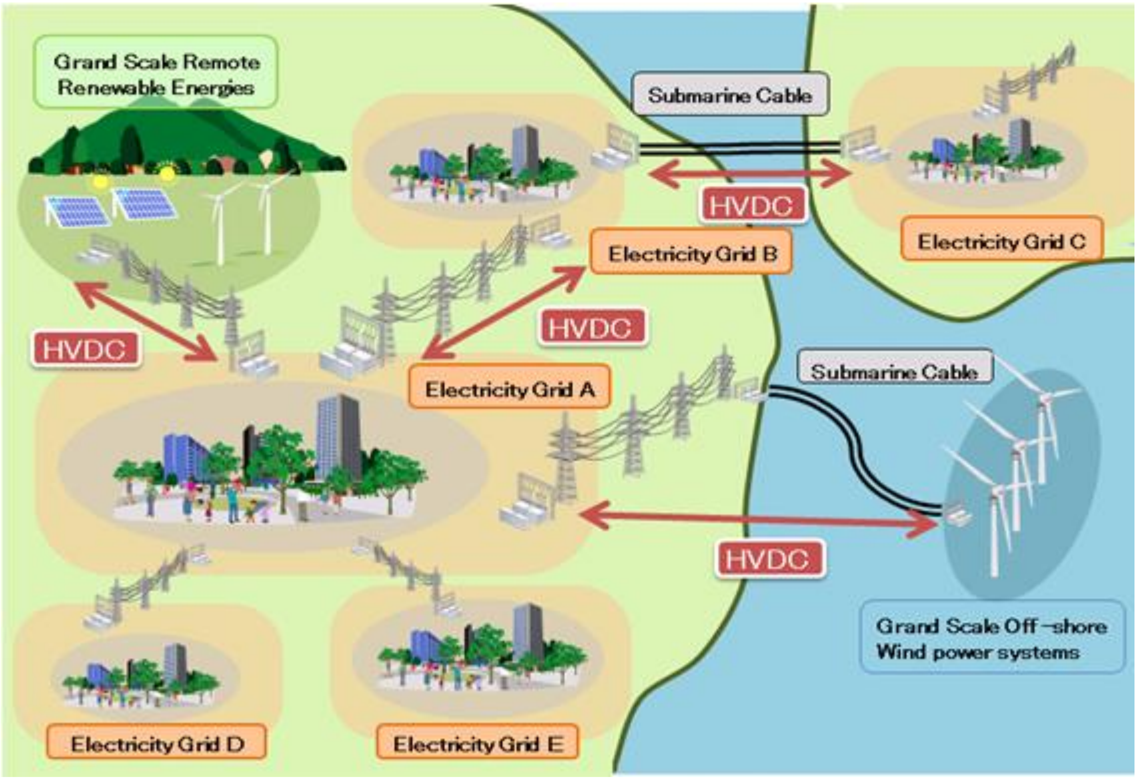


Fig. 1: HVDC application in transmission systems.[2]

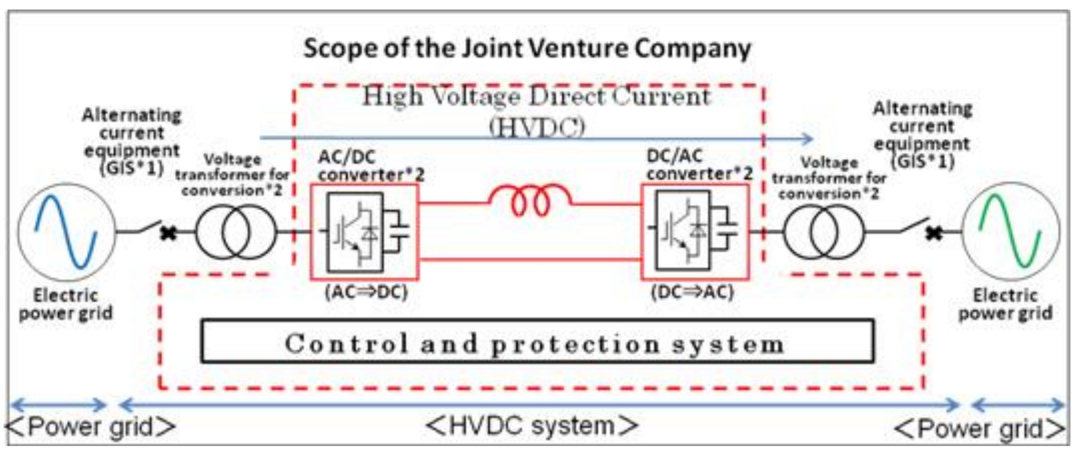


Fig. 2: Scheme of a HVDC connection.[2]

The MMC was first introduced in [3] by Marquardt and Lesnicar, and since have been used by the major HVDC manufacturers: Siemens, ABB, GE-Alstom. The following table shows the realized and planned HVDC plants based on MMC worldwide.

Project	Year	Power (MW)	AC (kV)	DC (kV)	Main reason for choosing HVDC	Application
East West Interconnector	2013	500	400	± 200	Length of sea and land cables, controllability, black start and P-Q support	Interconnecting grids
Skagerrak Pole 4	2014	700	400	± 500 (HVDC Light)	Length of sea crossing, asynchronous link. For pole 4, HVDC Light was chosen for its premier power quality features.	Interconnecting grids
Kraftnät Åland AB	2015	100	110	± 80	Length of sea crossing, Asynchronous networks, reliable backup power	Interconnecting grids
DolWin1	2015	800	380(Dörpen/West) 155 (Platform DolWin Alpha)	± 320	Length of land and sea cables	Offshore wind connections
Valhall	2011	78	300 (Lista), 11 (Valhall)	150	Reduce costs and improve efficiency. Minimize emissions.	Power from shore
NordLink	2020	1400	400 (Tonstad, Norway 380 (Wilster, Germany)	± 525	Long submarine cable distance, stabilizing features	Interconnecting grids
Kriegers Flak Combined Grid Solutions	2019	410	Germany side:400 Offshore side:150	± 140	Interconnecting asynchronous grids	Interconnecting grids
North Sea Link	2021	1400	420 (Kvilldal, Norway) 400 (Blyth, UK)	± 525	Long submarine cable distance, stabilizing features.	Interconnecting grids
Caithness Moray HVDC Link	2018	1200	Spittal side:275 Blackhillock side: 400	±320	Length of subsea cable, reinforcing AC network, connecting renewables	Interconnecting grids
Maritime Link	2017	500	Newfoundland side:230 kV Nova Scotia side:345 kV	±200	Long distance, stabilizing features	Connecting remote generation and interconnecting grids
Mackinac	2014	200	Both sides: 138 kV	±71	islanded operation, under certain operating conditions, voltage stability and power flow control	DC links in AC grids
NordBalt	2015	700	Swedish side:400 Lithuanian side:330	±300	Length of sea crossing Asynchronous networks	Interconnecting grids
BorWin2	2015	800	380 (onshore side); 155 (offshore side)	± 300 (HVDCPLUS)	Length of land and sea cables	Offshore wind connections
HelWin1	2015	576	380 (onshore side); 155 (offshore side)	±250 (HVDCPLUS)	Length of land and sea cables	Offshore wind connections
SylWin1	2015	864	380 (onshore side); 155 (offshore side)	±320 (HVDCPLUS)	Length of land and sea cables	Offshore wind connections
South West Link	2014	1440	300 between two sites	±300	Black start, Reduce costs and improve efficiency	Balancing the power supply between central and southern Sweden.
ULTRANET	2019	2000	400	±380 (HVDCPLUS)	Black start, integrated DC lines at exisiting pylons, stabilizing functions.	Interconnecting grids
INELFE	2015	2000	400	±320 (HVDCPLUS)	Black start	Interconnecting grids
COBRAcable	2019	700	400	±320	improve cohesion in the European transmission grid by increasing the exchange of surplus wind power with neighbouring countries and strengthen the infrastructure, security of supply and the market.	Interconnecting grids
DolWin 2	2016	916	155 (Platform DolWin beta),380 (Dörpen West)	*pm*320	Length of land and sea cables	Offshore wind connections

Table 1: List of MMC in HVDC plants [5]

1.3 Project Objectives

The control of the MMC in steady state operation is a deeply searched and developed field. However, in cases of AC faults, special strategies have to be followed, that can ensure the Low Voltage Ride Through (LVRT) of the converter, as long as the fulfilment of special grid requirements and stable operation.

This project aims at:

- Development of strategies of current injection suitable for the case of fault
- Current Limitation in case that the control produces reference over the rated value
- Simulation and laboratory implementation on a MMC prototype to verify and compare the control strategies.

1.4 Project Limitations

- Only the arm-level averaged model was considered in simulation.
- Only AC Faults were considered.
- No special strategy for Capacitor Voltage reduction was designed.
- Different modulation techniques were not investigated. Only NLC was used.
- The lab setup was tested below its rated values for reasons related to EMI.

1.5 Thesis Outline

In chapter 2, the MMC is described and its internal dynamics are analyzed. The controllers used in the steady state operation are also described, and the principles that they should follow are investigated. The arm balancing control is also analyzed.

In chapter 3, the need for expansion of the conventional control for the case of a Fault is analyzed. The grid requirements for special injection according to the fault characteristics are depicted, and different injection strategies in case of AC faults are introduced. A current limitation technique with priority to the reactive injected components is also developed. Simulation results for all injection strategies and the current limitation method are validating the proposed technique.

In chapter 4, the experimental part is shown. Description of the setup used, and experimental results for the arm balancing control and injection strategies with the current limitation are taken under AC fault condition.

Finally, in chapter 5 conclusions are stated and possible future work is proposed.

2 Description of MMC and control under steady state operation

2.1 Description of a MMC

The per-phase configuration of a MMC is depicted in Fig. 3. The MMC consists of M legs, as the amount of phases. Each leg consists of various series connected basic units, which are called submodules (SM). A SM has two different possible configurations, half bridge and full bridge. In this project, half bridge SM was considered, which has the inner structure of a capacitor and two IGBTs with antiparallel diodes, as depicted in Fig. 3. Each leg contains two arms, an upper and a lower. The upper arm is connected to the positive pole of the DC link, whereas the lower to the negative. The arms are connected to the AC side through a transformer, used to adjust the voltage to the rated values of the converter and to cancel the zero sequence of the components of the current. An inductance is used on every arm to filter the output current, cut off the high order harmonic components and limit the current change in case of a fault. Furthermore, for the protection of the converter from overvoltage, a parallel connection of a resistance and an AC breaker is implemented.[4][5]

The SM, as depicted in Fig. 3, acts in the following way. During normal operation, the capacitor is charged with its nominal value, with a small ripple component. The control of the SM, which is achieved through controlling the signals in the gates of the IGBTs, leads to three different states of function:

- Inserted: The IGBT of the branch with the capacitor is turned on, and the capacitor voltage is summed to the arm voltage.
- Bypassed: The IGBT in parallel to the capacitor is turned on, and so the capacitor is not summed to the arm voltage.
- Blocked: Both IGBTs are turned off.

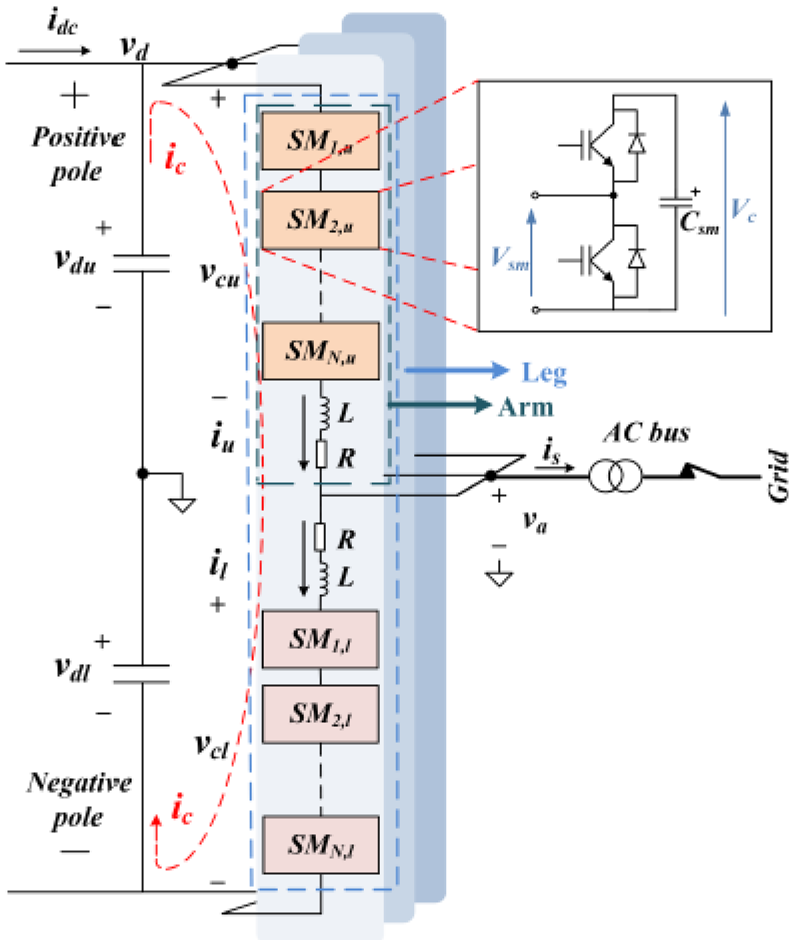


Fig. 3: Scheme of a MMC. The inner structure of a SM can also be seen. [5]

2.1.1 Analysis of the basic principles

A basic part of the analysis for the MMC is the definition of two different components for the current of each leg, as it can be seen in Fig. 4. The first component is the output current, that is provided to the grid, and the second is the circulating current which runs through the arms and the DC link. These two components are defined as:

$$i_s = i_u - i_l \tag{2.1}$$

and

$$i_c = \frac{i_u + i_l}{2} \tag{2.2}$$

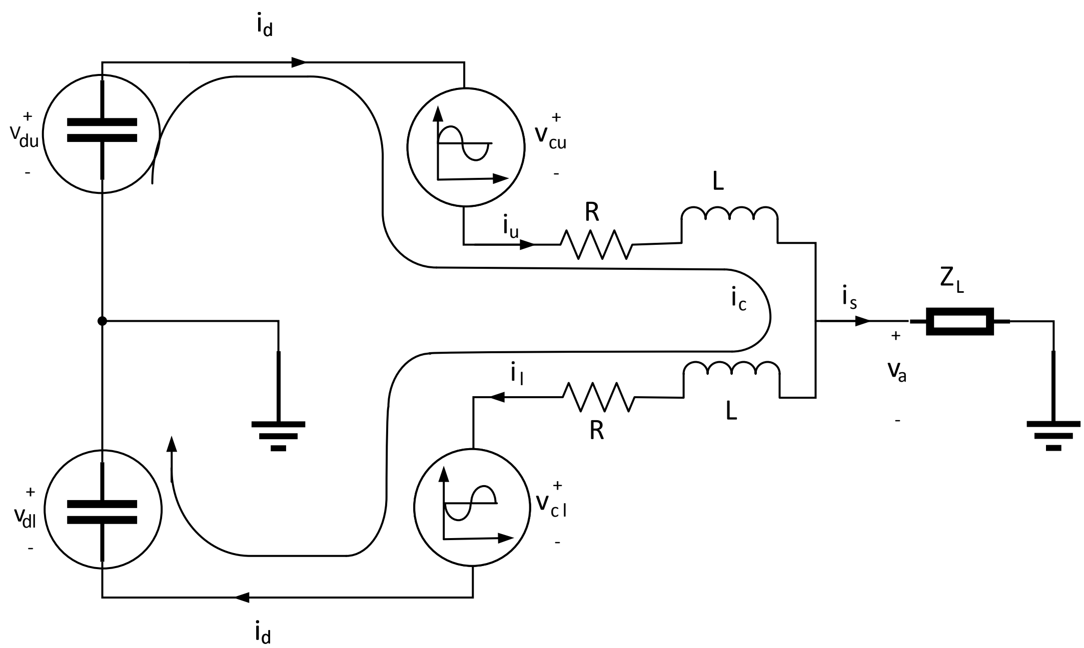


Fig. 4: Equivalent circuit of one phase of the MMC.[5]

In the above equations, i_u is the current flowing through the upper arm, whereas i_l is the current of the lower arm.

From the aforementioned equations, an expression can be derived for i_u and i_l in relation with i_s and i_c:

$$i_u = \frac{i_s}{2} + i_c \tag{2.3}$$

and

$$i_l = -\frac{i_s}{2} + i_c \tag{2.4}$$

To achieve a constant DC voltage, the sum of the mean values of currents of both upper and lower arm must produce a dc current:

$$\sum_{k=1}^{M} \overline{i_{u,l}^{k}} = i_d \tag{2.5}$$

For a balanced system, the equation implies that:

$$\overline{i_u} = \overline{i_l} = \overline{i_c} = \frac{i_d}{M} \tag{2.6}$$

2.1.2 Dynamics of the MMC

In order to describe the MMC dynamics, an analysis must be performed according to the Kirchhoff Voltage Law for one phase.

Assuming a balanced system, the pole to pole DC link voltage can be divided equally between two pole to ground voltages, as:

$$v_{du} = v_{dl} = \frac{v_d}{2} \tag{2.7}$$

Then, from Fig. 4, it can be deduced that, for the upper arm:

$$\frac{v_d}{2} - v_u - Ri_u - L\frac{di_u}{dt} = v_a \tag{2.8}$$

And for the lower arm:

$$-\frac{v_d}{2} + v_l + Ri_l + L\frac{di_l}{dt} = v_a \tag{2.9}$$

By addition and subtraction of the previous equations, the following is obtained:

$$\frac{L}{2}\frac{di_s}{dt} = \underbrace{\frac{-v_u + v_l}{2}}_{v_s} - v_a - \frac{R}{2}i_s \tag{2.10}$$

And

$$L\frac{di_c}{dt} = \frac{v_d}{2} - \underbrace{\frac{v_u + v_l}{2}}_{v_c} - Ri_c \tag{2.11}$$

It is obvious that the first equation regards the dynamics governing the output current i_s and its driving voltage, whereas the second those of circulating current i_c. In order to receive the desired DC circulating current, the differential component is substituted by 0 and the driving voltage becomes:

$$v_c = \frac{v_d}{2} - Ri_c \approx \frac{v_d}{2} \tag{2.12}$$

It is obvious that the maximum output voltage occurs when all SMs of the upper arm are bypassed, whereas all those of the lower arm are inserted. In this case:

$$v_u = 0, \qquad v_l = v_{cl}^{\Sigma} \tag{2.13}$$

And the minimum in the opposite case:

$$v_u = v_{cu}^{\Sigma}, \qquad v_l = 0 \tag{2.14}$$

Then, the output voltage for each case becomes:

$$v_s^{max} = \frac{v_{cl}^{\Sigma}}{2}, \qquad v_s^{min} = -\frac{v_{cu}^{\Sigma}}{2} \tag{2.15}$$

The condition for the circulating current to be kept DC, is given by Eq. (2.12). From Eq. (2.13) and Eq. (2.14), it is seen that to achieve the condition in the case of the maximum output voltage, it must be $v_{cl}^{\Sigma} = v_d$. Equally, for the case of minimum output voltage, $v_{cu}^{\Sigma} = v_d$. So, ideally the sum capacitor voltage for both arms should fulfill Eq. (2.16):

$$\overline{v_{cu,l}^{\Sigma}} = v_d \tag{2.16}$$

The mean value in the equation, is used because the total voltage of the capacitor of one SM consists of this mean value and a ripple component, defined by the charging or discharging current through the SM. The ripple from all the capacitors produce a sum capacitor voltage ripple.

Assuming now similar contribution from each capacitor to the total voltage,

$$\overline{v_{cu,l}^{i}} = \frac{\overline{v_{cu,l}^{\Sigma}}}{N} = \frac{v_d}{N} \tag{2.17}$$

2.1.3 Average model of a MMC

In order to proceed with the dynamic analysis of the MMC, it is important to introduce the averaging principle. According to this:

- All capacitors in the SMs are considered to be identical, as also their capacitance and voltage.
- The SMs of each arm are substituted by an ideal voltage source equal to the sum capacitor voltage and an equivalent capacitance (Arm-Level Averaged (ALA) model).
- The ALA model is useful for analysis of the dynamics and of the sum capacitor voltage with its ripple components, however it ignores some features such as the PWM dynamics, the discrete values that the insertion indices receive normally (as it will be analyzed in this subchapter) and the same arm's unbalanced SMs. The introduction of the average model is made in order to

simplify the analysis of the MMC, and to reduce the complexity of the control and the computational time.[4][5]

The state of a SM, inserted or bypassed, can be indicated by a number ($n_{u,l}^{i}$) that can take only two values: 0 if the respective SM is bypassed, or 1 if the SM is inserted.

Then the voltage equation for each arm is the sum of the voltages of the inserted capacitors:

$$v_{u,l} = \sum_{i=1}^{N} n_{u,l}^{i} v_{cu,l}^{i} \tag{2.18}$$

By considering the differences of the capacitor voltages to be kept relatively low, the previous can be rewritten as:

$$v_{u,l} \approx \sum_{i=1}^{N} n_{u,l}^{i} \frac{v_{cu,l}^{\Sigma}}{N} = \frac{v_{cu,l}^{\Sigma}}{N} \sum_{\imath=1}^{N} n_{u,l}^{i} \tag{2.19}$$

Finally, the resulting sum can be substituted by a term that is defined as insertion indices, and it is given as:

$$n_{u,l} = \frac{1}{N} \sum_{i=1}^{N} n_{u,l}^{i} \tag{2.20}$$

It is obvious that the insertion indices receive discretized values between 0 and 1, and differing by steps of 1/N.

The Eq. (2.9) and Eq.(2.10) now become:

$$\frac{L}{2}\frac{di_s}{dt} = \underbrace{\frac{-n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2}}_{v_s} - v_a - \frac{R}{2} i_s \tag{2.21}$$

and

$$L\frac{di_c}{dt} = \frac{v_d}{2} - \underbrace{\frac{n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2}}_{v_c} - Ri_c \tag{2.22}$$

A system like the MMC described includes a large number of state variables. These are the 2N capacitor voltages, along with the i_s and i_c. That implies a very high complexity and computational difficulty. A way to minimize this inconvenience, is to apply the averaging principle to the capacitor voltages. With the use of the insertion indices as continuous, the equation describing the dynamics of each capacitor voltage becomes:

$$C\frac{dv_{cu,l}^{i}}{dt} = n_{u,l}^{i} i_{u,l}, \qquad \text{i=1,2,…,N.} \tag{2.23}$$

For all N capacitors, the equation becomes:

$$\underbrace{C\sum_{i=1}^{N}\frac{dv_{cu,l}^{i}}{dt}}_{dv_{cu,l}^{\Sigma}/dt} = \sum_{i=1}^{N} n_{u,l}^{i}\, i_{u,l} = i_{u,l}\underbrace{\sum_{i=1}^{N} n_{u,l}^{i}}_{Nn_{u,l}} \tag{2.24}$$

Reduced to:

$$\frac{C}{N}\frac{dv_{cu,l}^{\Sigma}}{dt} = n_{u,l} i_{u,l} \tag{2.25}$$

And by substituting the arm currents with the output and circulating current:

$$\frac{C}{N}\frac{dv_{cu}^{\Sigma}}{dt} = n_u\left(\frac{i_s}{2} + i_c\right) \qquad \frac{C}{N}\frac{dv_{cl}^{\Sigma}}{dt} = n_l\left(-\frac{i_s}{2} + i_c\right) \tag{2.26}$$

It is indicated that for the average model consideration, the effective arm capacitance is equal to C/N.

So, with the average model, the state variables of the system are v_{cu}^{Σ}, v_{cl}^{Σ}, i_s, i_c, and unrelated to the number of SM.

2.1.4 Arm Energy Analysis

Solving the expressions derived from Eq. (2.10) and (2.11) for v_s and v_c for v_l, v_u, the following is derived:

$$v_u = v_c - v_s \tag{2.27}$$

$$v_l = v_c + v_s \tag{2.28}$$

So, the power in upper and lower arm respectively is given by:

$$p_u = v_u \cdot i_u = (v_c - v_s)\left(\frac{i_s}{2} + i_c\right) = \frac{v_c i_s}{2} - \frac{v_s i_s}{2} + v_c i_c - v_s i_c \tag{2.29}$$

$$p_l = v_l \cdot i_l = (v_c + v_s)\left(-\frac{i_s}{2} + i_c\right) = -\frac{v_c i_s}{2} - \frac{v_s i_s}{2} + v_c i_c + v_s i_c \tag{2.30}$$

Analyzing the above, as already mentioned v_c can be considered equal to $\frac{v_d}{2}$. Considering sinusoidal signals for

$$v_s^* = \widehat{V_s} cos(\omega_1 t) \qquad\qquad i_s = \widehat{I_s}\cos(\omega_1 t - \varphi) \tag{2.31}$$

, DC value for i_c and because of power being the derivative of energy, for the upper leg it is derived that:

$$\begin{aligned}\frac{dW_u}{dt} &= \frac{v_d}{4} I_s \cos(\omega_1 t - \varphi) - V_s \cos(\omega_1 t) I_s \cos(\omega t - \varphi) + \frac{v_d}{2} i_c - V_s i_c cos(\omega t) \\ &= \frac{v_d}{4} I_s \cos(\omega_1 t - \varphi) - \frac{V_s I_s \cos(2\omega_1 t - \varphi)}{2} - \frac{V_s I_s cos\varphi}{2} + \frac{v_d}{2} i_c - V_s i_c cos\omega_1 t\end{aligned} \tag{2.32}$$

In this expression, it can be seen that $\frac{V_s I_s cos\varphi}{2}$ is the AC side power for one phase $\left(\frac{P}{M}\right)$ and $v_d i_c$ is the DC side power. For a stable operation, those two are equal, and the result is:

$$i_c = \frac{P}{M v_d} \tag{2.33}$$

So, with the two terms cancelling each other, it is derived that:

$$\frac{dW_u}{dt} = \frac{v_d}{4} I_s \cos(\omega_1 t - \varphi) - \frac{V_s I_s \cos(2\omega_1 t - \varphi)}{2} - V_s i_c cos\omega_1 t \tag{2.34}$$

Same for the lower leg,

$$\frac{dW_l}{dt} = -\frac{v_d}{4} I_s \cos(\omega_1 t - \varphi) - \frac{V_s I_s \cos(2\omega_1 t - \varphi)}{2} + V_s i_c cos\omega_1 t \tag{2.35}$$

Integration of the above equations gives the energy stored in the upper and lower arm of one leg ($W_u$and W_l respectively).

$$W_u = W_{u0} + \frac{v_d}{4\omega_1} I_s \sin(\omega_1 t - \varphi) - \frac{V_s i_c}{\omega_1} sin\omega_1 t - \frac{V_s I_s}{4\omega_1} sin(2\omega_1 t - \varphi) \tag{2.36}$$

$$W_l = W_{l0} - \frac{v_d}{4\omega_1} I_s \sin(\omega_1 t - \varphi) + \frac{V_s i_c}{\omega_1} sin\omega_1 t - \frac{V_s I_s}{4\omega_1} sin(2\omega_1 t - \varphi) \tag{2.37}$$

From the above analysis it can be seen that the energy of each leg contains two ripple terms with the fundamental frequency, and one term with second harmonic ripple.[6]

2.1.5 Ideal Selection of Insertion Indices

The analysis made for the average model is used for further investigation of the control of the MMC. With given reference values for v_c^* and v_s^*, the insertion indices n_l and n_u can be calculated. From Eq. (2.21) and Eq. (2.22), it was defined that

$$v_s = \frac{-n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2} \tag{2.38}$$

$$v_c = \frac{n_u v_{cu}^{\Sigma} + n_l v_{cl}^{\Sigma}}{2} \tag{2.39}$$

By manipulating the above equations, it is given that:

$$n_u = \frac{v_c - v_s}{v_{cu}^{\Sigma}} \tag{2.40}$$

$$n_l = \frac{v_c + v_s}{v_{cl}^{\Sigma}} \tag{2.41}$$

And by inserting the reference values,

$$n_u = \frac{v_c^* - v_s^*}{v_{cu}^{\Sigma}} \tag{2.42}$$

$$n_l = \frac{v_c^* + v_s^*}{v_{cl}^{\Sigma}} \tag{2.43}$$

Further investigation on the dynamic response of the sum capacitor voltage as given previously, is made by analyzing its ripple. By substituting the expression for the insertion indices in Eq. (2.26), the result is:

$$\frac{C}{N}\frac{dv_{cu}^{\Sigma}}{dt} = \frac{v_c^* - v_s^*}{v_{cu}^{\Sigma}}\left(\frac{i_s}{2} + i_c\right) \qquad \frac{C}{N}\frac{dv_{cl}^{\Sigma}}{dt} = \frac{v_c^* + v_s^*}{v_{cl}^{\Sigma}}\left(-\frac{i_s}{2} + i_c\right) \tag{2.44}$$

Given the equation regarding the energy of a capacitor, by multiplying with v_{cu}^{Σ} and v_{cl}^{Σ} and with derivative properties, the equations transform into:

$$\underbrace{\frac{C}{2N}\frac{d(v_{cu}^{\Sigma})^2}{dt}}_{dW_u/dt} = (v_c^* - v_s^*)\left(\frac{i_s}{2} + i_c\right) \qquad \underbrace{\frac{C}{2N}\frac{d(v_{cl}^{\Sigma})^2}{dt}}_{dW_l/dt} = (v_c^* + v_s^*)\left(-\frac{i_s}{2} + i_c\right) \tag{2.45}$$

As it was mentioned in the arm energy analysis, the quantities $W_{u,l}$ describe the upper and lower arm energies. The expression for the upper and lower arm energy can be rewritten in a way that describes it as a total energy for the leg and a difference between the arms energy:

$$W_{\Sigma} = W_u + W_l \qquad W_{\Delta} = W_u - W_l \tag{2.46}$$

Then, by substituting in the Eq. (2.45) and after proper manipulation, the expression derived is:

$$\frac{dW_{\Sigma}}{dt} = 2v_c^* i_c - v_s^* i_s \qquad \frac{dW_{\Delta}}{dt} = v_c^* i_s - 2v_s^* i_c \tag{2.47}$$

With the same considerations as in the arm energy analysis,

$$\frac{dW_{\Sigma}}{dt} = v_d i_c - \frac{\widehat{V}_s \widehat{I}_s}{2} cos\varphi - \frac{\widehat{V}_s \widehat{I}_s}{2}\cos(2\omega_1 t - \varphi) \tag{2.48}$$

$$\frac{dW_{\Delta}}{dt} = \frac{v_d \widehat{I}_s}{2} cos(\omega_1 t - \varphi) - 2\widehat{V}_s i_c \cos(\omega_1 t) \tag{2.49}$$

By integrating Eq. (2.48) and Eq. (2.49), the following is derived:

$$W_{\Sigma} = W_{\Sigma 0} - \underbrace{\frac{\widehat{V}_s \widehat{I}_s}{4\omega_1}\sin(2\omega_1 t - \varphi)}_{\Delta W_{\Sigma}} \tag{2.50}$$

$$W_{\Delta} = W_{\Delta 0} + \underbrace{\frac{v_d \widehat{I}_s}{2\omega_1}\sin(\omega_1 t - \varphi) - \frac{2\widehat{V}_s i_c}{\omega_1} sin(\omega_1 t)}_{\Delta W_{\Delta}} \tag{2.51}$$

The above expressions consist of the mean values ($W_{\Sigma 0}$, $W_{\Delta 0}$) and the ripple. The ripple for the total energy is shows a second harmonic frequency, while that of the unbalanced energy has two first harmonic components. Because of typically $\overline{v_{u,l}} = v_d$, and considering the equivalent arm capacitance C/N for the averaged model, the energy stored in each arm is $Cv_d^2/2N$. As the total energy is the sum of upper and lower arm, and the arms are considered to have balanced energy, the mean values become:

$$W_{\Sigma 0} = \frac{Cv_d^2}{N} \qquad\qquad W_{\Delta 0} = 0 \tag{2.52}$$

By considering the arm energy equations, and given that $W_\Sigma = W_u + W_l$ and $W_\Delta = W_u - W_l$, proper manipulation and appropriate approximations with use of limit properties (due to the small relative values of the ripples) result in:

$$v_{cu}^{\Sigma} = \sqrt{\frac{2N}{C}W_u} = \sqrt{\frac{N}{C}(W_{\Sigma 0} + \Delta W_\Sigma + \Delta W_\Delta)} = \sqrt{v_d^2 + \frac{N}{C}(\Delta W_\Sigma + \Delta W_\Delta)} \approx v_d + \underbrace{\frac{N}{2Cv_d}(\Delta W_\Sigma + \Delta W_\Delta)}_{\Delta u_{cu}^{\Sigma}} \tag{2.53}$$

$$v_{cl}^{\Sigma} = \sqrt{\frac{2N}{C}W_l} = \sqrt{\frac{N}{C}(W_{\Sigma 0} + \Delta W_\Sigma - \Delta W_\Delta)} = \sqrt{v_d^2 + \frac{N}{C}(\Delta W_\Sigma - \Delta W_\Delta)} \approx v_d + \underbrace{\frac{N}{2Cv_d}(\Delta W_\Sigma - \Delta W_\Delta)}_{\Delta u_{cl}^{\Sigma}} \tag{2.54}$$

From these expressions, the sum capacitor voltages can be found, as well as the voltage unbalances, in the following way:

$$v_c^{\Sigma} = v_{cu}^{\Sigma} + v_{cl}^{\Sigma} = 2v_d + \frac{N}{Cv_d}\Delta W_\Sigma \tag{2.55}$$

$$v_c^{\Delta} = v_{cu}^{\Sigma} - v_{cl}^{\Sigma} = \frac{N}{Cv_d}\Delta W_\Delta \tag{2.56}$$

2.1.6 Modulation index for minimized ripple

The modulation index is defined as:

$$m = \frac{\widehat{V}_s}{V_d/2} \tag{2.57}$$

As already mentioned in Eq. (2.51),

$$W_{\Delta} = W_{\Delta 0} + \frac{v_d \widehat{I_s}}{2\omega_1}\sin(\omega_1 t - \varphi) - \frac{2\widehat{V_s} i_c}{\omega_1} sin\omega_1 t \tag{2.58}$$

In order to have minimum ripple, the above is set to 0. With $W_{\Delta 0} = 0$, and assuming ϕ=0, it is:

$$0 = \left(\frac{v_d \widehat{I_s}}{2} - 2\widehat{V_s} i_c\right)\frac{\sin(\omega_1 t)}{\omega_1} \tag{2.59}$$

It must be

$$\frac{v_d \widehat{I_s}}{2} = 2\widehat{V_s} i_c \tag{2.60}$$

Also, the condition for stable operation for the converter is:

$$2V_d I_d = \widehat{V_s}\widehat{I_s}\cos(\varphi) <=> I_d = \frac{\widehat{V_s}\widehat{I_s}}{2v_d} \tag{2.61}$$

Substituting, the derived condition is:

$$\widehat{V_s} = \frac{1}{\sqrt{2}} V_d = \frac{\sqrt{2}}{2} V_d <=> \frac{\widehat{V_s}}{V_d/2} = \sqrt{2} = m \tag{2.62}$$

The effect of the modulation index in the energy ripple can be seen in Fig. 5:

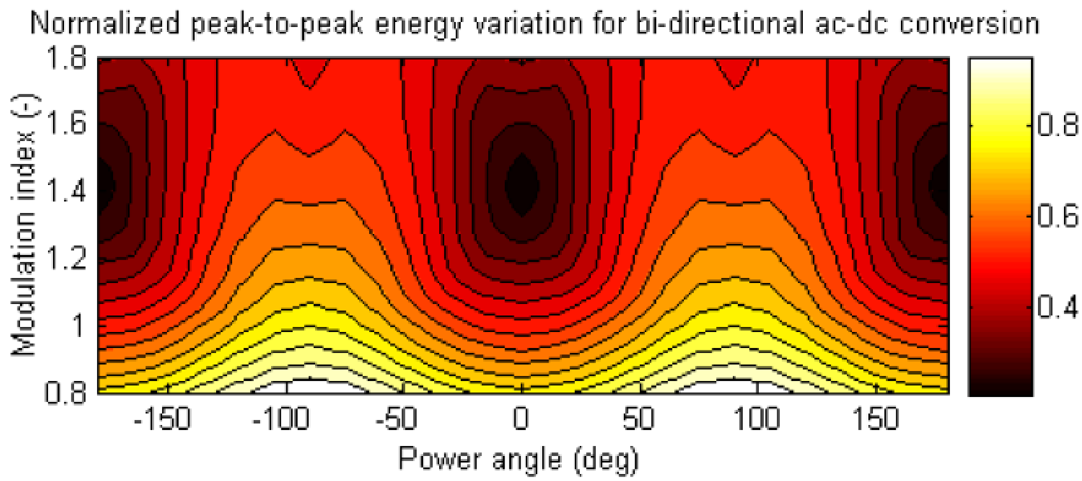


Fig. 5: Effect of the modulation index in the Energy Variation.[6]

It must be mentioned that in order to achieve higher modulation index, Full bridge converters have to be used, as they allow double voltage amplitude because they can create negative voltage also.[6]

2.2 Control of the MMC

2.2.1 Type of Controller

In Fig. 6 the standard control process is shown. After the higher level control (used for purposes like grid synchronization or power exchange regulation), the output current reference is generated. The output current controller compares this value with the real output current, and the output voltage reference is generated. Then the circulating current reference is determined in order to achieve an internal balancing between the energies of the arms. Finally, the insertion indices are calculated and fed into the modulation technique so as to drive the gates of the controllable switches. The internal balancing process is achieved with the internal control, whereas the output current control is achieved with the external control. [4]

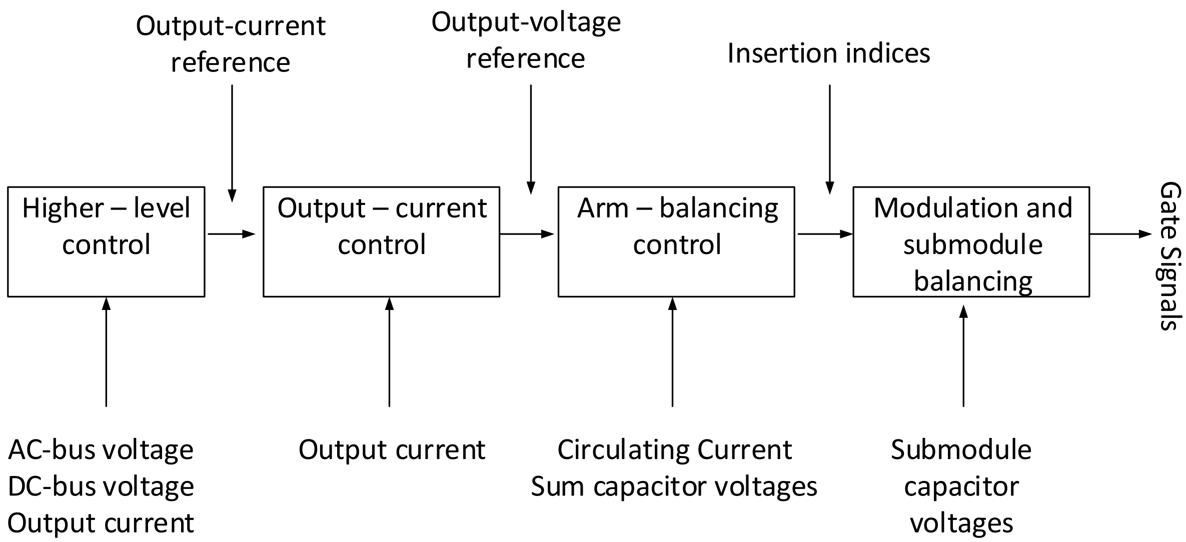


Fig. 6: Diagram of the control process of MMC.[4]

Although a very commonly used type of controller, the PI controllers are ineffective in the case of MMC.

Assuming a closed loop system with an inductance and relatively low resistance, as depicted in Fig. 7, the transfer function is given by:

$$G_c(s) = \frac{K_p s + K_i}{s^2 L + K_p s + K_i} \tag{2.63}$$

The condition for no error, is that for a given frequency $G_c(j\omega) = 1$, as in that case the input is equal to the output. By observing the transfer function, this is true only for the case of $\omega = 0$. For every other value, the amplitude is not equal to 1, so a sinusoidal reference is unable to be tracked.

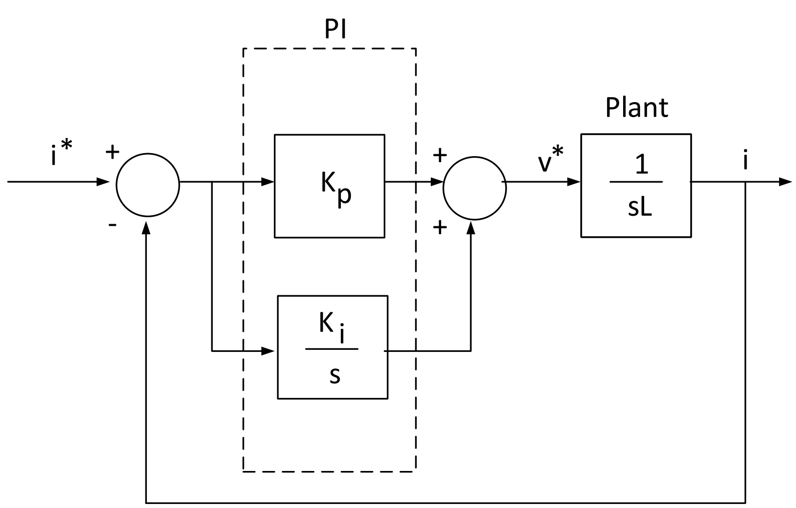


Fig. 7: Closed Loop scheme of current through inductance with a PI controller.[5]

For the aforementioned reasons, the type that is actually used is that of the Proportional Resonant (PR) controller. The advantage or this controller is that it can provide with accurate tracking of a reference that consists of a desired frequency, with unity gain, whereas the gain is not unity for different values of frequency. This means that for more different frequencies to be tracked, more resonant parts should be added and properly tuned.

The transfer function in open loop G_k and closed loop G_c operation respectively is described in the following (with $h\omega_1$ the wanted frequency to be tracked).

$$G_k(s) = \frac{K_p[s^2+(h\omega_1)^2]+K_h s}{[s^2+(h\omega_1)^2]sL} \quad , \quad G_c(s) = \frac{G_k(s)}{1+G_k(s)} = \frac{K_p[s^2+(h\omega_1)^2]+K_h s}{(sL+K_p)[s^2+(h\omega_1)^2]+K_h s} \tag{2.64}$$

2.2.2 Design of the controller:

The scheme of a PR controller is shown in Fig. 8.

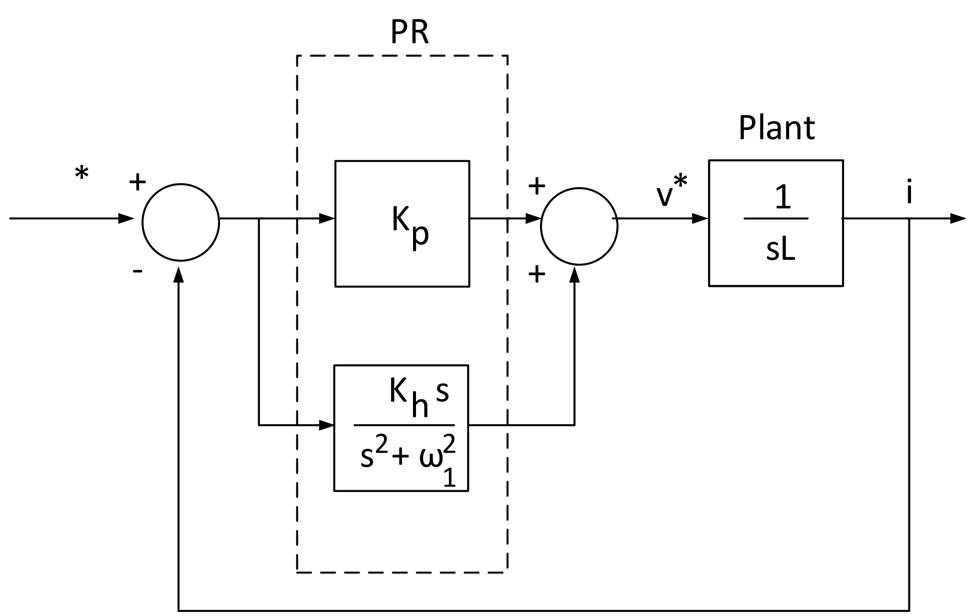


Fig. 8: PR controller for regulation of a current flowing through an inductance.[5]

The PR controller consists of 2 parts that must be parametrized: The Resonant and the Proportional. Each of them will be designed separately, as they are decoupled from frequency view. So, by setting $K_h = 0$, the following is derived:

$$G_c(s) = \frac{K_p/L}{s + K_p/L} \tag{2.65}$$

From this transfer function, the bandwidth of the system can be defined as a_c, with:

$$a_c = \frac{K_p}{L} \tag{2.66}$$

From the above equation, it is obvious that the desired value for the bandwidth defines the proportional gain, with

$$K_p = a_c L \tag{2.67}$$

2.2.3 Closed Loop System Bandwidth Selection

In its real time operation, the system encounters delays, produced either due to the physical limits of the devices used, such as communication systems and real time computations, consisting of two different components, or due to the switching effects. The first introduces delay with a value T_c close to the sampling period T_s and the latter with $T_s/2$. The PWM is also introducing delay due to the switching delay, T_c, which can be approximated as half of the sampling period. So, the total delay is:

$$T_d = T_c + 0.5\, T_s \tag{2.68}$$

Due to the existence of the delays, in order to achieve stability in the operation of the closed-loop system with margins taken into account, a compromise must be made for the value of a_c. A practically approved value for this is:

$$a_c \leq \frac{\omega_s}{10} \tag{2.69}$$

, where

$$\omega_s = \frac{2\pi}{T_s} \tag{2.70}$$

With the delay represented as a term e^{-sT_d}, and still only P control mode, the open loop transfer function becomes:

$$G_k(s) = \frac{K_p e^{-sT_d}}{sL} = \frac{a_c e^{-sT_d}}{s} \tag{2.71}$$

From the above, it is clear that unity gain is achieved for $\omega = a_c$. For this case, the phase margin is found as:

$$\varphi_m = \pi - \arg G_k(ja_c) = \frac{\pi}{2} - a_c T_d \tag{2.72}$$

And according to Eq. (2.70),

$$\varphi_m = \frac{\pi}{2} - \frac{\omega_s T_d}{10} \tag{2.73}$$

With $T_d = 1.5\, T_s$ (as T_c is almost equal to T_s) and $\omega_s T_d = 1.5 \cdot 2\pi$,

$$\varphi_m = 0.2\pi\, rad = 36^o \tag{2.74}$$

, which is an acceptable margin. The switching frequency defines a reasonable value according to Eq. (2.69).

2.2.4 Design of the Resonant Gain

A parametrization that can be made for the R part calculation is:

$$K_h = 2a_h a_c L = 2a_h K_p \tag{2.75}$$

In the above, a_h is the bandwidth of this control.

With substitution in Eq. (2.64), the following is derived:

$$G_c(s) = \frac{a_c[s^2 + (h\omega_1)^2] + 2\alpha_h a_c s}{(s + a_c)[s^2 + (h\omega_1)^2] + 2a_h a_c s} \tag{2.76}$$

This can be reexpressed as:

$$G_c(s) = \frac{a_c[s^2 + 2\alpha_h s + (h\omega_1)^2]}{(s + a_c)[s^2 + 2a_h s + (h\omega_1)^2] - 2a_h s^2} \tag{2.77}$$

Which, for $a_h \ll a_c$, can be simplified as

$$G_c(s) \approx \frac{a_c[s^2 + 2\alpha_h s + (h\omega_1)^2]}{(s + a_c)[s^2 + 2a_h s + (h\omega_1)^2]} = \frac{a_c}{s + a_c} \tag{2.78}$$

This Indicates a value for a_h in the area of hundreds of [rad/s], with the condition:

$$a_h < \omega_1 \tag{2.79}$$

From Eq. (2.78), it is evident that a pole will exist at:

$$s = -a_c \tag{2.80}$$

, and another pole pair canceled by the zero in the nominator. The value of a_h defines the resonant bandwidth, which means the speed of the convergence achieved by the resonant part.

2.2.5 DC Voltage Control

The condition for the DC voltage to remain constant is that the mean value of the total current produced by the phase arms is the DC value calculated in Eq. (2.6). However, the ripple induced by the arm currents produces deviations in the DC voltage. The dynamics of these phenomena is described through the following process.

From Fig. 3, it can be seen that for the DC voltage, it is:

$$2C_d \frac{dv_{du,l}}{dt} = i_d - \sum_{k=1}^{M} i_{u,l}^k \tag{2.81}$$

Calculating now the pole to pole DC voltage as $v_d = v_{du} + v_{dl}$, and through Eq. (2.2)

$$C_d \frac{dv_d}{dt} = i_d - \sum_{k=1}^{M} i_c^k \tag{2.82}$$

The DC voltage is controlled through the following process. From Eq. (2.26) and adding the two equations together, it is derived that:

$$\frac{C}{N} \frac{d(v_{cu}^{\Sigma} + v_{cl}^{\Sigma})}{dt} = n_u \left(\frac{i_s}{2} + i_c\right) + n_l \left(-\frac{i_s}{2} + i_c\right) \tag{2.83}$$

And including Eq. (2.55),

$$\frac{C}{N}\frac{dv_c^{\Sigma}}{dt} = (n_u - n_l)\frac{i_s}{2} + (n_u + n_l)i_c \tag{2.84}$$

From Eq. (2.42) and Eq. (2.43), assuming $v_c^* = v_d/2$ and omitting the ripple of the capacitor voltage, it is derived for the insertion indices that:

$$n_u \approx \frac{v_d/2 - v_s^*}{v_d} \qquad n_l \approx \frac{v_d/2 + v_s^*}{v_d} \tag{2.85}$$

Including Eq. (2.85) in Eq. (2.84), it is derived that:

$$\frac{C}{N}\frac{dv_c^{\Sigma}}{dt} = -\frac{v_s^* i_s}{v_d} + i_c \tag{2.86}$$

Assuming now only the mean values of the sum capacitor voltage and pure DC i_c, the expression transforms into:

$$\frac{C}{N}\frac{\overline{dv_c^{\Sigma}}}{dt} = -\underbrace{\frac{\overline{v_s^* i_s}}{v_d}}_{P/(Mv_d)} + i_c \tag{2.87}$$

Since the desirable sub capacitor voltages are considered to be equal to v_d, and as the controller for them is much faster than the deviations for v_d. That means that $\overline{v_c^{\Sigma}}$can be substituted with $2v_d$ in Eq. (2.87), and thus:

$$\frac{2C}{N}\frac{dv_d}{dt} = -\frac{P}{Mv_d} + i_c \tag{2.88}$$

Assuming now that the phases are kept balanced, from Eq. (2.82) setting $\sum_{k=1}^{M} i_c^k = Mi_c$, it is derived that:

$$C_d\frac{dv_d}{dt} = i_d - Mi_c \tag{2.89}$$

And with manipulations of Eq. (2.88) and Eq. (2.89) in order to eliminate i_c,

$$\underbrace{\left(C_d + \frac{2MC}{N}\right)}_{C_d'}\frac{dv_d}{dt} = i_d - \frac{P}{v_d} \tag{2.90}$$

Where the C_d' is defined to be the effective DC bus capacitance, larger than C_d.

From that point, the analysis for the DC voltage control can be established.

Multiplying Eq. (2.90) with v_d, it is derived

$$C'_d v_d \frac{dv_d}{dt} = v_d i_d - P => \frac{C'_d}{2}\frac{dv_d^2}{dt} = v_d i_d - P \tag{2.91}$$

The effective DC bus energy is defined as $W_d = C'_d v_d^2/2$ and the DC power as $P_d = v_d i_d$. Then it is derived:

$$\frac{dW_d}{dt} = P_d - P \tag{2.92}$$

Since the control of the DC Voltage is a higher level control loop, and the output current control is considered to have faster dynamics, the active power can be substituted by its reference. A PI controller then is set as:

$$P^* = a_d\left(1 + \frac{a_{id}}{s}\right)(W_d - W_d^*) \tag{2.93}$$

And a closed loop system is designed as:

$$W_d = \frac{a_d(s + a_{id})}{s^2 + a_d s + a_d a_{id}} W_d^* + \frac{s}{s^2 + a_d s + a_d a_{id}} P_d \tag{2.94}$$

From the above, the condition for a zero static gain is $a_{id} > 0$. A recommended value for a_{id} is $a_{id} < \frac{a_d}{2}$ [4]. For the a_d value, it must be:

$$a_d < \omega_1 \tag{2.95}$$

The control diagram is shown in Fig. 9. As it can be seen, a filter $H_p(s)$ is placed in order to eliminate any existing ripple. The Q reference is then added in order to produce the total reference current i_s^{*0}. Then a saturation block is added, and also an anti-windup system.

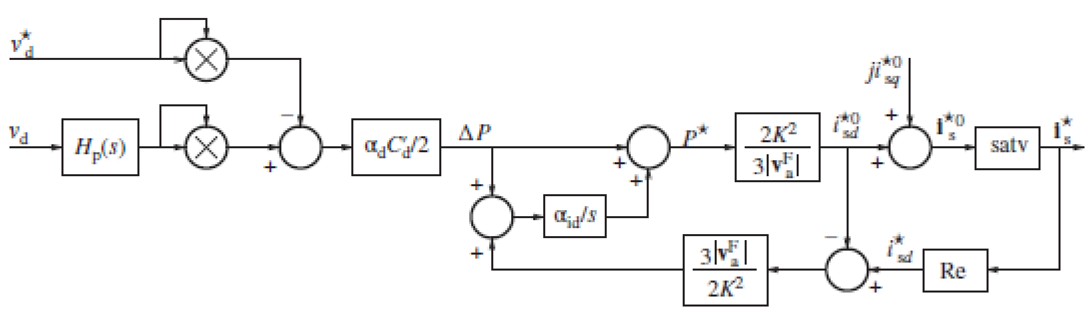


Fig. 9: Control Diagram for DC Voltage Regulation.[4]

2.2.6 Output Current Controller

The advantage of PR controller on the tracking of a given frequency reference make it suitable for the case of the output current control, since it is a pure sinusoidal signal of fundamental frequency. This means that the value for the parameter h should be 1 for this case. By manipulating Eq. (2.21), it is derived that:

$$\frac{L}{2}\frac{di_s}{dt} = v_s - v_a - \frac{R}{2}i_s => i_s = \frac{2}{sL+R}(v_s - v_a) \quad (2.96)$$

It is shown that the value of the current depends on the difference $(v_s - v_a)$. Given the fact that v_a, often described as load disturbance, is depended on the output current in a relation with the Short Circuit Ratio, and also that asymmetrical faults lead in fast angle changes and negative sequence components, a feed forward compensation for the v_a can be used in the control.

The calculated voltage reference v_s^* is not to be directly implemented in the control. It must be ensured that the value respects the rating and limits of the system. Therefore, saturation blocks have to be added in the output of the control. But this method creates the problem of the control keeping on building an error that is not real. Therefore, a solution is given with the technique of anti-windup, that is further analyzed in the following subchapter.

2.2.7 Anti-windup

As aforementioned, the saturation blocks in the output of the control lead in incorrect implementation of the control. The reason is that the saturation creates a different output than that of the controller, and the result is that the controller builds further error (something that is called windup). This means that in order to implement the saturation block without affecting the rest of the controller, the changes performed by the saturation block should be also fed into the controller. In other case, the error built during the saturated case will lead in inappropriate response once the system is back in unsaturated operation.

The method that is used in this project for the anti-windup is the back calculation, as it is explained in [4].

The output current control scheme, along with the Anti-wind up can be seen in Fig. 10. The Anti-wind up in this figure subtracts the v_s^* output of the saturation block from the v_s^{*0} input, and by making it a current error quantity it adds it back to the current reference input.

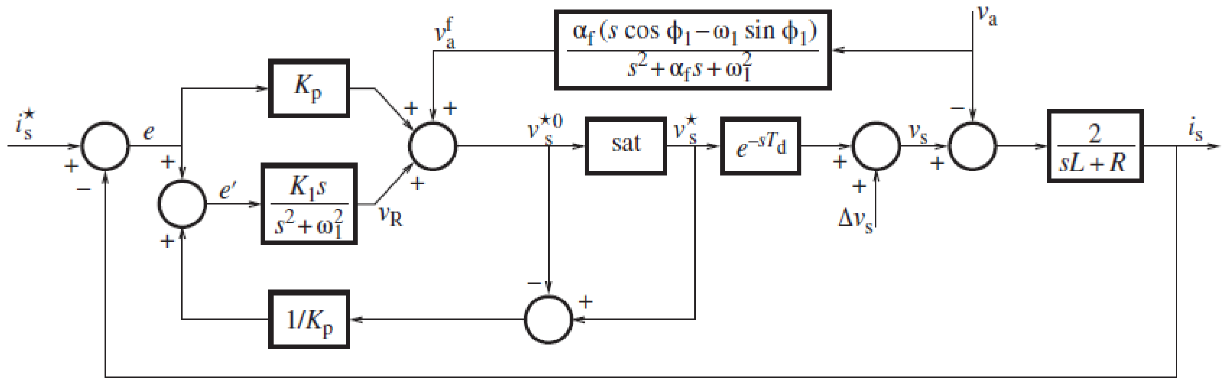


Fig. 10: Output current control loop, including Anti-wind up protection.[4]

2.2.8 Arm-Balancing Control

After the analysis of the output-current control, the remaining variables to be controlled are the circulating current and the sum capacitor voltages.

These variables are included in Eq. (2.22) and Eq. (2.26), and as already mentioned, the value of circulating current should fulfill Eq. (2.33), whereas the sum capacitor voltages should normally have a mean value equal to v_d. The process of this control is called arm-balancing control (or internal control). As the control is achieved through the insertion indices n_l and n_u, it is obvious that three state variables are to be controlled through two input variables. This might seem as an impossible goal.

Since the output current is defined by its own reference without taking into account the inner state of the MMC, the circulating current is chosen to achieve transfer of energy between arms in order to create balanced conditions. The use of circulating current for this purpose is analyzed in the following subchapter. Then, the control of the sum capacitor voltages must be achieved, in a way that they approach the value of v_d. For this purpose, which is called voltage control, different strategies have been developed, out of which the Direct Voltage Control strategy is analyzed in subchapter 2.3.

2.2.9 Circulating Current Control

From Eq. (2.22), it was derived that:

$$L\frac{di_c}{dt} = \frac{u_d}{2} - v_c - Ri_c \Rightarrow i_c = \frac{1}{sL+R}\left(\frac{v_d}{2} - v_c\right) \tag{2.97}$$

The value of v_c is its reference with the time delay, and a parasitic Δv_c.

$$v_c = e^{-sT_d}v_c^* + \Delta v_c \tag{2.98}$$

, where the Δv_c describe switching harmonic effects. As from the control a second harmonic component is added to that value, a resonant controller with h=2 is added in order to cancel this. With the inclusion of a fed forward value of $v_d/2 - Ri_c^*$ as described in Eq. (2.96), the reference of the voltage for the circulating current becomes:

$$v_c^* = \frac{v_d}{2} - Ri_c^* - R_a\left(1 + \frac{2a_2 s}{s^2 + (2\omega_1)^2}\right)(i_c^* - i_c) \tag{2.99}$$

$$i_c^* = \frac{i_d}{M} + \Delta i_c^* \tag{2.100}$$

, with R_a being the proportional gain and the Δi_c^* is a optional value included in some types of control.

The scheme for the circulating current controller is shown in Fig. 11.

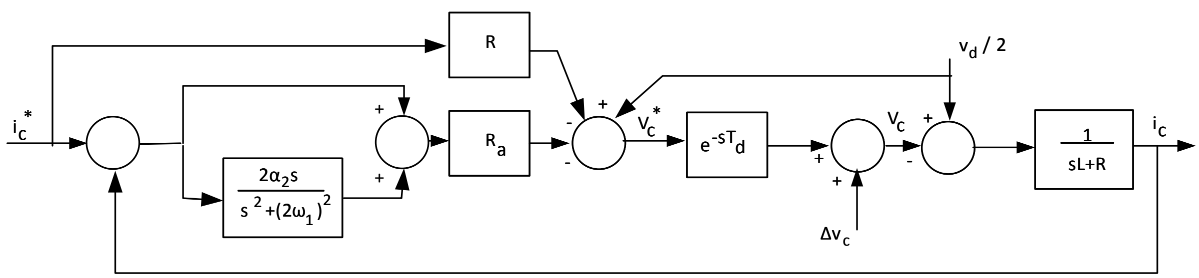


Fig. 11: Circulating Current Controller.[4]

2.3 Direct Voltage Control with Arm Balancing

2.3.1 Direct Voltage Control

In this type of control, the sum capacitor voltages in Eq. (2.42) and (2.43) for the insertion indices are approximated by the DC voltage v_d. As already discussed, in this method second harmonic components are introduced, which are solved in the way discussed in the circulating current section (subchapter 2.2.9).[5]

$$n_u = \frac{v_c^* - v_s^*}{v_d} \qquad\qquad n_l = \frac{v_c^* + v_s^*}{v_d} \tag{2.101}$$

2.3.2 Arm Balancing

In order to achieve arm energy balancing control, the Δi_c^* value discussed above is modified in a way to take into account energy unbalances between the upper and lower arm. A component of this value is calculated by the difference between the reference and the real value for the sum energy of the upper and the lower arm, and another component is fixed by the difference between the energies of the two arms. The value of Δi_c is then added to the circulating current controller as described.

Analytically, from Eq. (2.47), it was derived that:

$$\frac{dW_\Sigma}{dt} = 2v_c^* i_c - v_s^* i_s \qquad \frac{dW_\Delta}{dt} = v_c^* i_s - 2v_s^* i_c \tag{2.102}$$

The sum and unbalance energies W_Σ and W_Δ must be controlled to be equal to their references $W_{\Sigma 0}$ and 0. This ensures that the mean values of v_{cu}^Σ and v_{cl}^Σ are kept close to v_d. In reality, the circulating current carries the amount of energy charging or discharging according to what is implied by the control. The generated value to be added in the circulating current control is then:

$$\Delta i_c^* = K_\Sigma(W_{\Sigma 0} - BSF\{W_\Sigma\}) - K_\Delta BSF\{W_\Delta\}cos(\omega_1 t) \tag{2.103}$$

The BSFs (Band Stop Filters) included are supposed to clear the signal from any ripple included in the fundamental and second harmonic frequencies. The cosine term is used to provide with an AC component for the circulating current in case of unbalanced arm energies. The subsequent generated value is fed to the circulating current control, and a proportional controller will create the reference according to:

$$v_c^* = \frac{v_d}{2} - R_a(i_c^* + \Delta i_c^* - i_c) \tag{2.104}$$

For the acquisition of Δi_c, the method described in [7] is used. For the W_Σ regulation, from Eq. (2.102) it can be seen that the second term of its equation ($v_s^* i_s$)is referring to the output power, and the first ($2v_c^* i_c$) to the active power exchange between the different legs of the MMC. So, with the reference for W_Σ stated in (2.52) as$W_{\Sigma 0} = \frac{Cv_d^2}{N}$, a simple gain K_Σ can regulate the DC part of the circulating current. The W_Σ is calculated, passed through 50 Hz and 100 Hz band-stop filters in order to remove any ripple existing, and multiplied with gain K_Σ.

For the arm energy difference, from Eq. (2.102), and neglecting oscillating terms, it is derived that:

$$\frac{dW_\Delta}{dt} = -\hat{V}_s \hat{\imath}_{c1} \cos(\varphi_c) \tag{2.105}$$

, which means that with the injection of a sinusoidal component for the i_c, active power can be regulated to bring balance between different legs. For this purpose a gain K_Δ is inserted. The W_Δ is calculated for each leg, passed through a band-stop filter for 50 and 100 Hz, and an error signal for each phase is generated (e_a, e_b, e_c respectively).

The problem that arises, is that an injection of current into one leg affects also the other legs. So, a decoupling process must be implemented. The method proposed in [7] suggests that in the unbalanced phase, a fundamental frequency active current is injected. Then, since there is no sinusoidal component in DC side, for the circulating currents of all phases it is:

$$I_{ca1} + I_{cb1} + I_{cc1} = 0 \tag{2.106}$$

This can be achieved by creative a reactive power reference in the other two phases such that the total vector produced by the total effect of the three currents is equal to zero, as shown in Fig. 12.

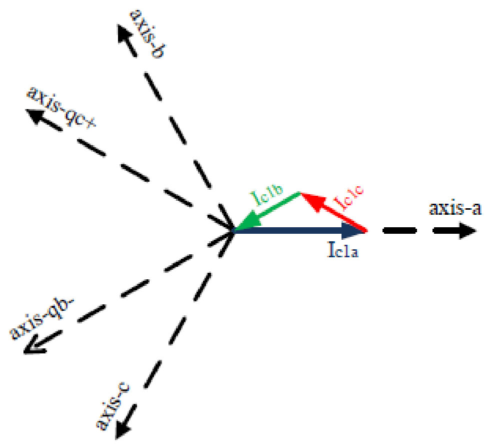


Fig. 12: Reactive current injection in B, C phases for canceling the effect of phase A active current Injection. [7]

It can be seen that in order to achieve this condition for injection of active current in phase A, then in phase B and phase C the current injection is in -90^o and 90^o phase shift respectively. With simple trigonometry, it is derived that the amplitude of the injection for this purpose is $\sqrt{3}$ times smaller than the amplitude of phase A current. Expanding the principle for all phases, the total injection reference is:

$$i^*_{c1_a} = K_\Delta\left(e_a\cos(\omega t) + \frac{1}{\sqrt{3}}e_b\cos\left(\omega t + \frac{\pi}{2}\right) + \frac{1}{\sqrt{3}}e_c\cos\left(\omega t - \frac{\pi}{2}\right)\right) \tag{2.107}$$

$$i^*_{c1_b} = K_\Delta\left(e_b\cos\left(\omega t - \frac{2\pi}{3}\right) + \frac{1}{\sqrt{3}}e_\alpha\cos\left(\omega t - \frac{7\pi}{6}\right) + \frac{1}{\sqrt{3}}e_c\cos\left(\omega t - \frac{\pi}{6}\right)\right) \tag{2.108}$$

$$i^*_{c1_c} = K_\Delta\left(e_c\cos\left(\omega t + \frac{2\pi}{3}\right) + \frac{1}{\sqrt{3}}e_\alpha\cos\left(\omega t + \frac{7\pi}{6}\right) + \frac{1}{\sqrt{3}}e_b\cos\left(\omega t + \frac{\pi}{6}\right)\right) \tag{2.109}$$

,with e_a, e_b, e_c as already mentioned being the error fed to the controller in each phase.

The scheme for the Direct Voltage Control is shown in Fig. 13, the general principle of the energy control in Fig. 14, and the analytical generation of the current reference with the arm balancing is in Fig. 15.

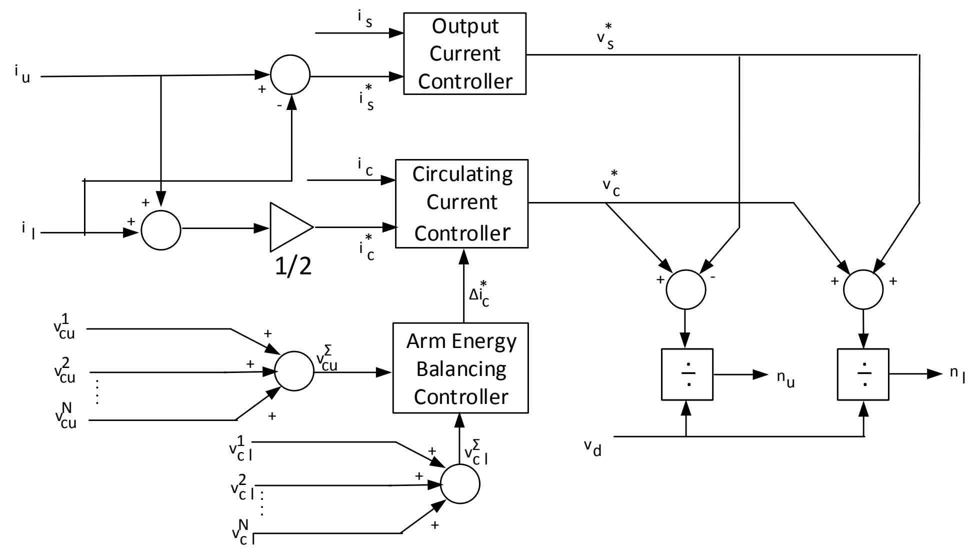


Fig. 13: Direct Voltage Control with Arm Balancing.[4]

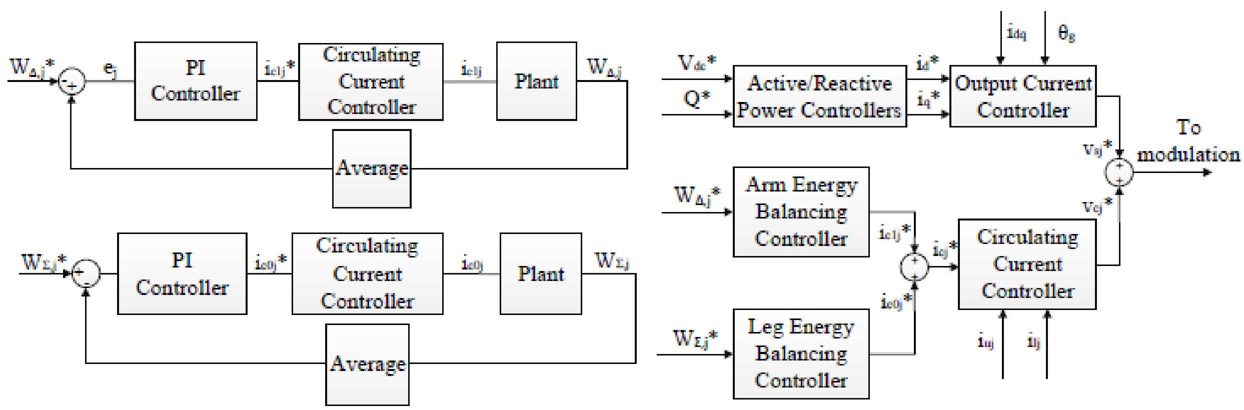


Fig. 14: General Principle of Energy Control Implementation.[7]

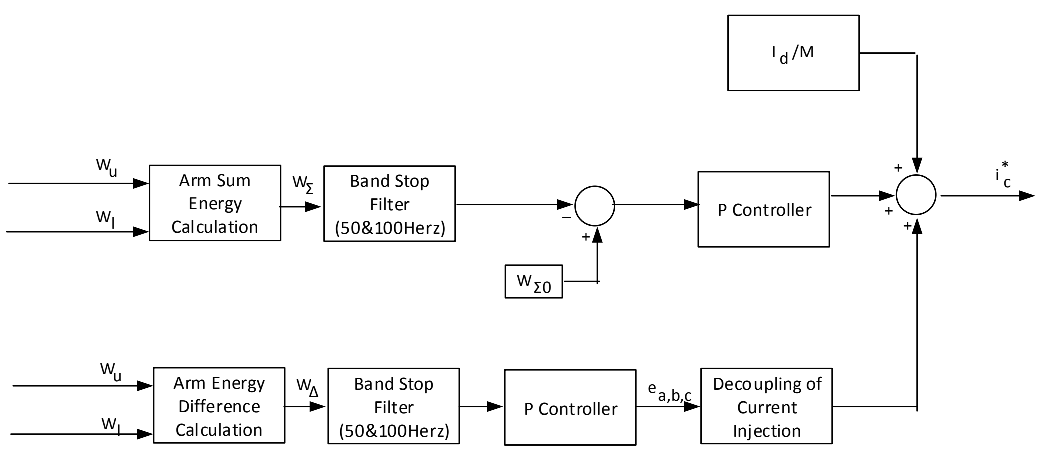


Fig. 15: Circulating Current Reference generation with Arm Balancing.

3 Control of MMC under unbalanced conditions

3.1 Grid requirements

In some countries, the regulations regarding the operation of HVDC stations require for some specific characteristics in the case of unbalanced conditions (for example, a grid fault). The station should be able to stay connected for at least 150ms, and it should be also able to inject reactive power for voltage support, in order to achieve the low voltage ride through operation (LVRT). There are two desirable functions for this. The first is the avoidance of the tripping of the converter which could happen because of AC overcurrent or DC overvoltage. The second is the injection of positive sequence reactive current in a relation with the magnitude of the positive sequence voltage drop.[4]

$$i_{q^+} = k_+(0.9 - V_+) \tag{3.1}$$

, where V_+ is the positive voltage component in per unit. k_+ is a constant that works as a droop constant, with a value varying from 0 to 10 (typical value 2.5). There is also a deadband. The described condition is further called positive-sequence injection low-voltage ride-through (PSI-LVRT).

Another requirement includes the case of negative sequence voltage components, in the case of which the system should be able to inject negative sequence reactive current component, related to the negative sequence voltage as:

$$i_{q^-} = -k_-(V_- - 0.05) \tag{3.2}$$

,with V_- being the negative sequence voltage in per unit. The principle regarding the k_- is the same as k_+, and there is again a part of the curve with no injection (Fig. 16). This condition will be further called negative-sequence injection low-voltage ride-through (NSI-LVRT).

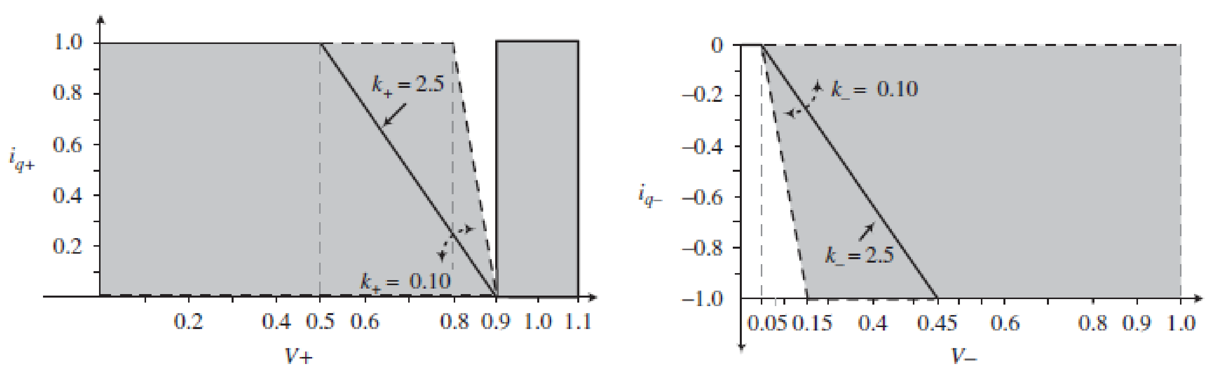


Fig. 16: Grid Requirements for LVRT with reactive current injection in Germany. The positive sequence is depicted on the left, the negative on the right.[4]

The two sequences are controlled independently during the case of a fault. This means that the normal control strategy explained in Chapter 2, need to be expanded. In the next subchapters, PSI, MSI-BP (mixed injection of the two sequences balancing the active power) and MSI-GC (mixed injection of reactive current according to the grid requirements) methods are further analyzed.

3.2 Disadvantages of the conventional control

3.2.1 PLL with notch filter

According to the conventional vector control, the current reference is derived as follows:

The instantaneous power in a voltage-aligned dq frame is given by [4]:

$$P + jQ = \frac{3}{2K^2}\left|\mathbf{v}_{\mathrm{a}}^{\mathrm{F}}\right|\left(i_{sd} - ji_{sq}\right), \tag{3.3}$$

where K is a space vector scaling factor, and P and Q the active and reactive power reference. The derived active and reactive current references are:

$$i_{sd}^{*0} = \frac{2K^2}{3\left|\mathbf{v}_{\mathrm{a}}^{\mathrm{F}}\right|}P^* \qquad\qquad i_{sq}^{*0} = \frac{2K^2}{3\left|\mathbf{v}_{\mathrm{a}}^{\mathrm{F}}\right|}Q^* \tag{3.4}$$

By setting the K factor equal to 1, and assuming $v_{ad} = \left|\mathbf{v}_{\mathrm{a}}^{\mathrm{F}}\right|$, which means the ac voltage through an LPF, aligned with the d-axis, the current reference is derived as:

$$\begin{cases} i_{sd}^* = \dfrac{2}{3}\dfrac{P^*}{v_{ad}} \\ i_{sq}^* = -\dfrac{2}{3}\dfrac{Q^*}{v_{ad}} \end{cases} \tag{3.5}$$

The negative sequence oscillations present in the grid voltage thereby induce a second harmonic ripple into the reference current, since they are tracked by the PR controllers and entered in the calculation of the reference. This means that there is a not desirable simultaneous negative current injection. The reason for that is that the PLL cannot track the exact angle and magnitude of the positive sequence of the grid voltage during an asymmetrical fault.[4]

This problem is solved through the connection of a PR controller, able to track and eliminate the second harmonic component.

$$H_n(s) = \frac{s^2 + (2\omega_1)^2}{s^2 + a_n s + (2\omega_1)^2} \tag{3.6}$$

With $H_p(s)$ being the LPF that is normally placed in the PLL input [4], the total filter transfer function is given as $H_p(s)H_n(s)$. That way, it is ensured that the oscillations are reduced in the produced reference and thus a more clear positive sequence injection reference is generated.

Although the method enhances the conventional control, it still fails to achieve the NSI-LVRT by injecting proper negative sequence current. In order to achieve this feature, an accurate Positive/Negative Sequence Extraction (PNSE) should be implemented.

There are two ways of achieving this goal. The decoupled double synchronous reference frame (DDSRF) which is done in the dq reference frame, and the double second order generalized integrator (DSOGI) which is done in αβ stationary frame. For a number of reasons reasons the DSOGI is preferred, and is used in the present thesis.

3.2.2 The DSOGI-PNSE

This technique, depicted in Fig. 17, is able to calculate the positive and negative sequences in the αβ reference frame. In order to achieve this, it makes use of a 90 degrees lagging phase-shifting operator $= e^{-\frac{j\pi}{2}}$, which creates quadratic values of the voltage components, such that:

$$\begin{aligned} \mathbf{v}^{s+} &= [T_{\alpha\beta^{+1}}]\mathbf{v}^{s} \quad &: \quad [T_{\alpha\beta^{+1}}] = \frac{1}{2}\begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix} \\ \mathbf{v}^{s-} &= [T_{\alpha\beta^{-1}}]\mathbf{v}^{s} \quad &: \quad [T_{\alpha\beta^{-1}}] = \frac{1}{2}\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix} \end{aligned} \tag{3.7}$$

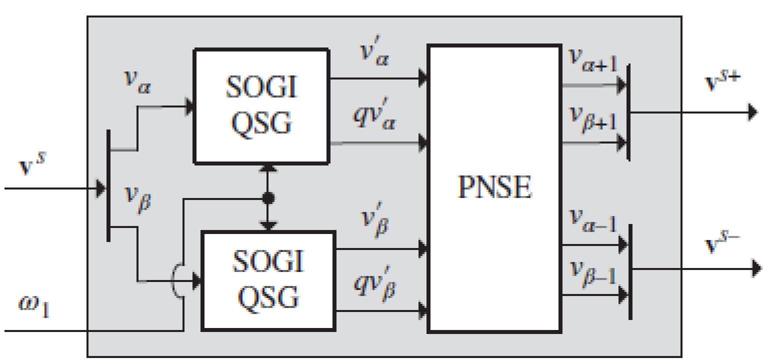


Fig. 17: Depiction of DSOGI – PNSE.[4]

The quadratic values are generated with the use of a quadratic signal generator (SOGI-QSG), shown in Fig. 17. The α-β components of the input voltage are fed into the system, and the values $v'_\alpha, v'_\beta, qv'_\alpha, qv'_\beta$ are generate, the former two being the direct and the latter two the quadratic values. These values are then fed into the PNSE for the extraction of the positive and negative sequence components. The implementation of the SOGI-QSG and PNSE are shown in Fig. 18.

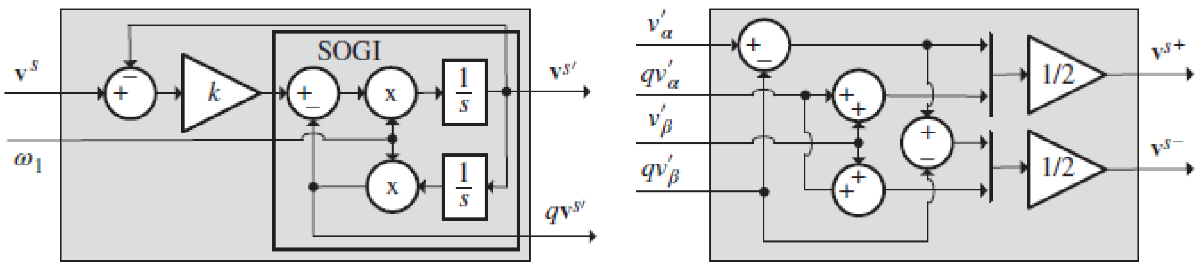


Fig. 18: SOGI-QSG on the left and PNSE on the right.[4]

The transfer function for the SOGI-QSG is given by:

$$\frac{v'(s)}{v(s)} = \frac{k\omega_1 s}{s^2 + k\omega_1 s + \omega_1^2} \tag{3.8}$$

$$\frac{qv'(s)}{v(s)} = \frac{k\omega_1^2}{s^2 + k\omega_1 s + \omega_1^2} \tag{3.9}$$

Assuming accurate estimation of ω_1, the two equations give equal amplitude. A compromise for value k between band-width and fast response can be:

$$k = \sqrt{2} \tag{3.10}$$

The filtering effect provided by the SOGI-QSG ensures that no harmonic content is transferred from the input, which cancels the necessity for a filter in the PLL.

3.3 Injection Strategy

A strategy for the generation of the current reference can be the flexible positive/negative sequence control (FPNSC). According to that, with given references of P and Q and arbitrary voltage v, the current reference is given by:

$$\mathbf{i}^* = \underbrace{P \cdot \left(\frac{k_1}{|\mathbf{v}^+|^2} \cdot \mathbf{v}^+ + \frac{1-k_1}{|\mathbf{v}^-|^2} \cdot \mathbf{v}^- \right)}_{i_p^*} + \underbrace{Q \cdot \left(\frac{k_2}{|\mathbf{v}^+|^2} \cdot \mathbf{v}_{\perp}^+ + \frac{1-k_2}{|\mathbf{v}^-|^2} \cdot \mathbf{v}_{\perp}^- \right)}_{i_q^*} \tag{3.11}$$

In this equation, the values k_1 and k_2 are droop factors that are used to change the between the positive and the negative sequence respectively, and $\mathbf{v}_{\perp}$is an orthogonal version of the grid voltage.

$$\mathbf{v}_{\perp abc} = \frac{1}{\sqrt{3}} \begin{bmatrix} 0 & 1 & -1 \\ -1 & 0 & 1 \\ 1 & -1 & 0 \end{bmatrix} \mathbf{v}_{abc} \quad ; \quad \mathbf{v}_{\perp \alpha\beta} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \mathbf{v}_{\alpha\beta} \quad ; \quad \mathbf{v}_{\perp dq} = \begin{bmatrix} 0 & -1 \\ 1 & 0 \end{bmatrix} \mathbf{v}_{dq} \tag{3.12}$$

The factor $k_1$can receive values from 0 to 1. By changing the value, the active power to be delivered to the grid can be shared between the two sequences in different ways. A value equal to 1 means that only positive sequence current is delivered, whereas a value equal to 0 means that pure negative sequence current is injected. The factor k_1 can also take values between 0 and -1. In this scenario, the MMC absorbs active power from the grid with one of the sequences, and delivers a proper amount of active power with the other sequence in order to both achieve the desirable amount of power and cancel existing unbalances.

For the reactive power, the injection of positive sequence acts as grid voltage support in case of a fault. Pure positive sequence injection is achieved by setting $k_2 = 1$. On the other hand, the negative sequence injection cancels the negative sequence component of the voltage, thus it cancels the unbalances. Pure negative sequence injection is achieved with $k_2 = 0$. Combined injection of both sequences can be achieved with proper values of k_2, according to the desirable function.

The reference current is then calculated with use of the Instantaneous Power Theory. For the general case of a rectifying converter, the power is described with:

$$p = P + \underbrace{P_{c2}\cos(2\omega_1 t) + P_{s2}\sin(2\omega_1 t)}_{\tilde{p}} \tag{3.13}$$

$$q = Q + \underbrace{Q_{c2}\cos(2\omega_1 t) + Q_{s2}\sin(2\omega_1 t)}_{\tilde{q}} \tag{3.14}$$

It can be seen that both equations contain a DC component (P and Q) and a second harmonic ripple (described by the terms P_{c2}, P_{s2}, Q_{c2}, Q_{s2}). Therefore, there are six terms to be controlled through the control of four available variables (i_{d^+},i_{q^+}, i_{d^-}, i_{q^-}). So two of the terms are excluded, Q_{c2}, Q_{s2}, and the final expression becomes:

$$\begin{bmatrix} P \\ Q \\ P_{c2} \\ P_{s2} \end{bmatrix} = \frac{3}{2} \underbrace{\begin{bmatrix} v_{d^{+1}} & v_{q^{+1}} & v_{d^{-1}} & v_{q^{-1}} \\ v_{q^{+1}} & -v_{d^{+1}} & v_{q^{-1}} & -v_{d^{-1}} \\ v_{d^{-1}} & v_{q^{-1}} & v_{d^{+1}} & v_{q^{+1}} \\ v_{q^{-1}} & -v_{d^{-1}} & -v_{q^{+1}} & v_{d^{+1}} \end{bmatrix}}_{A} \cdot \begin{bmatrix} i_{d^{+1}} \\ i_{q^{+1}} \\ i_{d^{-1}} \\ i_{q^{-1}} \end{bmatrix} \tag{3.15}$$

Therefore, the current reference is calculated by:

$$\begin{bmatrix} i^*_{d^{+1}} \\ i^*_{q^{+1}} \\ i^*_{d^{-1}} \\ i^*_{q^{-1}} \end{bmatrix} = A^{-1} \cdot \frac{2}{3} \begin{bmatrix} P \\ Q \\ P_{c2} \\ P_{s2} \end{bmatrix} \tag{3.16}$$

And with the use of FPNSC, the instantaneous power can be derived as $p = P + \tilde{p}$, with:

$$\tilde{p} = \left(\frac{P \cdot k_1}{|\mathbf{v}^+|^2} + \frac{P \cdot (1 - k_1)}{|\mathbf{v}^-|^2} \right) \mathbf{v}^+ \cdot \mathbf{v}^- + \left(\frac{Q \cdot k_2}{|\mathbf{v}^+|^2} - \frac{Q \cdot (1 - k_2)}{|\mathbf{v}^-|^2} \right) \mathbf{v}_{\perp}^+ \cdot \mathbf{v}^- \tag{3.17}$$

The above expression contains two ripple factors, one from P and one from Q. It must be mentioned that an analytical solution for both droop factors cannot be derived, since there are two unknown values for one equation.

The FPNSC method can be adjusted in order to achieve the different strategies that will be mentioned.[4]

3.3.1 Positive Sequence Injection (PSI) with Low Voltage Ride Through (LVRT) Compliance

This strategy focuses on the injection of positive sequence current. The active current aims at delivering the desirable active power, whereas the reactive current follows the grid code. The reference is derived from the FPNSC by keeping k_1 and k_2 equal to 1:

$$\mathbf{i}^* = P \underbrace{\frac{\mathbf{v}^+}{|\mathbf{v}^+|^2}}_{\mathbf{i}_p^*} + Q \underbrace{\frac{\mathbf{v}_{\perp}^+}{|\mathbf{v}^+|^2}}_{\mathbf{i}_q^*} \tag{3.18}$$

As the PLL is supposed to align the dq frame with the d axis of the voltage, it is derived that $v_{d^+} = \hat{V}_+$, $v_{q^{+1}} = 0$, and Eq. (3.16) transforms into:

$$\begin{cases} i_{d^+}^* = \dfrac{2}{3}\dfrac{P}{v_{d^+}} \\ i_{q^+}^* = \dfrac{2}{3}\dfrac{Q}{v_{d^+}} \end{cases} \tag{3.19}$$

By demanding reactive current to comply with the PSI-LVRT requirement, the former results into:

$$\begin{cases} i_{d^+}^* = \dfrac{2}{3}\dfrac{P}{v_{d^+}} \\ i_{q^+}^* = -k_+(0.9 - V_+) \end{cases} \tag{3.20}$$

This strategy does not deal with the unbalances, as no negative sequence current is injected. Thus, a second harmonic ripple exists in the power delivered.

3.3.2 Mixed Sequence Injection (MSI) with Balanced Power (BP)

This strategy aims at injecting both positive and negative sequence current to the grid. The positive active current is keeping the load, the positive reactive current meets the grid requirements, whereas the negative sequence current aims at cancelling the ripple in the power. For this goal, from Eq.(3.17) and setting $\tilde{p} = 0$, it is derived that:

$$\tilde{p} = \left(\frac{P \cdot k_1}{|v^+|^2} + \frac{P \cdot (1 - k_1)}{|v^-|^2}\right) v^+ \cdot v^- + \left(\frac{Q \cdot k_2}{|v^+|^2} - \frac{Q \cdot (1 - k_2)}{|v^-|^2}\right) v_{\square}^{+} \cdot v^- = 0 \tag{3.21}$$

Both terms must be 0. Thus, this condition results into:

$$k_1 = \frac{|v^+|^2}{|v^+|^2 - |v^-|^2} \geq 1 \tag{3.22}$$

$$k_2 = \frac{|v^+|^2}{|v^+|^2 + |v^-|^2} \leq 1 \tag{3.23}$$

Substituting in Eq. (3.11), results into:

$$\mathbf{i}^* = P \cdot \underbrace{\frac{\mathbf{v}^+ - \mathbf{v}^-}{|\mathbf{v}^+|^2 + |\mathbf{v}^-|^2}}_{\mathbf{i}_p^*} + Q\,\underbrace{\frac{\mathbf{v}_{\square}^{+} - \mathbf{v}_{\square}^{-}}{|\mathbf{v}^+|^2 + |\mathbf{v}^-|^2}}_{\mathbf{i}_q^*} \tag{3.24}$$

For the reactive current, the reference is derived from the compliance with the grid requirements:

$$i_{q^+}^* = -k_+(0.9 - V_+) \tag{3.25}$$

And finally, the negative reactive current is derived as:

$$i_{q^-}^* = -k_+(0.9 - V_+)\frac{V_-}{V_+} \tag{3.26}$$

So, the total expression in dq form:

$$\begin{cases} i_{d^+}^* = \dfrac{2}{3}\dfrac{P}{v_d^+} \\ i_{q^+}^* = \dfrac{2}{3}\dfrac{Q}{v_d^+} \\ i_{d^-}^* = -\dfrac{2}{3}\dfrac{P \cdot v_d^-}{(v_d^+)^2} \\ i_{q^-}^* = \dfrac{2}{3}\dfrac{Q \cdot v_d^-}{(v_d^+)^2} \end{cases} \tag{3.27}$$

In order to comply with the grid requirements for the positive sequence reactive current, its reference is derived as:

$$i_{q^+}^* = -k_+(0.9 - V_+) \tag{3.28}$$

And finally, the negative sequence reactive current is derived as:

$$i_{q^-}^* = -k_+(0.9 - V_+)\frac{V_-}{V_+} \tag{3.29}$$

So, finally

$$
\begin{cases}
i_{d^+}^* = \frac{2}{3}\frac{P}{v_d^+} \\
i_{q^+}^* = -k_+(0.9 - V_+) \\
i_{d^-}^* = -\frac{2}{3}\frac{P \cdot v_d^-}{(v_d^+)^2} \\
i_{q^-}^* = -k_+(0.9 - V_+)\frac{V_-}{V_+}
\end{cases} \tag{3.30}
$$

3.3.3 MSI with grid compliance (GC)

This strategy aims at complying with both positive and negative sequence reactive current injection. The positive sequence is given as above, whereas the negative sequence is given by:

$$
i_{q^-}^* = -k_-(V_- - 0.05) \tag{3.31}
$$

No negative sequence active current injection is considered for this strategy ($i_{d^-}^* = 0$) .

So finally, the total injection reference is described by:

$$
\begin{cases}
i_{d^+}^* = \frac{2}{3}\frac{P}{v_d^+} \\
i_{q^+}^* = -k_+(0.9 - V_+) \\
i_{d^-}^* = 0 \\
i_{q^-}^* = -k_-(V_- - 0.05)
\end{cases} \tag{3.32}
$$

3.3.4 Implementation of Output Current Vector Control with DSOGI-PNSE

There are two major ways of implementing the aforementioned control strategies. The DDSRF and the DSOGI-PNSE methods. In this project, the latter is used.

In this technique, the positive and negative sequence references can be added together algebraically, as they are in stationary form. The scheme of the controller is given in Fig. 19.

Three different parts of control can be seen in the controller. First, the controller receives the voltage measurement and through the DSOGI-PNSE and the PLL calculates the positive and negative sequence voltage components. Then, those values are entered in the block of the injection strategy, and with the addition of a component regarding the control of the DC voltage, the total output current reference is produced. Finally, the output current reference is inserted in the output current controller, and the generated reference is fed to the internal control.

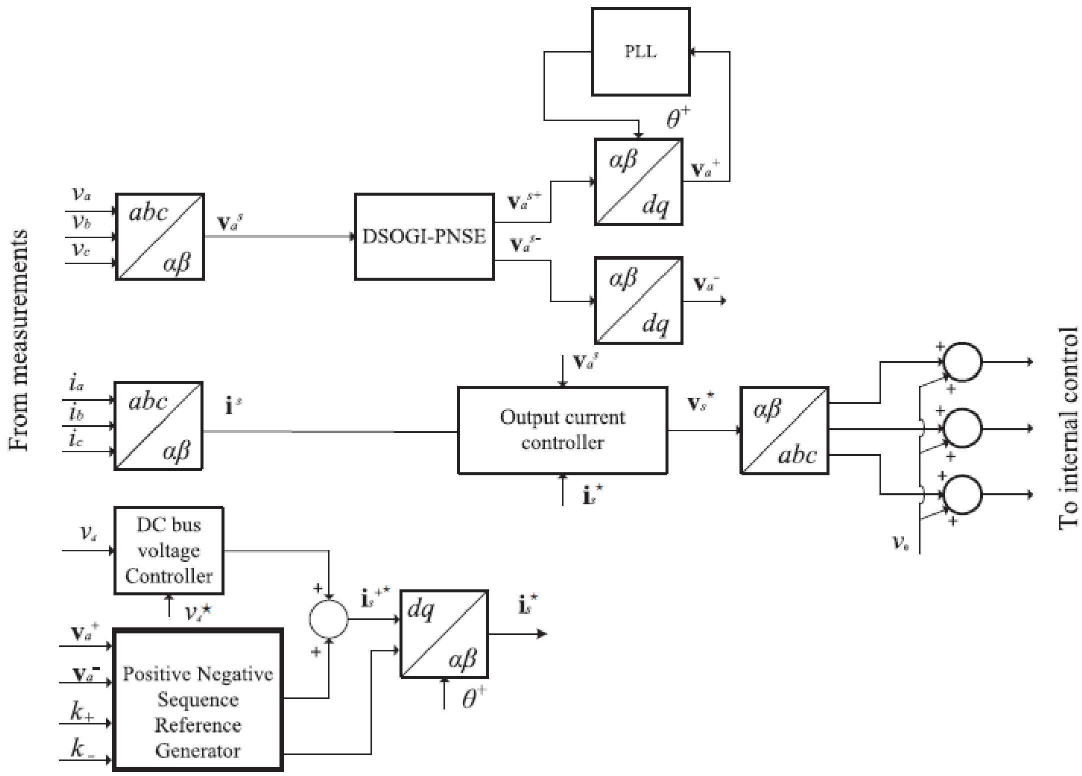


Fig. 19: DSOGI-PNSE method scheme.[4]

3.4 Current Limitation

The strategies mentioned do not take into account the limits of the MMC in current amplitude. The total current reference is generated in order to achieve the LVRT, the DC voltage control or the power references but the current range must be also taken into account. Since there are four different components injected, the current limitation technique should take into account the priority of the injection. For this purpose, the following technique is proposed.

First, the technique is implemented in total dq reference of the mixed injection. Since the positive and negative sequence dq components cannot be algebraically added in dq reference frame, the positive and negative sequence injections are transformed in αβ reference and then added together. The acquired αβ reference is then transformed to dq, that now contains both sequences.

The priority of the method is given to the reactive current injection. So, in case that the total current exceeds a current limit (I_{max}), the active current reference is reduced, by reducing the active power reference. Furthermore, in case that the reactive current reference exceeds the limit by itself, it is set to the limit.

The principle of this control is described with the following expressions:

$$\left.\begin{array}{c} I_d^2 \le I_{max}^2 - I_q^2 \\ I_q \le I_{max} \end{array}\right\} \tag{3.33}$$

In case that the I_d has to be limited, then the reference that generates it has to be limited also (either it is a dc voltage controller or an active power reference). For that purpose a variable k_{red} is introduced, ranging from 0 to 1. It is multiplied with the power reference, in a way that $k_{red} = 0$ means no active power, and $k_{red} = 1$ means the original reference.

The method is shown in Fig. 20. The current reference in dq for each sequence is transformed in αβ, the two sequences are added together and then, the current is transformed again in dq, in order to implement the limitation. First the reactive current is limited to I_{max} with a saturation block. Then the amplitude of the total current is compared to I_{max}, and in case that it is greater, the value of value of k_{red} is reduced in the following way:

$$k_{red} = \sqrt{\frac{I_{max}^2 - I_q^2}{I_d^2}} \tag{3.34}$$

And the power reference limitation is generated as:

$$P_{lim}^* = P^* \cdot k_{red}$$

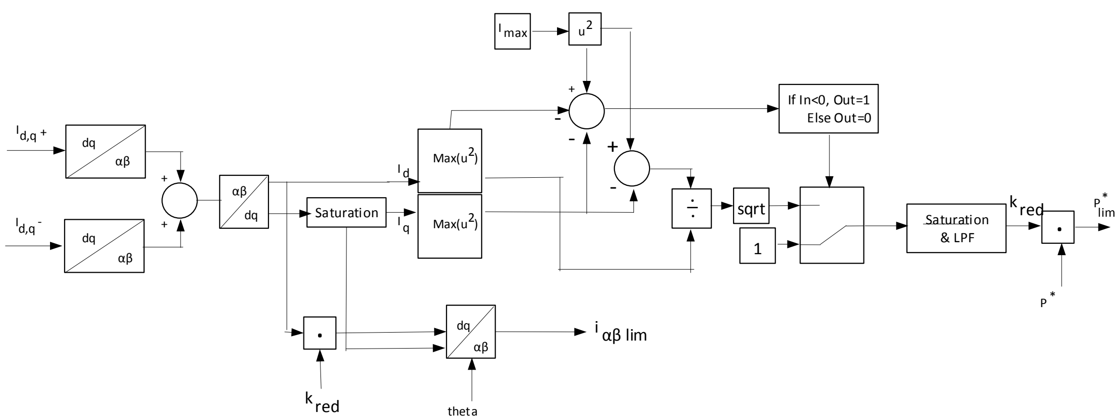


Fig. 20: Current limitation method.

Since the total reference is the result of two rotating references, the resulting dq reference is not a dc value. As it can be derived from [8], the resulting current in αβ is an ellipse, as depicted in:

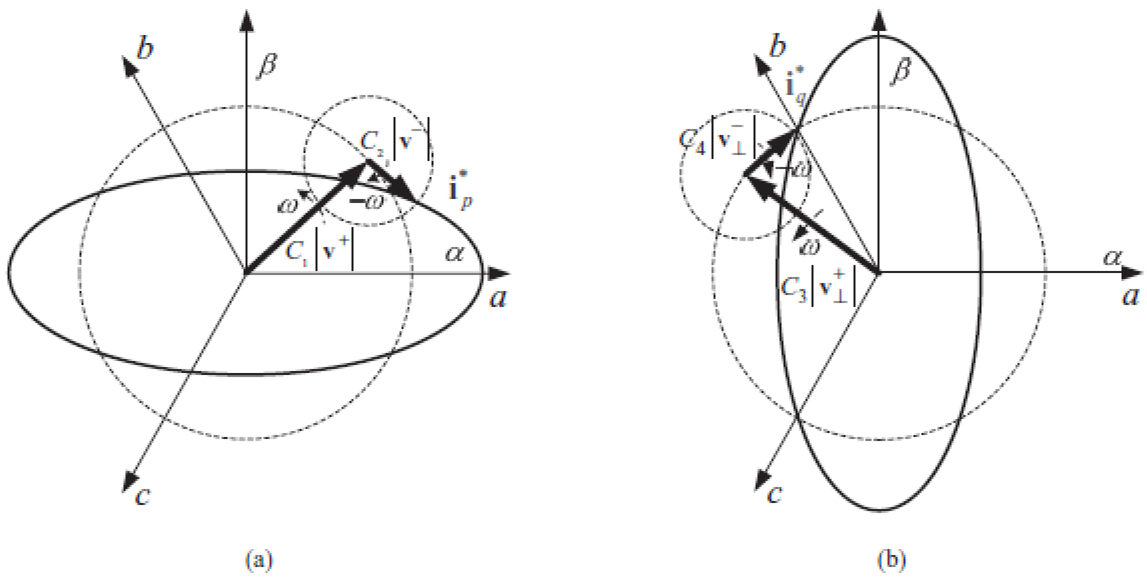


Fig. 21: Ellipse of combined sequence current reference. [8]

So, in dq, the resulted reference is both d and q is a signal with a mean value indicating the positive sequence component and a 2nd harmonic ripple produced by the negative sequence component. For the reactive power injection, in case of excess of the limit, special actions can be taken according to which sequence should have priority (reduction of the mean value would affect the positive sequence injection, whereas reduction of the ripple is related to the negative sequence component).

For the reduction of the active current, the reduction factor is adjusted according to the maximum values of the dq references.

3.5 Simulation Test Results

3.5.1 Injection Strategies test

For comparison between the aforementioned strategies, MMC-HVDC system is simulated in PLECS software. Its characteristics are shown in the following table:

$V_{DC,rated}$	200 kV
$V_{a,LineRMS}$	121.2 kV
f_{grid}	50 Hz
$I_{s,rated}$	700 A
N	100 SMs per arm
PF	0.85
S_{rated}	147 MW
L_{arm}	50 mH

R_{arm}	1 Ω
L_{grid}	21 mH
R_{grid}	13 mH
C_{sm}	4 mF

Table 2: Simulated HVDC parameters.

The controller parameters selected are depicted in

a_f	1000
a_c	4000
a_h	50
a_2	200
R_a	10
a_d	50
a_d	20

Table 3: Controller Parameters.

An asymmetric AC fault occurs at 0.6 [s] with a duration of 0.2 [s]. During this fault, phases B and C voltage falls to 50% of its nominal value.

The response with the conventional method is shown in Fig. 22 and Fig. 23:

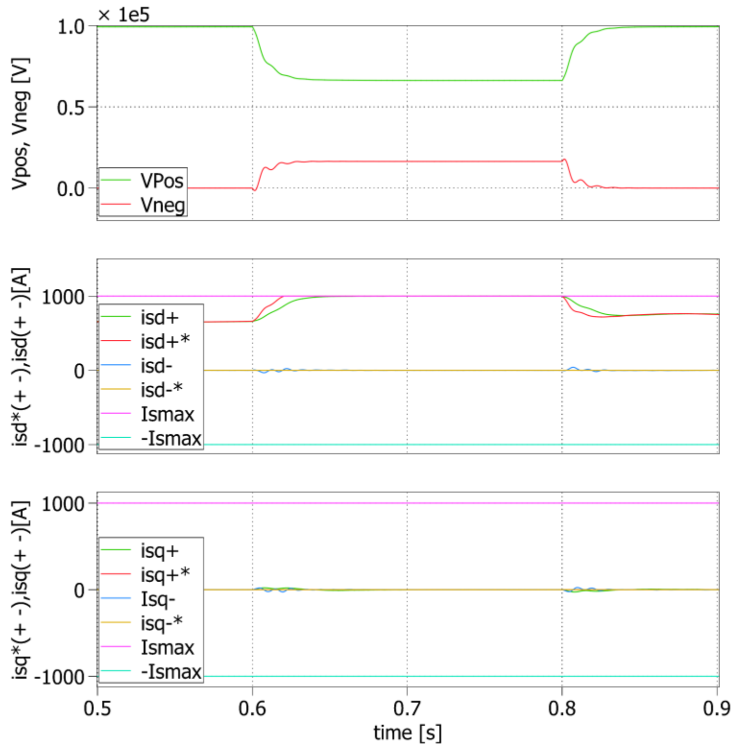


Fig. 22: Results from Conventional Injection. (a) positive and negative sequence voltage components along d-axis. (b) d-axis current components. (c) q-axis current components.

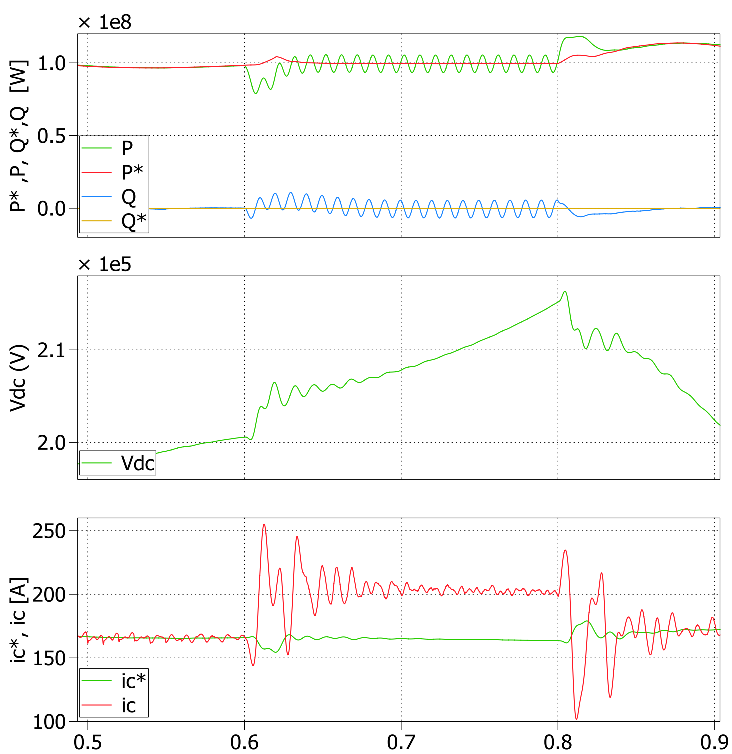


Fig. 23: Results from conventional strategy. (a) Active & reactive power. (b) DC link voltage. (c) Circulating current in phase A.

The response with the PSI strategy is shown in Fig. 24 and Fig. 25:

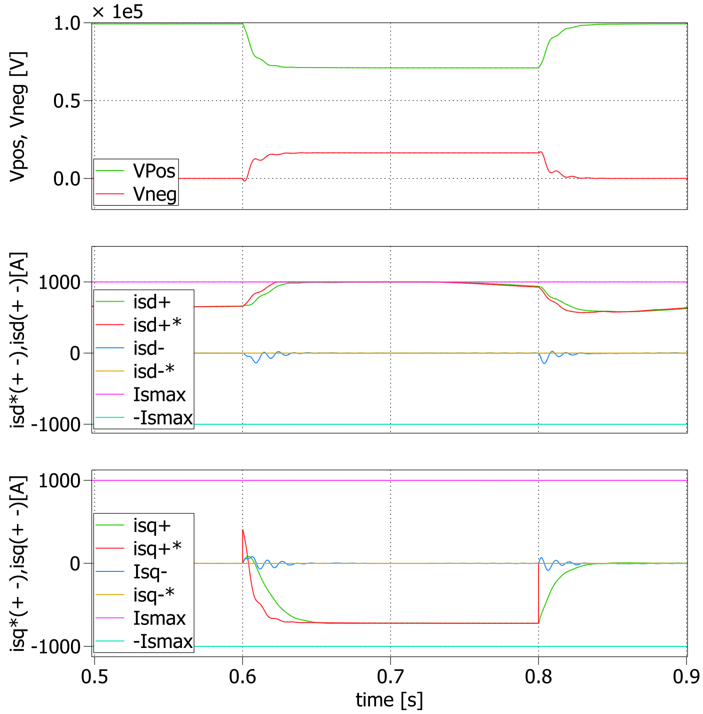


Fig. 24: Results from PSI. (a) positive and negative sequence voltage components along d-axis. (b) d-axis current components. (c) q-axis current components.

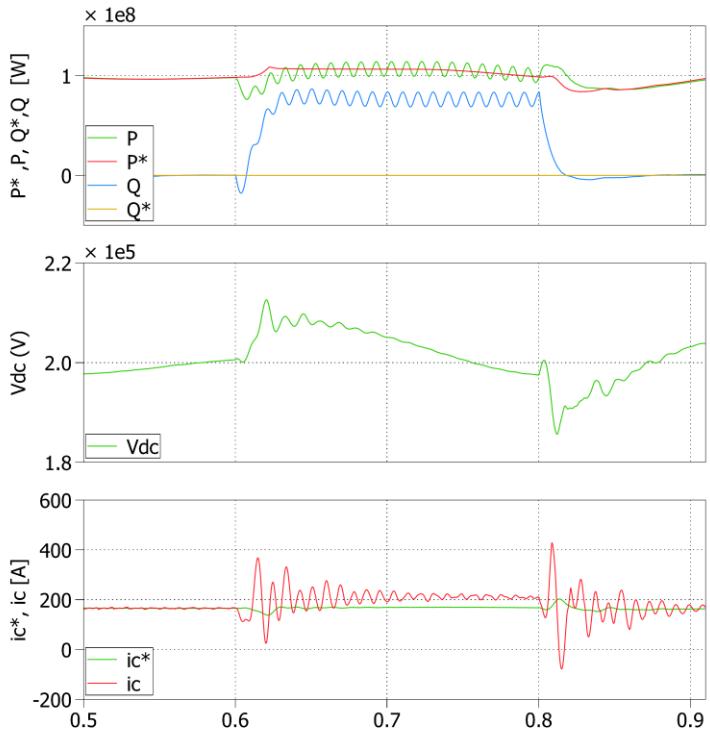


Fig. 25: Results from PSI strategy. (a) Active and reactive power. (b) DC link voltage. (c) circulating current in phase A.

The results from the MSI-BP are shown in Fig. 26 and Fig. 27:

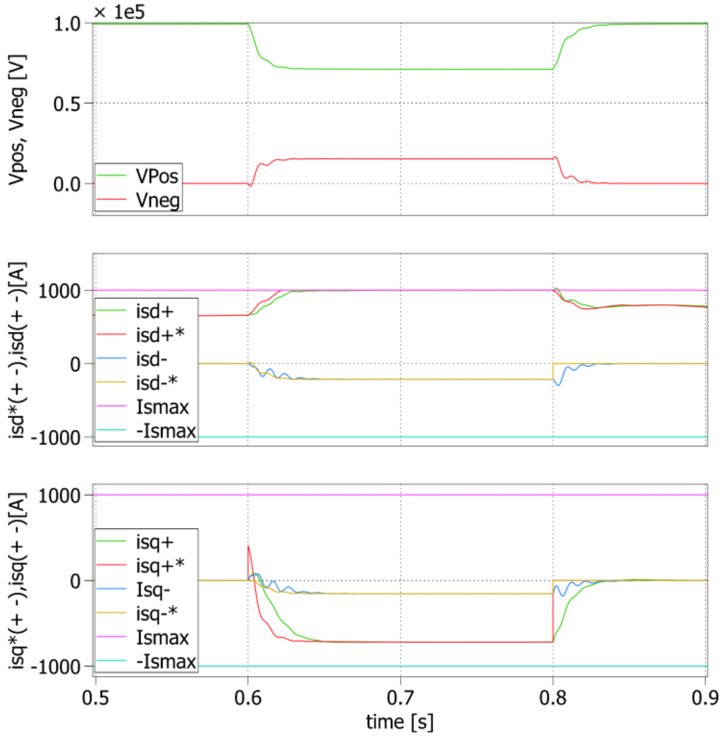


Fig. 26: Results from MSI-BP Injection. (a) positive and negative sequence voltage components along d-axis. (b) d-axis current components. (c) q-axis current components.

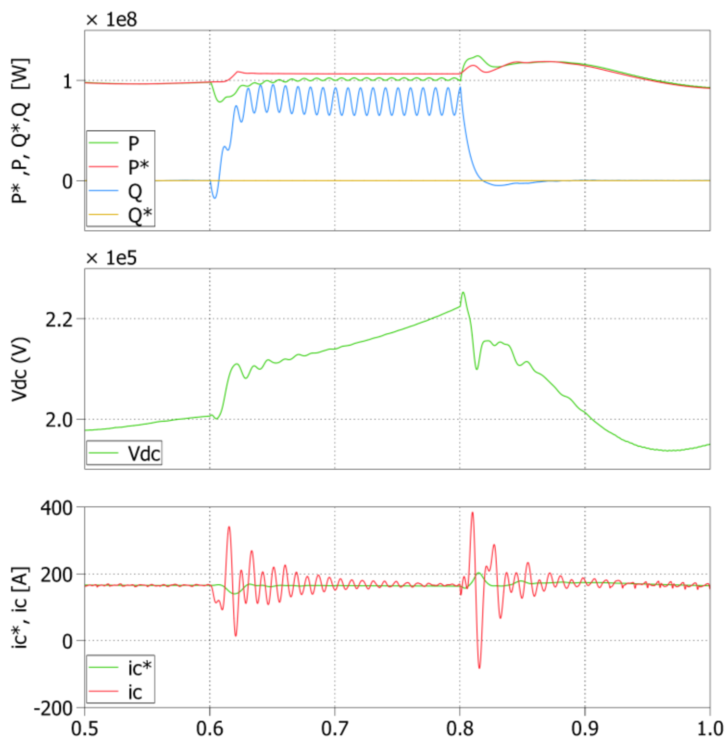


Fig. 27: Results from MSI-BP strategy. (c) Active and reactive power. (b) DC link voltage. (c) circulating current in phase A.

Finally, the results from the MSI-GC, with slope parameters $k_+ = 0.04$ and $k_- = 0.08$, are shown in Fig. 28 and Fig. 29:

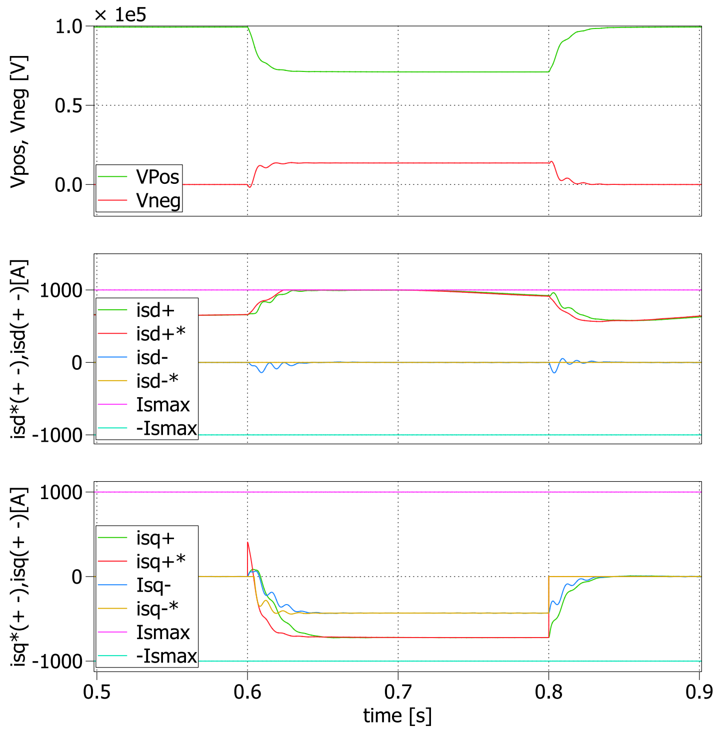


Fig. 28: Results from MSI-GC Injection. (a) positive and negative sequence voltage components along d-axis. (b) d-axis current components. (c) q-axis current components.

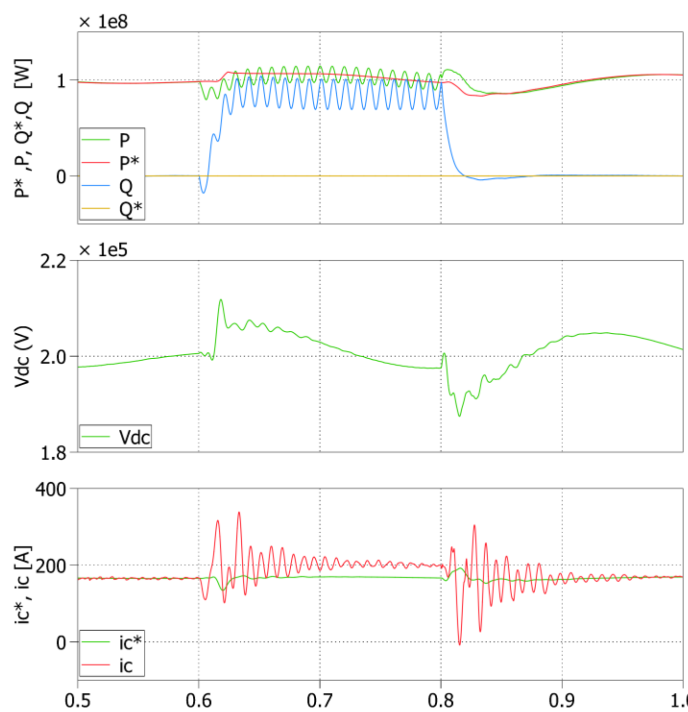


Fig. 29: Results from MSI-GC strategy. (a) Active and reactive power. (b) DC link voltage. (c) circulating current in phase A.

By comparing the results of the three strategies, it can be seen that:

- PSI is able to increase the positive sequence voltage component, whereas the MSI injections are able to decrease the negative sequence voltage component
- MSI-BP strategy, through the negative sequence active current injection, is effective at removing the 100 Hz oscillations in active power, at the exchange of bigger oscillations in reactive power, which is a less undesirable characteristic.
- The MSI-GC strategy shows larger oscillations in both active and reactive power, but it manages to fulfill the grid requirements.
- The circulating current is lower for the MSI-BP strategy and its oscillations appear to be bigger in the MSI-GC.
- In all strategies, during the implementation of the fault, the current increases. This is the result of the voltage decreasing, while the system tries to fulfill the load demand. The injected reactive current is also higher in the MSI-GC injection than that in MSI-BP.

3.5.2 Current limitation test

For the previously simulated scenarios, the current limitation method will be tested with a limit set at 1000 A amplitude.

First, for the PSI method, without the current limitation, the phase voltages and phase currents appear as shown in Fig. 30. The dq currents with their references, active and reactive power and sum capacitor voltages with DC voltage are depicted in Fig. 31.

For the PSI method, with current limitation to 1000 A amplitude, the phase voltages and phase currents appear as shown in Fig. 32. The dq currents with their references, active and reactive power and sum capacitor voltages with DC voltage are depicted in Fig. 33.

For the MSI-BP method, without the current limitation, the phase voltages and phase currents appear as shown in Fig. 34. The dq currents with their references, active and reactive power and sum capacitor voltages with DC voltage are depicted in Fig. 35.

For the MSI-BP method, with current limitation to 1000 A amplitude, the phase voltages and phase currents appear as shown in Fig. 36. The dq currents with their references, active and reactive power and sum capacitor voltages with DC voltage are depicted in Fig. 37.

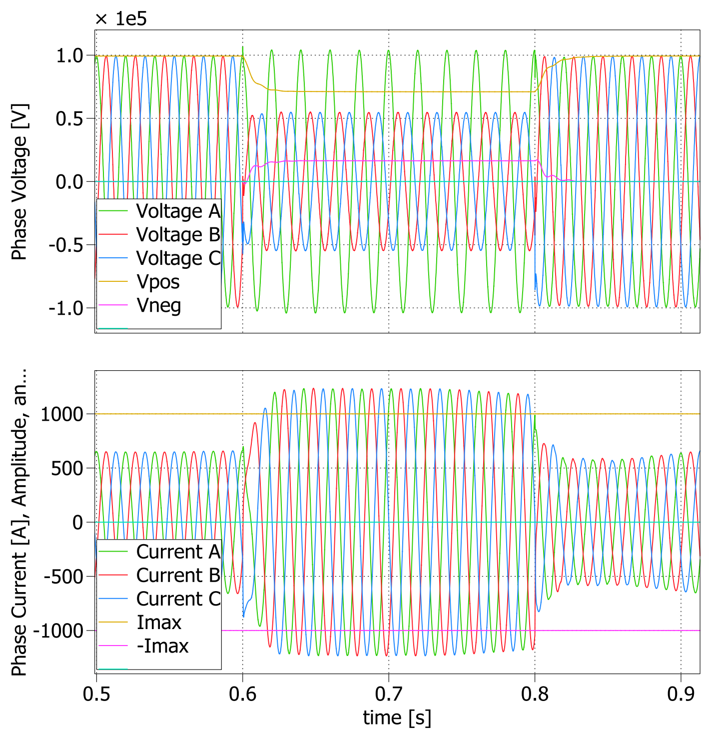


Fig. 30: PSI without Current Limitation.

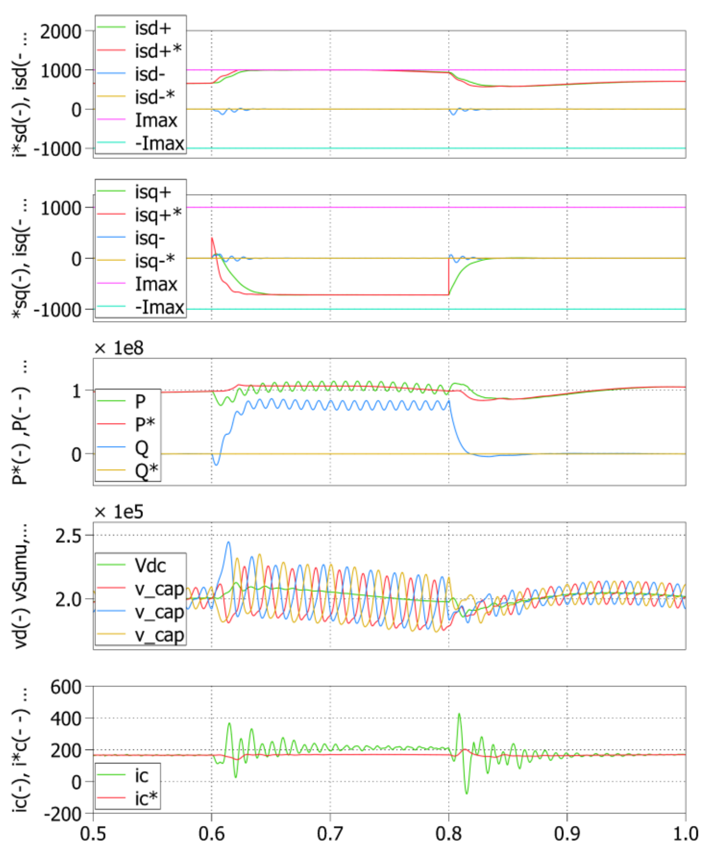


Fig. 31: PSI without current limitation.

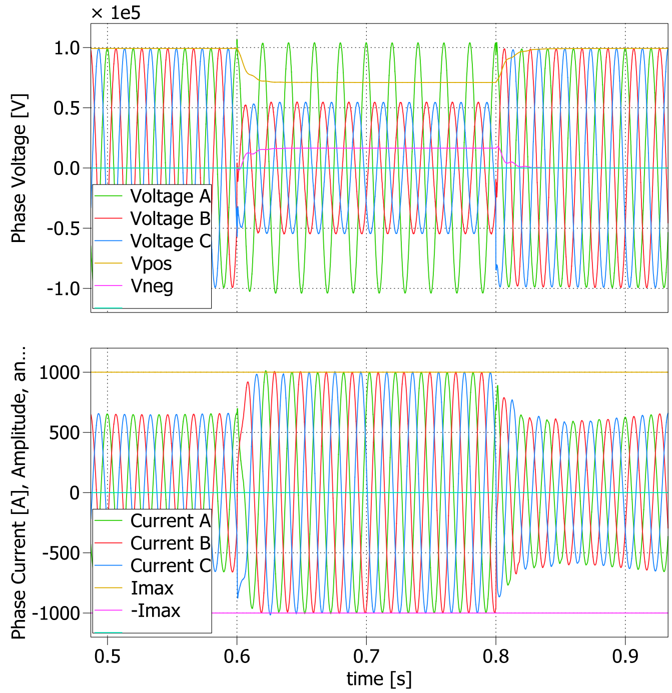


Fig. 32: PSI with current limitation.

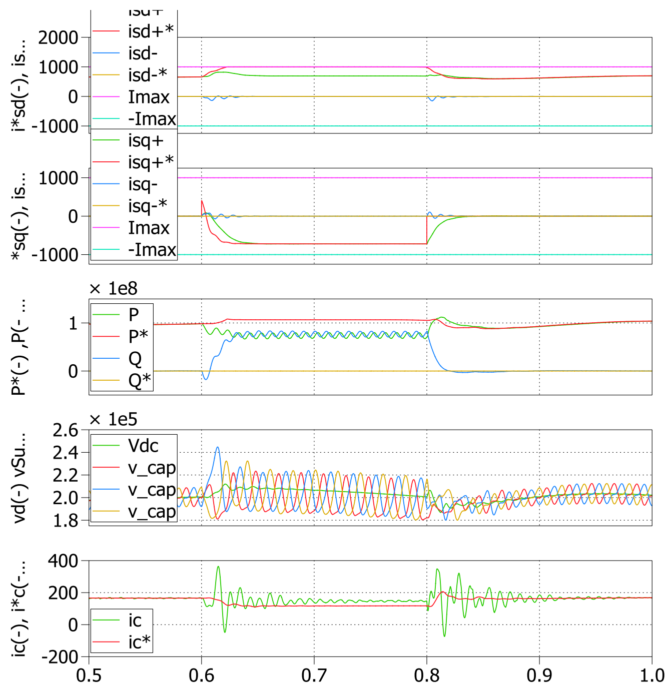


Fig. 33: PSI with Current limitation.

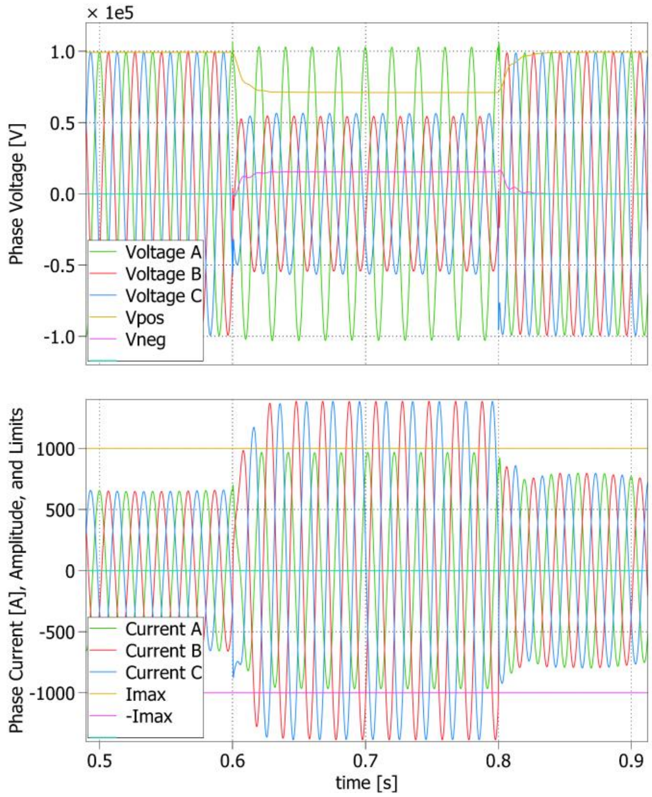


Fig. 34: MSI - BP without Current Limitation.

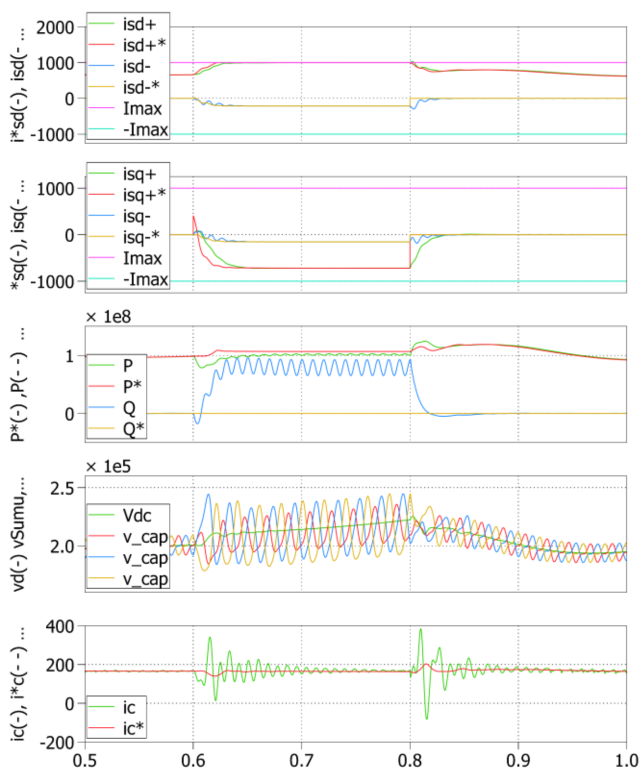


Fig. 35: MSI - BP without Current limitation.

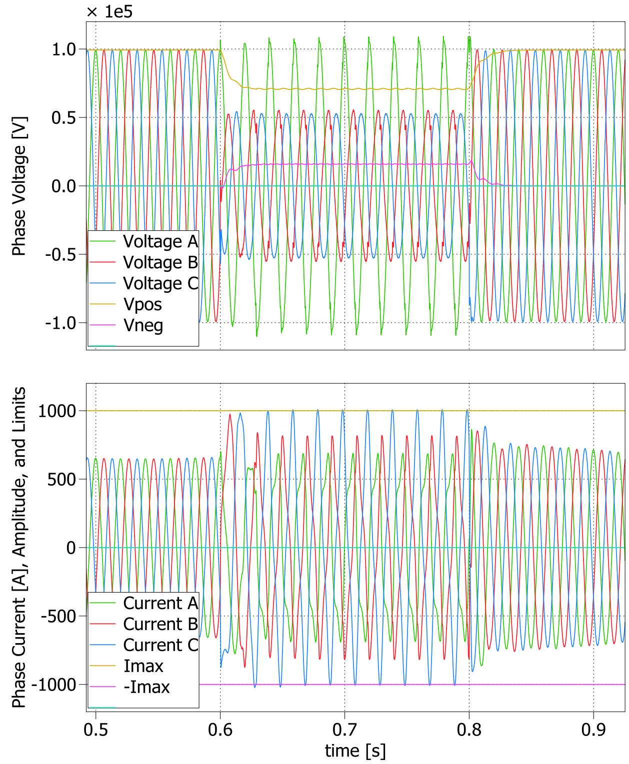


Fig. 36: MSI-BP with current limitation.

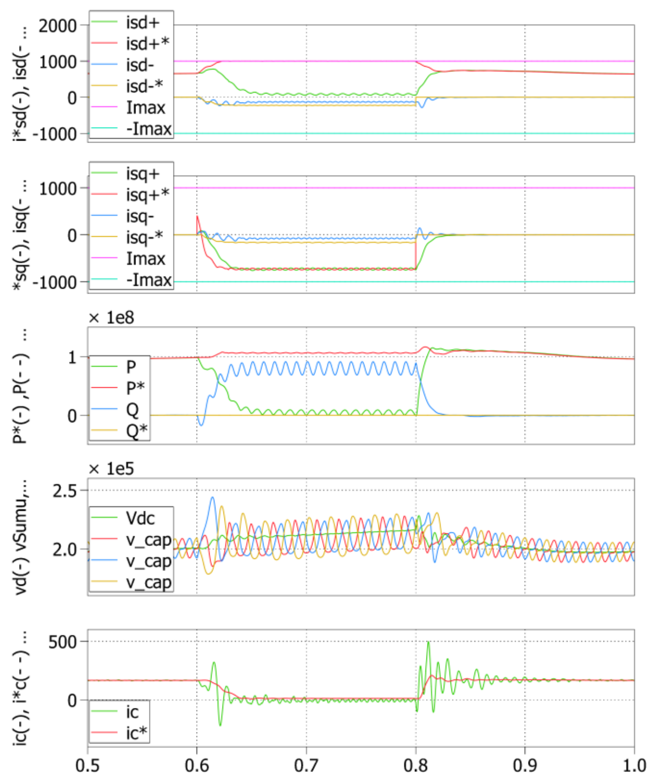


Fig. 37: MSI -BP with Current Limitation.

- It can be seen from Fig. 30 and Fig. 32 that for the PSI, current is limited after an initial period, and the power reference is reduced.
- It can be seen also in Fig. 31 and Fig. 34 that the DC voltage is controlled more effectively.
- It can be seen also that the method injects symmetrical three phase current, as no negative sequence current is injected.
- Finally, it is evident that the method gives priority to the reactive current injection and limits the active current.
- For the MSI – BP, as depicted in Fig. 34 and Fig. 36 the method is also able to reduce the phase current amplitude to the nominal value or below, with priority given to the reactive current injection.
- In this strategy it can be seen that the injection is not symmetrical, due to the negative sequence component injection.
- It can be seen also in Fig. 35 and Fig. 37 that the active power now has more oscillations, as the method reduces also the negative sequence active current injection that was supposed to remove the oscillations.

4 Experimental Results

4.1 Description of the Setup used

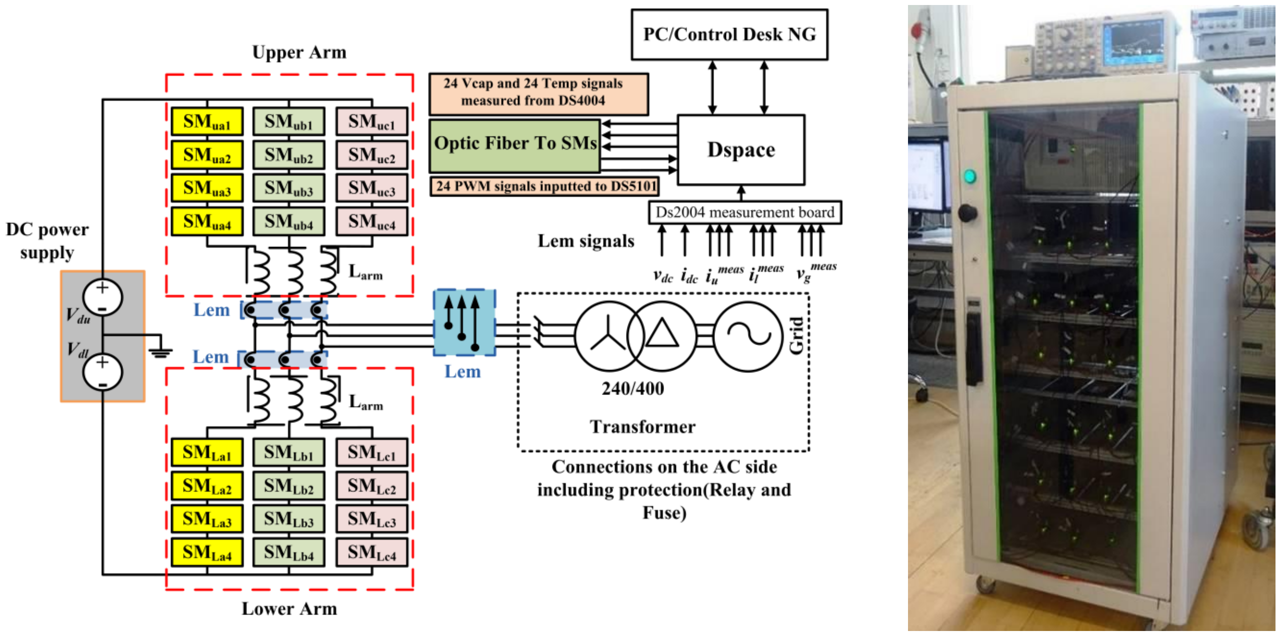


Fig. 38: Schematic and physical of the Hardware Setup and the Control System. [5]

The experimental verification of the aforementioned theoretical results, was done with the help of a prototype MMC. In

Fig. 38, the MMC system configuration and the control system is depicted.

The MMC consists of 3 phases, with 4 SMs per arm, connected as half bridge. The connection to the grid is achieved via a Δ-Y transformer. Measurements of the phase current and voltage are achieved through LEM Boxes and sent to the dSPACE. Other measurements, as the capacitor voltages or temperature are measured on the PCBs of the SMs and sent through optic fibers to the dSPACE, and dSPACE sends switching signals and resetting signals to the SMs. The interface between the user and the setup is achieved with the ControlDesk software.

The pole to pole DC rated voltage is equal to 400 V. However, due to reasons of EMI, the setup is operated with 80 V DC. The modulation technique used in the current project was the Nearest Level Control (NLC).

The parameters of the setup are given to the Table:

Table 4: Parameters for Experimental Setup

Rated Active Power (P(kW))	2.6
SMs/arm	4
DC Rated Voltage(V)	400
SM Capacitance (C_{SM}(mF))	3.6
Arm Inductance (L_{arm}(mH))	20
Grid Voltage Amplitude($V_g(V)$)	200
Grid Frequency (Hz)	50
Rated Current (I_{max}(A))	6.4

4.2 Experimental results

The setup is tested in inverting mode. A DC Voltage Supply is adjusted to 80 V at the DC side, whereas an AC Source is providing 40 V amplitude on the AC side, in the steady state operation.

4.2.1 Arm Balancing Control

The first control strategy to be tested, is the arm balancing control. The response of the system is depicted in Fig. 39.

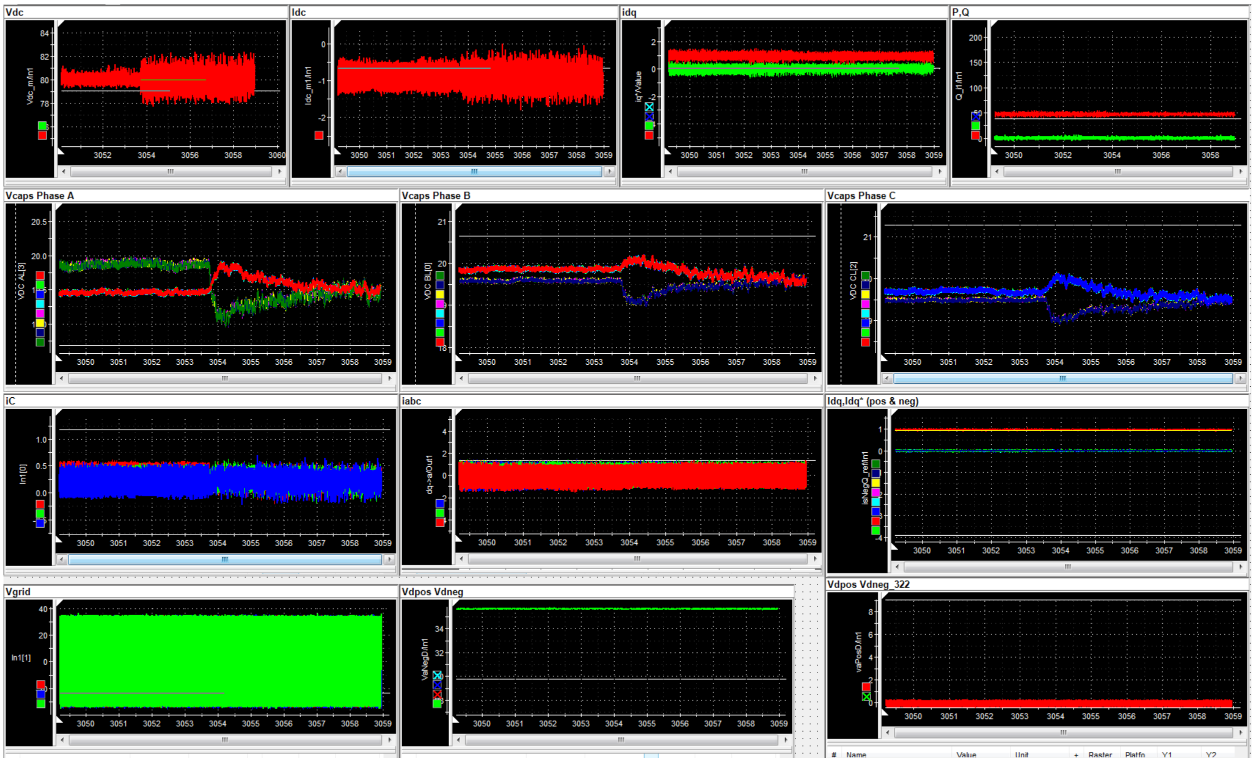
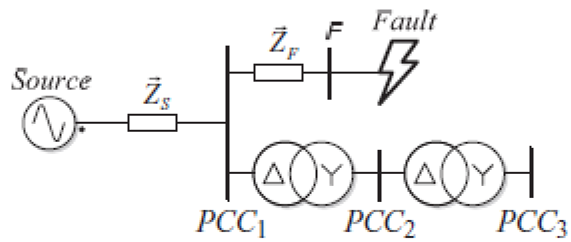


Fig. 39: Arm Balancing Control. The Capacitor Voltages for each phase are depicted in the graphs of the second row ("Vcaps Phase A", "Vcaps Phase B" and "Vcaps Phase C"). The DC Voltage is depicted in the graph "Vdc" (upper left corner). The time scale is in seconds.

Initially, the Vertical Balancing control is disabled. As it can be seen in the three graphs ("Vcaps Phase A", "Vcaps Phase B" and "Vcaps Phase C"), the upper and lower arms initially are not balanced. When the Circulating Current Control is implemented, after an initial overshoot the arm voltages converge to the same value. It can be seen that the Arm Balancing Control does not have fast response, and comes at the expense of a higher oscillation of the DC voltage (Graph Vdc)

4.2.2 Fault Implementation and Injection Strategies Testing

For the verification of the Injection Strategies, the fault scenario tested is a two phase voltage drop. However, the existence of the Δ-Y transformer, changes the type of fault that has to be implemented in order to receive the desired fault case, as it is explained in Fig. 40 [8]:



Fault type	Point of common coupling		
	PCC_1	PCC_2	PCC_3
Three-phase/three-phase to ground	A	A	A
Single-phase to ground	B	C	D
Two-phase	C	D	C
Two-phase to ground	E	F	G

Fig. 40: Propagation of voltage sags due to Δ-Y transformers.[8]

As it can be seen, in order to receive a two phase voltage sag fault (type C fault) in the secondary of the transformer, a one phase voltage sag fault has to be implemented on the primary (type B fault). For that reason, phase C of the AC source is set to 20 V. Furthermore, an active power reference of 50 W is inserted.

For better depiction of the effect of the fault and the injection strategies, the faults implemented have a high time duration. All injection strategies have been shown both in a non-fault to fault and back to non-fault condition (NF to F to NF), and in a permanent fault situation, for depiction of their characteristics and their contribution to the LVRT.

4.2.2.1 *Conventional Method testing*

First, the Conventional Injection Strategy is implemented. The NF to F to NF test is depicted in Fig. 41, and the zoomed depiction under permanent fault is in Fig. 42.

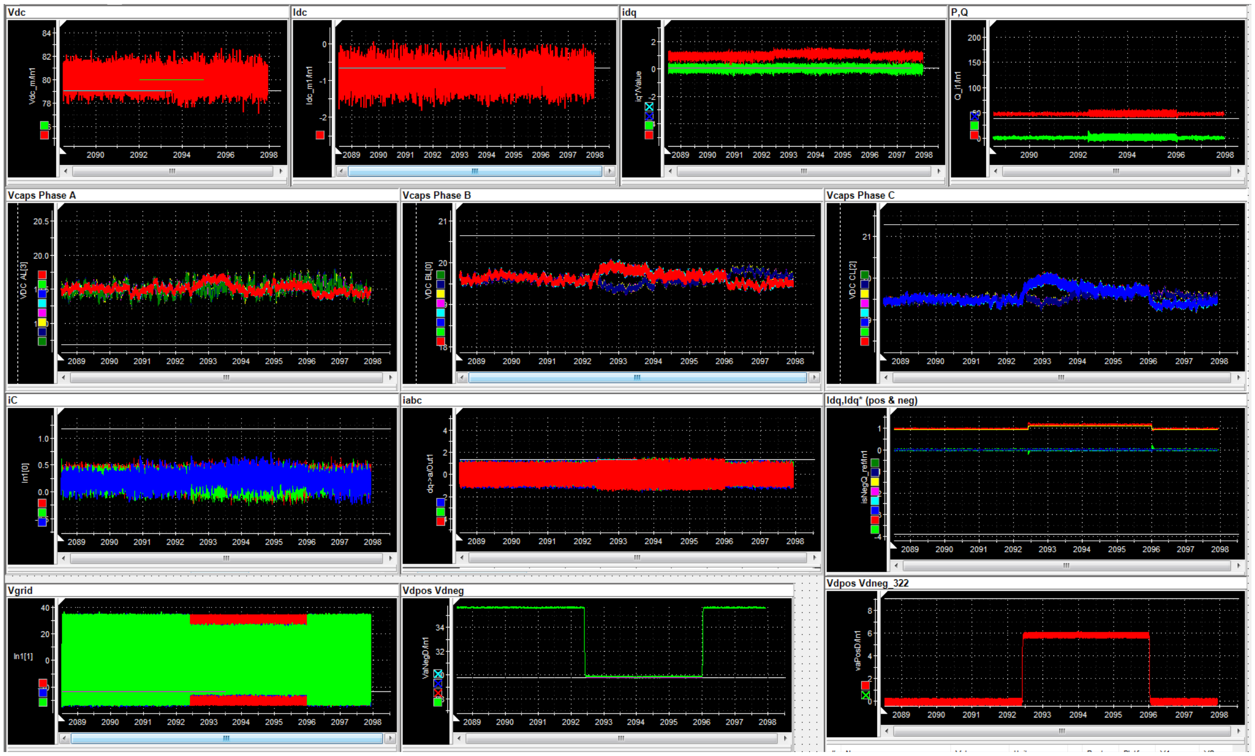


Fig. 41: NF to F to NF for Conventional Strategy: a) P and Q are shown in "PQ" graph (red: P, green: Q), b) id+, iq+, id-, iq- are shown in "Idq,Idq* (pos and neg)" graph (red: id+, cyan: iq+, green: id-, blue: iq-, rest: references), c) V positive is shown with green in "Vdpos Vdneg" graph and d) V negative is shown in "Vdpos Vdneg_322" graph.

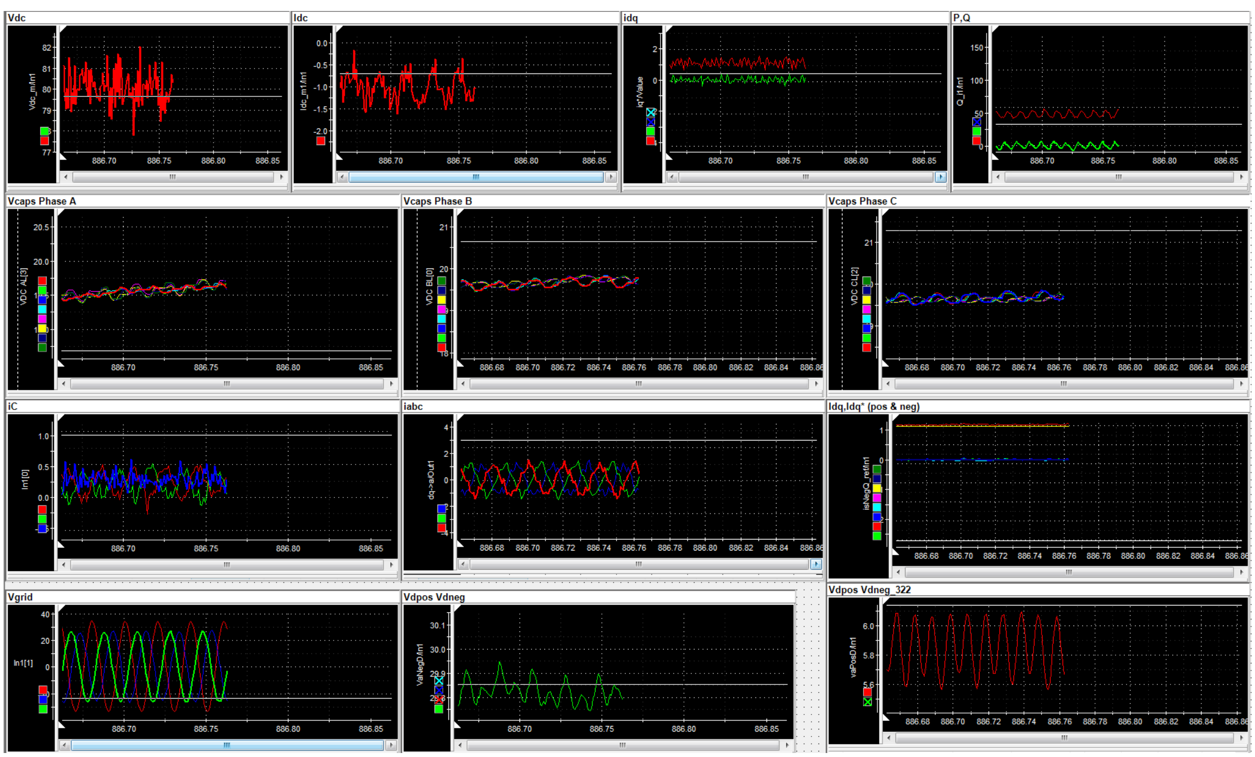


Fig. 42: Zoomed conventional strategy under permanent fault.

From the 2 figures, it can be derived that:

- During the fault, the V_+ component falls from a pre-fault value of 35.5 V to a fault value of approximately 29.8 V (16% drop or 84% of the initial value).(“Vdpos Vdneg” graph)
- The V_- component rises from 0 to 5.9 V (16% of the initial V_+ value).(“Vdpos Vdneg_322” graph)
- Ripple in P and Q increases. (“PQ” graph)
- Active current injection increases, because it is set to deliver the same amount of P with lower value of V. (“Idq,Idq* (pos and neg)” graph)
- Arm Balancing Control achieves to balance again the arm capacitor voltages of the same phase during fault, but its dynamics are slow.
- Capacitor voltages rise, but remain below a 10% of their previous operating condition, so within their tolerance.

4.2.2.2 *PSI testing*

As a second strategy, the PSI is implemented. The NF to F to NF test is depicted in Fig. 43, and the zoomed depiction under permanent fault is in Fig. 44.

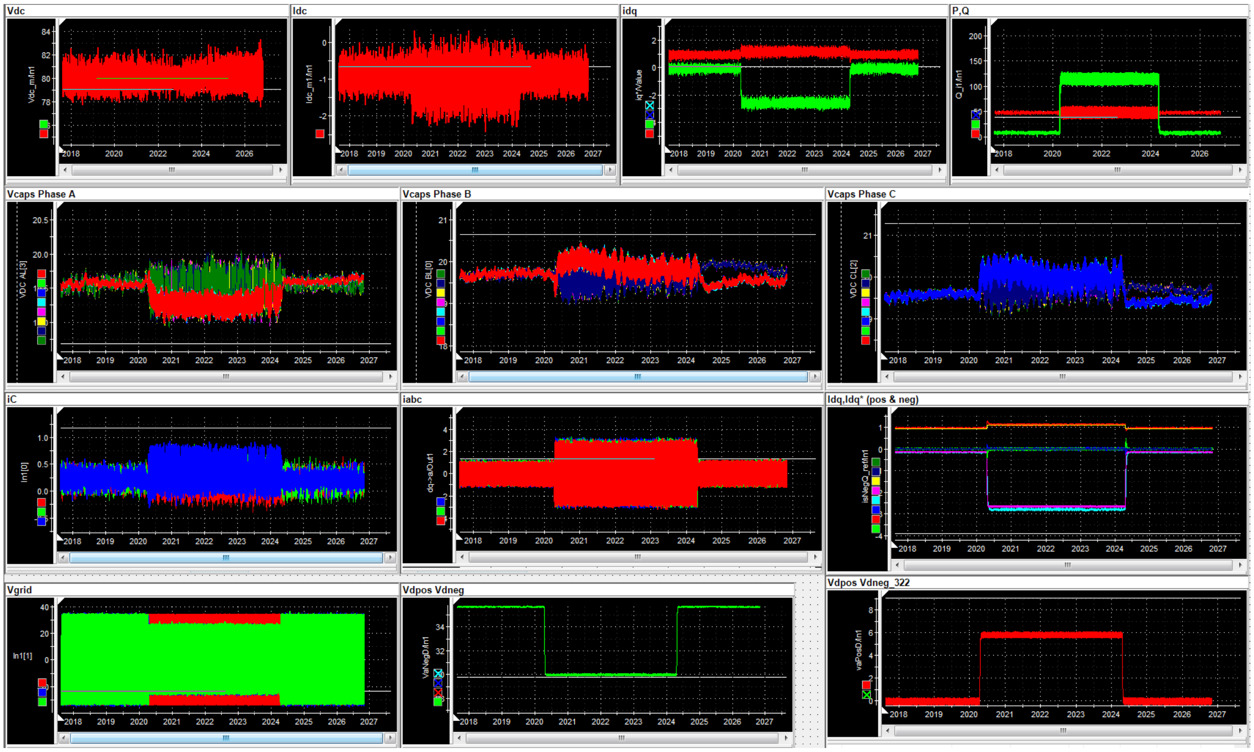


Fig. 43: NF to F to NF test for PSI: a) P and Q are shown in "PQ" graph (red: P, green: Q), b) id+, iq+, id-, iq- are shown in "Idq,Idq* (pos and neg)" graph (red: id+, cyan: iq+, green: id-, blue: iq-, rest: references), c) V positive is shown with green in "Vdpos Vdneg" graph and d) V negative is shown in "Vdpos Vdneg_322" graph.

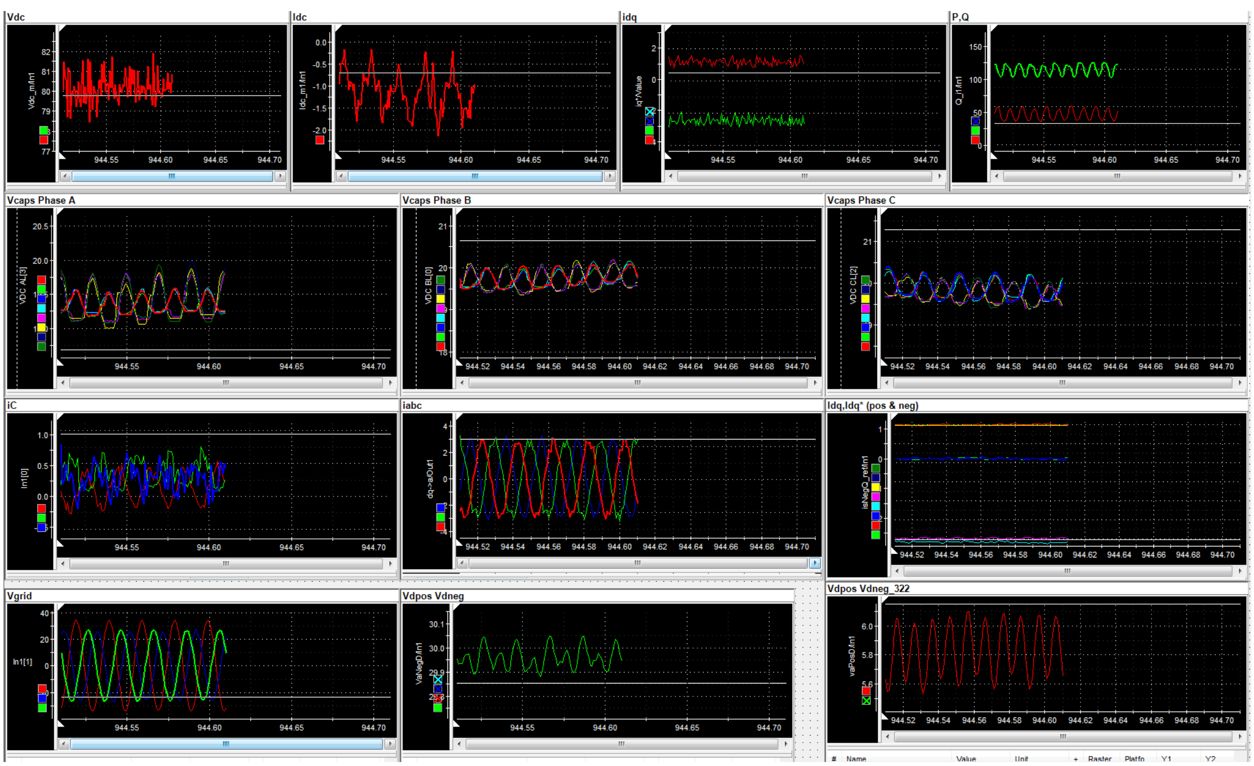


Fig. 44: Zoomed PSI strategy under permanent fault.

From the 2 graphs and comparing to the conventional method, it can be derived that:

- The PSI shows higher ripple in P and Q than the conventional method.
- The V_+ value falls to 30 V from 35.5 pre-fault, showing a reduction of 15.5% or a 0.5% improvement compared to the conventional method.
- Phase current is 100% higher than the conventional method (3 A amplitude in PSI, 1.5 A in conventional).
- Higher ripple in the circulating current. ("Ic graph")
- Lower Vdc ripple.
- Capacitor voltages rise, but remain below a 10% of their previous operating condition, so within their tolerance.

4.2.2.3 *MSI -BP testing*

As next strategy, MSI – BP is tested. The NF to F to NF test is depicted in Fig. 45, and the zoomed depiction under permanent fault is in Fig. 46.

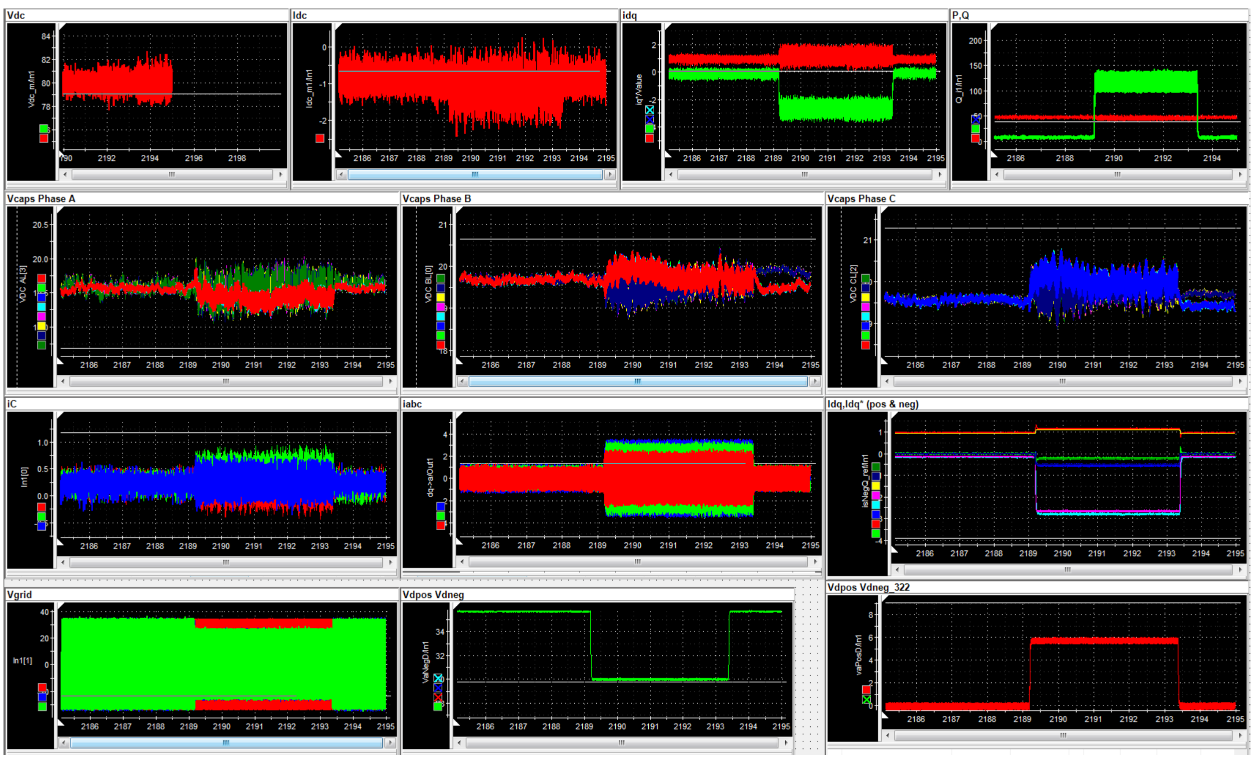


Fig. 45: NF to F to NF test for MSI - BP: a) P and Q are shown in "PQ" graph (red: P, green: Q), b) id+, iq+, id-, iq- are shown in "Idq,Idq* (pos and neg)" graph (red: id+, cyan: iq+, green: id-, blue: iq-, rest: references), c) V positive is shown with green in "Vdpos Vdneg" graph and d) V negative is shown in "Vdpos Vdneg_322" graph.

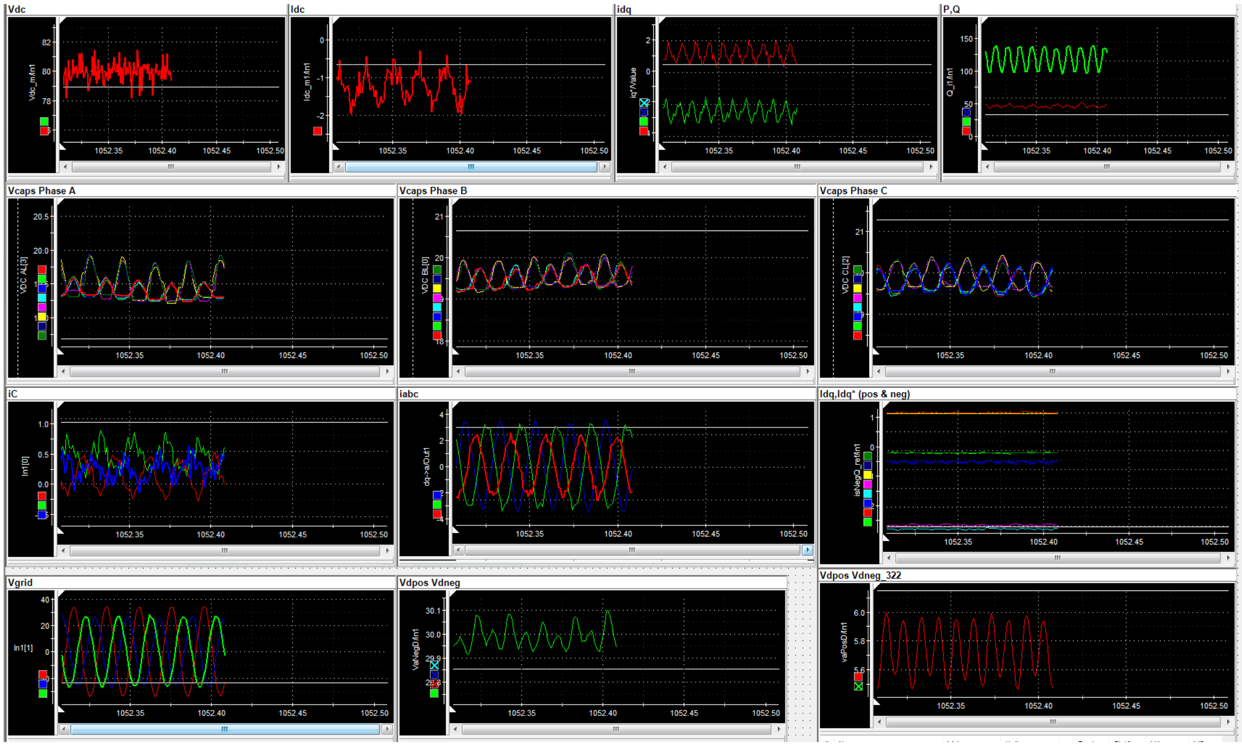


Fig. 46: Zoomed MSI - BP strategy under permanent fault.

From the 2 graphs and comparing to the conventional and PSI method, it can be derived that:

- The MSI - BP shows the lowest ripple in P, but the highest in Q.
- The V_- value increases to 5.7 V from 0 pre-fault, showing a reduction of 3.4% compared to the conventional method.
- Phase current is asymmetrical (due to the negative sequence injection)
- Higher ripple in the circulating current than the conventional method.
- Capacitor voltages rise, but remain below a 10% of their previous operating condition, so within their tolerance.

4.2.2.4 *MSI – GC testing*

As final strategy, MSI – GC is tested. The NF to F to NF test is depicted in Fig. 47, and the zoomed depiction under permanent fault is in Fig. 48.

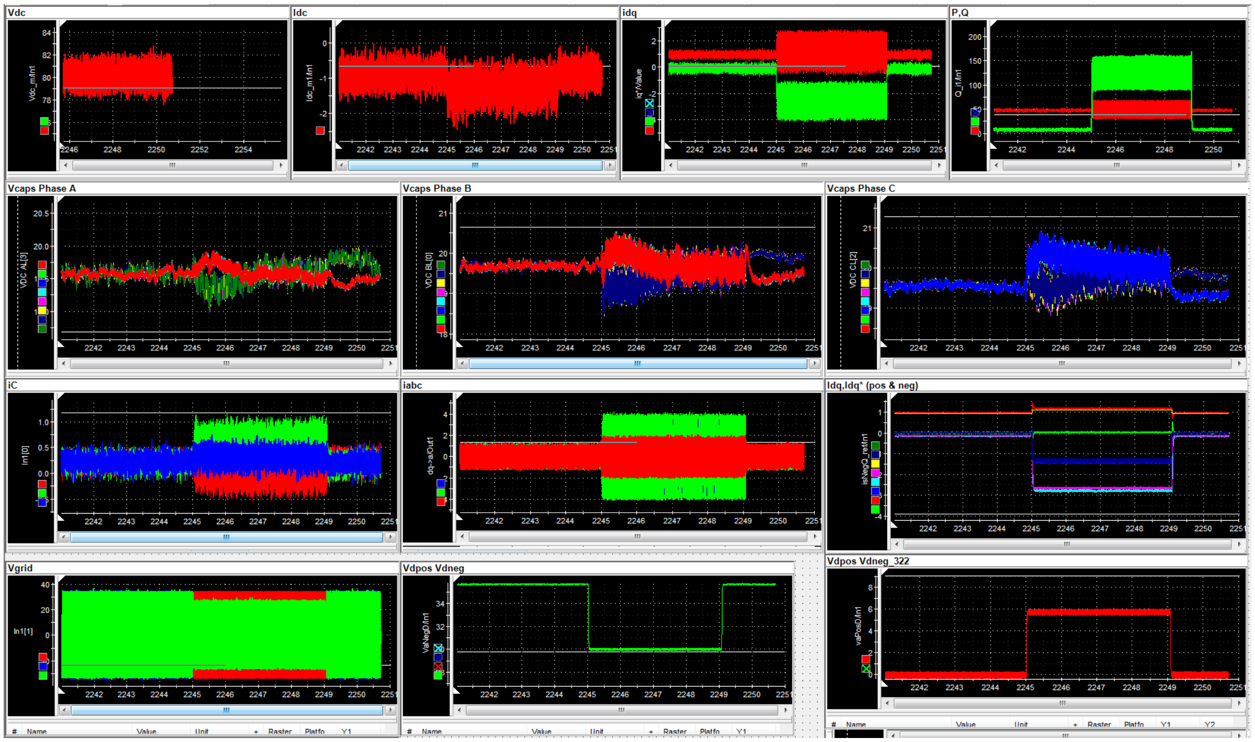


Fig. 47: NF to F to NF test for MSI - GC: a) P and Q are shown in “PQ” graph (red: P, green: Q), b) id+, iq+, id-, iq- are shown in “Idq,Idq* (pos and neg)” graph (red: id+, cyan: iq+, green: id-, blue: iq-, rest: references), c) V positive is shown with green in “Vdpos Vdneg” graph and d) V negative is shown in “Vdpos Vdneg_322” graph.

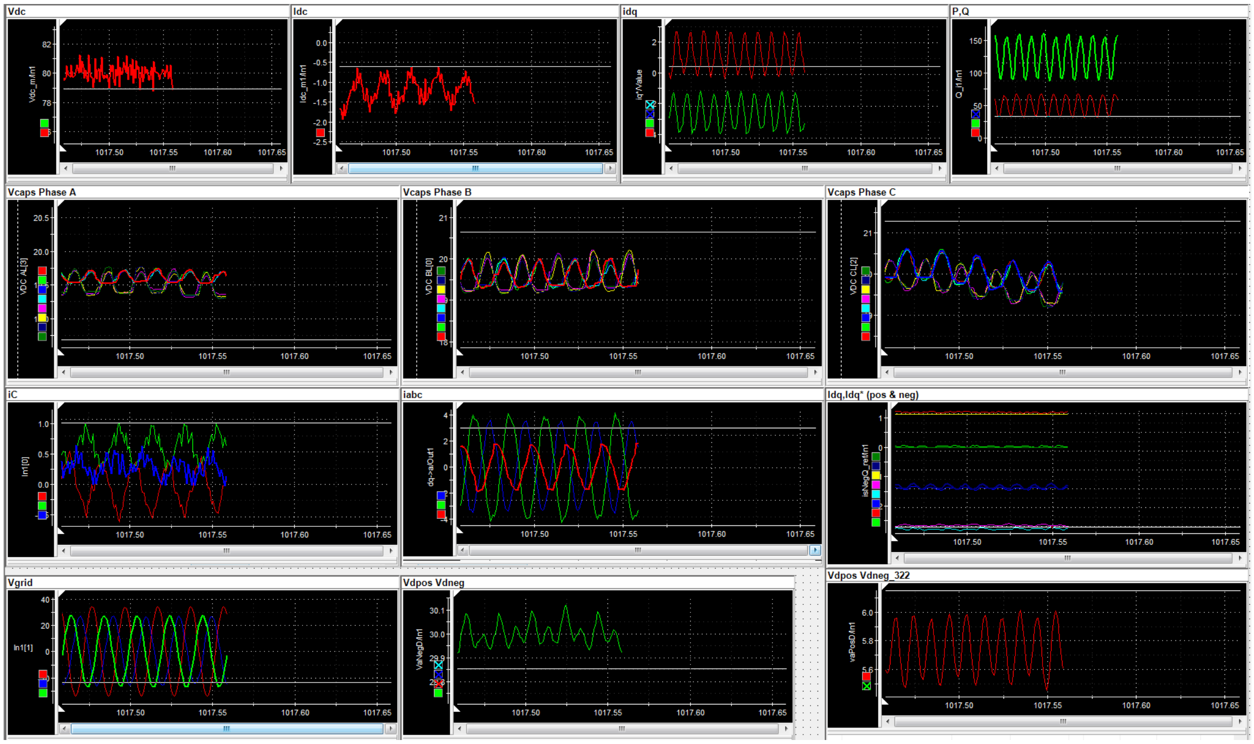


Fig. 48: Zoomed MSI - GC strategy under permanent fault.

From the 2 graphs and comparing to the conventional, the PSI and the MSI – BP method, it can be derived that:

- The MSI - BP shows the highest ripple of all injection strategies.
- The V_- value increases to 5.7 V from 0 pre-fault, showing a reduction of 3.4% compared to the conventional method.
- Phase current is asymmetrical and higher than in the rest of the methods.
- Higher ripple in the circulating current than the conventional method.
- Capacitor voltages rise, but remain below a 10% of their previous operating condition, so within their tolerance. However, the method seems to add to the capacitor voltage ripple (due to the high current.

For all strategies aforementioned, it is noted that the support of the positive sequence component and the reduction of the negative sequence component, seem to be not really significant. However, it must be taken into account that the AC source used in the lab can be considered to act as a strong grid, and the transformer inductance is much lower than the arm inductances. Given the fact that the measurements for the voltage are taken in the secondary of the transformer, but before the arm inductances of the MMC, the voltage drop or rise caused by the injected current cannot be high. Also, the k_+ and k_- slope factors that were used, were chosen to be lower than the usual values, so as to better depict the characteristics of the strategies and the current limitation.

4.3 Current Limitation Testing

The rated phase current of the MMC is set at 6.5 A amplitude. Since it is not safe to operate over this value, the current limitation testing will be done by setting a new limit value at 5.5 A amplitude. Before the implementation of the proposed method, the limitation of the current was implemented by a saturation block in the built model at the total current reference. This type of limitation does not give the desired priority to the reactive current, as it was discussed previously. The new limitation is implemented in the way that it was analyzed in the respective chapter.

The testing is done under permanent fault, with two ways of depiction: one with transition from the conventional limitation to the proposed one and back (Con to Prop to Con), and one zoomed to the characteristics of the method itself. It was done for all three types of injection strategies, but with more severe faults than the previous cases (Phase to ground fault for PSI, Phase sag from 40 V to 5 V for MSI BP and Phase sag from 40 V to 8 V for MSI GC) in order to create higher current references.

It has to be mentioned that due to computational complexity, the arm balance control had to be disabled.

4.3.1 Current limitation testing under PSI

The initial testing will be for the PSI method. C phase on the primary of the transformer is set to 0. Con to Prop to Con appears in Fig. 49, and Zoomed version in Fig. 50:

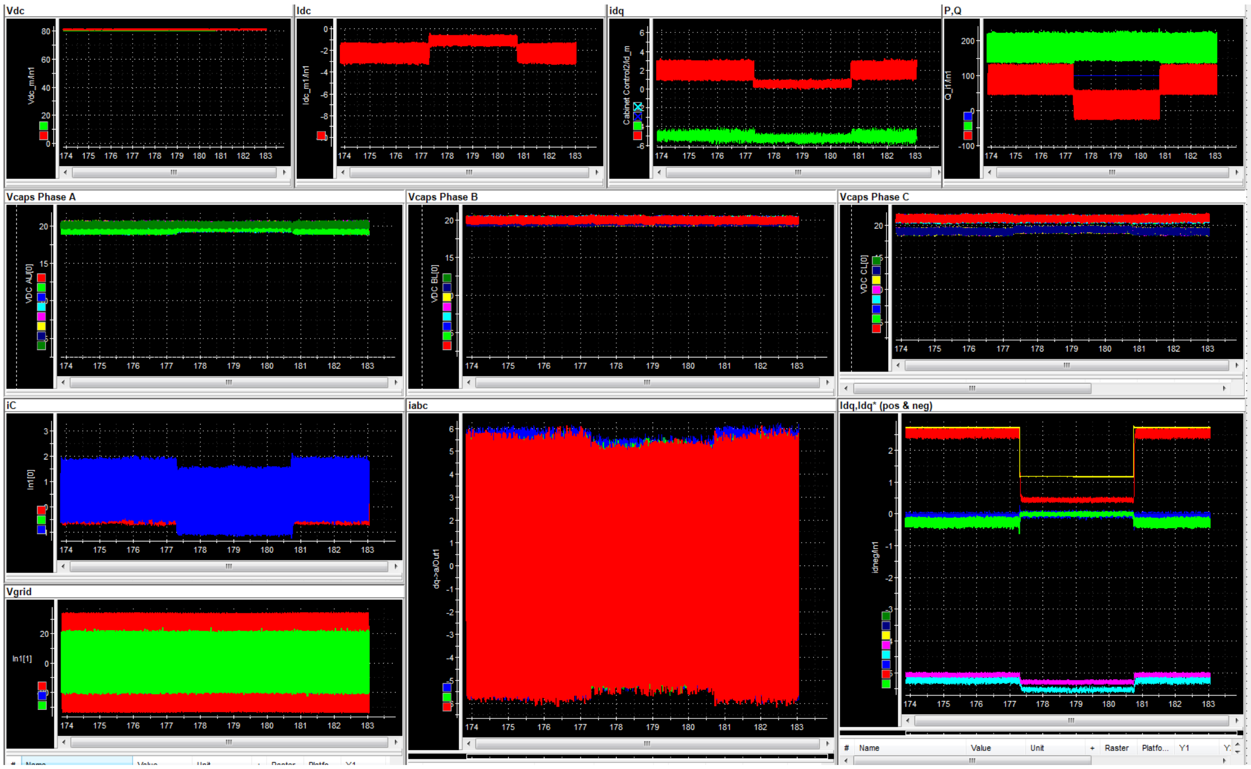


Fig. 49: Conventional to Proposed to Conventional Current Limitation Method with PSI injection: a) Phase Currents shown in "Iabc" graph, b) id+, iq+, id-, iq- are shown in "Idq,Idq* (pos and neg)" graph (red: id+, cyan: iq+, green: id-, blue: iq-, rest: references)

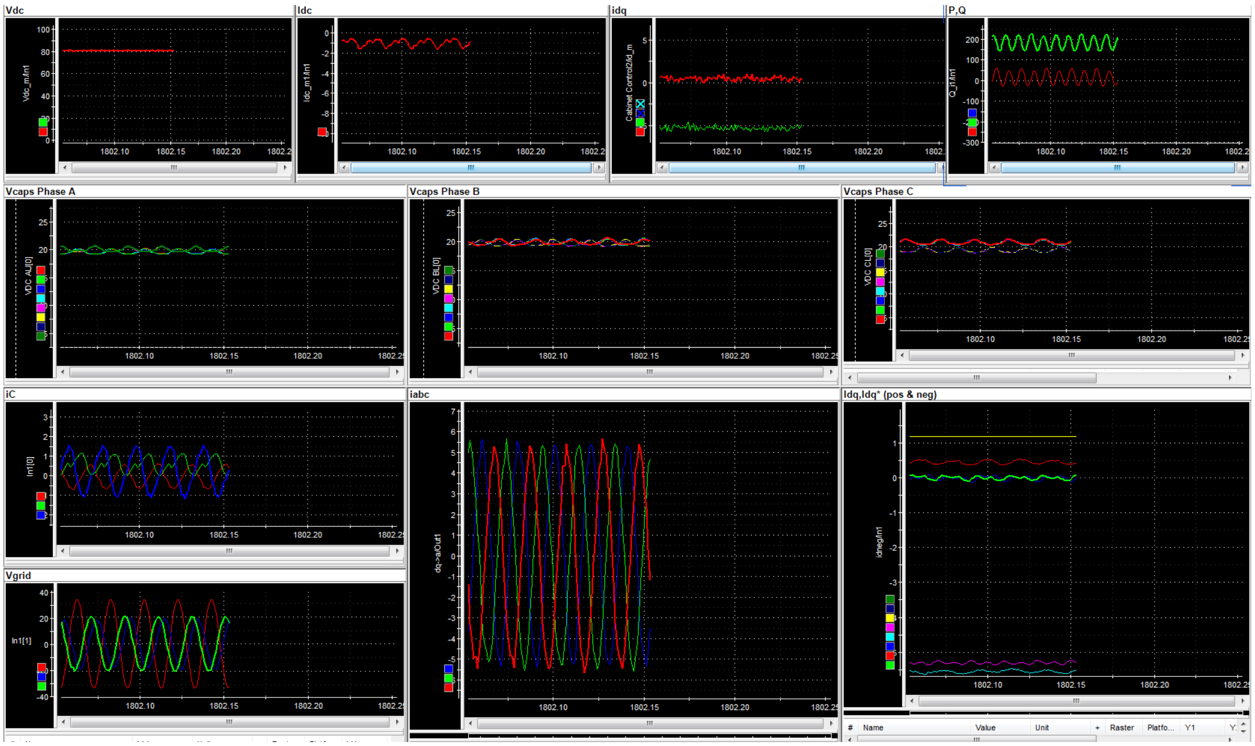


Fig. 50: Zoomed version of the Proposed Current Limitation Method under PSI.

It can be seen that the phase currents are successfully limited to 5.5 A amplitude, from 6 A that they were previously, and that only the active current injection becomes lower (the reactive current injection becomes slightly higher due to the fact that the positive sequence voltage component reduces slightly also).

4.3.2 Current Limitation Testing under MSI BP

For the test for the MSI BP, C phase Voltage on the primary of the transformer is set to 5. The test from conventional method to proposed and back to conventional is depicted in Fig. 51 and the zoomed version in Fig. 52:

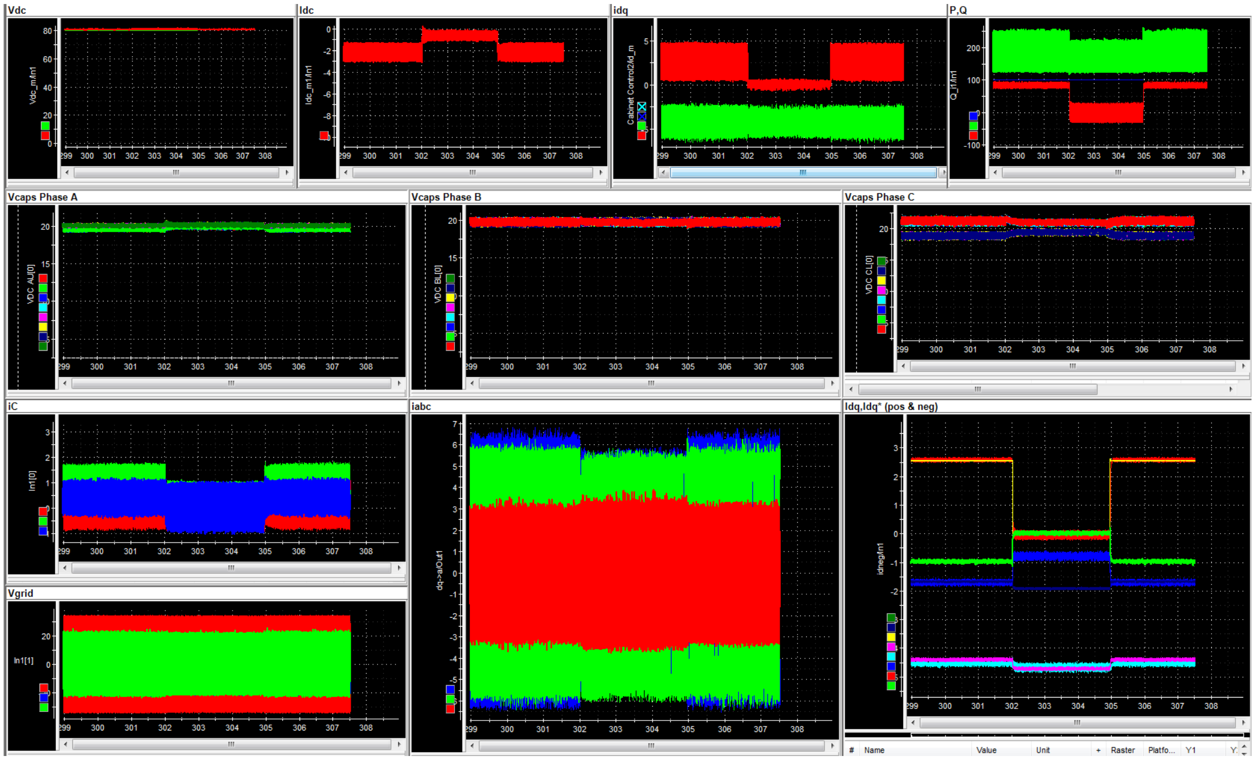


Fig. 51: Conventional to Proposed to Conventional Current Limitation Method with MSI BP injection: a) Phase Currents shown in "Iabc" graph, b) id+, iq+, id-, iq- are shown in "Idq,Idq* (pos and neg)" graph (red: id+, cyan: iq+, green: id-, blue: iq-, rest: references)

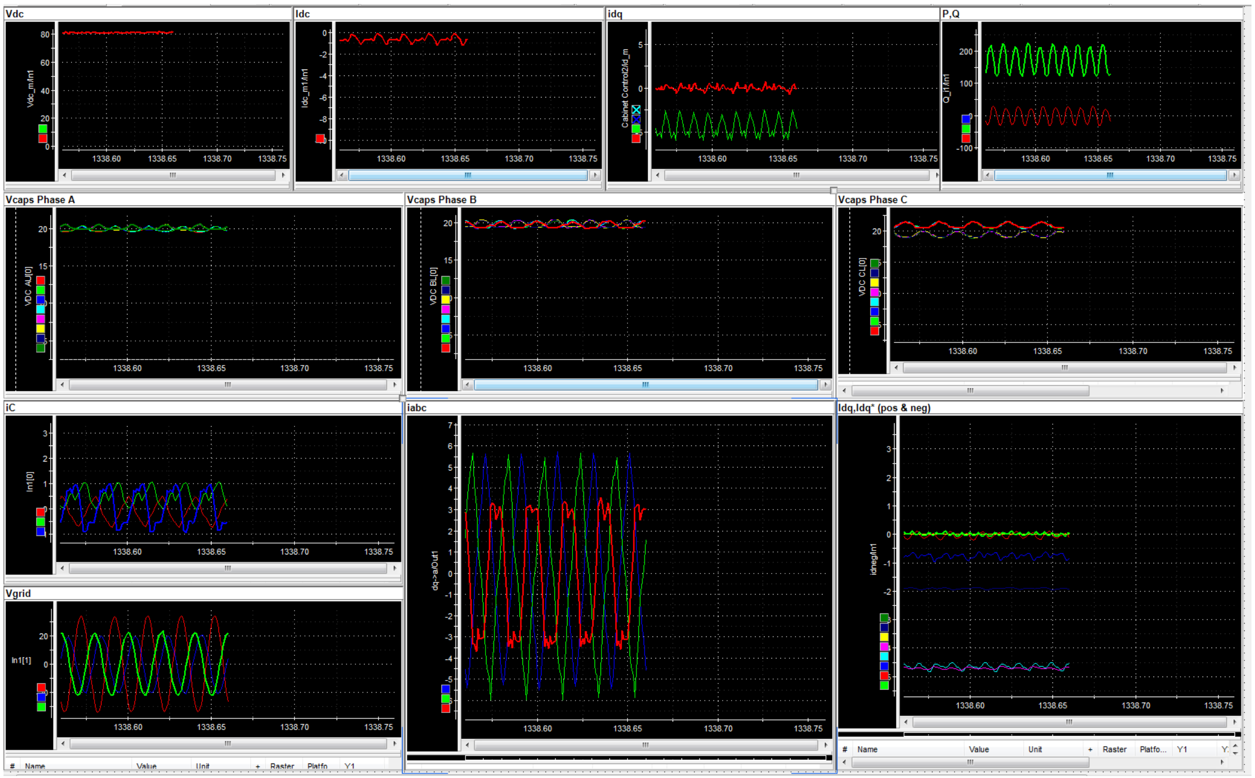


Fig. 52: Zoomed version of the Proposed Current Limitation Method under MSI BP.

It can be seen that for this scenario, the current is successfully limited from an initial 6.5 A amplitude to a final 5.5 A, but the reduction of the active current component is not enough, and the controller has to limit also the reactive current. Although the implementation here gives priority to the positive sequence component, that can be altered by adjusting the priority between the negative or the positive sequence reactive current injection (adjustment of the mean value or the ripple of the total q component). It can be also mentioned that the fact that the negative sequence active and reactive components are reduced, means that the balancing of the power is not achieved any more and P ripple increases.

4.3.3 Current Limitation Testing under MSI – GC

The response of the controller during the MSI – GC is similar to the case of MSI - BP. The Con to Prop to Con test is depicted in Fig. 53:

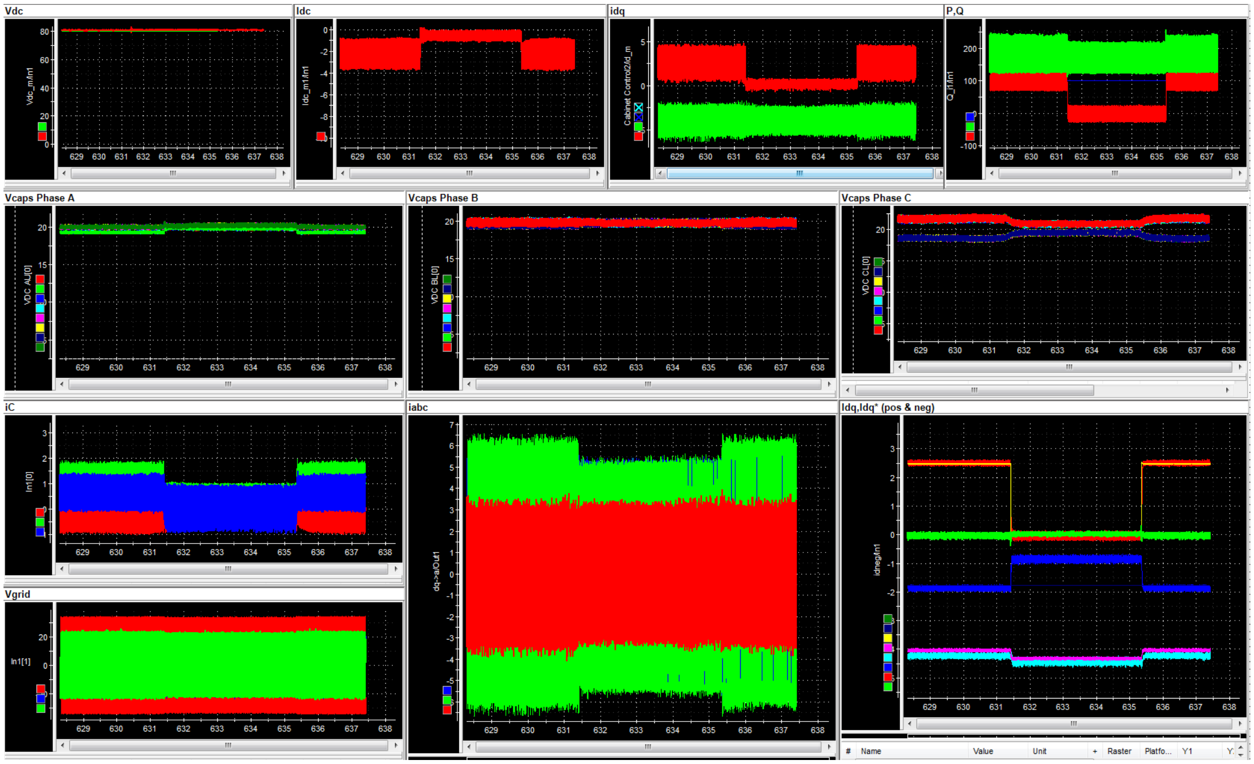


Fig. 53: Conventional to Proposed to Conventional Current Limitation Method with MSI GC injection: a) Phase Currents shown in "Iabc" graph, b) id+, iq+, id-, iq- are shown in "Idq,Idq* (pos and neg)" graph (red: id+, cyan: iq+, green: id-, blue: iq-, rest: references)

- As it can be seen, the limitation strategy works also for the case of MSI – GC in a similar way describe in the case of MSI -BP.

5 Conclusions and Future Work

5.1 Conclusions

- Problems of the PLL control associated with the existence of an AC Fault have been mitigated by the use of SOGI-PNSE in the experimental validation for the improved extraction of the positive and negative sequence voltage components of the fault.

- For steady state operation, the arm balancing control with use of the circulating current control is described, tested and proved to effectively balance the voltages between the arms of the same phase. However, in the case of an AC Fault, the response of the controller is proved to be slow.

- For the case of AC fault, three different current injection strategies were proposed to improve the performance of the MMC during AC fault and comply with the grid requirements. These strategies were created with manipulation of the FPNSC equations and the implementation of the grid requirements for reactive current injection during an AC fault.

    - The PSI succeeds in the support of the positive sequence component of the voltage during an AC fault with the injection of positive sequence reactive current.
    - The MSI -BP succeeds in minimizing the ripple in active power, by proper injection of negative sequence active current component. However, the method shows higher oscillation in reactive power. This characteristic though is not as undesirable as the active power ripple. The method also manages to reduce the negative sequence component of the fault in the PCC and support the positive sequence component of the voltage.
    - The MSI – GC aims at injecting reactive current according to the grid requirements. The method manages to reduce the negative sequence component and support the positive sequence component of the voltage, however it shows high ripple in both active and reactive power. The method injects also higher amount of current which results in the Sum capacitor voltage to have higher ripple.
- The high current references and the many different injected current components, created the necessity for a targeted current limitation that would take into account the different goals that are aimed to be achieved. For this purpose, a current limitation method with priority to the reactive current component was implemented. The result shows successful limitation of the references, with correct priority in the limitation.
- The overall conclusion is that MMC – HVDC can be controlled in order to comply with the newest grid codes (MSI). The utility can decide the most appropriate current injection strategy.

5.2 Future Work

- The strategies proposed in the current project could be also tested in a back to back connection in a HVDC prototype application. This test would give essential information about the ability of the system to coordinate its operation in case of a fault, since a communication system between two remote MMCs could be slow. This means that both the MMCs should be able to diagnose the fault and undertake a proper action for the system to remain stable.
- The current limitation proposed could be also investigated further in order to find an optimal combination of reduction for positive and negative sequence reactive currents. Since in case of a severe fault the active current has become zero, further necessity for reduction of the current could result in different behavior when moving from positive sequence priority to negative sequence priority.
- Another aspect that would be useful to be further investigated, is the sum capacitor voltage reduction in the case of the fault. The tests showed that with the faults implemented, the system was able to keep operating, but the capacitor voltage increase shows that in different cases of faults or setup this response could be not acceptable. Since the energy balancing is proved to have slow dynamics, another faster solution should be implemented. A possible solution could be the feed forward of a voltage component related to the fault severity, to lower the mean value of the capacitor voltages so as to withstand an increased ripple component (caused by the increase of the current).

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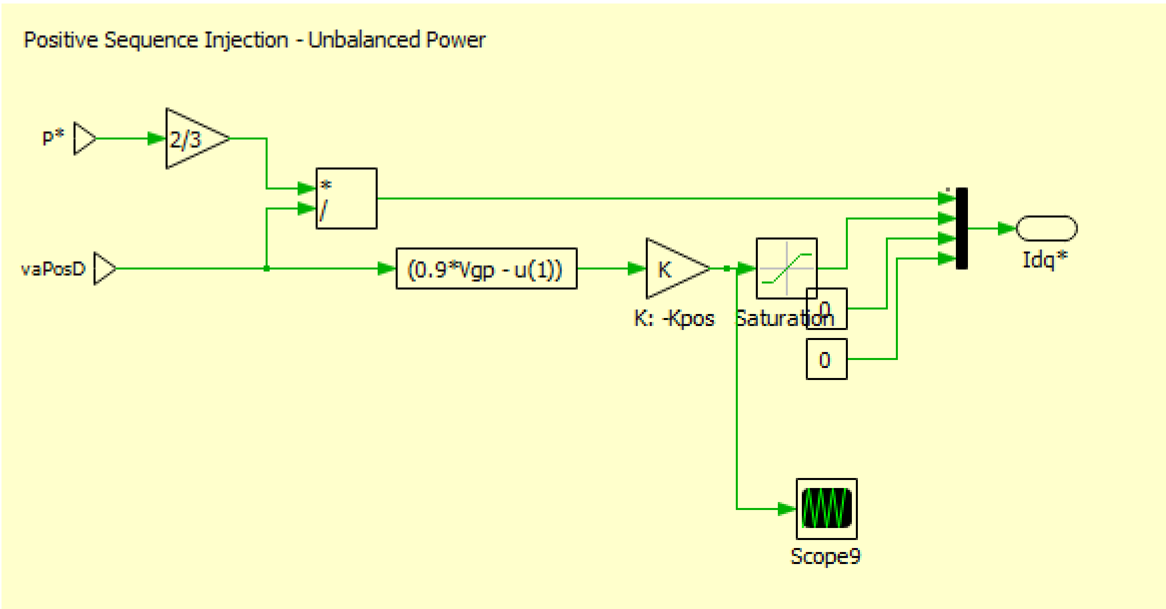
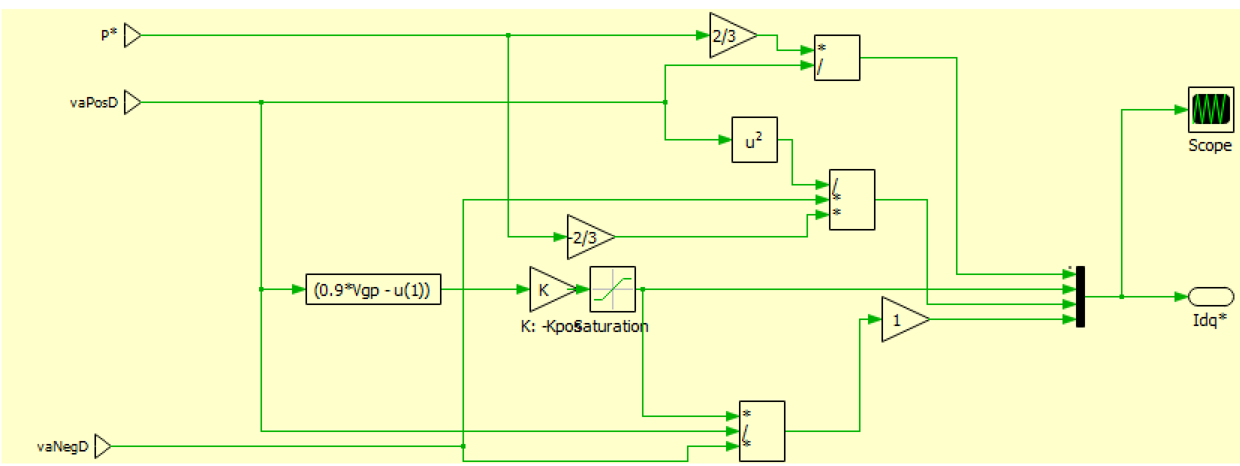
Appendix A

"Description of the simulation model in PLECS"

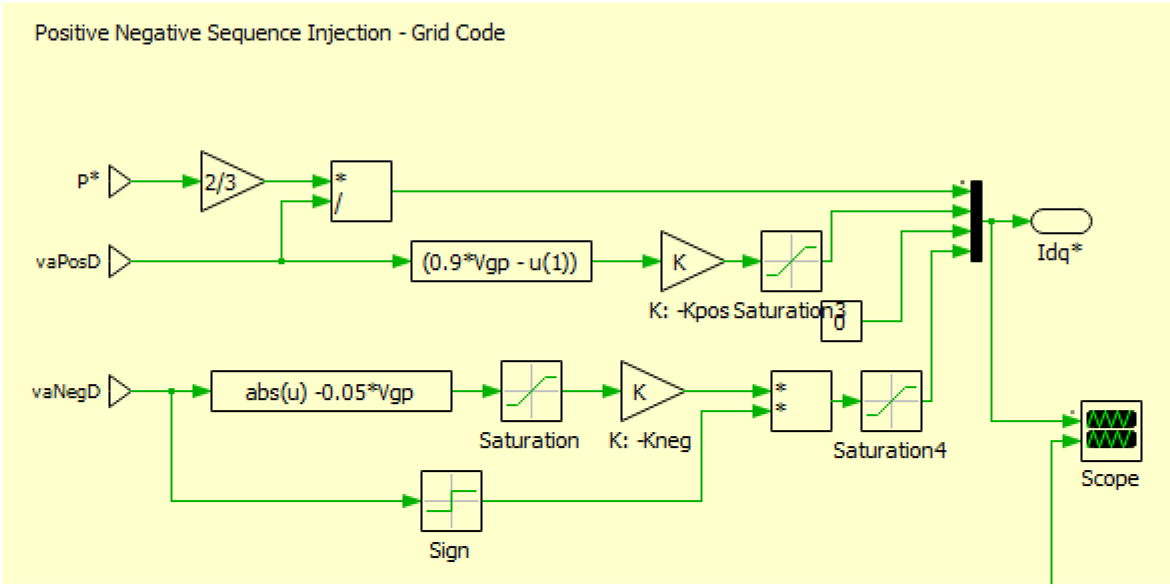
Implementation of PSI:



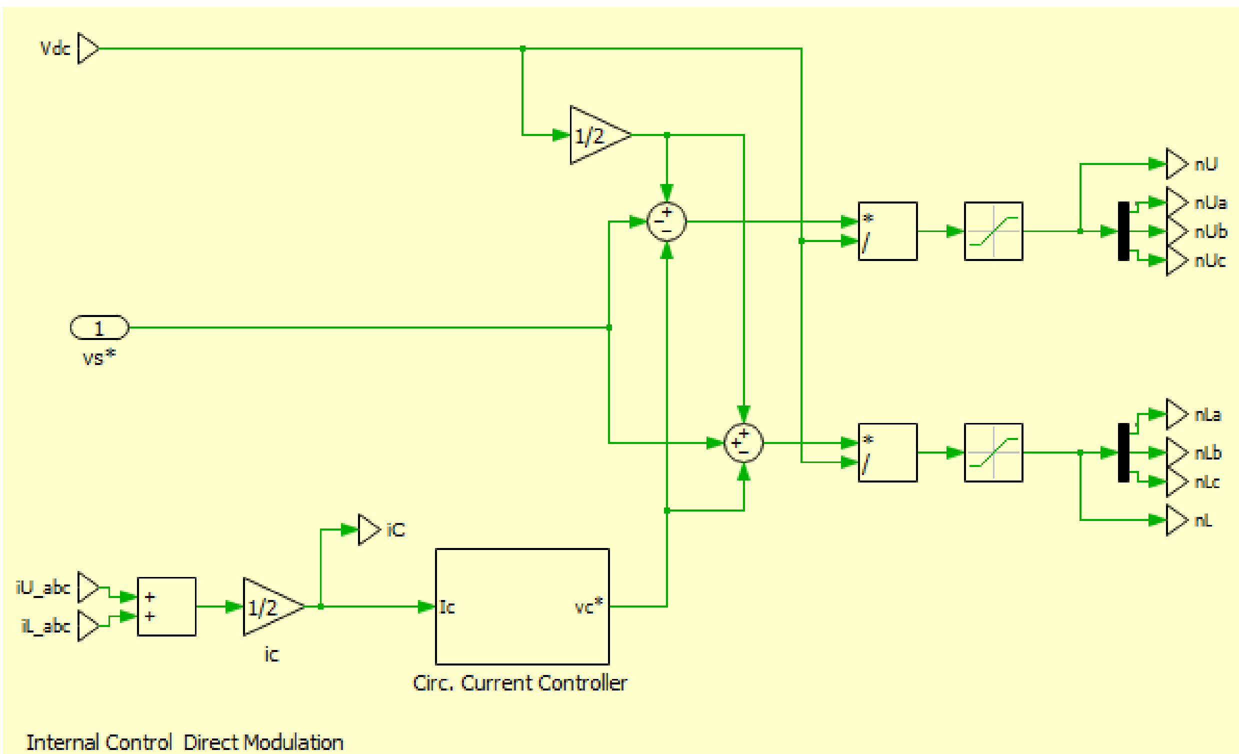
Implementation of MSI-BP:



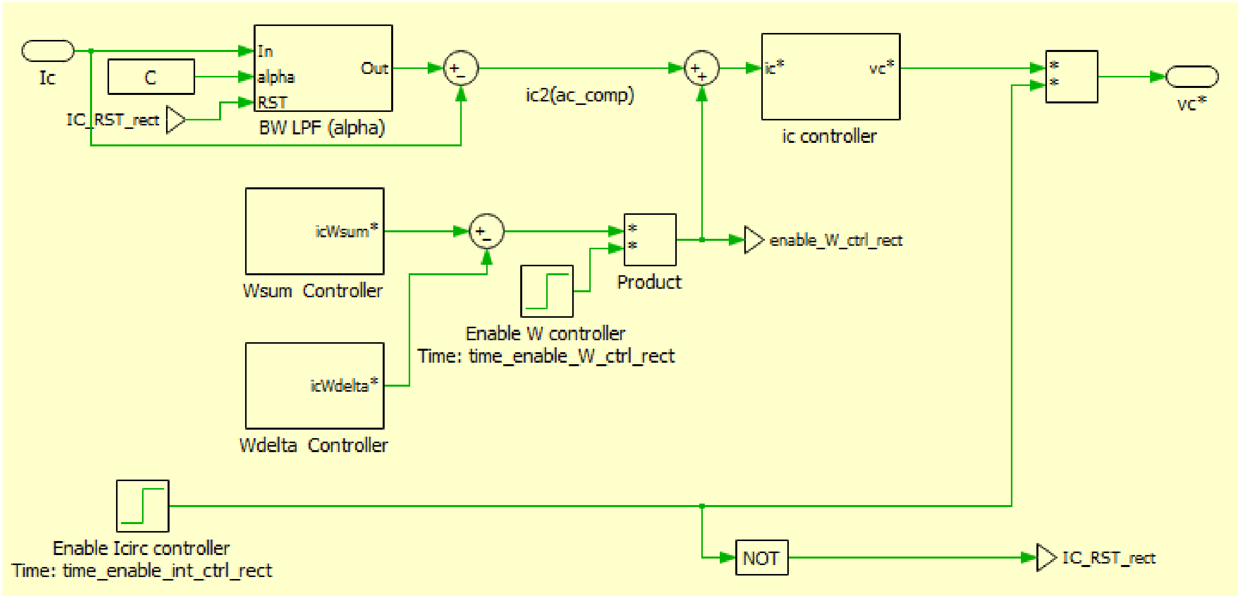
Implementation of MSI-GC:



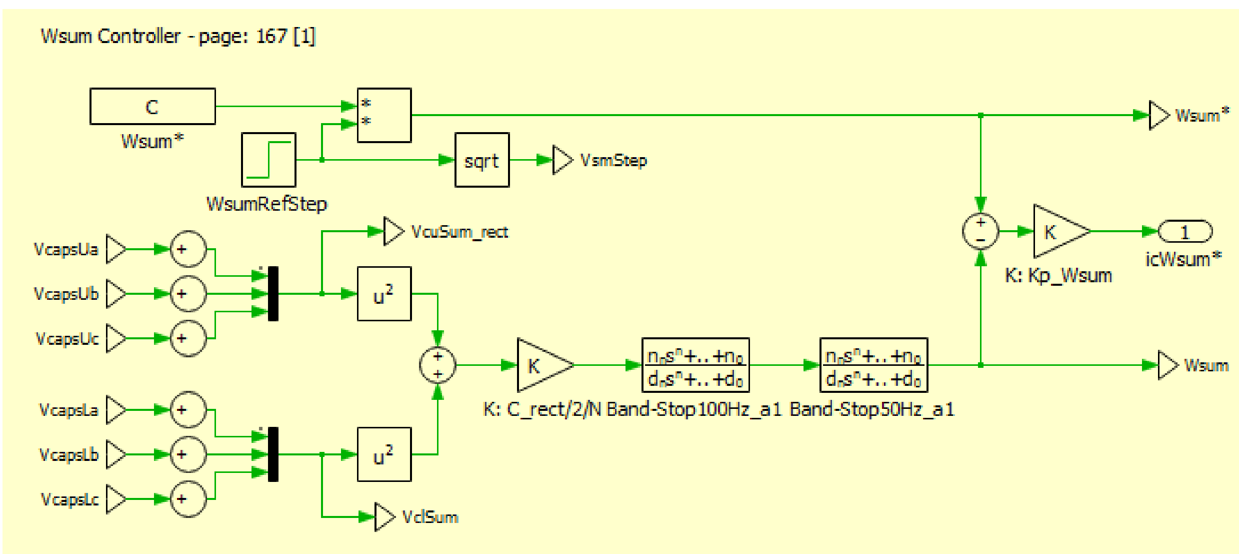
Direct Voltage Modulation:



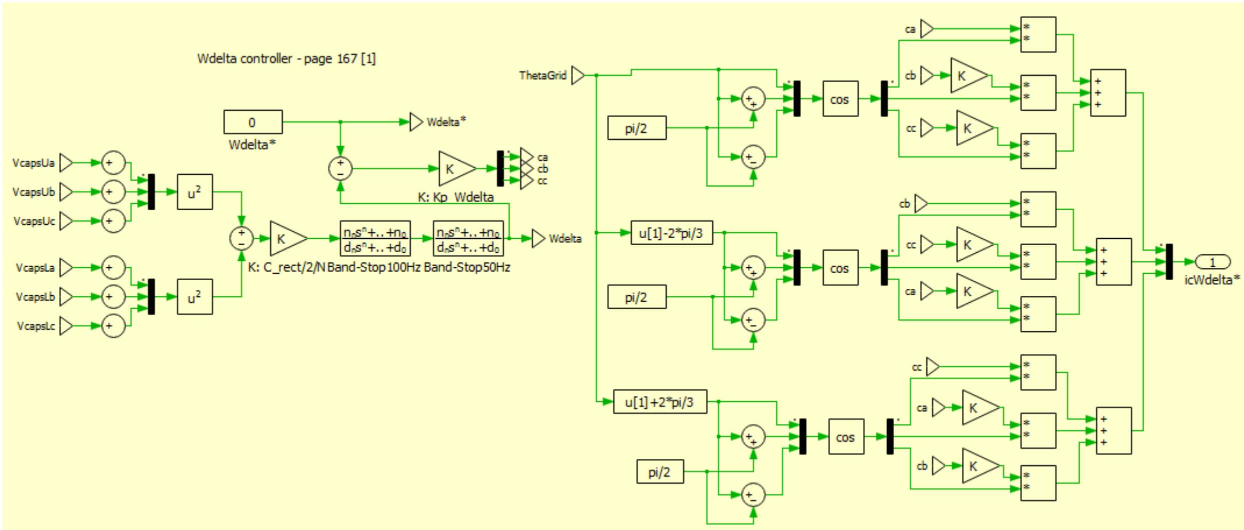
Circulating Current Controller:



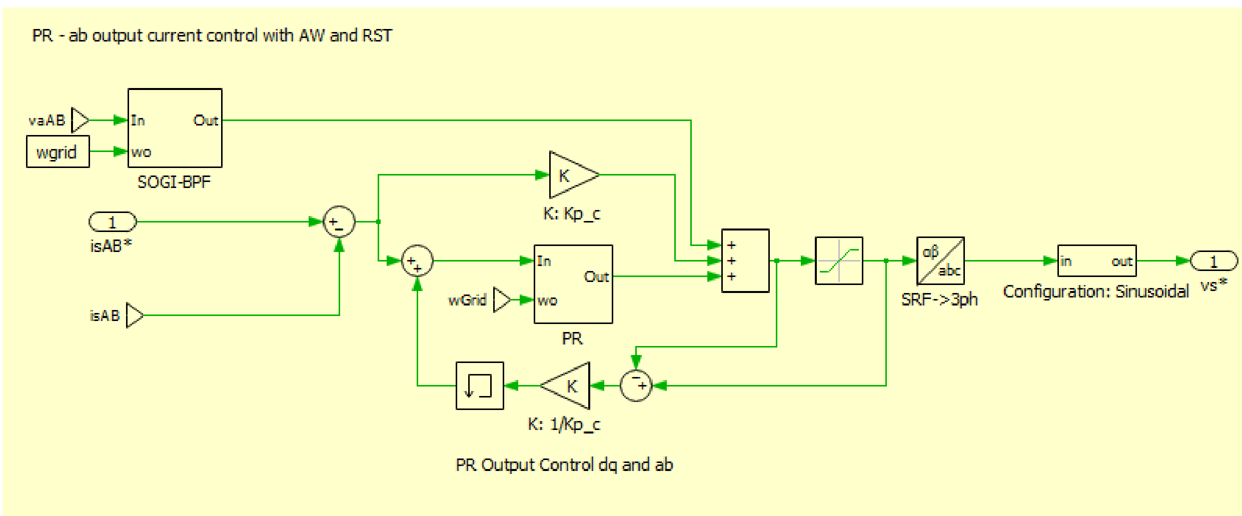
W_Σ Controller



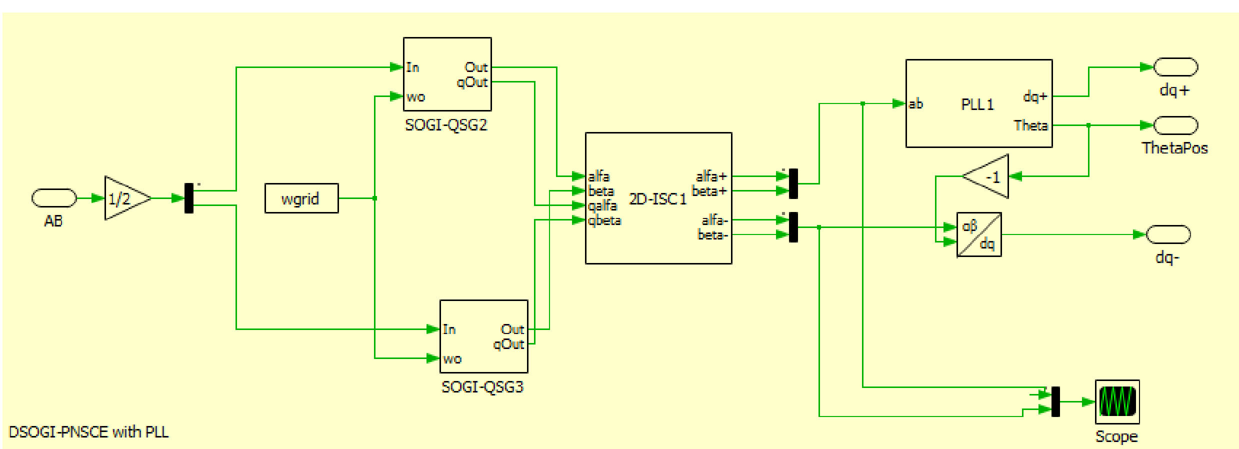
W_Δ Controller



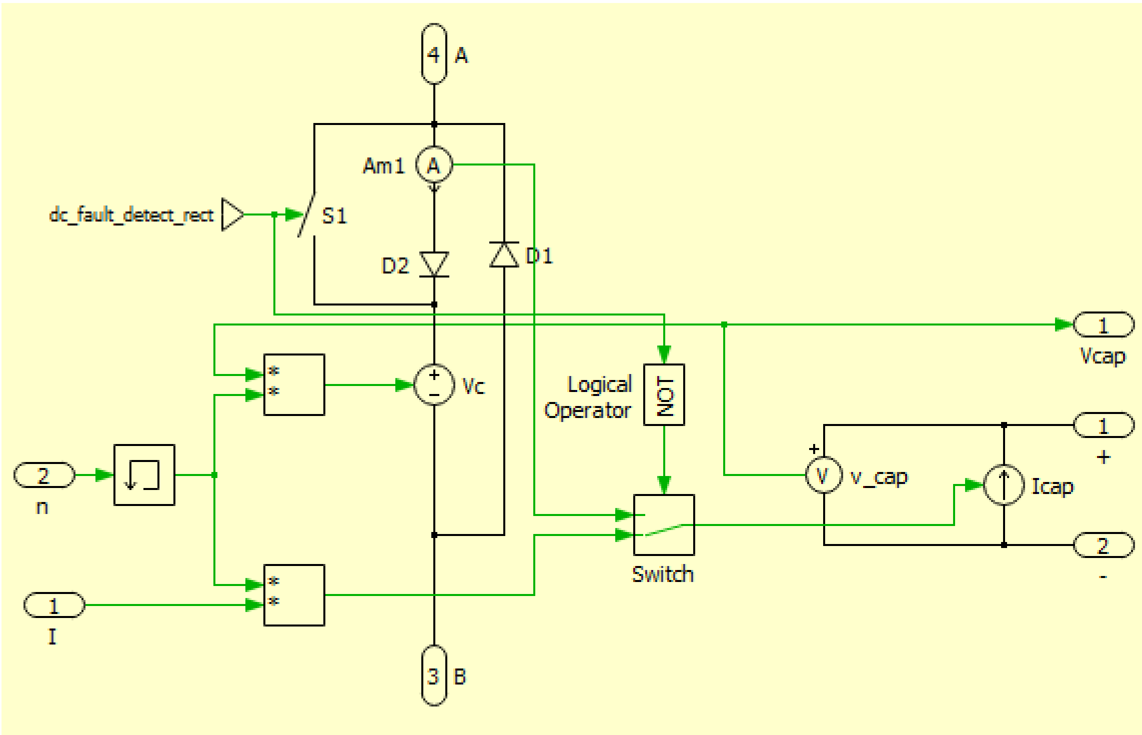
Output Current Controller:



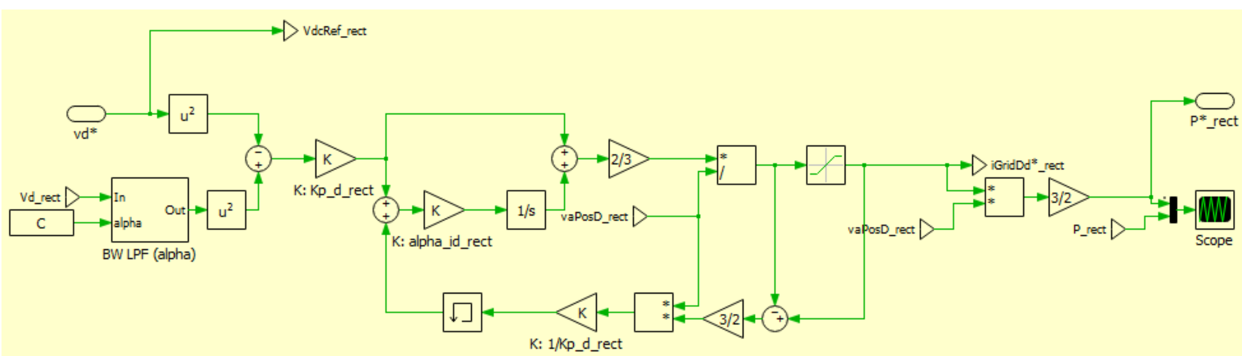
DSOGI - PNSE (DSOGI-QSG and PNSE) and PLL



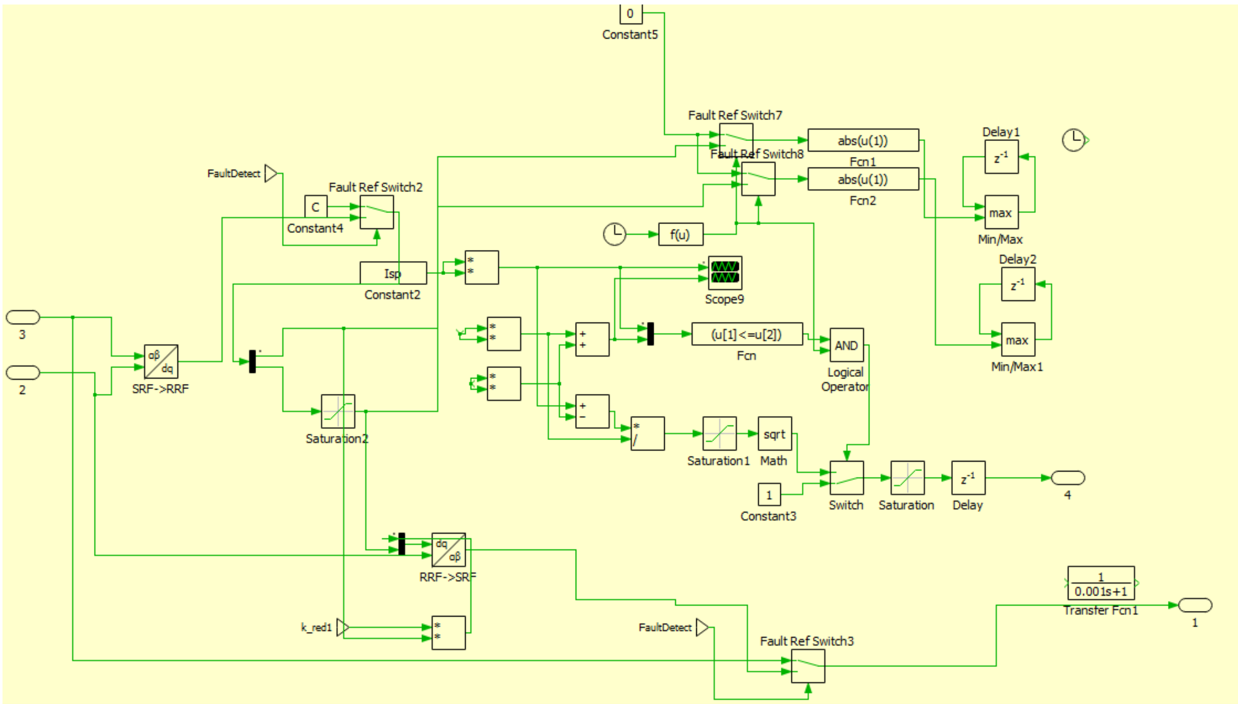
Averaged Model of MMC:



DC Voltage Control:



Current Limitation:


0
Constant5
Fault Ref Switch7
Fault Ref Switch8
abs(u(1))
Fcn1
abs(u(1))
Fcn2
Delay1
max
Min/Max
Delay2
max
Min/Max1
FaultDetect
Fault Ref Switch2
C
Constant4
f(u)
Isp
Constant2
Scope9
3
2
SRF->RRF
(u[1]<=u[2])
Fcn
AND
Logical Operator
Saturation2
Saturation1
sqrt
Math
Switch
Saturation
Delay
4
1
Constant3
RRF->SRF
k_red1
FaultDetect
Fault Ref Switch3
1
0.001s+1
Transfer Fcn1
1

Appendix B

Control Parameters for the setup

```
%Ideal Model of MMC for dynamic studies
%       - by Remus Teodorescu, Laszlo Mathe, Ariya Sangwongwanich Dec 2015

%Assumptions:
%   1- All cap voltages are equal (ideal balancing)
%   2- Insertion index are continuous functions

% The model is CONTINOUS based on ideal voltage source for ac side and
equivalent arm cap feede by n*Iarm
%Memory blocks have been inserted to avoid algebraic loops
%Both output current and circulating current control loop can be designed by
selecting the BW
%The strength of the grid can be set by changing SCR
%All input parameters are marked with "INPUT" label

freq=600; % carrier frequency

%Select Modulation type: NLC-1, PS_PWM-2
Modulation_type=1;

%Select Cap Voltage Balacning Method type: NLC_SORT-1, NLC_SORTLevCh-2,
NLC_CTB-3, NLC_ATB-4
VC_BAL = 1;
%Grid parameters
fgrid=50; %INPUT  grid frequency
wgrid = 2*pi*fgrid;
Vgrid = 244.9489743; % INPUT Grid line-line RMS [V]
%Vgp=Vgrid/sqrt(3)*sqrt(2); % peak phase voltage
Vgp=40;
Vgrid=Vgp*sqrt(3)/sqrt(2);
GridPhaseInit = 0; % INPUT initial grid phase angle
Is = 5; %  INPUT Output rated current RMS
Srated=sqrt(3)*Vgrid *Is;
Ptest=4e3;
SCR=10;% INPUT SCR of grid at PCC
Lg=(Vgrid^2)/(sqrt(3)*1.1*wgrid*SCR*Srated); %Calculate Lg out of SRC and
neglecting R
Rg=wgrid*Lg/10; % assume R = 10% of X
Tinit=50; % INPUT initial temparature
Tol_Band = 0.10;%tolarance band in per unit!

%MMC power ratings - Test converters
VdcRated=80;
%  INPUT Total Vdc
PF=0.85; % INPUT Power Factor
N=4;%  INPUT  Nr of SM per arm
N_1=N-1; % MUX dimension for cloning
VsmRated=VdcRated/N;
Larm=20e-3; % INPUT Arm inductance [H]
Rarm= 0.2; % INPUT arm resistance equivalent for losses [ohms]
```

```
%SM capacitance calculation
%Wrated=30e-3;% [J/VA] for m=1, Q=0, paper Harnefors Energy Storage
Requirements..
%C = N*2*Wrated*Srated/6/(VdcRated)^2; % [F]
C=4e-3; % INPUT SM capacity average value
Carm = C/N; % INPUT equivalent arm capacitance

%initialize and create vectors
Csm = ones(1, N);
VsmInit = ones(1, N);
Rsm = ones(1, N);

PlossSM = 0.01*Srated/3/(2*N);% INPUT average internal losses in each SM (1%)
VsmRated=VdcRated/N; % Rated cell voltage
RsmAvg =VsmRated^2/PlossSM; % Equivalent average shunt resistor for internal
losses modelling
%Tolerances
TolC=0;% INPUT Maximum manufacturing tolerance in %
TolRc=0; %INPUT Maximum internal losses variation in %
TolVcInit = 0.0; % INPUT Maximum initial voltage difference in %
for k=1:N
    Csm(k) = C*(1 + TolC*rand/100); %tolerance = +Ctol
    VsmInit(k) = VsmRated*(1 + TolVcInit*(rand-0.5)*2)*0; %tolerance =+/-
VcInitTol
    Rsm(k) = RsmAvg*(1 + TolRc*(1+(rand-0.5)*2)); %tolerance =+/- RcTol
end

%Grid fault generation
FaultStart= 1; % INPUT fault start time [s]
FaultEnd = 2; %INPUTfault start time [s]'
VgpPosPrefault=1; %INPUT Prefault positive voltage in pu
VgpPosFault=0.8; %INPUT Fault positive voltage in pu
VgpNegPrefault=0; % INPUT Prefault negative voltage in pu
VgpNegFault=0.2; %INPUT Fault negative voltage in pu
Isp=Is*sqrt(2);%peak current rated
Kneg=Isp/(0.5*Vgp); %Neg seq reactive current droop: rated current at 50% neg
seq
Kpos=Isp/(0.4*Vgp); %Pos seq reactive current droop: rated current at 50% pos
seq drop

% Total impedance
L = Lg + Larm/2;
R = Rg + Rarm/2;

%PWM parameters
MaxCarrier = 1;%INPUT
MinCarrier = 0;%INPUT
DutyCycle = 0.5;%INPUT
CarrierHz = 600;%INPUT 1025/5
fs= 20000; %CarrierHz*N; %Control sampling frequency
Ts=1/fs;%Control sampling period
pwm_en=0;%INPUT 0-Disable pwm in NLC, 1-Enable pwm in NLC
Kpspwm = 0.000005/10; %Controller gain for voltage balancing
%PLL parameters

KsogiPLL = sqrt(2)/2; %INPUT SOGI gain
```

```
alpha_p=50; % INPUT BW of PLL for tr=1/alpha=20ms
alpha_ip=10; %INPUT alpha_ip < alpha_p/2 - Lennart!?
alpha_b=200; % INPUT LPF to PLL
alpha_n=0; %INPUT Notch filter PLL BW


%Output current control PR with AW and resetable integrators
alpha_c= 8144.86;%5282; %INPUT Desired BW output control test converter
alpha_c0= 406.5;%265; %INPUT Desired BW of the resonant integrator
alpha_c2= 406.5;%265;
Kp_c=alpha_c*L/2; %Proportional gain PR conrtoller for output currnet
Kh_c0=2*alpha_c0*Kp_c; %Integral gain PI conrtoller for output currnet
Kh_c2=2*alpha_c2*Kp_c; %Integral gain PI conrtoller for output currnet
alpha_f = 1000; %INPUT Desire BW of the VFF
Kp_c=24;
Kh_c2=2400;


%Circulating current control - PR
Ra= 20;%INPUT Proportional gain of circ current control (R<<Ra<Kp)
alpha_2 = 50; % INPUT BW for circulating current test converter (alpha_c <
wgrid)
K2h_c=2*alpha_2;% integral gain for resonant controller for icirc
alpha_cr=50; %INPUT  BW of LPF of te circ current to get the reference (dc
value)


%DC  voltage control
% Cd=500e-7;%INPUT - dc bus capacitance 100e-3
% alpha_d=50; %INPUT BW
% alpha_id=25;% INPUT Integral BW
% Ce=Cd+C*6/N;
% Kp_d=alpha_d*Ce/2;% Gain of PI

%Measurements
%Cut-of frequency for LPF used in Power Meter
wc=2*pi*50;% Input wc=5Hz

%Initialize carrier initial phase vectors
PhaseCarrier = ones(1, N);

for k=1:N
    PhaseCarrierU(k) = (k-1)/((CarrierHz*N));
end

PhaseCarrierL = ones(1, N);

for k=1:N
    PhaseCarrierL(k) = (k-1+0)/((CarrierHz*N));
end



Kp_ver=0.2;
```

```
Ki_ver=0.3;

%Initial Values
Kp_d=0.001;
alpha_id=7;

%horizontal

Kp_hor=0.2;
Ki_hor=0.5;

Ki_CC=0;
h_order=0;
EnableH=0;
Td=0;

% Kh_c5=10;
% Kh_c7=14;
% Kh_c11=22;
% Kh_c13=15;

Kh_c5=0;
Kh_c7=0;
Kh_c11=1;
Kh_c13=1;

Kp_filter=0;
Ki_filter=0;

Vg_lim=40;
cab1.oc.Kpq=0.15;
cab1.oc.Kiq=1;
```