MODELING OF FAILURE MECHANISM IN SIC MOSFETS SUBJECT TO SHORT-CIRCUITS

Ole Damm Kristensen

DEPARTMENT OF ENERGY TECHNOLOGY
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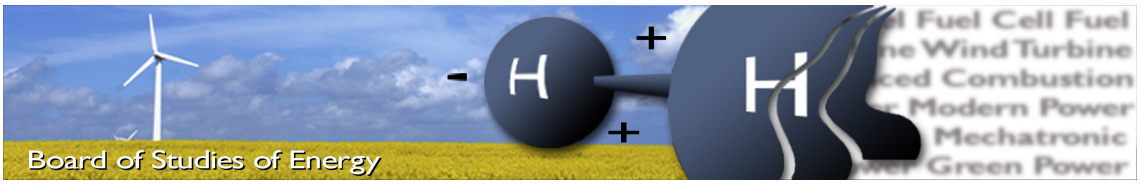

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Ole Damm Kristensen

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SYNOPSIS:

Because of their good performance it is desired to use SiC MOSFETs for high power applications. However, it has been observed that they are more vulnerable to thermal runaway and related failure mechanisms during short-circuits than the commonly used Silicon IGBTs. Therefore, a model of a SiC MOSFET that resembles the behavior of commercially available chip was implemented in the TCAD program Sentaurus for performing numerical simulations of the device during operation. The model was adjusted to have similar performance to the datasheet of the device, a CREE CPM12000080B. This model was exposed to short-circuit to investigate the inner failure mechanisms. It was found that due to simplifications of the model, a breakdown occurred that was not related to the studied failure mechanism.

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Preface

This report is the result of a master thesis carried out in the period from 1st of February 2017 to 1st of June 2017 at the Department of Electrical Energy Technology at Aalborg University. The project corresponds to 30 ECTS

All simulations of this project have been performed in the TCAD program Sentaurus, made by Synopsys. The report has been written in Latex, and all graphs have been made using MATLAB.

The author would like to thank his master thesis supervisors; Lorenzo Ceccarelli, Paula Diaz Reigosa, and Francesco Iannuzzo for the supervision during this master thesis. A special thanks goes to Paula Diaz Reigosa for the massive support in the use of the simulation tool Sentaurus.

Reading instructions

All sections, tables, equations, and figures are labelled according to chapter number in chronological order. Hence the first section in Chapter 2 is numbered 2.1, the second 2.2 etc. All figures are chronologically listed in the list of figures, and all tables are chronologically listed in the list of tables.

The reference system used in this report is the IEEE Method. The IEEE Method show the references with the label [Number of Reference]. In the section called Bibliography, the complete list of references with Author and Title can be found.

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Summary

Wide band gap materials are of great interest for power semiconductors due to their beneficial material properties. The most promising material for high power applications is 4-H Silicon-Carbide (4H-SiC) due to its high critical field strength, high thermal conductivity, and high melting point. This allows devices to be build that posses desirable attributes such as high breakdown voltages, low on-state losses and good thermal properties.

With the introduction of 4H-SiC, it has become feasible to introduce MOSFETs with a high blocking voltage while preserving a reasonable on-state loss. Using these, a higher switching frequency can be achieved for the same losses which can reduce size of the energy storing components in power electronic converters.

One of the major barriers for the introduction of SiC MOSFETs in high power applications is the limited short-circuit capability of these. Therefore, this is the main focus of this report. Short-circuits can occur due to erroneous turn-on of both switches in a phase-leg for example due to a gate driver failure. In this case both a high voltage and a high current is applied simultaneous, resulting in a high dissipated power in the device. This power is dissipated in the device until the gate driver has detected the short-circuit and turned off the device. Therefore, the device needs to be able to withstand this power for some time to provide enough response time for the gate driver to respond.

Even if the device is not immediately destroyed, the device might still fail due to a so-called thermal runaway. This can happen due to the increased leakage current introduced by the heating of the device. In combination with the high blocking voltage of the device, this will produce an additional heating of the device. If this produced power exceeds the dissipated power of the device a further increased heating is experienced and positive feedback mechanism is created. This results in destruction of the device.

In this project, a Techology Computer Aided Design (TCAD) model is made with the purpose of investigating the failure mechanisms related to short-circuits. The model was implemented in the TCAD program Sentaurus. Through a combination of analytical expressions and iterative changes, it is attempted to create a model that resembles the behavior of the 1200 V SiC MOSFET chip CPM2-1200-0080B manufactured by CREE.

The TCAD model was found to recreate the breakdown characteristics and the transfer characteristic in the desired range. On the other hand, the output characteristics was found to be less accurate.

The transient behavior of the device was simulated by a low voltage short-circuit performed at a DC-link voltage of 100 V. This test showed that the model did not exhibit the same failure modes as a real device. Due to the lack of a highly doped p^+-layer, the intrinsic BJT is activated during the short-circuit which leads to a failure of the device. Therefore, the model cannot be used for investigating the inner states during a thermal runaway, as

it fails due to the activation of the intrinsic BJT at an earlier stage.

Introduction 1

In this chapter, the motivation for this project is presented. The importance of power semiconductors is introduced and the reasoning for changing from Si-based semiconductors to SiC is presented.

1.1 Introduction to Power Semiconductors

With the increasing use of renewable energy sources, the number of power converters are increasing. Therefore, the reliability and efficiency of these converters are of great concern[4]. It is estimated that by 2020, the total installed capacity of wind power will be approximately 760 GW, and the largest wind turbines will be rated for more than 10 MW[5].

Power semiconductors are one of the main components of power converters and therefore also the efficiency and reliability of these components are of great interest as they play a major role in the overall reliability of the power converters.

The semiconductors used for high power applications, such as wind power converters, are often based on Silicon (Si). However, Si-based devices have limitations when it comes to blocking voltage capability, operation temperature, and switching speed. Wide Bandgap (WBG) devices such as Gallium Nitride (GaN), or Silicon Carbide (SiC), are starting to be used as they provide better performance than the commonly used Si-based devices. Therefore, WBG-devices are expected to enter the market in the near future to achieve smaller and more efficient power converters[6].

In Fig. 1.1, the common application of different types of power modules is presented.

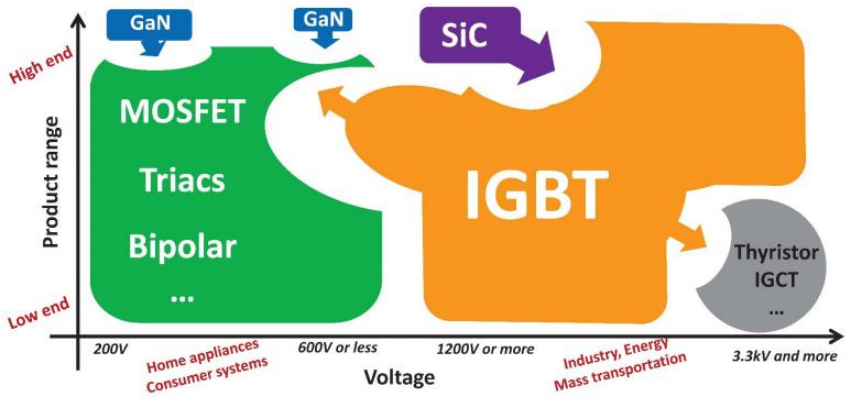

Figure 1.1. The current applications of power modules and the expected use for replacing Silicon-based power modules with either Silicon Carbide or Gallium Nitride [6].

From the figure, it is observed that while GaN-based devices are expected to enter the market for low-voltage applications, SiC-components are expected to enter the market for higher voltage applications, such as converters for wind turbine and renewable energy sources. In this project, converters for these types of systems are the main systems of interest, and therefore SiC is the material of greatest interest.

One of the major barriers for the introduction of SiC MOSFETs in power converters is the higher costs of the devices compared to similar Si-based devices. Due to the non-compability between the production of SiC devices and normal Si devices, new investments in production facilities are needed. Therefore the price of SiC devices largely depends on the quantity of sold devices in order to pay off the investments in new equipment. In 2014, one of the leading manufacturer of SiC devices, CREE, made a projection of the price of SiC MOSFET as a function of the number of sold devices. In this it is estimated that by the end of 2017 the price will be reduced to approximately 10 % of the price in 2014, as the number of produced devices increases. However, the cost of the SiC components will still be higher of the comparable Si-based devices [7]. This is mainly explained by the fact that SiC wafers are more difficult to produce than a similar Si wafer. Higher temperatures are needed to implement the desired doping concentrations, and obtaining the needed quality during mass-production is more difficult for 4H-SiC than for Si [8].

However, despite the higher price due to these challenges, the devices are still interesting due to their lower losses and higher performance [7]. The advantages of WBG-based devices are based on their material properties. In Fig. 1.2 the material properties for Si-, SiC-, and GaN-devices are shown

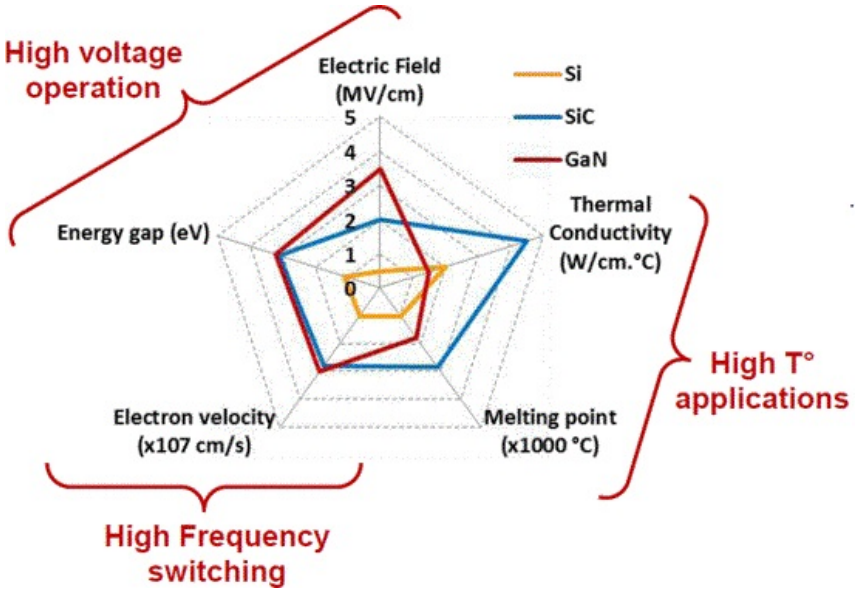

Figure 1.2. The different properties of Silicon, Silicon-Carbide and Gallium-Nitride, where the link between material properties and device capabilities are explained. [9].

From this, it is seen that both SiC and GaN have a higher critical electric field than Si, hence they will be able to sustain a higher blocking voltage for the same device thickness, making it highly applicable for high voltage operation. The higher critical field strength is also an advantage if the same blocking voltage is desired, as this makes it possible to reduce the thickness of the lightly doped n^- drift layer. This layer is a major contributor to the on-state resistance of the device, $R_{DS,on}$, and therefore a major contributor to the on-state losses.
The ideal on-state resistance is given by [10]

$$R_{DSon,ideal} = \frac{4 \cdot BV}{\epsilon_s \cdot \mu \cdot E_c^3} \tag{1.1}$$

where BV is the breakdown voltage of the device, ϵ_s is the permittivity of the material, μ is the electron mobility in the material, and E_c is the critical electric field in the material. The material properties of the most commonly used structure of SiC, the 4H-SiC, are given and compared with Si in Table 1.1.

Table 1.1. Material properties for Silicon and 4H-SiC.

Property	Unit	Silicon	4H-SiC	Source
Relative Permittivity	[-]	11.9	9.66	[11]
Electron Mobility	$[cm^2/(V \cdot s)]$	1450	1000	[11]
Critical Electric Field	$[kV/cm]$	300	2200	[11]
$R_{DSon,ideal}$ at 1200 V	$[m\Omega \cdot cm^2]$	0.12	$5.3 \cdot 10^{-4}$	

Tab. 1.1 shows that while Si has a slightly higher permittivity and electron mobility, the achievable R_{on} is still significantly lower for 4H-SiC due to the very high critical field for

the material and the cubic dependency on this for the on-state resistance.
An additional advantage of SiC MOSFETs can also be seen from Fig. 1.2. SiC provides a much higher thermal conductivity and melting point than Si. While Si devices often are rated for up to 175° C, SiC MOSFET are capable of operating at well above 200° C. However, in reality the devices are often limited to 175° C due to limitations of the device packaging [12]. Both the low on-state resistance and the higher operation temperature makes the material even more suitable for medium and high power applications.
Nowadays, IGBTs are used for these medium and high voltage applications, in the range from volts to several megavolts due the possibility of achieving a high blocking voltage, while preserving a reasonable on-state loss. However, since IGBTs are bipolar devices, a tail current is present when the device is turned off. This tail current increases the turn-off losses and therefore the switching frequency has to be reduced to keep the temperature of the device within the rated specifications. As a MOSFET is an unipolar device, the tail current is not present during turn-off. This makes it possible to achieve a higher switching frequency for the same current rating, as seen in Fig. 1.3

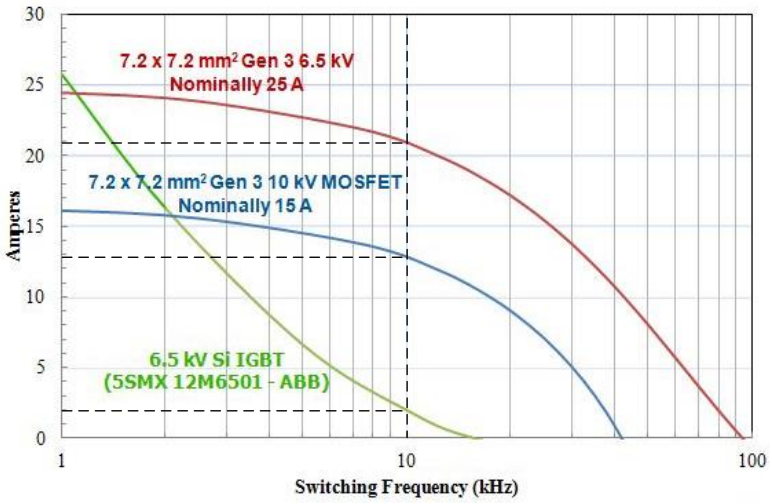

Figure 1.3. A comparison of high-voltage SiC MOSFETs with a currently used Si-based IGBT. Modified after [7]

Figure 1.3 presents the maximum allowable current as a function of the switching frequency for a 6.5 kV and a 10 kV CREE SiC MOSFETs compared to a commercially available Si IGBT from ABB. It can be noted that the current rating of the IGBT at 10 kHz is only 2 A, due to the high switching losses. The SiC MOSFETs have a rated current of 13 A and 22 A at the same frequency, making it realistic to use a higher switching frequency for high power applications. This allows smaller capacitive and magnetic components, while maintaining the same current ripple and output harmonics. For all of these reasons it is desirable to choose SiC MOSFETs over Si-devices for medium and high voltage applications. However, there are still major hurdles to be overcome regarding the reliability of SiC MOSFETs. Therefore, the failure mechanisms must be deeply investigated in order to increase their reliability.

1.2 Motivation of this work

One of the barriers for the use of SiC MOSFETs in high power applications is the reliability of these during short-circuit. Due to the low short-circuit withstand time, the MOSFETs are susceptible to failures under these conditions which limits the operational lifetime of the devices in high-power applications.
As it is desired to implement SiC MOSFET in high-power applications in the future, these issues need to be solved. The first step towards solving the issue is to understand the failure mechanism of these devices, and the internal behavior.
Furthermore, if a model can be built which represents the real device, it could be possible to predict the behavior of this device during more complex situations. Examples of this could be the short-circuit capability of multiple devices in parallel, or the impact of degradation of the modules.

1.3 Problem statement

The purpose of this project is to understand the failure mechanisms of SiC MOSFETs during short circuit conditions. To understand these mechanisms, it is desired to have a model that links the external behavior of the device exposed to a short-circuit to the inner physical mechanisms during these conditions.

Therefore, a 2D Technology Computer Aided Design (TCAD) model is built in the FEM program Sentaurus to study the operation of a MOSFET during short-circuit conditions. Using this model, the physical mechanisms of the MOSFET will be simulated, to show the current distribution, electric field variation, temperature, etc. which would not be possible to observe by experimental results.
This knowledge can be used to understand which parameters that affect the reliability of SiC MOSFETs during short-circuit conditions.

1.3.1 Limitations

As the actual geometry of the MOSFET is unknown, a simplified model is built based on the parameters given in datasheet of the device. To simplify this model, certain assumptions are made:

- The actual geometry is unknown, therefore the device only resembles the performance of the real device
- The influence of material defects such as interface traps will be neglected
- The influence of the packaging on the thermal properties will be omitted
- To reduce the computational complexity, the device is assumed to be symmetric so that a 2D model can be build. Furthermore, only a halfcell is simulated to reduce the need for computational power.

1.4 Overview of report

In this section the advantages of SiC MOSFETs were introduced, and the motivation for modeling the short-circuit behavior of these during short-circuits were discussed.

Furthermore, the problem statement was presented and the limitations of the project were introduced.

In the following chapter, the theory about MOSFET as a device will be presented. The physical structure of a MOSFET and the typical IV-characteristics will be explained. Additionally, the internal resistances of the MOSFET will be presented, and their influence during normal operation and short-circuit will be discussed.

In Chapter 3, the TCAD model is introduced, and the different doping concentrations are either analytically derived or found through a series of iterations. At first, the breakdown characteristics are modeled, then the doping level and the depth of the device is modified to obtain the correct IV-characteristics. Finally, the different characteristics of the final device is presented.

Chapter 4 describes the behavior of MOSFETs during a short-circuit of type 1. In this chapter the failure mechanisms of a MOSFET subject to a short-circuit is discussed, and the difference between different types of failure is explained.

This knowledge is used in Chapter 5, where a short-circuit is simulated using the TCAD model described in Chapter 3. However, due to simplifications of the model, other failure modes than thermal runaway is encountered. This failure mode is investigated and possible solutions are suggested. However, none of these are implemented.

Finally, in Chapter 6 the conclusions are drawn and Chapter 7 discusses the limitations and challenges of this project. In this, the implications of the different assumptions of the project are discussed, and some suggestions for improvement of the project is given.

MOSFET theory 2

Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) are often used for low voltage power electronic circuits. However, with the introduction of SiC it has become realistic to manufacture power MOSFET with the necessary breakdown voltage for high power application while still maintaining relatively low on-state losses. In this section, the structure and working principle of the power MOSFET will be described.

2.1 Device overview

Due to the possibility of achieving higher breakdown voltages, vertically integrated MOSFETs are often used as the structure for high power devices. The internal structure of a vertically integrated NMOS can be seen in Fig. 2.1.

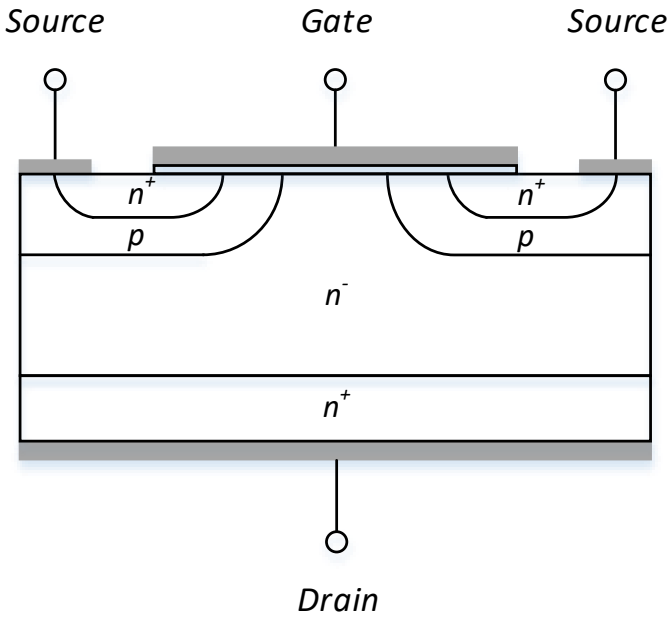

Figure 2.1. A vertical MOSFET with the different doping regions illustrated.

The device consists of a source region with a highly doped n-type region. This region has excess of electrons, commonly known as donors. The p-well is doped with materials with

a lack of electrons, also known as an excess of holes. These are denoted as acceptors or p-type material. To adjust the breakdown voltage of the device, a layer of lightly doped n-type material is used. This region is known as the drift region. Finally, the device consists of a drain region which has a high concentration of n-type material, named the substrate.

The flow of current between the two power terminals, drain and source, is controlled by the applied voltage at the gate terminal with respect to the source terminal, ie. the gate-source voltage V_{GS}. When a positive voltage is applied across these terminals, an electric field is applied and a channel for conduction of electrons is formed through the p-well. The IV-characteristics of the MOSFET depends on the applied gate voltage, V_{GS}, and the applied voltage across the power terminals, V_{DS}. For the case where V_{GS} is lower than the threshold voltage, V_T, the MOSFET is in its off-state. If a positive drain-source voltage is applied,$V_{DS} > 0$, ideally the MOSFET will not be conducting any current. In reality, a small leakage current will be present.

When a gate voltage greater than the threshold voltage is applied, $V_{GS} > V_T$, a channel in the p-well is formed and the current will start to flow. As the voltage is increased, the width of this channel is increased causing the channel to be more conductive.

2.2 IV-characteristics

From the properties of the gate-channel the following equation can be derived for the drain current for an when the device operates in its linear range [11]

$$I_D = \mu \cdot \frac{W_{channel}}{L_{channel}} \cdot \frac{C_{ox}}{2} \cdot [2 \cdot (V_{GS} - V_T) \cdot V_{DS} - V_{DS}^2] \tag{2.1}$$

where μ is the channel mobility, $W_{channel}$ is the out of plane width of the channel, $L_{channel}$ is the channel length, and C_{ox} is the per area capacitance of the gate. Eq. 2.1 is often simplified by assuming the device to be in one of two states. When the drain-source voltage is small the channel is not fully saturated and the device is in its linear mode. When the drain-source voltage is large, the channel is assumed to be fully saturated and an increase in drain-source voltage will not result in a further increase of the drain current.

When V_{DS} is small, the MOSFET is the linear region. In this region, the drain-source voltage can be assumed to be small; hence the term V_{DS}^2 can be neglected [10]. Therefore, the IV-characteristic in the linear region can be approximated by

$$I_D = \mu \cdot \frac{W_{channel}}{L_{channel}} \cdot C_{ox} \cdot (V_{GS} - V_T) \cdot V_{DS} \tag{2.2}$$

From this equation, the equivalent resistance of the MOSFET in the linear region can be found as the increase in the drain-source voltage when the drain current increases

$$R_{on} = \frac{dV_{DS}}{dI_D} = \frac{L_{channel}}{\mu \cdot W_{channel} \cdot C_{ox} \cdot (V_{GS} - V_T)} \tag{2.3}$$

From these expressions, it can be seen that the resistance of the MOSFET depend on material properties, device geometry, and the applied gate voltage. As the drain-source

voltage increases, the channel will saturate and the drain current will no longer increase as V_{DS} is increased. The condition were this occurs can be found from the point where the derivative of the drain current with respect to the drain-source voltage is zero. The solution to this equation is the so-called pinch-off condition, which is the voltage at which the MOSFET is saturated. This is given by

$$V_{DS} = V_{GS} - V_T \tag{2.4}$$

In the saturation region the current can be found by considering the drain-source voltage to be fixed at the pinch of voltage. Substituting $V_{DS} = V_{GS} - V_T$ into Eq. 2.1, the saturation current can be found by

$$I_D = \frac{W_{channel} \cdot \mu \cdot C_{ox}}{2 \cdot L_{channel}} \cdot (V_{GS} - V_T)^2 \tag{2.5}$$

where
From Eq. 2.5, the current is seen to be independent of the drain-source voltage once the channel is fully saturated. This is under the assumption that the channel shape is not affected by the drain-source voltage. In reality, a small increase in the output current is seen due to the changes in the shape of the channel when the drain-source voltage is increased [10].

As seen from the equations Eq. 2.2, Eq. 2.4, and Eq. 2.5 the drain current and the transition between the linear region and the saturation region depends on the applied gate voltage. Fig. 2.2 shows the output characteristics of a device at different gate voltages.

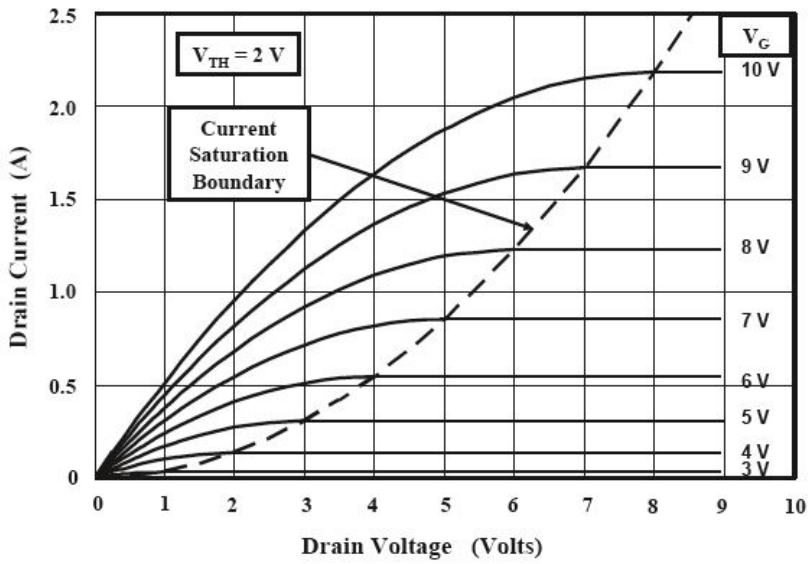

Figure 2.2. The output characteristics of a MOSFET at different gate voltages. The dashed line indicates the crossover from the linear region to the saturation region [10].

The dashed line in Fig. 2.2, the drain-source voltage where pinch-off occurs increases as the gate voltage increases.

The transfer characteristics of the MOSFET can be observed in Fig. 2.2. This is the current as a function of the applied gate voltage, when the drain-source voltage is fixed. An example of the transfer characteristics of an arbitrary power MOSFET is shown in Fig. 2.3

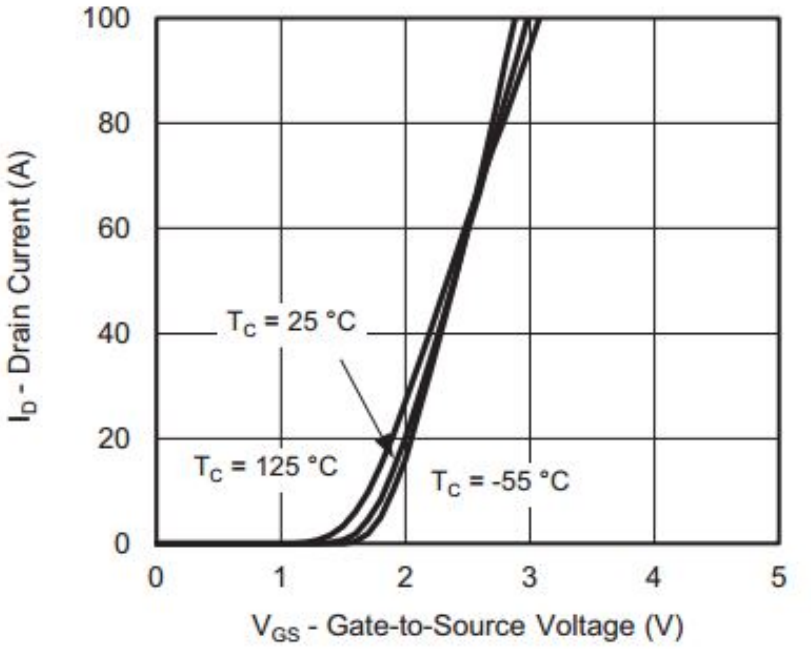

Figure 2.3. The transfer characteristic of an arbitrary power MOSFET [13]

The slope of the drain current versus the gate-source voltage is known as the transconductance of the device, g. This slope is found from the MOSFET IV-characteristics at a constant V_{DS} using the previously shown equation for the drain current. In the linear region the transconductance can be found by

$$g = \frac{dI_D}{dV_{GS}} = \mu \cdot \frac{W_{channel}}{L_{channel}} \cdot C_{ox} \cdot V_{DS} \tag{2.6}$$

Here it is noted that the transconductance depends on approximately the same parameters as the on-state resistance, hence the two parameters both have to be considered when modeling the MOSFET structure in Chapter 3.

2.3 Internal Resistances of the MOSFET

All of the internal resistances of the device both influence the on-state behavior of the device, and the behavior during a short-circuit, and therefore the origin of these resistances will be explained in this section.

The internal resistance of a MOSFET, R_{on}, can be divided into four major contributors. These different terms are given by [14].

$$R_{on} = R_{ch} + R_{acc} + R_{JFET} + R_{drift} \tag{2.7}$$

Where R_{ch} is the channel resistance, R_{acc} is the accumulation resistance, R_{JFET} is the JFET effect resistance, and R_{drift} is the drift layer resistance. The different resistances are depicted in Fig. 2.4.

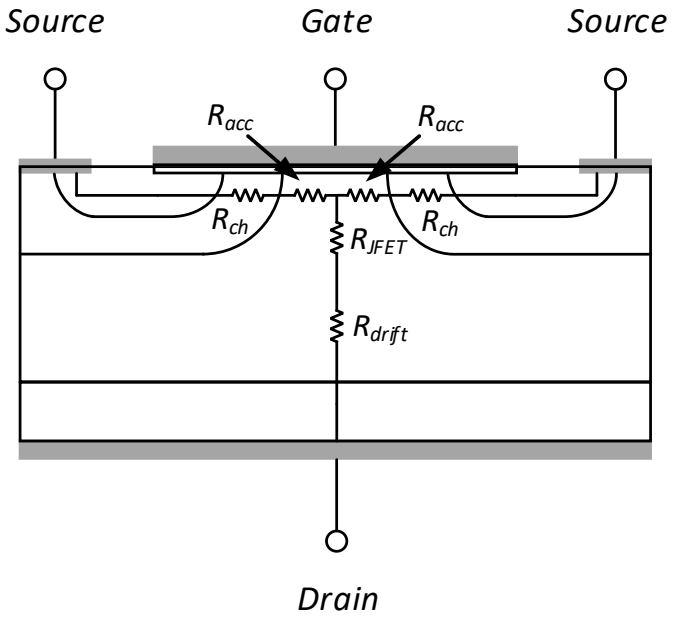

Figure 2.4. The four internal resistances of a vertical MOSFET, as described by Eq. 2.7.

The channel resistance, R_{ch}, is the resistance of the p-layer. As the concentration of acceptor doping in the channel is increased, this resistance is decreased, which is important when considering the turn-on of the intrinsic BJT. This will be explained in Chapter 4.

The accumulation resistance, R_{acc}, is caused by the fact that the current is injected from the channel to the drift region through a narrow region near the gate contact. Therefore, the current will flow through a small opening causing a higher effective resistance than the overall resistance of this layer. However, the total contribution to the total $R_{DS,on}$ is relatively small [11].

The JFET resistance is an increased effective resistance of the drift layer next to the PN-junction. The JFET effect is caused by depletion of the drift layer next to junctions. In these depleted regions, no electrons will flow, reducing the effective cross-sectional area of the this section and thereby increasing the resistances. As this region carries the full current during a short-circuit, an increased resistance in this region causes a local heating in this point during a short-circuit[15].

Finally, the drift layer resistance is caused by the lower doping concentration in the drift

layer. This layer is needed to obtain the desired voltage rating. As the voltage rating of the device is increased the thickness of the drift layer has to be increased to achieve the needed breakdown voltage, increasing the drift region resistance. [14]

Description of Model 3

To investigate the effects of short-circuits, it is desired to build a TCAD model of the chip under investigation, the SiC MOSFET CPM2-1200-0080B from Cree [16]. In this chapter, the dimensions and doping profiles of the TCAD model will be described.

3.1 Geometry of Model

As the geometry of the device under investigations is unknown, the geometry is inspired by a model made by Romano et. al. [15], which consider the same device but in a previous generation. The main takeaway from this model is the width of the device, $8.7\mu m$ which will be considered to be the fixed width of the device. Furthermore, the width and shape of the source and channel region from this device will be used. The borders of this half-cell without doping concentrations is shown in Fig. 3.1.

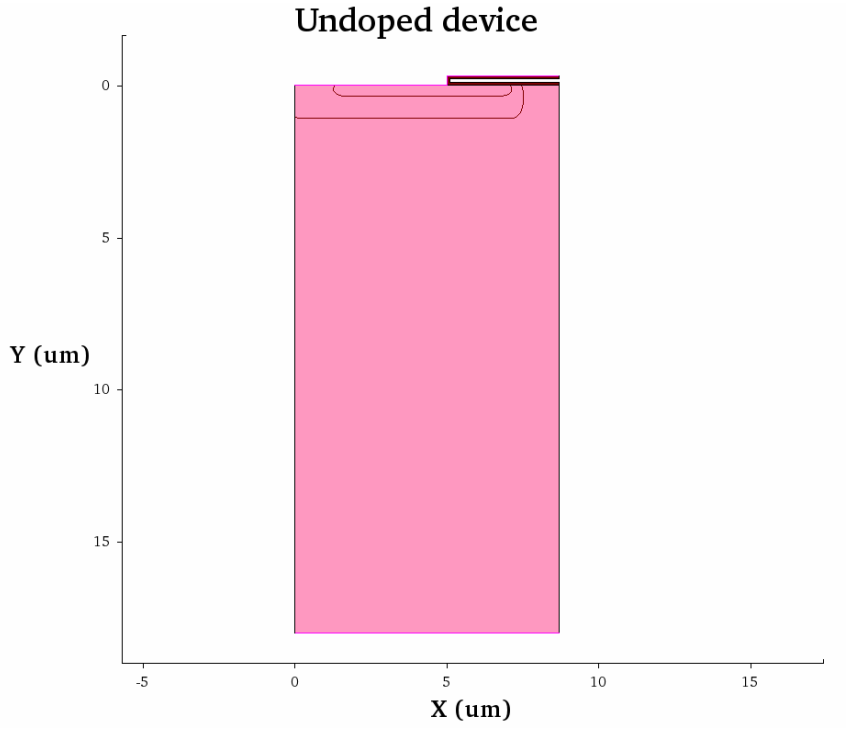

Figure 3.1. The geometry used for these investigations. All dimensions are in μm.

With this starting point, the different geometries and doping concentrations of the device is modeled through a combination of analytical calculations and iterations.

3.2 Determination of drift region characteristics

As the doping profile of the actual chip under investigation is unknown, the starting point is to determine the doping level of the different regions of the vertical MOSFET presented in Fig. 2.1.

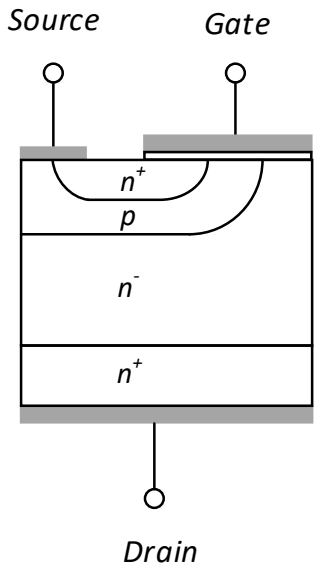

Figure 3.2. The different doping regions of the half-cell shown in Fig. 3.1.

The first two parameters to be determined are the width and the doping concentration of the n^- region, also known as the drift region. The drift region has a lower doping concentration than the n^+ regions, in order to allow the electric field to build up in this layer.

Since the main purpose of the drift layer is to sustain the drain-source voltage, the needed width of the drift layer is calculated from this requirement. The electric field is has a triangular shape, which extends to the end of the drift region with a peak at the PN-junction as seen in Fig. 3.3.

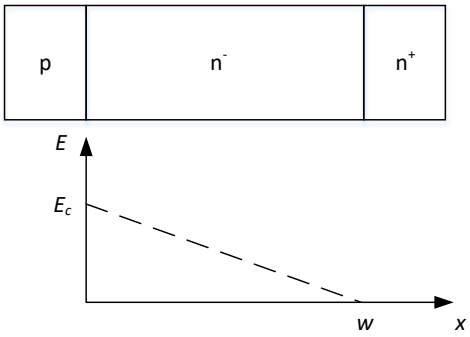

Figure 3.3. The desired shape of the electric field, when a reverse voltage of 1200 V is applied.

The applied voltage can be found from the integral of the electric field. As seen from Fig. 3.3, the desired electric field is triangular, thus the integral of this electric field can be found from

$$V = \frac{E \cdot w}{2} \tag{3.1}$$

The amplitude of the electric field should not exceed the critical electric field for 4H-SiC, in order to avoid the breakdown of the device. Therefore, the needed drift region width can be calculated from

$$w = \frac{2 \cdot BV}{E_c} \tag{3.2}$$

where BV is the desired breakdown voltage, 1200 V for the device considered in this work, and E_c is the critical electric field for 4H-SiC at 300 K , $2.2 \cdot 10^6$ V/cm [11]. From this, the needed width in order to obtain a breakdown voltage of 1200 V has been found to be 10.9 μm.

To ensure that the electric field extends to the end of the drift region when the applied voltage is at the breakdown voltage, the doping concentration of drift region must be adjusted to obtain the needed slope of the electric field. The decrease in the electric field can be found from Gauss' Law in one dimension [17].

$$\frac{dE}{dx} = \frac{\rho}{\epsilon} \tag{3.3}$$

where $\frac{dE}{dx}$ is the slope of the electric field along the drift region, ρ is the charge density, and ϵ is the total permittivity of the region. Assuming that a constant doping concentration across the entire drift region, the charge density will be $-q \cdot N_d$, where the sign is caused by the negative charge of electrons. The permittivity will be the permittivity of 4H-SiC. The slope of the electric field per unit width can then be found by

$$\frac{dE}{dx} = -\frac{q \cdot N_d}{\epsilon_r \cdot \epsilon_0} \tag{3.4}$$

where q is the elementary charge $1.6 \cdot 10^{-19}\ C$, N_d is the doping concentration of the drift region, ϵ_s is the relative permittivity of 4H-SiC 9.66, and ϵ_0 is the vacuum permeability $8.85 \cdot 10^{-14}\ F/cm$.
To ensure that the electric field is zero by the end of the drift region, the doping concentration is found by

$$E_c - \frac{q \cdot N_d}{\epsilon_r \cdot \epsilon_0} \cdot w = 0 \tag{3.5}$$

which can be rearranged to

$$N_d = \frac{E_c \cdot \epsilon_r \cdot \epsilon_0}{q \cdot w} \tag{3.6}$$

Using Eq. 3.6, the required doping concentration of the drift region can be found to be $1.07 \cdot 10^{16}\ cm^{-3}$.

Using this drift region doping, the device is simulated during the blocking state. As recommended by Sentaurus [18], a transient simulation is used with a relatively low slew rate of 1 V/s. At the same time, the size of the floating points used for the simulation is increased. This is required due to represent the very low values of the intrinsic current in 4H-SiC [18].

It is seen from Fig. 3.4, that the current is negligible, until the device breaks down at $V_{DS} = 1150\ V$. The simulation is stopped at this point as the drain current exceeds the 100 μm that is given as the test condition for the blocking voltage in the datasheet of the chip [16].

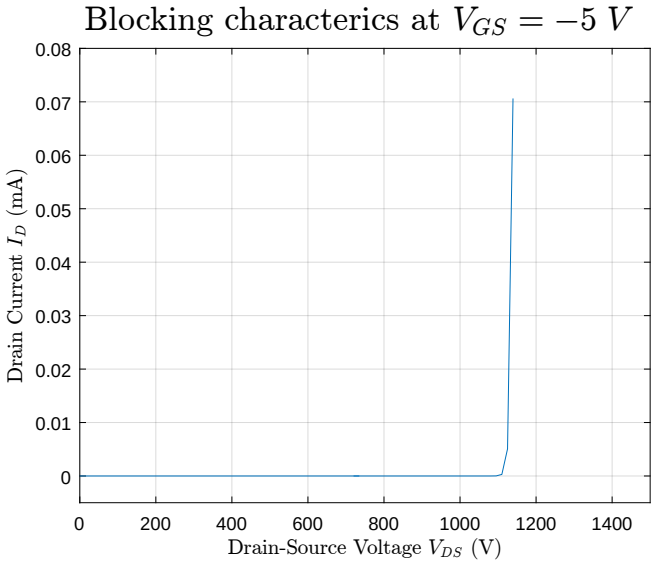

Figure 3.4. The drain current during a blocking state. The current rises abruptly at $V_{DS} = 1150\ V$.

The electric field at $V_{DS} = 1000\ V$ seen in Fig. 3.5. In this the cutline for evaluating the electric field is also shown. This will be used for Fig. 3.6, where the electric field is plotted
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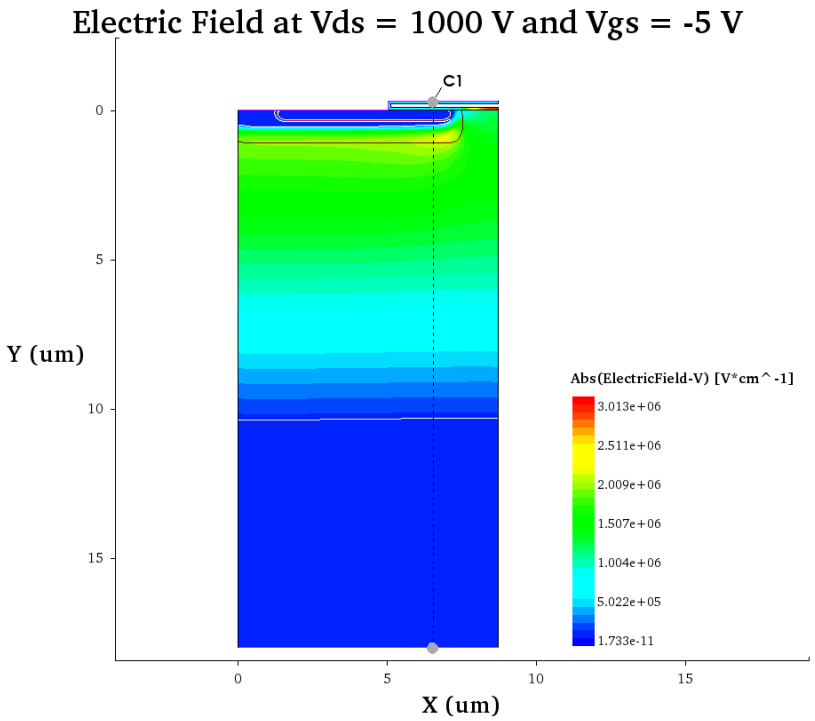


Figure 3.5. The electric field at $V_{DS} = 1000\ V$ and $V_{GS} = -5\ V$

It is see that the electric field has a maximum at the round of the p-well. Therefore, a cut is made along the device at this position for a different voltages during the breakdown simulation. The electric field along this cut line can seen in Fig. 3.6.

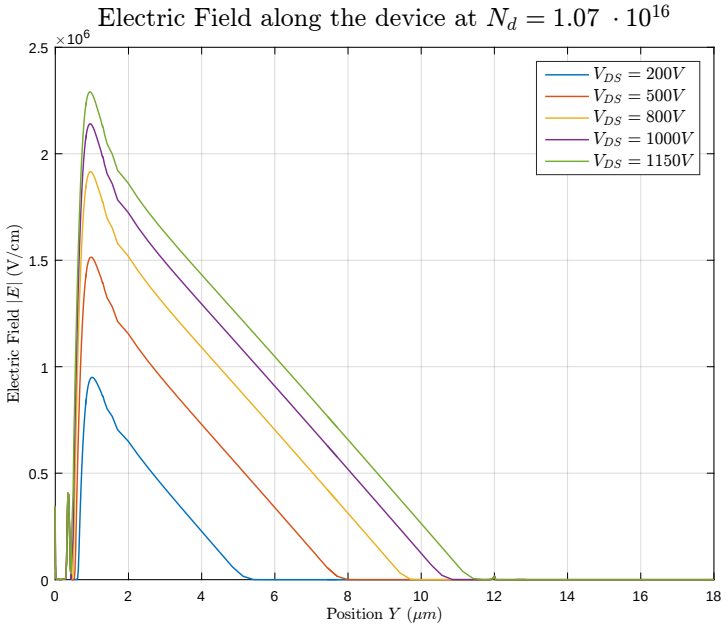


Figure 3.6. The simulated electric field along the device with the used doping profile and width.

Two things can be noted from this figure. First of all the electric field at the PN-junction reaches the critical electric field for 4H-SiC, 2200 kV/cm, at the instance of the breakdown. Secondly, the electric field is zero at the end of the drift region at the point of breakdown as calculated.
With this parameter fixed, the next task is to determine the area factor to achieve the desired current density of the device.

3.3 Calculation of Area Factor

To reduce the computational requirements, the simulated device is a 2D cross-section of the full 3D structure. As the current characteristics depends on the out-of-plane width of the device, there is a need to account for this simplification of the model. In Sentaurus, this is done by including an area factor, which is the ratio between the simulated top surface of the chip and the actual surface of the chip.

By default, Sentaurus assumes a device thickness of 1 μm. As the modeled device has a width of 8.7 μm, this gives a modeled surface area of 8.7 μm^2.

The surface of the real device can be found in Fig. 3.7.

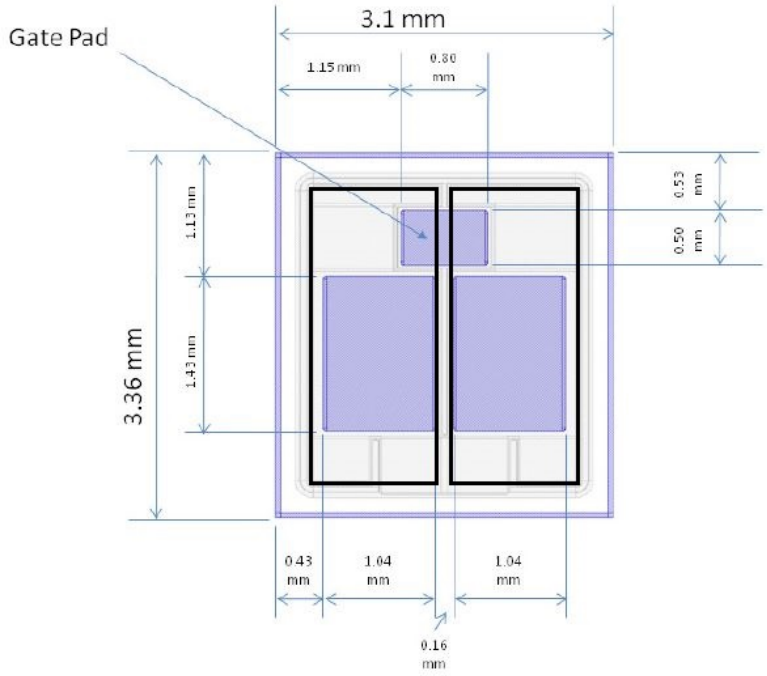


Figure 3.7. The surface area of the real device. The black rectangles indicate the area approximated as the active area. Modified after [16].

As an approximation, the active area is considered to be the entire surface of the chip neglecting the corners and a small area for the gate connections. This approximated active area of the device has a surface area of $6.339 \cdot 10^6$ μm^2 and therefore the starting

point for the area factor is

$$AF = \frac{6.339 \ \cdot \ 10^6 \ \mu m^2}{8.7 \ \mu m^2} = 7.28 \cdot 10^5 \tag{3.7}$$

However, as this is a rough approximation, the actual value of the area factor will be adjusted to fit the IV-characteristics of the device.

3.4 Determination of Threshold Voltage and Transfer Characteristics

The next characteristics to consider are the threshold voltage and the transfer characteristics. The threshold voltage is needed to form the channel, in which the current can flow from the drain to the source. The threshold voltage consists of three different terms due to different barriers that needs to be overcome for the channel to be formed. The equation is given by

$$V_T = \theta_{MS} + \Delta V_{ox} + V_s \tag{3.8}$$

The first term due to differences in the so-called work function of the two materials in contact with each other. This is the potential needed to ensure that the potential of the materials are identical. For simplicity it is often assumed that the two materials have the same work function, $\theta_m = \theta_s$, and therefore $\theta_{ms} = 0$.

The second term is the voltage drop across the gate oxide. This voltage drop is proportional to the surface charge stored at top of the oxide, hence at the interface between the gate oxide and the gate contact.

$$\Delta V_{ox} = \frac{Q_m}{\epsilon_{ox}} \cdot t_{ox} \tag{3.9}$$

where Q_m is the stored charge, ϵ_{ox} is the permittivity of the gate oxide, and t_{ox} is the thickness of the gate oxide.

The stored charge on the oxide is derived by [11] to be

$$Q_M = \sqrt{4 \cdot N_A \epsilon_{si} \cdot k \cdot T \cdot ln(\frac{N_A}{n_i})} \tag{3.10}$$

where k is the Boltzmann constant, $1.38066 \cdot 10^{-23} \ J/K$, T is the temperature in Kelvin, N_A is the doping concentration of the channel, and n_i is the intrinsic current of the device, the current that is flowing when no voltage is applied.
Therefore, the voltage drop across the gate oxide can be found from

$$\Delta V_{ox} = \frac{\sqrt{4 \cdot N_A \epsilon_{si} \cdot k \cdot T \cdot ln(\frac{N_A}{n_i})}}{\epsilon_{ox}} \cdot t_{ox} \tag{3.11}$$

Substituting the capacitance per unit area $C_{ox} = \epsilon_{ox}/t_{ox}$, the voltage drop across the gate oxide can be found to be

$$\Delta V_{ox} = \frac{\sqrt{4 \cdot N_A \epsilon_{si} \cdot k \cdot T \cdot ln(\frac{N_A}{n_i})}}{C_{ox}} \tag{3.12}$$

The third term is the voltage needed to raise the potential of the channel region enough to become conducting. This is known as strong inversion. The difference in potential energy is derived in [11] to be

$$\Delta E = 2 \cdot k \cdot T \cdot ln(\frac{N_A}{n_i}) \tag{3.13}$$

This energy is related to the potential energy by

$$V_s = \frac{\Delta E}{q} = 2 \cdot \frac{k \cdot T}{q} \cdot ln(\frac{N_A}{n_i}) \tag{3.14}$$

where q is the elementary charge.
Combining all of these three equations, the final expression ends up being

$$V_T = \frac{\sqrt{4 \cdot N_A \epsilon_{si} \cdot k \cdot T \cdot ln(\frac{N_A}{n_i})}}{C_{ox}} + 2 \cdot \frac{k \cdot T}{q} \cdot ln(\frac{N_A}{n_i}) \tag{3.15}$$

From this equation, it is seen that for the same temperature, two parameters can be varied: Either the gate capacitance, C_{OX}, can be modified or the concentration of acceptor doping can be changed.
The change of the C_{ox} corresponds to a change in the properties of the gate, such as other dimensions or the use of a gate material with a higher permittivity. For high voltage devices, a gate thickness of 50 nm, and the material SiO_2, are often used hence these parameters are not changed.

As the gate properties are fixed, the acceptor doping of the p-well is modified to achieve the desired threshold voltage. As a starting point, a channel doping of $N_A = 2 \cdot 10^{17}\ cm^{-3}$ is considered, as this is the value suggested in the original model from Romano et al [15]. The resulting transfer characteristic is shown in Fig. 3.8, where the simulated results are compared with the transfer characteristics given in the datasheet at $25^\circ\ C$.

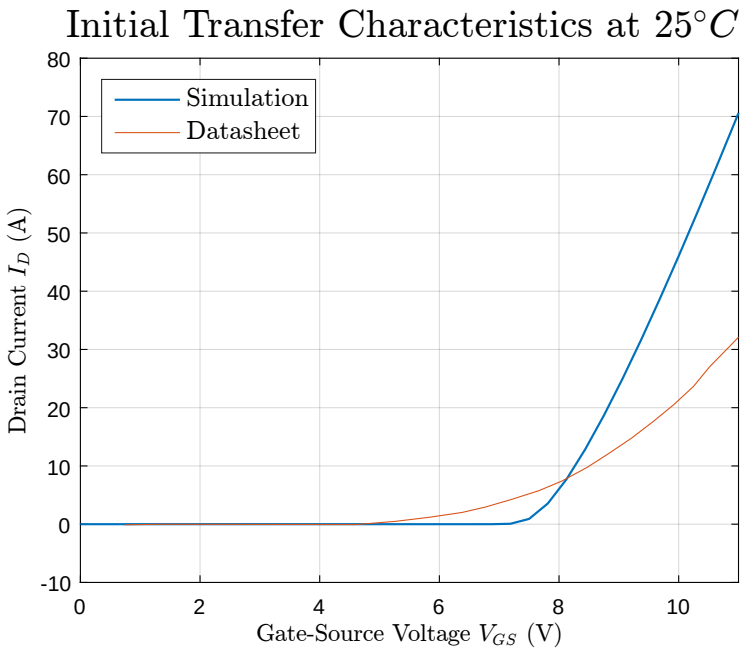


Figure 3.8. A comparision of the transfer characteristics of the initial simulation and the datasheet at 25° C.

From this figure, two differences between the simulations and the real device can be seen. The simulated threshold voltage is higher than the threshold voltage of the real device. At the same time, the transconductance of the simulated device is higher than the one of the real device.
As explained by Eq. 3.4, the threshold voltage can be lowered by decreasing the doping concentration of the channel region. The transconductance can be lowered by changing some of the parameters in Eq. 2.6. The two parameters that are adjustable are the out-of-plane width of the channel or the length of the channel. From Eq. 2.6 it is noted that the transconductance decreases when the out of plane- width of the channel decreases. Therefore, the area factor is modified as this corresponds to decreasing the out-of-plane width of the device.

As a starting point for obtaining the correct threshold voltage,the channel doping is reduced as this reduces the threshold voltage. The variation of the transfer characteristics as a function of the p-well doping in the channel region is presented in Fig. 3.9. At the same time, the area factor is to reduced as the lower out-of-plane width, which leads to a smaller transconductance.

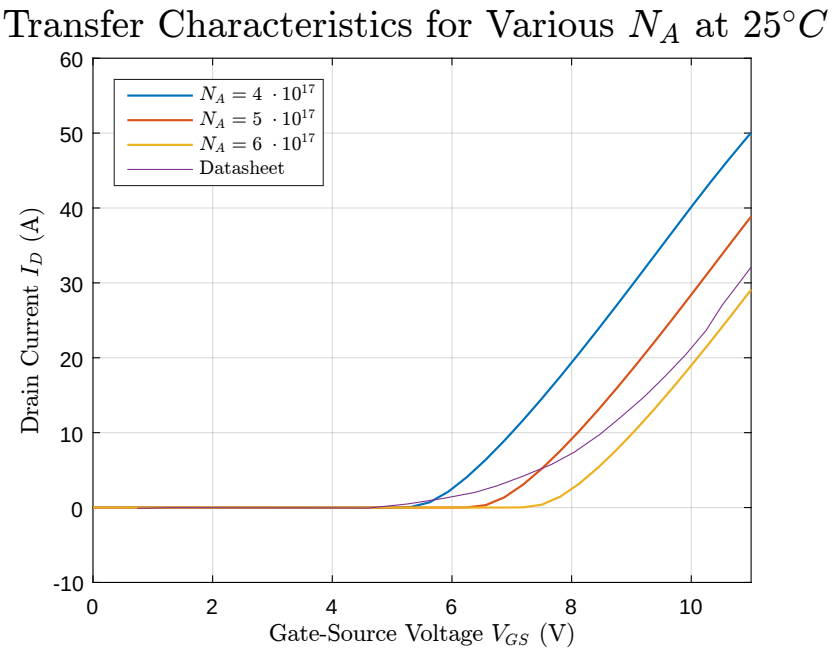


Figure 3.9. Variation of the channel doping to achieve the desired transfer characteristics using an area factor of $3 \cdot 10^5$.

The results of Fig. 3.9 show that the lowered chosen area factor of $3 \cdot 10^5$ results in a transconductance that resembles the real device. It is also seen that a doping concentration between $N_A = 5 \cdot 10^{17}\ cm^{-3}$ and $N_A = 6 \cdot 10^{17}\ cm^{-3}$ give approximately the desired transfer characteristics during the on-state of the device when a high gate voltage is applied. However, it is also seen that while the simulated device has a relatively well-defined threshold voltage, the real device has a lower threshold voltage but does not reach the full transconductance before a significantly higher gate voltage is applied.

The difference between the modeled threshold behavior and the datasheet can be explained by the assumption of a perfect interface between the gate oxide and the 4-H SiC. Non-idealities at this interface is shown in other works to cause shifts in the threshold voltage as presented in Fig. 3.10 [19] .

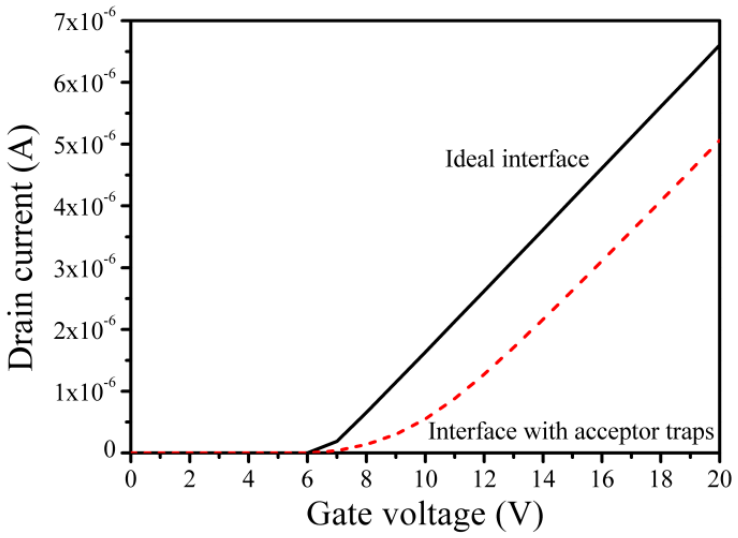


Figure 3.10. The shift in threshold voltage due to non-idealities at the gate oxide. The transconductance is identical, but shifted due to the defects [19].

The figure shows the same difference between an ideal interface and an interface with traps, as the difference between the simulated characteristics and the datasheet values. It is recommended both by Sentaurus [18] and Romano et. al [15], to include these material defects to obtain higher accuracy of the threshold voltage.
However, as multiple types of interface traps exists, a full analysis of this is outside the scope of this project. It can be noted from Fig. 3.10 that at higher gate voltages the transconductance of the non-ideal device is identical to the one of the ideal device, but shifted due to the interface traps.
Therefore, the device will have the same transfer characteristics in a fully on state, which is the desired area of operation, with a ideal interface that resembles the behavior in this area. This is achieved by using a doping concentration of $N_A = 5.7 \cdot 10^{17}\ cm^{-3}$ in the channel region.

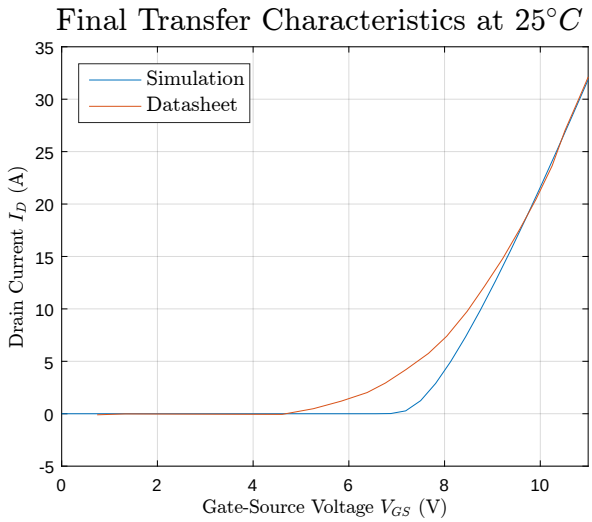


Figure 3.11. A comparison between the simulated characteristics and the datasheet values at 25° C using $V_{DS} = 20\ V$, $N_A = 5.7 \cdot 10^{17}\ cm^{-3}$, and $AF = 3 \cdot 10^5$.

It can be noted from the figure that the transfer characteristics of the simulated device approximately resembles the characteristics of the real device in the high gate voltage region. In Fig. 3.12 the transfer characteristic for the model of the device up to $V_{GS} = 20\ V$ oat a temperature of 25° C and a Drain-Source Voltage of 20 V.

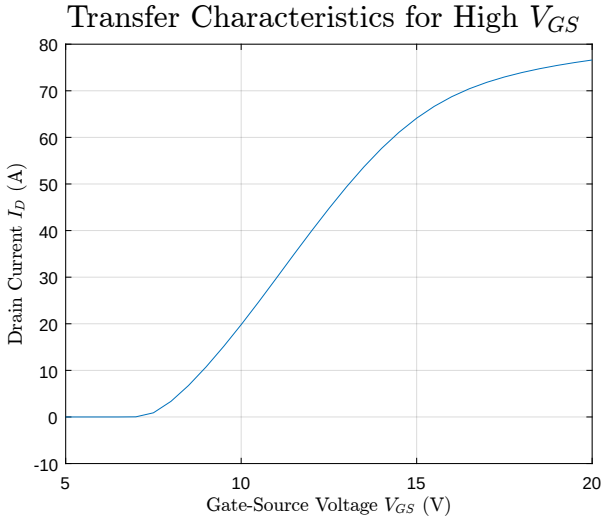


Figure 3.12. The full transfer characteristics at $V_{DS} = 20\ V$, $T = 25°\ C$, $N_A = 5.7 \cdot 10^{17}\ cm^{-3}$ and $AF = 3 \cdot 10^5$

3.5 Presentation of Output Characteristics

In Fig. 3.13, the output characteristics at 25° C are presented. As previously explained, the IV-characteristics of the device depend on the applied gate voltage. Hence each of the lines correspond to a gate voltage starting at $V_{GS} = 12\ V$ increasing with 2 V to $V_{GS} = 20\ V$

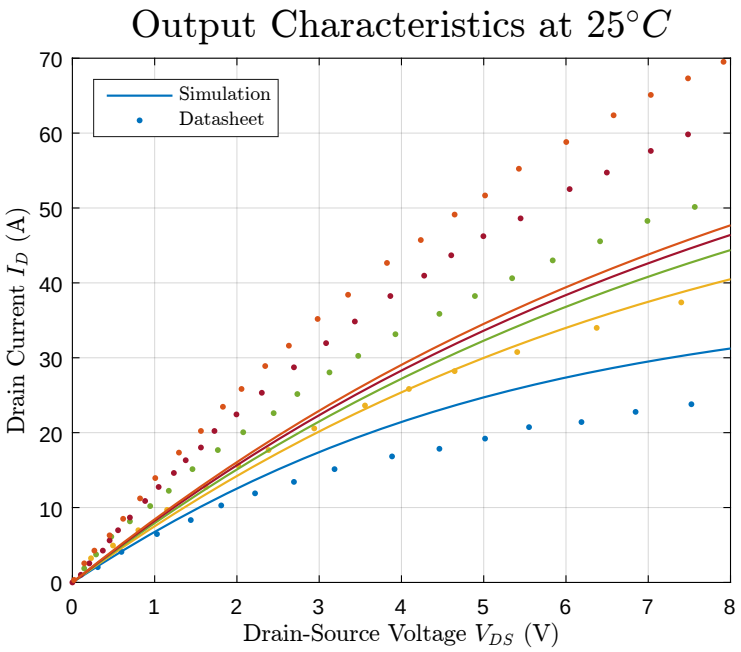


Figure 3.13. The output characteristics of the modelled MOSFET at a junction temperature of 25° C with gate voltages increasing from $V_{GS} = 12\ V$ increasing with 2 V to $V_{GS} = 20\ V$.

As seen from this figure, the device does not resemble the output characteristics very well. This can be caused by the area factor, but as the change of the area factor implies a change of the transfer characteristics, a further improvement would require the geometry of the device to be changed. Another possibility is that it is due to the that the channel properties are changed due to the neglegtion of the traps at the interface.

In Fig. 3.14 the current flow of the device during on-state is shown. In this case the flow is shown for $V_{GS} = 20\ V$ and $V_{DS} = 5\ V$.

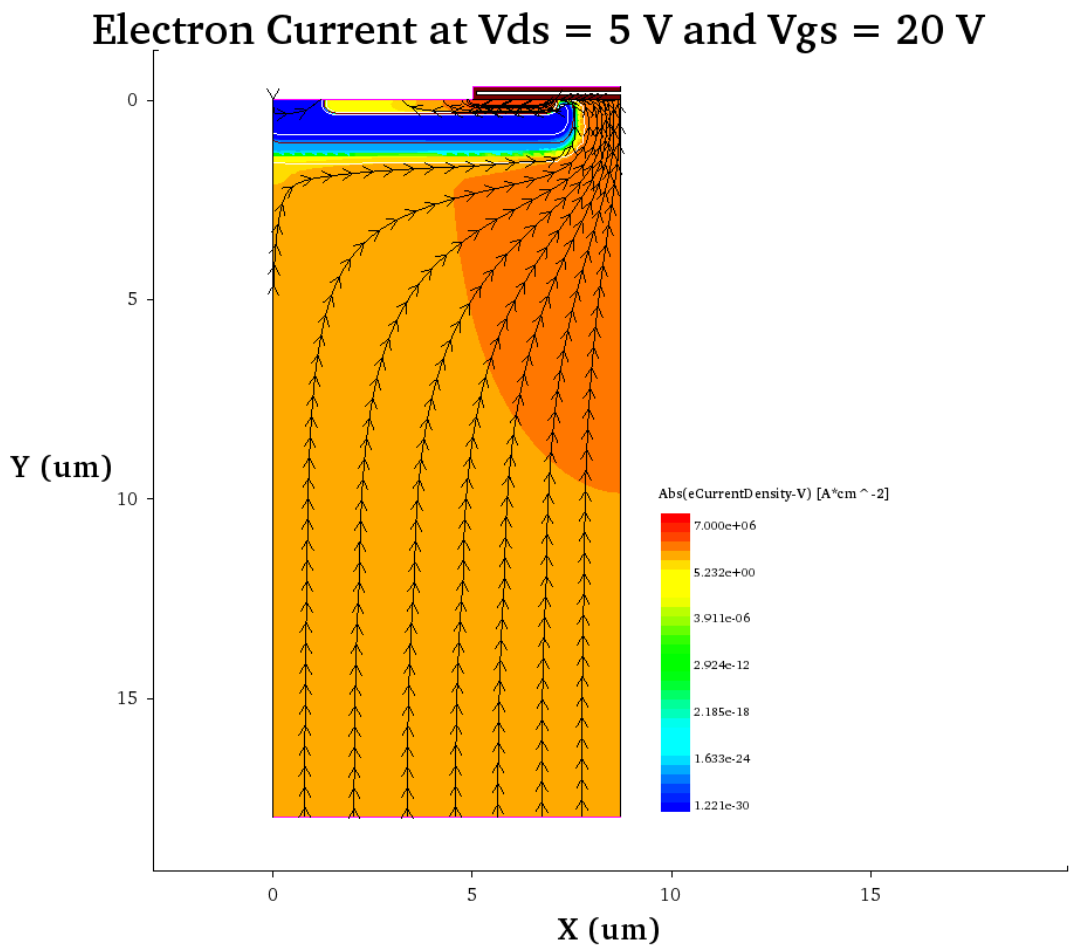


Figure 3.14. The electron current streamlines at $V_{GS} = 20\ V$ and $V_{DS} = 5\ V$. It is seen that all current is flowing through the channel, and that a uniform distribution thorough the channel region is achieved.

It is seen that the current flows through the channel as desired. At the same time, a uniform current distribution is seen through the JFET region. The current spreading through the JFET region is also seen in 3.15, which present a zoomed view of the channel and JFET region of Fig. 3.14.

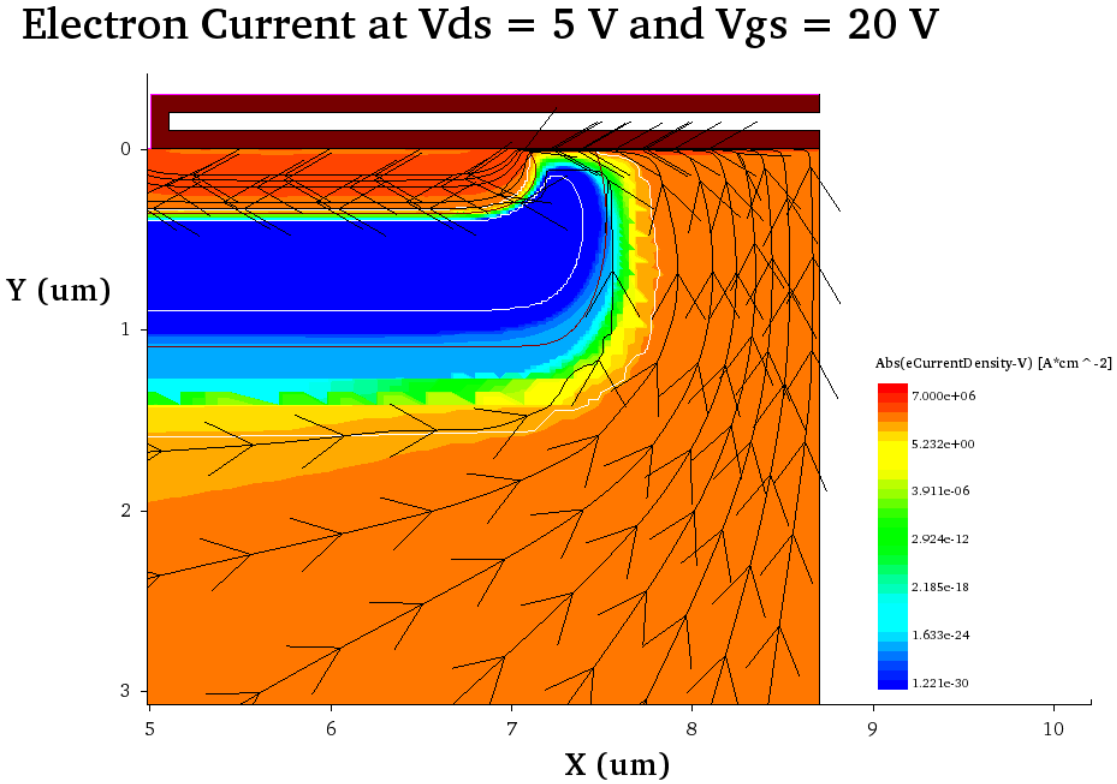


Figure 3.15. The electron current streamlines in the channel region at $V_{GS} = 20\ V$ and $V_{DS} = 5\ V$. The current is flowing close to the gate contact due to the higher conductivity of the channel in

From this figure, also the accumulation resistance can be seen. As explained in section 2.3, there is a small increase in resistance due to the fact that the channel is most conductive near the gate contact and therefore the current tends to flow there.

In Fig. 3.16, the current spreading at $V_{DS} = 50\ V$ and $V_{GS} = 20\ V$ is shown.

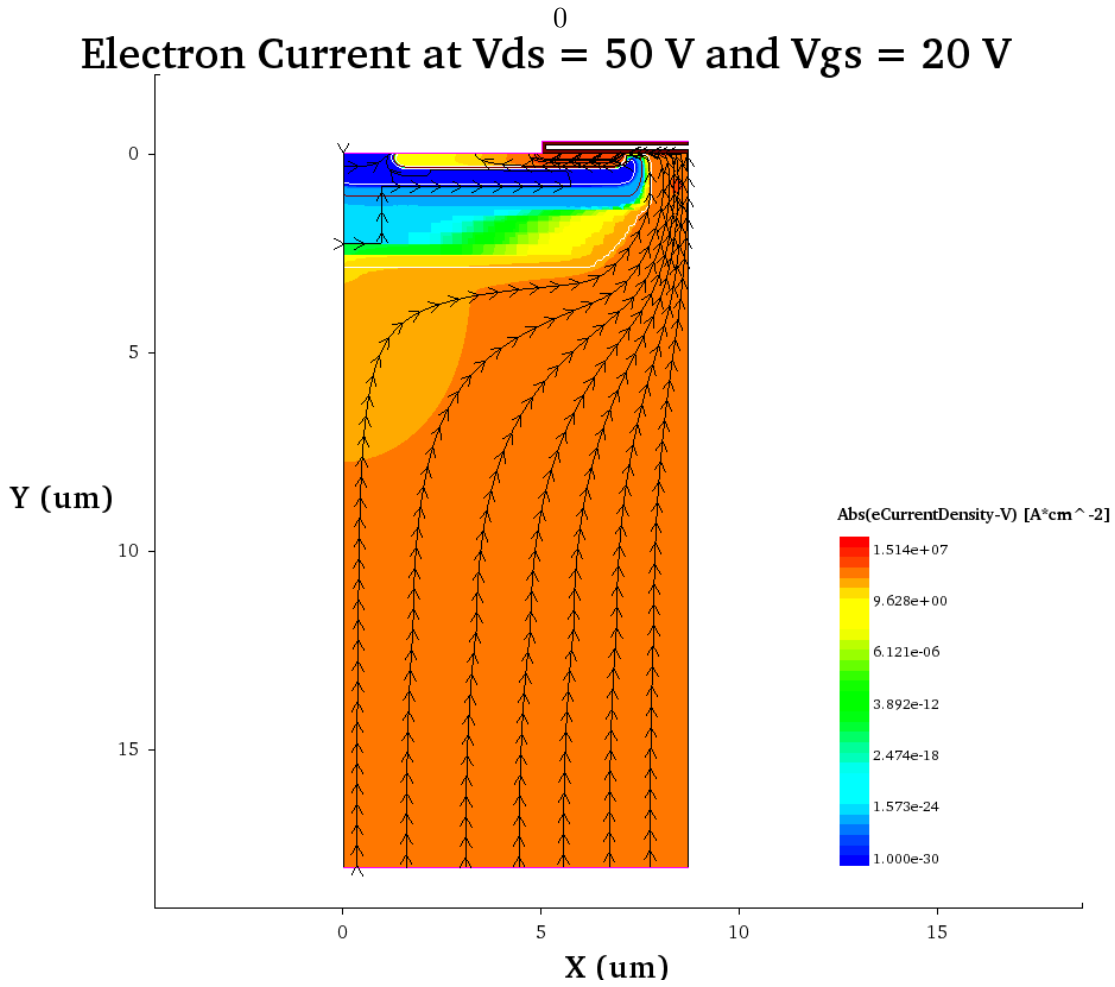


Figure 3.16. The electron current streamlines at $V_{GS} = 20\ V$ and $V_{DS} = 50\ V$. Due to the JFET effect, the current density is higher at positions away from the PN junction, reducing the effective cross-sectional area.

Due to the higher voltage, a larger depletion layer is seen next to the PN junction. This results in a less uniform spreading of the drain current.

In Fig. 3.17, the electrostatic potential is shown for $V_{DS} = 5\ V$. A solution at $V_{DS} = 0\ V$ has been subtracted to compensate for the potential difference due to the different work functions of the materials, and the applied gate voltage.

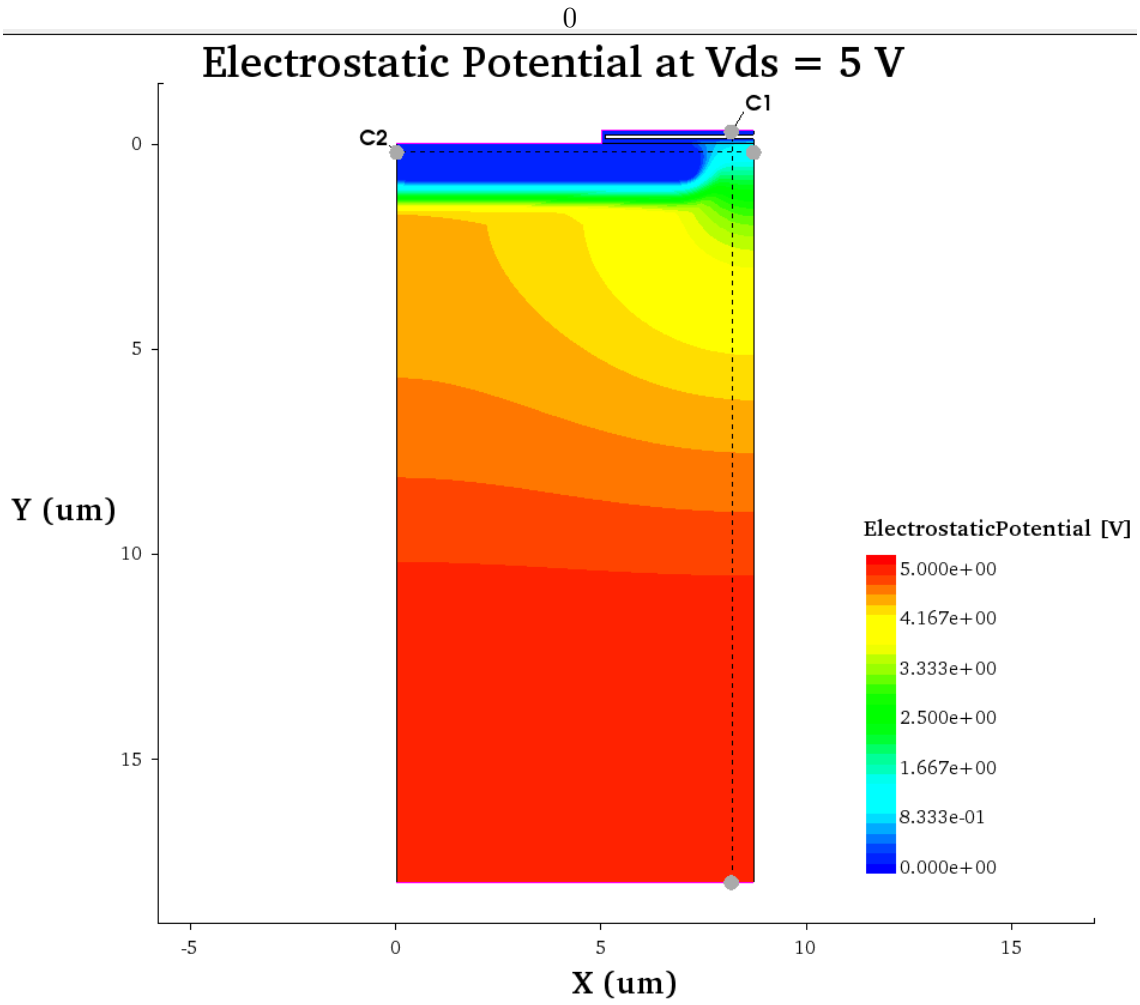


Figure 3.17. The electrostatic potential at $V_{DS} = 5\ V$. A solution at $V_{DS} = 0\ V$ has been substracted.

As expected the drain contact is at 5 V, and the source contact is at 0 V. In Fig. 3.18 and Fig. 3.19, the potential along the two cutlines are presented.

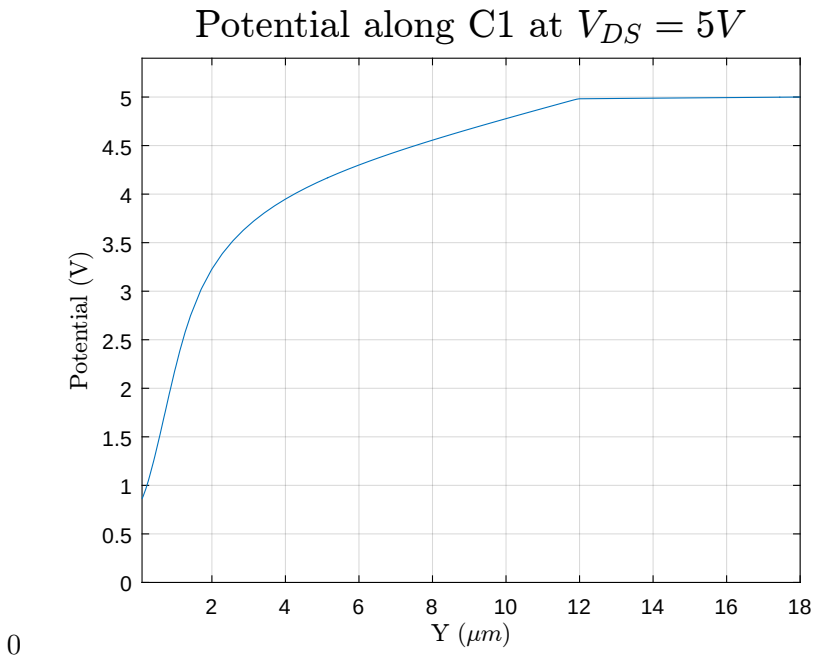


Figure 3.18. The electrostatic potential along C1. The potential rises quickly across the drift region due to the large resistance.

Fig. 3.18, shows that much of the potential drop occurs across the drift region due to the large resistance of this region. The potential is almost identical in the entire highly doped substrate region from $Y = 12\ \mu m$ to $Y = 18\ \mu m$. Similarly, the potential is plotted along C2 which cover the source region and the channel.

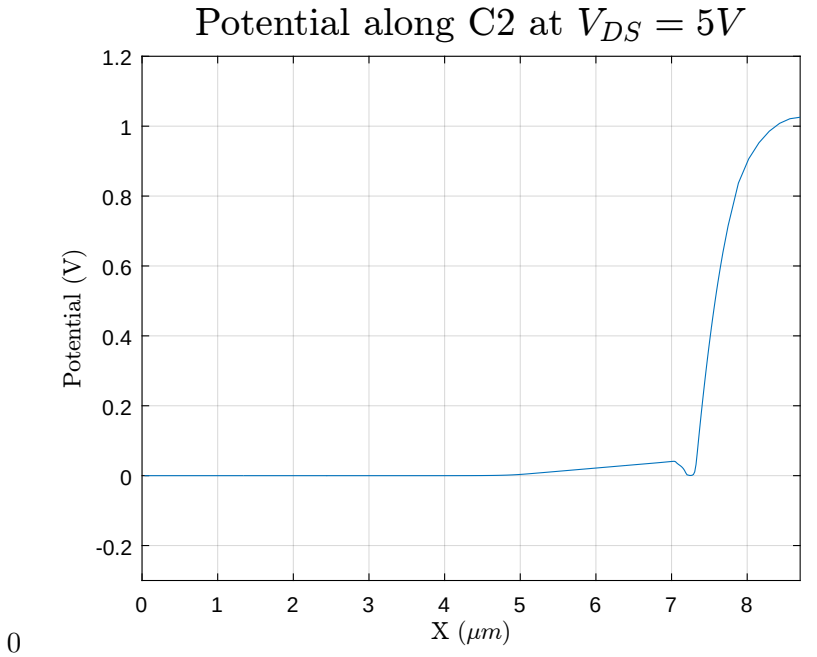


Figure 3.19. The electrostatic potential along C2. A voltage drop of approximately 1 V occur across the channel.

From this it is seen that the source contact is at 0 V as previously mentioned. A voltage drop of approximately 1 V is seen across the channel, which also corresponds with the potential found from C1. With these characteristics documented, the model is considered finalized and is presented in the next section.

3.6 Model Overview

As the different doping concentrations and parameters have been determined, an overview of the model is presented in this section.

An overview of the device is presented in Fig. 3.20. The parameters that have not been determined in this chapter is taken from the original model by Romano [15].

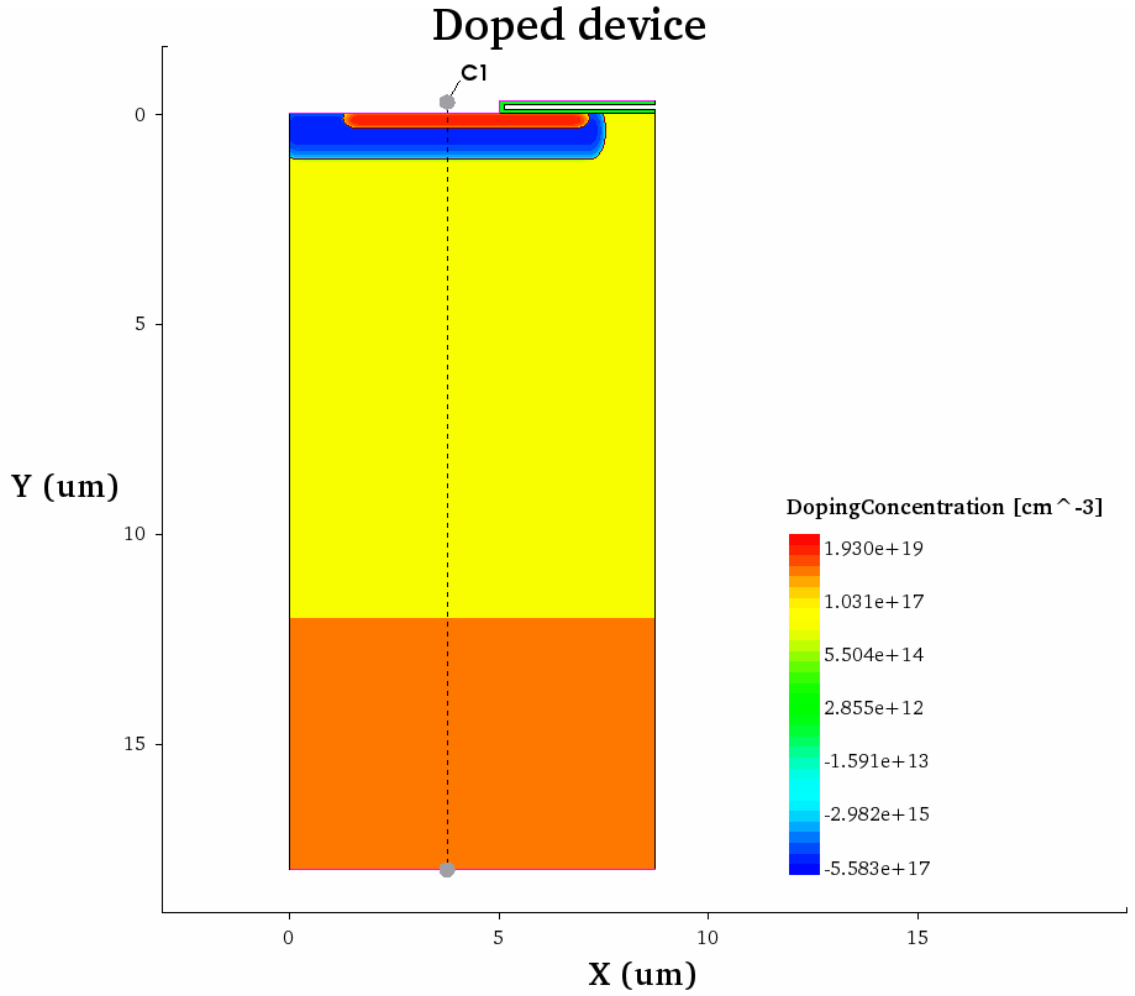


Figure 3.20. The final model with identifications of the doping levels. The doping concentrations of the different regions are also given in Table 3.1.

The doping concentration along the cutline C1 is presented in Fig. 3.21, where the absolute value of the doping concentration has been extracted in order to present both the acceptor and donor concentration in the same plot.

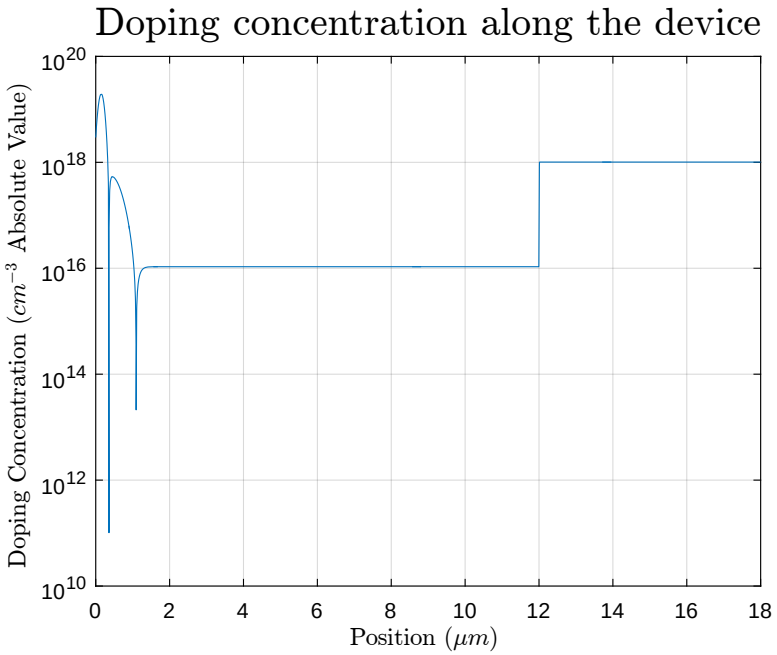


Figure 3.21. The magnitude of the doping profile along the device.

From this figure, the doping concentration of the four different regions are seen; the source region, the p-well region, the drift region, and the drain region. At all PN or NP junctions, the doping concentration is gradually reduced in order to reduce the gradients at the interface between the two doping types.

The peak values of the doping concentrations can also be seen from Table 3.1.

Table 3.1. Doping concentrations for the final device

Region	Peak Concentration	Unit
Source	$2 \cdot 10^{19}$	$[cm^{-3}]$
Channel	$5.7 \cdot 10^{17}$	$[cm^{-3}]$
Drift	$1.07 \cdot 10^{16}$	$[cm^{-3}]$
Drain	$1 \cdot 10^{18}$	$[cm^{-3}]$

With the device model implemented, the theory of failures due to short circuits is investigated in the following chapter.

Short Circuit Capability of SiC MOSFETs 4

One of the major reliability concerns of high power modules is the capability of withstanding an externally applied short-circuit, the so-called short-circuit capability. In this section, the different failure mechanism due to short circuit will be explained.

4.1 Description of Short-Circuit Behavior

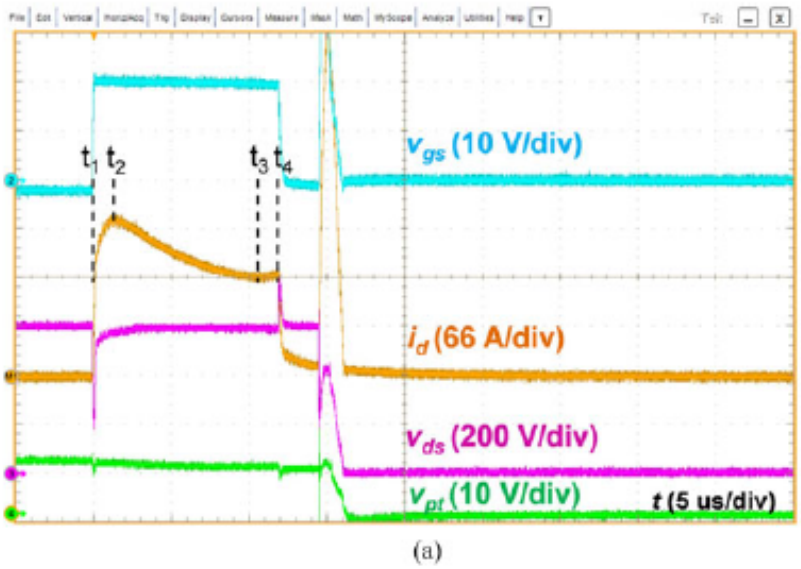
During a short-circuit, high voltage and high current is simultaneous applied to the device, hence a high power is dissipated in the device. This may occur if two devices in the same inverter leg is turned on simultaneous, for example due to the failure of a gate driver, or a second turn-on because of induced EMI. This high power is applied until the gate driver has detected the failure and the device is turned off. Often this time is in the order of 10 μs, as this is a usual short-circuit withstand time of a conventional Si IGBT [20].

The power applied to the device is determined by the applied voltage across the device, and the characteristics of the device in its saturation region. The dissipated energy can be found by the integral of this power [2].

$$E_{sc} = \int_0^{t_{sc}} V_{DS}(\tau) \cdot I_D(\tau)\, d\tau \tag{4.1}$$

Where V_{DS} is the voltage across the device, I_D is the drain current, t_{sc} is the time period before the device is turned off, and τ is an integration variable.
The energy dissipated in the device will result in an increased temperature. This increased temperature can cause a so-called thermal runaway. In this failure mode, the device does not fail immediately at the time of the short-circuit. Instead an increased leakage current is seen after the shut-off of the device due to the higher internal temperature of the device. Because of the combination of a high blocking voltage and an increased current, a high amount of power is generated in the device despite the fact that the short-circuit conditions are no longer present. If this power is higher than the power transfered away from the hot-spot, the temperature will increase even further. This will results in an even bigger leakage current, creating a positive feedback mechanism that leads to a thermal runaway.

Wang et al. [1], the so-called Short-Circuit Withstand Time (SCWT) was investigated. It was investigated how long time a 1200 V device from Cree can sustain short-circuit conditions. One of these short-circuit tests is shown in Fig. 4.1.



(a)

Figure 4.1. A 1200 V device subject to a short circuit, with the different time periods marked [1].

From this figure the dynamics of the current during short-circuit conditions can be seen. During the first period, from t_1 to t_2, the current rise is limited by the stray inductance of the connecting circuit. This limits the slope of the current, avoiding that the current reaches the saturation current of the device immediately.

In the following period from t_2 to t_3 the current is limited by the maximum saturation current of the MOSFET. As explained in Chapter 2, this saturation current depends on the electron mobility in the material and therefore it changes during the short-circuit. This occurs due to the influence of temperature on the electron mobility in the device. One suggested model for the temperature is given by [21]

$$\mu(T) = 1140 \cdot (\frac{T}{300})^{-2.70} \tag{4.2}$$

where T is the temperature in Kelvin. This implies that the current of the device will drop as more energy is dissipated in the device, as it is also seen in Fig. 4.1.

From t_3 to t_4 the current is no longer decreasing. This can be explained by the increasing temperature of the device. As the temperature increases, the leakage current rises due to the rise of the so-called intrinsic current. This current rises exponentially when the temperature is increased [11].

$$n_i \propto \left(\frac{E_i}{2 \cdot k \cdot T}\right) \tag{4.3}$$

where E_i is the bandgap of 4H-SiC, k is the Boltzmann constant, and T is the temperature in Kelvin. At the same time the temperature is rising at a lower rate due to the lower drain current. For this device, this means that the leakage current is increasing faster than

the saturation current is decreasing due to the lower electron mobility.

Finally, at t_4 the gate driver has detected the short circuit and switched the device off. Ideally, this would imply a negligible current flowing through the device. However, due to the high internal temperature an increased leakage current is still present because of the thermally generated intrinsic current . This current causes an additional heating of the device, which eventually causes the device the fail in a thermal runaway. Whether this failure mode would occur was found to depend on how much energy was dissipated during the short-circuit. If the critical energy level is not exceeded, the temperature will not rise sufficiently to cause a thermal runaway due to the thermally generated current. [1]
Even if the dissipated energy is not sufficient to generate a thermal runaway, the device might still fail due to a damage to the gate oxide [22]. This can either cause a thermal runaway due to gate leakage, or a failure due to a melting of the surface metalization.

This has also been shown by [23], which showed that the gate oxide is subject to a degradation when it is exposed to multiple low energy pulses. Each of these pulses did not dissipate enough heat to generate a thermal runaway, but as the gate oxide was degrade

4.2 Failure mechanisms due to short-circuit

After the short-circuit, the device can either fail catastrophically with a rapid increase in the drain current, or non-catastrophic non-catastrophic with a short-circuit of of the gate.

Romano et al. [15] tested devices at different values of DC-link to investigates failures that happens at different DC-link voltages and different short-circuit times, to investigate the impact of different voltages and durations.
In this, it is suggested that failures can occur either due to a surface degradation of the chip, or due to a thermal runaway because of a local heating of device. The surface degradation causes a short circuit between the gate and the source, resulting in an inability to turn on the device after the short circuit, while the thermal runaway caused an excessive drain current.
An example of the two different cases are shown in Fig. 4.2 for a short pulse of 5 μs with a high DC-link voltage, and Fig. 4.3 for a longer pulse of 17 μs with a lower DC-link voltage.

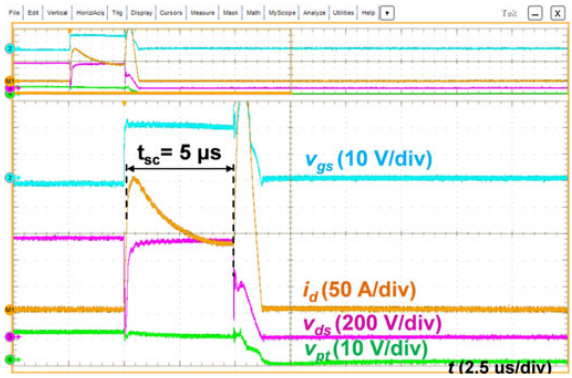


Figure 4.2. A low duration short-circuit test with $V_{DC} = 750\ V$ and $t_{sc} = 5\ \mu s$. A thermal runaway is seen by the high current after shut-off [1].

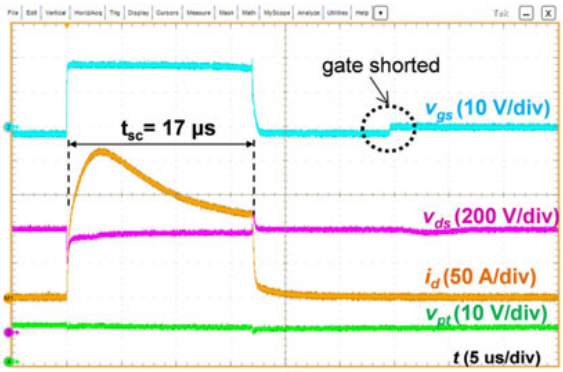


Figure 4.3. A longer duration test with $V_{DC} = 600\ V$ and $t_{sc} = 17\ \mu s$. No thermal runaway is seen, but the device fails due to shorted gate [1].

From this, it is seen that the fast pulse causes a thermal runaway due to energy dissipated in the device during the short-circuit. On the other hand, the longer pulse caused a short-circuit of the gate connection.

[15] defined two limits for the critical short circuit energy; one limit for when a device would fail due to a thermal runaway, and one limit for when a damage to the gate would happen.
The difference in limits are mainly related to the voltage and the duration of the short circuit. If a high voltage is applied during the short-circuit, the dissipated power in the device will be high, and the device will reach a high local temperature. This will trigger a thermal runaway.

If a lower voltage is applied for a longer time, the entire device will heat up to a lower temperature. This temperature will not be high enough to cause a thermal runaway, but can still cause a failure due to damage of the gate oxide or a melting of the surface metalization.

The thermal runaway occurs when the intrinsic current increases. As explained by Eq. 4.3, this rises very rapidly due to its exponential dependency on the temperature. Due

to the higher band gap of SiC, this happens at a higher temperature than in Si. This is illustrated in Fig. 4.2 where the intrinsic current is shown as a function of temperature for both Si and SiC.

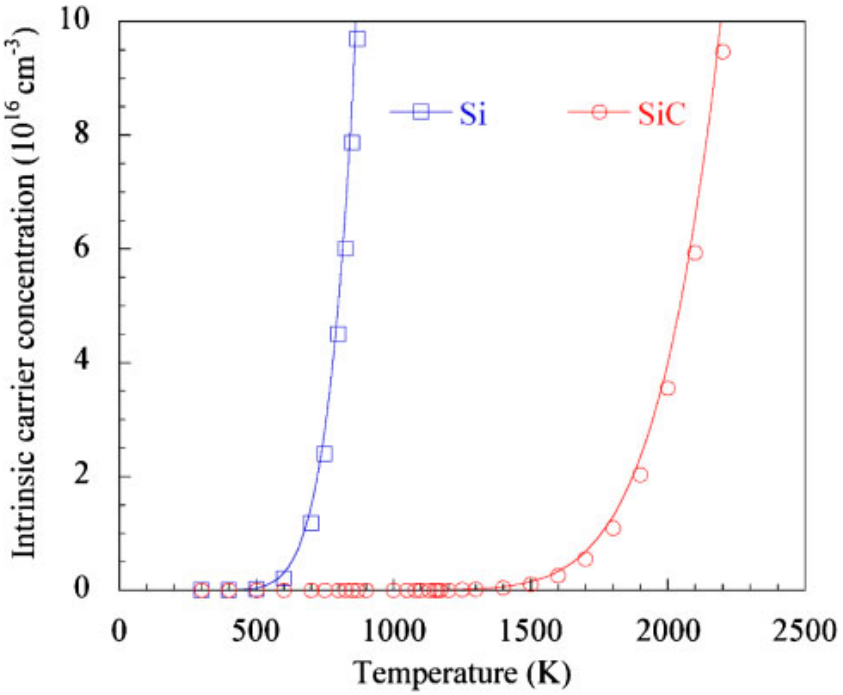


Figure 4.4. The intrinsic current as a function of the temperature for Si and SiC. It is noticed that the current rises at a higher temperature for SiC [2].

.

As it can be seen from this figure, the thermal runaway happens when the local temperature of a spot inside the device rises to more than approximately 1500 K (1230° C). On the other hand, damages to the gate oxide has been reported to happen already at 844 K (571° C) [24].

Therefore, if the device fails due to a thermal runaway or a damages to the gate oxide depends on whether all the energy is dissipated in one point or spread in the device. In [24], the heat spreading is shown to be related to the short-circuit time by

$$T(z, t_{sc}) \propto exp(-\frac{z}{\sqrt{D \cdot t_{sc}}}) \tag{4.4}$$

where z is the depth of the device, D is the thermal diffusivity, a material parameter, and t_{sc} is the short-circuit time.

This means that a short circuit with a low duration will dissipate all of its energy in a narrow area and therefore a thermal runaway is likely to happen. If the duration of short-circuit is longer, a more uniform heating of the area will be seen and other damages such as gate oxide degradation or damages to the surface metalization can be seen.

The thermal diffusivity depends on the material properties as it expresses how well heat is transferred within the material. It can be calculated by

$$D = \frac{k}{\rho \cdot c_p} \tag{4.5}$$

where k is the thermal conductivity, ρ is the density and c_p is the specific heat capacity. The thermal parameters of 4H-SiC are given in Tab. 4.1.

Table 4.1. Thermal properties for 4H-SiC [2].

Property	Unit	Value
Density	$[g/cm^3]$	3.21
Specific Heat Capacity	$[J/(g \cdot K)]$	0.6736
Thermal Conductivity	$[W/(cm \cdot K)]$	4.5

Using this knowledge, it is desired to use the derived model to test a short-circuit at different voltages, to understand the inner failure mechanism. Furthermore, it is desired to check at which voltages the local heating is enough to cause a thermal runaway and at which voltages the short circuit causes a more uniform heating which may damage the gate oxide.

Short-circuit setup 5

To investigate the dynamics of a short-circuit, the TCAD model is connected to an external circuit to resemble the behavior of a MOSFET that is subject to a short-circuit. In this chapter the setup for this short-circuit will be described, and the results will be investigated. Towards the end of the chapter it is explained why the device fails in a way that is not associated with a thermal runaway or a gate oxide degradation.

To simulate the effects of a short-circuit, a relatively simple circuit is used. The circuit approximates a device connected to a fixed DC-link and an external gate driver, including the parasitic components of these connections. This circuit is presented in Fig. 5.1.

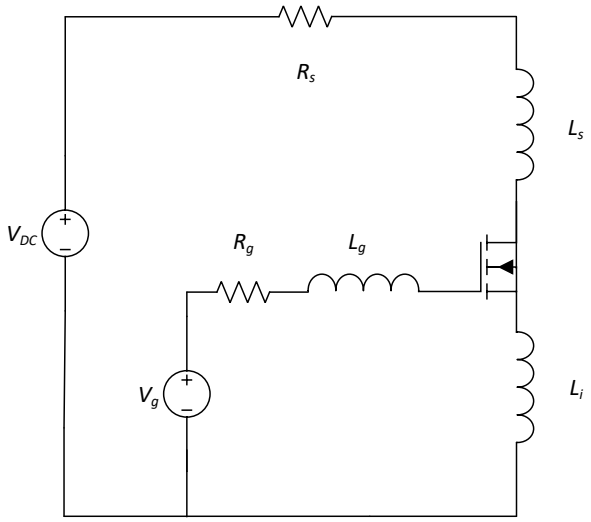


Figure 5.1. A schematic of the simulated setup for the short-circuit test.

In this figure, the gate drive is represented by three different components, V_g, R_g, and L_g. R_g is the externally mounted gate resistor, L_g is the stray inductance of the gate driver, and V_g is the applied gate voltage.
At the same time, the externally connected circuit is represented V_{DC}, L_s, and R_s. V_{DC} is the applied DC voltage at the time of the short-circuit. This often represent the full DC-link voltage of the system. L_s is the stray inductance of the connection between the DC-link and the MOSFET, often consisting of a busbar or a wire. L_i is the inductance due to inner connections in the device, such as bond wires and connectors. Finally, R_s is the resistance of the system, such as resistance of the connectors and busbars.

Table 5.1. Parameters for the short-circuit test shown in Fig 5.1.

Symbol	Parameter	Value	Unit
V_g	Gate Voltage	$-5/20$	$[V]$
R_g	Gate Resistor	10	$[\Omega]$
L_g	Gate Inductance	40	$[nH]$
V_{DC}	DC-Voltage	800	$[V]$
L_s	Circuit Inductance	100	$[nH]$
R_s	Stray Resistance	1	$[m\Omega]$
L_i	Stray Inductance	10	$[nH]$

For this project, a so-called Hard Switching Failure, HSF, is considered. This happens when the device is switched on while the full DC-link voltage is still applied. This can for instance happen if the other MOSFET of the phase leg in an inverter fails to turn off, and thereby is not blocking any voltage.

5.1 Simulation of Short-circuit

At first, a low voltage short-circuit is performed to test the setup of the short-circuits. This test is performed at $V_{DC} = 100\ V$. To improve convergence the thermodynamic effects are neglected.

At first the simulated DC-link voltage is ramped up by applying a quasi-stationary simulation with an increased voltage. A slew rate of one volt per second is used to ensure that no excessive in-rush current is occurring. At the same a gate voltage of $V_{GS} = -5\ V$ is applied that the device is fully off. Afterwards, a transient analysis is performed using the initial conditions established during the quasi-stationary simulation. In this simulation, the gate voltage is kept at $-5\ V$ for 2 μs. After this period the gate supply voltage is changed from $-5\ V$ to $20\ V$ during a time period of 0.1 μs. A gate resistance of 10Ω is used. Finally, the device is turned off after 8 μs by applying a negative gate voltage of $-5\ V$. The total gate pulse is shown in Fig. 5.2.

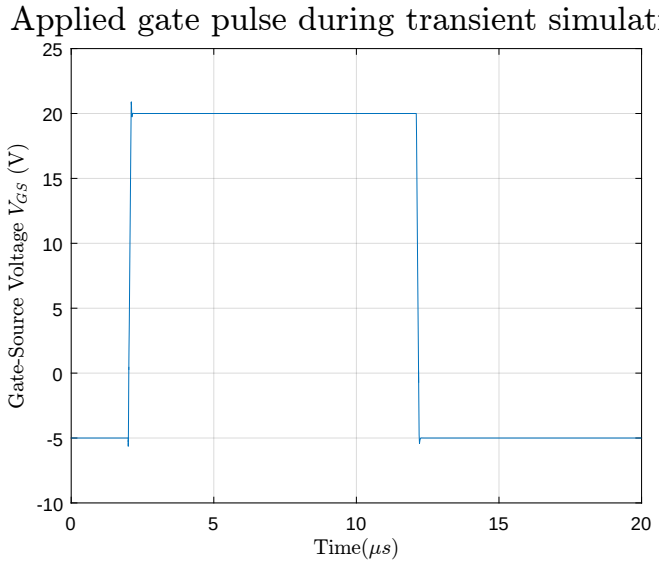


Figure 5.2. The applied gate voltage during the transient short-circuit simulation.

It is noticed that during the turn-on and turn-off of the device, a small overshoot and undershoot of the gate voltage occur. However, none of these are exceeding the absolute maximum values for the gate voltage of the device $V_{GS,max} = -10/25\ V$.

The drain-source voltage V_{DS} and the drain current I_D is shown in Fig. 5.3.

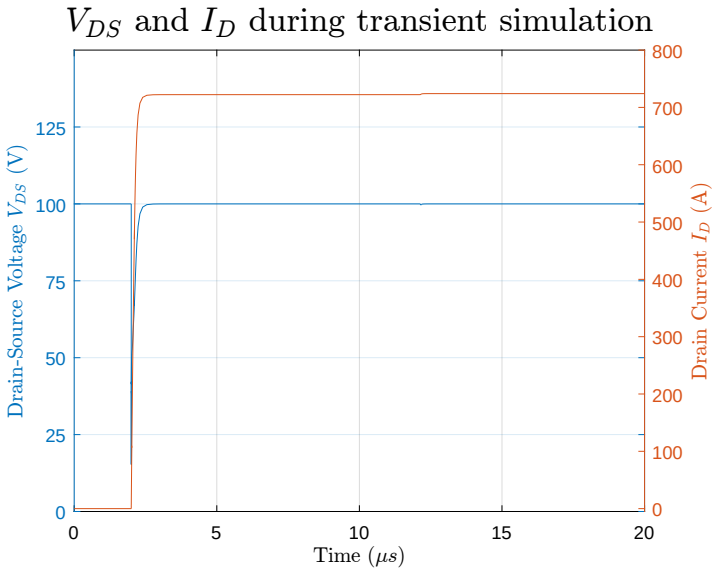


Figure 5.3. V_{DS} and I_D during the transient simulation. The current rises at turn-on at 2 μs, but does not reduce at turn-off $t = 12\ \mu s$.

From this figure it is noted that during the initial off-state the device is blocking the full DC-link voltage with a negligible drain current. At the instance of turn-on, $t = 2\ \mu s$, the voltage drops to a minimum of $V_{DS} = 20\ V$, while the current rises to approximately $I_D = 700\ A$. This is expected, as the main limiting factor of the current is the resistance of

the device. Also, the current is constant after the turn-on as no thermodynamical effects are considered in this simulation. However, at the time of turn-off, $t = 12\ \mu s$, the current should drop to a negligible value. From Fig. 5.3 it is seen that this is not the case during this simulation. The current remains approximately constant at 700 A. In the following section this will be explained by considering the inner states of the device during the simulation.

5.1.1 Inner states during transient simulation

One of the purposes of TCAD modeling is to investigate the mechanisms inside the device during the short-circuit. Therefore, the snapshots of the device are saved at different time instances to compare the electrostatic potential and the flow of current under different conditions.

The device is saved at these time instances

- Before turn-on, $t = 2\ \mu s$
- During on-state, $t = 3\ \mu s$
- After turn off, $t = 15\ \mu s$

At $t = 2\ \mu s$, the device in its off-state due to the applied gate voltage, $V_{GS} = -5\ V$. In this state the device is blocking the full DC-link voltage as during normal operation. The electrostatic potential of the device during this blocking state can be seen in Fig. 5.4. It is seen that that the device blocks the full dc-link voltage of the applied test, $V_{DC} = 100\ V$.

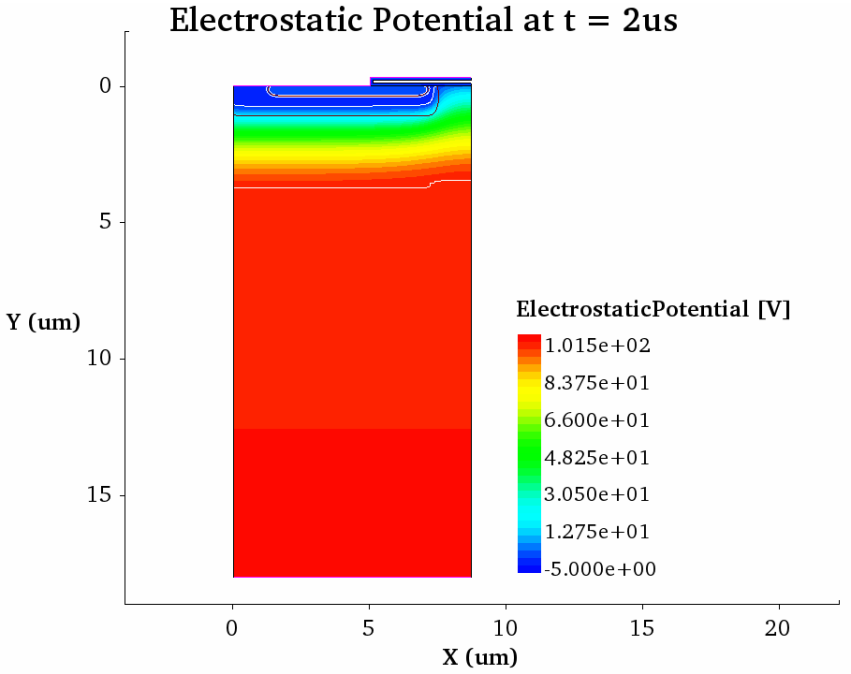


Figure 5.4. The initial electrostatic potential of the device before the turn-on of the device.

At the time of turn-on, the currents starts to flow. The current density in the device is seen in Fig. 5.5 for $t = 3\ \mu s$, where the device is in a fully on-state.

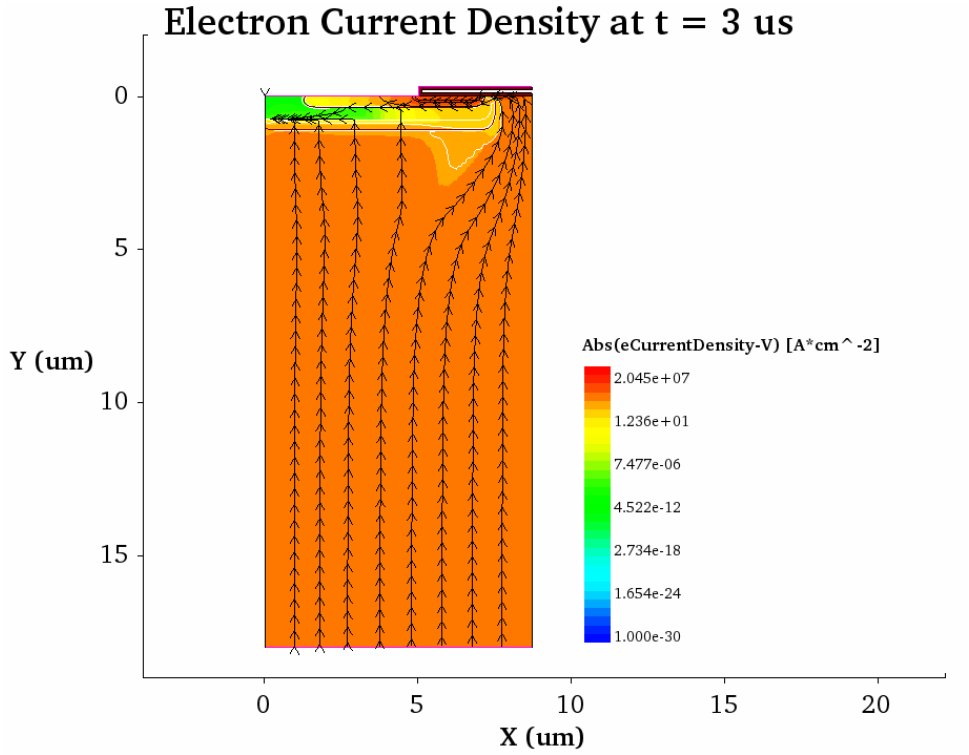


Figure 5.5. The electron current during the on-state of the device, at $t = 3\ \mu s$ .The turn-on of the intrinsic BJT is seen as current is flowing outside the channel region.

As it is seen from this figure, a breakdown occurs at the instance of turn-on. While a part of the current is flowing in the channel region, a large part of the current is flowing through the PN-junction outside the channel region. This is caused by the intrinsic BJT that is present in a MOSFET structure. The turn-on of this BJT is initiated by the voltage drop that occurs due to a flow of holes inside the p-well.

This voltage drop depends on the amount of hole current flowing to the source contact, and the resistivity of the p-layer. As the geometry is simplified, no additional p^+ layer has been implemented. Therefore the doping concentration of the p-layer is lower than for a properly designed device.

Due to this activation of the intrinsic BJT, the device is still conducting as the gate voltage is reduced and the device should be turned off. This is seen both from the drain current in Fig. 5.3 and from the flow of current in the Fig. 5.6.

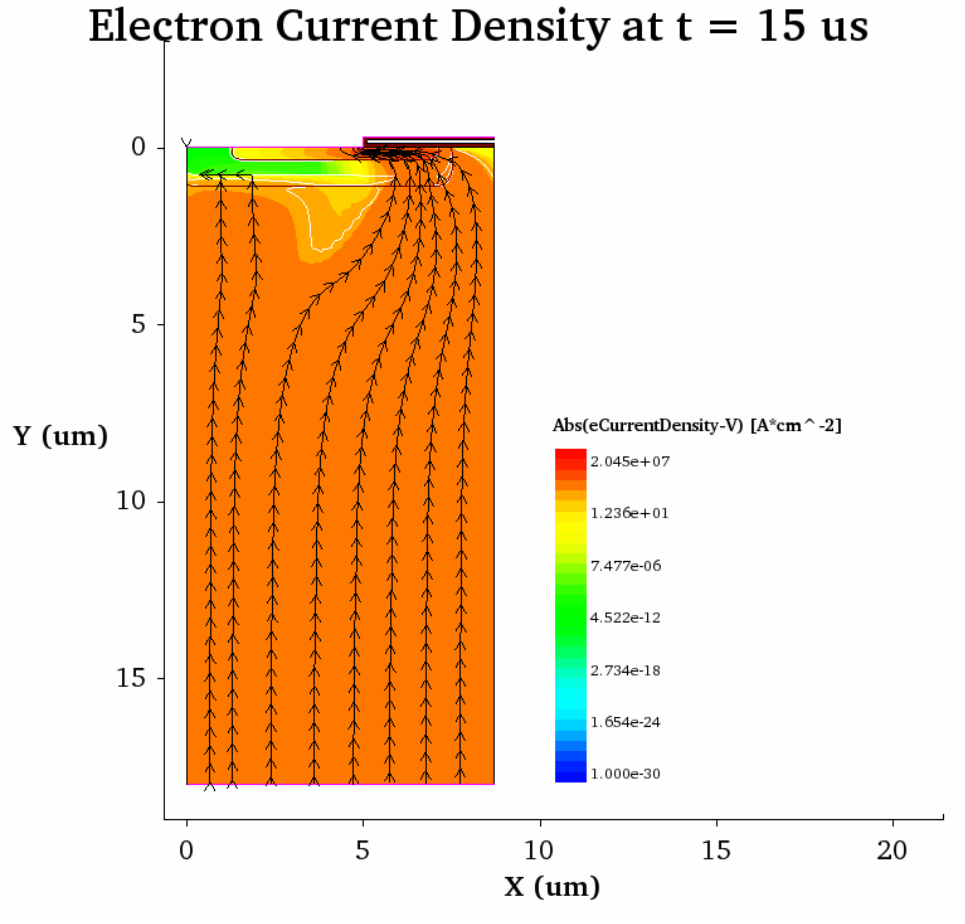


Figure 5.6. The current flow after the turn-off of the device. The device is still conducting due to the turn-on of the intrinsic BJT.

It is noted that the channel is fully off and no current is flowing through this. Therefore, the device should not conduct any current. This is also confirmed from the figure, as all current is flowing through the PN-junction due to the turn-on of the intrinsic BJT.

5.1.2 Activation of the Intrinsic BJT

The turn-on of the intrinsic BJT is caused by the excessive dv/dt that occurs at the device when the device is turned-on while the full blocking voltage is applied. During turn-on, a hole current is flowing in the p-well due to the change of the depletion layer width at the PN-junction. Because of the resistance of the p-well, this causes a voltage drop along the layer, as illustrated in Fig. 5.7 [11].

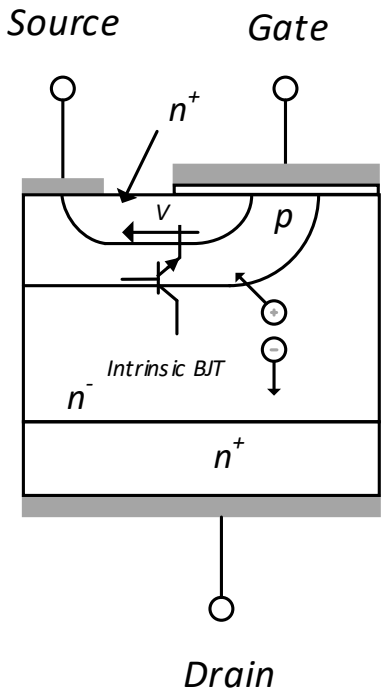


Figure 5.7. The intrinsic BJT of the MOSFET. During switching of the device, a voltage drop is created along the p-well, which may turn on the intrinsic BJT.

As the p-well and the source region is short-circuited by the source contact, ideally there would be no potential difference between the base and emitter of this intrinsic BJT. If this this is the case, the BJT will not be conducting. However, due to the voltage drop along the p-well region, a potential difference will exist between the two regions if a hole current is flowing . This is equivalent to a potential difference between the base and the emitter of the intrinsic BJT. This is shown by the equivalent circuit of a MOSFET in Fig. 5.8.

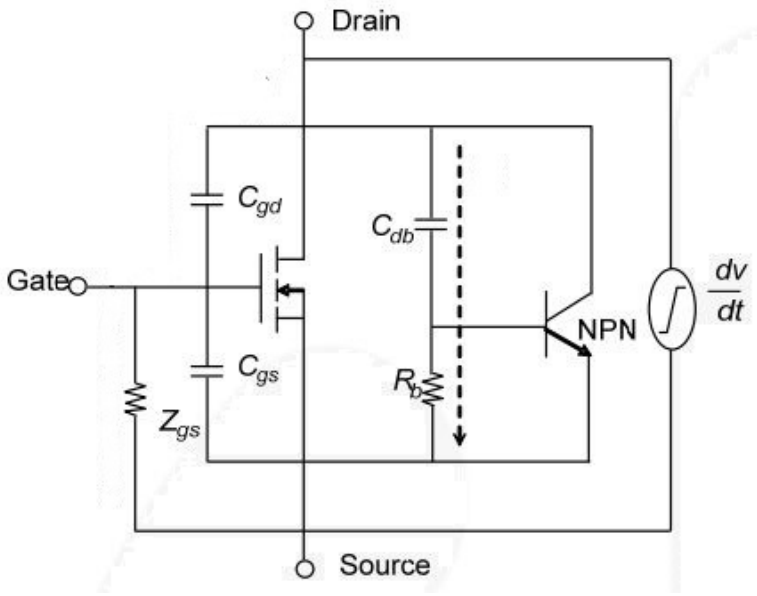


Figure 5.8. The equivalent circuit of a MOSFET, including the intrinsic BJT. Modified after [3].

As the hole current increases, the voltage drop across the p-well is increased due to the resistance, R_b. If this voltage drop exceeds the threshold voltage of the intrinsic BJT, the BJT will turn on and the device becomes conductive through the PN-junction as it was seen in Fig. 5.5 and Fig. 5.6 [3].

The corresponding hole current distributions are shown in Fig. 5.9 and Fig. 5.6, respectively.

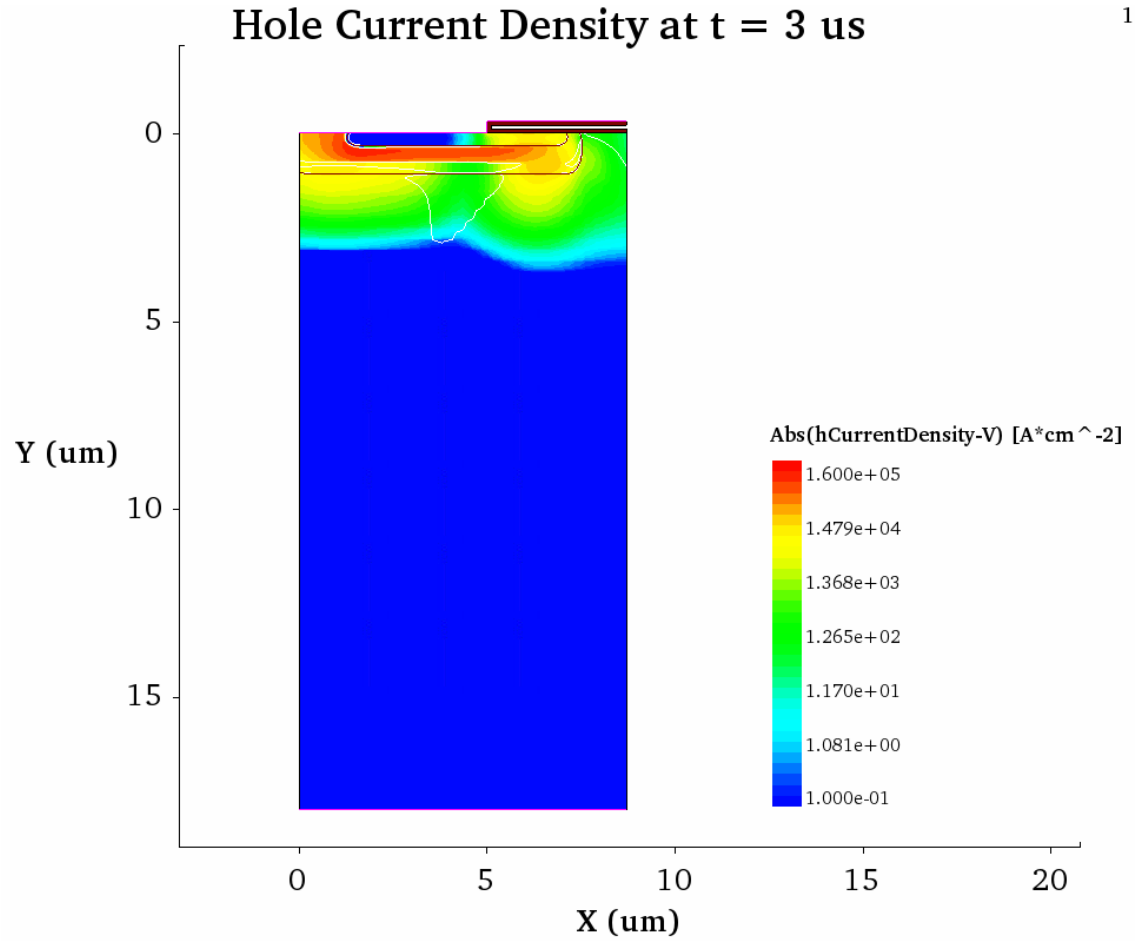


Figure 5.9. The hole current at $t = 3\mu s$, where the device is turned on. The hole current is causing the intrinsic BJT to conduct current.

At $t = 3\mu s$ a hole current is flowing in the p-well, and therefore the intrinsic BJT is conducting. The remains to be the case at $t = 15\mu s$, as shown in Fig. 5.10 and therefore the device is still conducting due to the BJT.

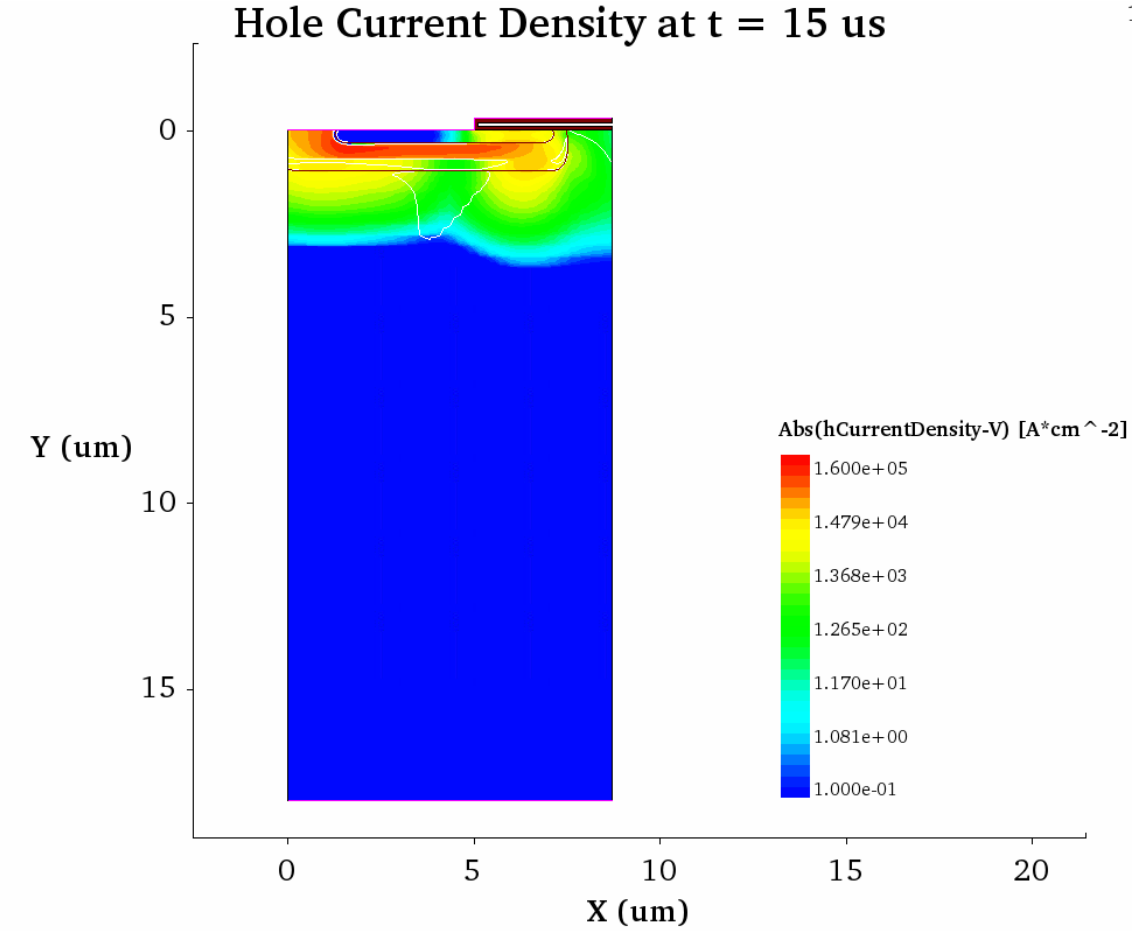


Figure 5.10. The hole current at $t = 15\mu s$ where the device is turned off. A hole current is flowing, causing the intrinsic BJT to remain turned on.

This BJT will remain activated as long as the current is not interrupted externally and therefore it leads to a failure of the device. To reduce the risk of the activation of this intrinsic BJT, it is desired to reduce the resistance of the p-well, R_b, to reduce the voltage drop for the same hole current. The resistance of the p-well depends on the doping concentration in this region. Therefore, in order to suppress the activation of the intrinsic BJT, the p-well doping concentration should be increased. As the threshold voltage of the device depends on the doping concentration in the channel region, the protection is often implemented by introducing an additional region of the device, in which the acceptor doping concentration is higher than in the channel region [11] .

Due to this activation of the intrinsic BJT, the device fails from another failure mechanism than the thermal runaway that it was desired to investigate. Therefore, no more short-circuits simulations are performed, as it does not bring any information regarding the short-circuit failure mechanism. In the following chapter the limitations and challenges of the project will be discussed. In this section it will also be proposed how these challenges can be solved, including the problem with the intrinsic BJT.

Discussion and Future Work 6

In this project a number of limitations and difficulties have been described. Many of these limitation have a severe impact on the accuracy of the model. While some of these limitations arise due to limited knowledge of properties of the actual device, others can be avoided by increasing the number of parameters to be determined during the fitting of the model.

First of all, the influence of the device interface traps was neglected due to the complexity of obtaining the the correct distribution of defects, as multiple types of defects exist. However, as presented in Section 3.4 it has been shown by [19] that the majority of the traps occurring in the interface is of the acceptor type. Using this knowledge, it might be possible to increase the accuracy of the model by being only specifying this type of traps. In Sentaurus [25] , it is possible to specify both the concentration and the type of traps. This could be used for achieving better static characteristics of the device, without adding an overwhelming amount of variables to the model due to the many types of interface traps.

Another simplification of the model that leads to erroneous results is the uniform doping concentration of the p-well. To simplify the implementation of the model, no additional p^+ shielding layer was implemented. As it was seen from the results of the short-circuit simulations in Chapter 5, the lack of this layer causes the device to be prone to an activation of the internal BJT. Therefore, this layer should be implemented to allow the transient behavior of the device to be simulated. However, as the threshold voltage depends on the doping concentration in the channel region, the doping concentration should remain unchanged in this region while it is raised in the rest of the p-well.

The final limitation is that the model was made by adjusting the doping concentration and geometry to resemble the characteristics given in the datasheet. As the datasheet only provide operational values for normal operation, this approach cannot be used comparison of the model during abnormal conditions, such as short-circuits. Therefore, a natural next step would be to compare the behavior of the modelled device with measurements of a device during these abnormal conditions.

During this project, another type of problems has been encountered: Due to the material properties of 4H-SiC, the numerical simulations of a SiC can be challenging [8]. One of the major problems in simulation of SiC MOSFETs is the very low intrinsic current of the device, which results in very low leakage currents during blocking voltage simulations [18]. This requires higher accuracy representation of the floating points, resulting in an

increased need for both computational power and memory. At the same time this results in an ill-conditioned problem due to the large difference in the numerical values of the large electric field and the small values of the leakage current. One possible method for improving this is to introduce an additional leakage current in the device. In [18], it is suggested that the real leakage current of the device in normal operation is significantly higher than the theoretical value due to background radiation. While it has very little significance to the operation of the device due to its small size, an additionally introduced current would cause the problem to be less ill-conditioned, and thereby easier to solve numerically.

Finally, due to the problems of achieving a satisfactory transient performance of the device, the temperature dependence of the short-circuit capability was not implemented. As this affects the short-circuit performance significantly, this has to be implemented to correctly evaluate the transient behavior. In Sentaurus, this is achieved by enforcing another set of boundary conditions to the device. Both [1], and [15] consider the heat flux unidirectional towards to drain contact as this is often connected to a heat sink with a much lower thermal resistance than the rest of the device. Therefore, the three other boundaries are defined to be adiabatic, hence no heat is transfered through these. Implementing these conditions into the simulations would make it possible to simulate the temperature of the device, including the temperature dependence of the materials. As a thermal runaway is caused by an increased leakage current due to a high internal temperature, this additional simulation is necessary to identify the short-circuit capability.

7 Conclusion

In this report, the modeling of a SiC MOSFET subject to a short-circuit was investigated. In Chapter 1, the background of the project was explained, and the motivation for replacing conventional Si IGBTs with SiC MOSFETs was given. In this it was found that SiC is capable of achieving a higher switching frequency and a lower on-state loss than Si IGBTs due to its beneficial material properties.

Afterwards, the different parameters of a MOSFET was presented in Chapter 2. The IV-characteristics was derived, and the influence of different parameters and geometrical properties was shown.

In Chapter 3, the derived properties from Chapter 2 was used for implementing a model in the Technical Computer Aided Design (TCAD) program Sentaurus. As the geometry of the device was unknown a starting point was found in literature, and used for a model that approximately resembled the behavior of the device. One of the main takeaways of this model is that the device performance is significantly affected by device interface traps at the interface between the 4H-SiC and the gate oxide, SiO2. The threshold voltage is shifted compared to the assumed ideal interface. Therefore, the transfer characteristics cannot be correctly resembled at low gate voltages using this assumption. To solve this problem, the transfer characteristics were adjusted to have similar characteristics to the real device at higher gate voltages.

In Chapter 4, the failure mechanisms due to short-circuits were described by examples from literature. The waveform of a Hard-switching Failure was described, and it was described Afterwards, a short-circuit was simulated by the applying an external circuit to the derived TCAD model. Due to the simplified geometry of the device, it was found that the transient behavior of the device is not satisfactory. At the instance of turn-on, the intrinsic BJT is active causing the device to conduct current after the turn-off due to the intrinsic BJT of a MOSFET. This causes the device to fail in a way that is not the normal failure mode for a well-designed MOSFET during a short-circuit. Therefore, a full short-circuit was not simulated, as the simulated results would not bring any further information about the physical mechanisms of a short-circuit.

Overall, it can be concluded that while the modeled device achieves a correct breakdown voltage and transfer characteristic, the simplification of the model leads to an unsatisfactory output characteristic and transient behavior of the device. Due to this unsatisfactory transient behavior, other failure modes than the studied are seen. Therefore it is finally concluded that the modelled device cannot be investigations of the failure mechanisms in SiC MOSFETs subject to short circuits.

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