MSc. Thesis

Testing modern Silicon Carbide MOSFET devices against short-circuit

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PED 1041

supervised by

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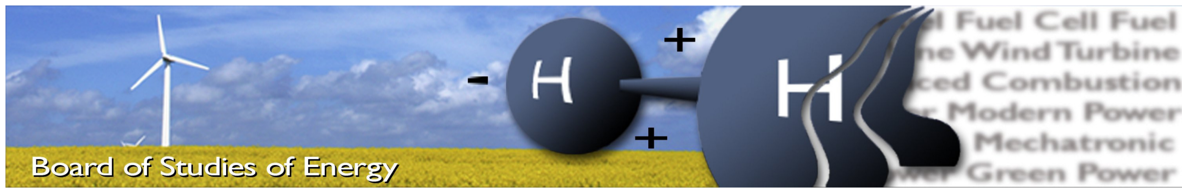

Title:	Testing modern Silicon Carbide MOSFET devices against short-circuit
Semester:	10
Semester theme:	-
Project period:	01.02.17 to 01.06.17
ECTS:	30
Supervisor:	Lorenzo Ceccarelli, Paula Diaz Reigosa and Francesco Iannuzzo
Project group:	PED-1041

Pablo Rodriguez de Mora

SYNOPSIS:

Two Silicon Carbide power MOSFET models, rated 1.2 kV 36 A and 90 A have been evaluated in this work. With the purpose of studying the influence of the drain-source leakage current on the short-circuit behaviour, static characterization at different conditions has been performed. The devices with the highest and lowest drain-source leakage current were selected for short-circuit testing. The test range has been set at a DC-link of 400 and 600 V, with case temperatures ranging from 25 to 150 ℃. Both models presented a drop in the gate voltage at the end of sufficiently long pulses and after turn off, a very high leakage current. This high leakage current difficults the identification of a relation for the leakage statically measured and the short-circuit behaviour.

Pages, total:	65
Appendix:	8
Supplements:	-

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Summary

In this project the short-circuit behaviour of discrete Silicon Carbide (SiC) MOSFETs is studied. SiC MOSFETs are becoming increasingly available and many manufacturers offer such devices among their products. The higher performance against Silicon (Si) IGBTs and MOSFETs is assessed in many works, however, under extremely demanding conditions such as short-circuit, SiC devices still present challenges. In the state of the art, two phenomena that may decrease the short-circuit ruggedness have been identified. On one hand, towards the end of sufficiently long pulses the gate voltage decreases a few volts, indicating that current flows through gate oxide which should behave as an insulator. On the other hand, just after turn off a tail in the drain-source current is observed. This is a phenomena that does not occur under normal operating conditions and indicates that current is leaking between the drain-source.
In the state of the art, different SiC MOSFET models are tested and the aforementioned issues are pointed out. However, an analysis of the relation between the static characteristics and short-circuit behaviour is not studied. This work originates from the need to assess the relation between the drain-source leakage current (I_{DSS}) measured by static test and the short-circuit behaviour .

For the short-circuit test, the Non Destructive Tester (NDT) available at the Energy Technology (ET) department, which is a flexible test ground for many topologies, is used. Two models have been studied in this work, a 1.2 kV/ 36 A and a 1.2 kV/ 90 A SiC MOSFET both from CREE, Devices Under Test (DUT). These devices present a TO-247 footprint. A PCB to adapt the NDT to the TO-247 footprint and also present the driver footprint was designed and manufactured. Special attention was taken to reduce the stray inductance. On one hand, with differential traces and also with the addition of a decoupling capacitor near the DUT.

Four 1.2 kV/ 36 A SiC MOSFETs have been evaluated. In order to select these devices with the highest and lowest drain-source leakage current, static characterization at a range of temperatures from 25 to 200 ℃ has been performed. In regards to the leakage measurements, a great variability has been observed between the DUTs.
The short-circuit tests have been carried out at junction temperature range from 25 to 150 ℃ and DC-link voltages of 300, 400 and 600 V. At 300 and 400 V, short circuit pulses of up to 10 μs could be achieved for the whole range of temperatures. At 600 V, pulses of 10 μs could not be achieved and breakdown was experienced.
During short-circuit a very high drain-source leakage current, in the order of the rated current, was measured for sufficiently long pulses. This was measured for both devices with high and low statically measured leakage current. Even though a difference was observed in the short-circuit test, it was much lower than in the static test. This difficults the correlation between the characterized leakage current and short-circuit behaviour of the studied device.
At breakdown two failure modes have been experienced. On one hand, a sudden breakdown with three terminal short-circuit is experienced at $V_{DS} = 600$ V, a 5 μs pulse and case temperature of $T_{case} =$ 25 ℃İn this failure mode, at the end of the pulse, the gate voltage drops 0.72 V from the reference value, the short-circuit energy is 4.96 J/cm^2 and the simulated junction temperature at breakdown is 714 ℃.
The second failure mode occurs at $V_{DS} = 600$ V and a case temperature of $T_{case} = 150$ ℃. In the pulse following a 3 μs short-circuit, the whole gate voltage degreases permanently. With further pulses, the gate suffers a gradual and permanent reduction of the whole voltage pulse. In the pulse prior to gate degradation (3 μs long), the short-circuit energy is 2.91 J/cm^2 and the simulated junction temperature is $T_j = 595$ ℃.

For the 1.2 kV/ 90 A SiC MOSFETs, five devices have been studied. No prior work on the behaviour of this model was found in the state of the art. Therefore, so as to gain a comprehensive view of the static characteristics of the model, the drain -source (I_{DSS}) and gate-source (I_{GSS}) leakage currents, gate-source threshold voltage (V_{Th}) and transfer characteristics ($V_{GS} - I_{DS}$) were measured. To obtain more precise measurements, a fixture which limited the test temperature to 125 ℃ was used. For short circuit testing, two devices (DUT) whose drain-source leakage was highest and lowest were chosen.
In terms of gate-source voltage and drain-source leakage current, the tested 90 A devices, presented a very similar behaviour to the 36 A devices. Care was taken so that both DUT followed the same test procedure. Only the device whose drain-source leakage was higher suffered permanent degradation. It occurred for a 4 μs pulse at $V_{DS} = 600$ V and $T_{case} = 100$ ℃. Similarly to the second failure mode experienced for the 36 A device, the whole gate voltage pulse decreased from its reference value. The post failure analysis revealed a gate oxide failure between the gate-source leads. An electrical resistance of $R_{GS} = 105{,}8\ \Omega$ was measured at room temperature.

This project has revealed a difficulty on relating static measurement of the drain-source leakage current and the short-circuit waveform. Nevertheless, it has shown a high temperature gate degradation which was not seen in the state of the art, and may indicate gate oxide weakness.

Abstract - In this work the short circuit behaviour of two models of Silicon Carbide MOSFETs, rated 1.2 kV 36 and 90 A are analysed. The static characterization of several devices of each model has been performed. Of each model, the devices with highest and lowest drain-source leakage current were selected for short-circuit testing. The behaviour at different DC-link voltage and case temperature has been performed. Additionally, the failure mode, the calculated gate drop, short circuit energy and a simulation of the junction temperature is presented.

Index Terms - SiC Power MOSFET, Short-Circuit, Failure, Drain-source leakage current

Acknowledgements

For the proposal of the topic and provide the necessary material for the completion of this project, as well as the guidance and open door to my doubts, I would like to thank my three supervisors, Lorenzo Ceccarelli, Paula Diaz Reigosa and Francesco Iannuzzo.

Since this project has been highly laboratory based. Understanding the operation of the different setup available at the Energy Technology department has been essential for the completion of this project. Therefore I would like to thank Paula Diaz Reigosa and Lorenzo Ceccarelli for investing their time in explaining me the operation of the setup used in this project.

For the correction of this report, which I have to recognize to be a tedious task I would like to express my gratitude to Lorenzo Ceccarelli and Paula Diaz Reigosa.

I am very grateful to my parents for the support I received of these last two years in which I have been living and studying in Aalborg.

Last but not least, I would like to express my gratitude to Denmark for the opportunity I have been granted to study the Master in Energy Engineering at Aalborg University.

Many thanks,

Pablo Rodriguez de Mora

Contents

1 Introduction **1**

1.1 The Silicon Carbide MOSFET 5

1.1.1 Channel resistance, R_{ch} 6

1.1.2 Drift region resistance, R_{epi} 7

1.1.3 Static behaviour 8

1.1.4 Dynamic behaviour 10

1.2 The short-ciruit in power electronic systems 11

1.2.1 Short circuit type I 11

1.2.2 Short circuit type II 12

1.3 SiC MOSFET failure in short-circuit type I 13

1.3.1 Failure modes 13

1.3.2 Short-circuit withstand time and critical energy 14

1.3.3 Gate Reliability 16

1.3.4 Thermal Properties and Influence of the case temperature 17

1.3.5 Hole current 18

1.4 Project motivation 20

1.5 Objective 20

1.6 Problem Formulation 20

1.7 Scope and Limits of the project 20

1.8 Outline of the Master Thesis 21

2 Hardware developed for testing **23**

2.1 Adapter 23

2.2 Decoupling Capacitor 24

3 1.2 kV/ 36 A SiC MOSFET **26**

3.1 Static testing 26

3.1.1 Drain-source leakage current (I_{DSS}) 26

3.1.2 Gate-source threshold voltage ($V_{GS\ Th}$) 27

3.2 Dynamic testing 29

3.2.1 Test procedure 29

3.2.2 Short-circuit time dependency 30

3.2.3 Case temperature dependence . . . 31
3.2.4 DC-link voltage dependence . . . 32
3.2.5 Device comparison . . . 33
3.2.6 Gate-source drop . . . 35
3.2.7 Degradation and destruction . . . 35
3.2.8 Short Circuit Energy analysis . . . 38
3.2.9 Junction Temperature analysis . . . 39
3.3 Conclusion . . . 41

4 1.2 kV/ 90 A SiC MOSFET 42

4.1 Static characterization . . . 42
4.1.1 drain-source leakage current (I_{DSS}) . . . 42
4.1.2 Gate-source threshold voltage ($V_{GS\,Th}$) . . . 43
4.1.3 Gate-source leakage current (I_{GSS}) . . . 44
4.1.4 Transfer characteristics ($V_{GS} - I_{DS}$) . . . 45
4.2 Dynamic testing . . . 46
4.2.1 Test Procedure . . . 46
4.2.2 Short-circuit time dependence . . . 47
4.2.3 Case temperature dependence . . . 48
4.2.4 DC-link voltage dependence . . . 49
4.2.5 Device comparison . . . 50
4.2.6 Gate-source drop . . . 51
4.2.7 Degradation at $T_{case} = 100$ ℃ . . . 51
4.2.8 Degraded S9, static characterization . . . 53
4.2.9 Short-Circuit Energy analysis . . . 54
4.2.10 Junction Temperature analysis . . . 54
4.3 Conclusion . . . 56

5 General conclusion and future work 57

5.1 General conclusion . . . 57
5.2 Future work . . . 57

A Appendix: Static characterization 58

A.1 Setup . . . 58

A.2 Tested Variables 60
A.2.1 Drain-source leakage current (I_{DSS}) 60
A.2.2 Gate-source threshold voltage ($V_{GS\,Th}$) 60
A.2.3 Gate-source leakage current (I_{GSS}) 60
A.2.4 Transfer characteristics ($V_{GS} - I_{DS}$) 61
A.3 Test conditions for C2M0080120D 61
A.4 Test conditions for C2M0025120D 61

B Appendix: Short-circuit test setup **63**
B.1 Test setup 63
B.2 Hardware 64

Literature **65**

Chapter 1

Introduction

Silicon power switches represent the foundation elements in modern power converters. As shown in Fig. 1.1, several silicon (Si) devices can be found in the market to address diverse needs in terms of current and voltage capability.

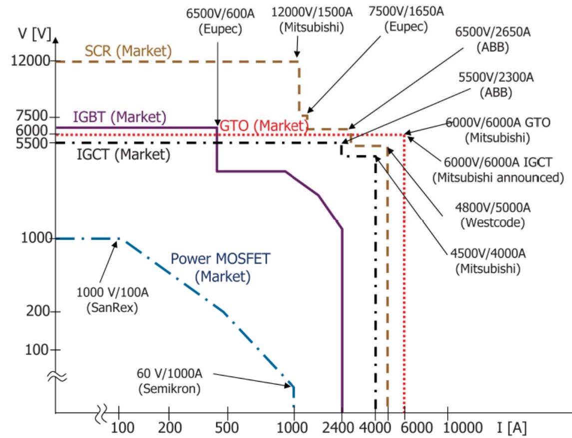


Fig. 1.1: Silicon Power devices and their range of application [1].

In this work, the devices of interest are in the voltage range of 1.2 kV and current rating between 40 and 90 A. As can be seen in Fig. 1.1, this area is covered by several devices, however, the Insulated Gate Bipolar Transistor (IGBT) stand out as the preferred device.

In January 2011 CREE introduced the first commercial 1.2 KV 24 A Silicon Carbide (SiC) Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET), CMF10120D [2]. The characteristics depicted by it did appear to be aimed to tap into the lower power range of the IGBT market and nowadays various manufacturers offer SiC devices among their products.

Silicon Carbide belongs to the Wide Band Gap (WBG) semiconductors family [3]. The WBG semiconductors are characterized by higher band gap energy (Eg) and higher critical electric field than the Si counterparts. As shown in Fig. 1.2, specifically SiC also presents higher thermal conductivity, melting point and electron velocity.

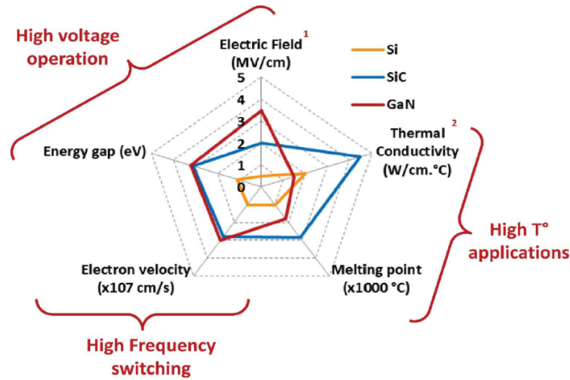


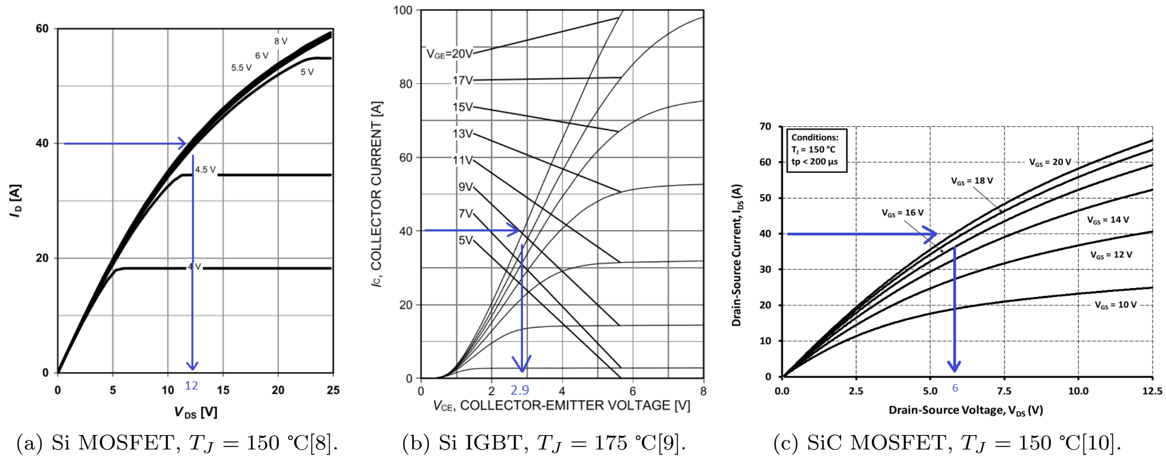
Fig. 1.2: Characteristics and advantages of Si, SiC and Galium Nitrade (GaN) semiconductors [1].

Many articles can be found comparing the performance between Si and SiC devices [4–7]. Here a hands-on comparison between three commercially available devices is shown, two Si devices i.e. a MOSFET and an IGBT, and a SiC MOSFET. The Si IPW90R120C3 MOSFET, Si IKW40T120 IGBT and SiC C2M0080120D MOSFET are rated for similar voltage blocking (V_{BD}) and current capability. In Table 1.1 their general characteristics are shown. Note that the Si MOSFET has the lowest V_{BD} rating .

Device	V_{BD} [V]	$I_{CE/DS}$ [A], $Tj = 100$ °C	Ref.
IPW90R120C3, Si MOSFET	900	23	[8]
IKW25T120H3, Si IGBT	1.2k	25	[9]
C2M0080120D, SiC MOSFET	1.2k	24	[10]

Table 1.1: Characteristics of the devices being compared.

To evaluate the losses in a switch, one should consider the conduction and switching losses. On one hand, the conduction losses occur during the on-state and are proportional to its collector-emitter/ drain-source voltage and current, $P_{cond} = V_{CE/DS} \cdot I_{CE/DS}$. In Fig. 1.3, the on-state $V_{CE/DS}$- $I_{CE/DS}$ characteristics of the three devices at high temperature is shown.



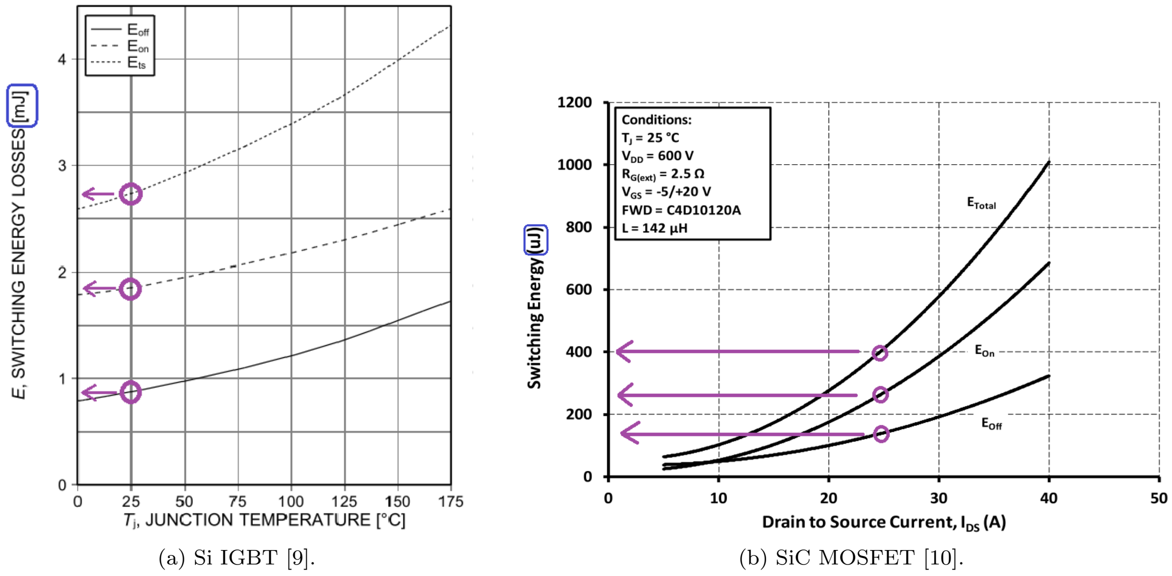
(a) Si MOSFET, T_J = 150 ℃[8]. (b) Si IGBT, T_J = 175 ℃[9]. (c) SiC MOSFET, T_J = 150 ℃[10].

Fig. 1.3: On state characteristics. Notice that for 40 A, the IGBT has the lowest forward voltage drop.

As can be seen in Fig. 1.3, for a high junction temperature and a current of 40 A the forward voltage drop of the Si MOSFET (a) is $V_{DS\ on}$ = 12 V. Ont the other hand, the SiC MOSFET (b) has a $V_{DS\ on}$ = 6 V, which is half the Si. But, it is the Si IGBT (c) the device with the lowest forward voltage drop, and thus the lowest conduction losses. It should be mentioned that for the SiC MOSFET it may be possible to reduce the conduction losses by selecting a device rated for higher current.

On the other hand, the switching losses appear during the turn on and off transients. Due to parasitic capacitances, inductances and gate resistance, the switching is not instant. Losses appear because either at turn on or off, the current and voltage cross each other at a high value [11].

In this sense to compare different MOSFETs it is popular the Figure of Merit (FoM) = $R_{(DS(on))} \cdot Q_G$ [12]. It accounts for the static and dynamic characteristics, and lowering its value is the merit indicator. For the devices shown in Fig. 1.3, $FoM_{Si\ MOSFET}$ = 33.12 ΩnQ and SiC MOSFET, $FoM_{SiC\ MOSFET}$ = 4.96 ΩnQ, six times smaller than its Si counterpart. Alternatively, the switching losses of the Si IGBT and SiC MOSFET may be directly compared by the losses given in the datasheet. In Fig. 1.4, the switching losses of a Si IGBT (a) and SiC MOSFET (b) at 600 V, 25 A and T_J = 25 ℃ are highlighted.



(a) Si IGBT [9].

(b) SiC MOSFET [10].

Fig. 1.4: Switching characteristics highlighted for 600 V, 25 A and $T_J = 25$ °C.

As can be seen in Fig. 1.4, the total switching losses of the Si IGBT (a) are around 2.75 mJ which are seven times higher than the SiC MOSFET (b).

It is concluded that the losses of the SiC MOSFET are lower than the Si MOSFET. By contrast, when comparing a Si IGBT against a SiC MOSFET only the switching losses are lower. But as is shown in many works [4–7], under the same conditions, the SiC devices have in overall lower losses than their Si counterparts.

However, not only is it interesting to compare the losses but also, in certain applications, the temperature limit plays a key role in the selection of a device. In Fig. 1.5, three regions can be identified. Starting at the lowest temperature is the freeze out region where the conduction is very poor, because the intrinsic and the dopant charges are not activated. Then at medium temperatures (operating temperature), the conduction is controlled by the extrinsic dopant density. At higher temperature, the intrinsic carrier density increases rapidly creating a positive feedback between the driven current and the device temperature [13].

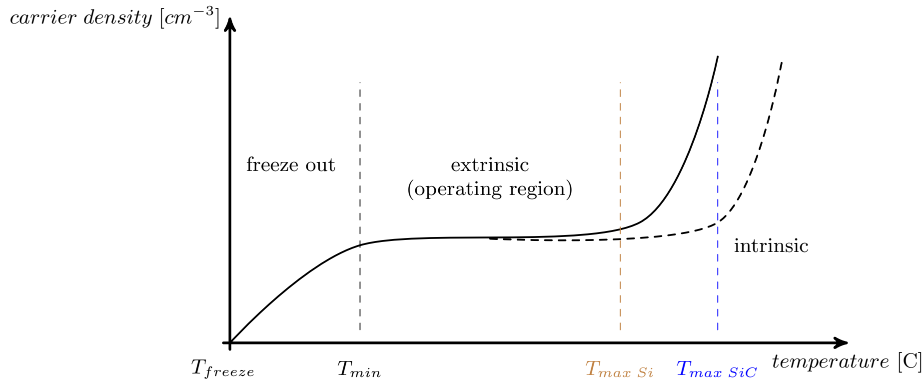


Fig. 1.5: Carrier density as a function of the temperature.

In Fig. 1.5, *carrier density* = *intrinsic* n^o *of electrons* (n_i) + *extrinsic* n^o *of electrons* (n_{ext}). The maximum temperature is the one at which, the intrinsic number of electrons reaches a value comparable to the lowest doped region. The graphical explanation of this phenomenon is shown in Fig. 1.5. For the same n_i limit, the SiC device reaches a higher temperature limit than Si [3].

1.1 The Silicon Carbide MOSFET

To understand the behaviour of the device during short-ciruit, a brief introduction of its physics and a relation to lumped electrical parameters will be presented.

In order to cope with higher voltage and current requirements, the power MOSFET presents several characteristic features. On one hand, the a single MOSFET die contains several cells connected in parallel. Additionally, the preferred construction for power MOSFETs is vertical instead of horizontal [13]. A device with planar gate cell structure is shown in Fig. 1.6. This type of SiC MOSFET is the one adopted for the tested devices.

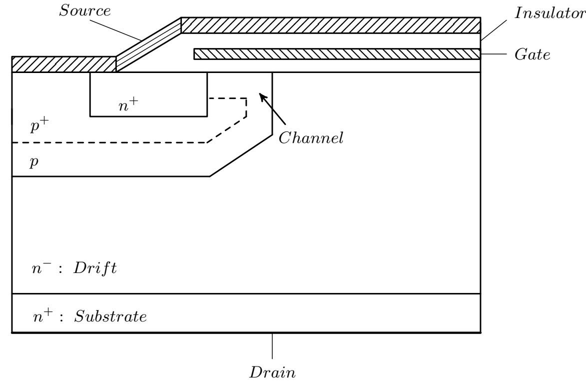


Fig. 1.6: Internal structure of a MOSFET, only half a cell is shown.

In the physical model shown in Fig. 1.6, several parasitic components may be identified, in Fig. 1.7 these are depicted. Between the drain and source, a BJT npn transistor and a diode are formed. The second set of elements are a series of resistances in the current conduction path, between the drain and source: R_n^+, R_{ch}, R_a, R_{FET}, R_{epi}, and R_{subs}. And third are capacitances between the three pads that together with the lead inductance determine the switching behaviour: C_{GS}, C_{DS} and C_{GD}.

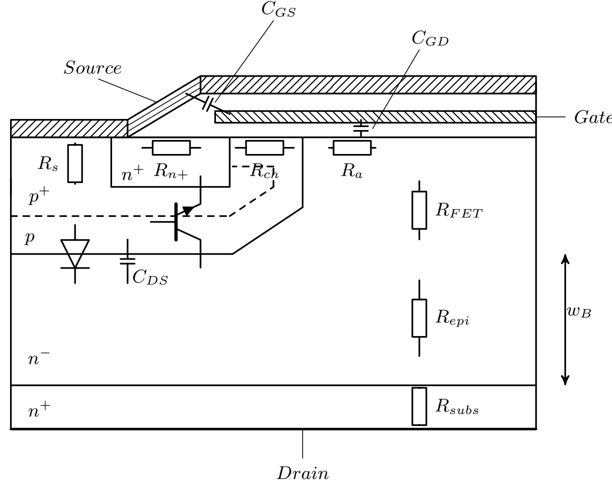


Fig. 1.7: Parasitic elements present in a half cell MOSFET [13].

The abrupt junction between the drift (n^-) and p region generates an intrinsic diode which allows the device to reverse conduct. But in the area where the p is in contact with the n^- region a parasitic BJT is formed. If this parasitic component is activated, it can cause the destruction of the device. The activation may happen if the current flows laterally in the p region towards the source. As seen Fig. 1.7, R_S models the equivalent resistance for the lateral flowing current that may trigger the parasitic BJT. Therefore, reducing its value is key to avoid turning on the parasitic BJT [3, 13].

During conduction, the current flows through a series of resistances, R_{n^+}, R_{ch}, R_a, R_{FET}, R_{epi} and R_{subs}. From a relevance point of view, only R_{ch}, and R_{epi} are examined here.

1.1.1 Channel resistance, R_{ch}

R_{ch} stands for the channel resistance, it is closely related with the MOSFET behaviour and therefore it is dependent on the relation $V_{DS} \leftrightarrow V_{GS} - V_{Th}$. During the normal conduction (ohmic region), $V_{DS} < V_{GS} - V_{Th}$ and the drain current is [3],

$$I_{DS} = \kappa \cdot \left[(V_{GS} - V_{Th}) \cdot V_{DS} - \frac{1}{2} \cdot V_{DS}^2 \right] \quad (1.1)$$

Where κ is,

$$\kappa = \frac{W_{channel} \cdot \mu_n \cdot C_{ox}}{L_{channel}} \quad (1.2)$$

Where as shown in Fig. 1.9a, $W_{channel}$ stand for the channel width and $L_{channel}$ is its length. C_{ox} stands for the capacitor built between the channel and gate electrode, and μ_n is the electron mobility [13].

For this region, it is possible to determine the resistance of the device as a function of the gate voltage,

$$R_{CH} = \frac{L_{channel}}{\mu_{n,channel} \cdot W_{channel} \cdot C_{ox}} \cdot \frac{1}{(V_{GS} - V_{Th})} \tag{1.3}$$

1.1.2 Drift region resistance, R_{epi}

During normal operation, for devices of high voltage blocking capability, the highest losses are dissipated by R_{epi} [11]. This term is proportional to the thickness needed to block high voltages. Therefore, R_{epi} has limited the use of Si MOSFETs to block high voltages, where IGBTs are commonly used. However, SiC devices have effectively reduced its value. According to [13], R_{epi} is given by Eq. 1.4.

$$R_{epi} = \frac{w_B}{q \cdot \mu_n \cdot N_D \cdot A} \tag{1.4}$$

Where as shown in Fig. 1.7, w_B is the width of the drift region, N_D is the doping concentration and A is the cross sectional area of the drift region.

The breakdown voltage may be approximated by, Eq. 1.5.

$$V_{BD} = \frac{\varepsilon \cdot E_C^2}{2 \cdot q \cdot N_D} \rightarrow N_D = \frac{\varepsilon \cdot E_C^2}{2 \cdot q \cdot V_{BD}} \tag{1.5}$$

Where E_C is the critical electric field and V_{BD} is the breakdown voltage.

The width may be approximated by,

$$w_B = \frac{2 \cdot V_{BD}}{E_c} \tag{1.6}$$

Introducing Eq. 1.5 and 1.6 into Eq. 1.4,

$$R_{epi} = \frac{4 \cdot q \cdot V_{BD}^2}{\mu_n \cdot \varepsilon \cdot E_C^3 \cdot A} \tag{1.7}$$

The mobility and critical electric field of Si and 4H-SiC are shown in Table 1.2.

	Si	4H-SiC
μ_n $[cm^2/Vs]$	1420	1000
Ec $[V/cm]$	$2 \cdot 10^5$	$2 \cdot 10^6$

Table 1.2: Mobility and critical electric field for Si and SiC. [3]

Therefore, with the data in Table 1.2, neglecting the differences in μ_n, if both the breakdown voltage (V_{BD}) and the area (A) are kept constant,

$$R_{epi} \propto \frac{1}{E_C^3} \rightarrow R_{epi}\,(Si) \sim 10^3 \cdot R_{epi}\,(SiC) \tag{1.8}$$

Eq 1.8, predicts that for devices of similar characteristics a SiC MOSFET device will have lower drift resistance than a Si MOSFET. This is confirmed in Fig. 1.3, where for a driven current of 40 A, a 900

V Si MOSFET has twice higher on-state voltage drop than a 1.2 kV SiC MOSFET.

1.1.3 Static behaviour

A method to understand the static behaviour of the device is through its characteristic I-V curve. As shown in Fig. 1.8, it depicts the relation between drain-source voltage (V_{DS}), gate-source voltage (V_{GS}) and drain-source current (I_{DS}).

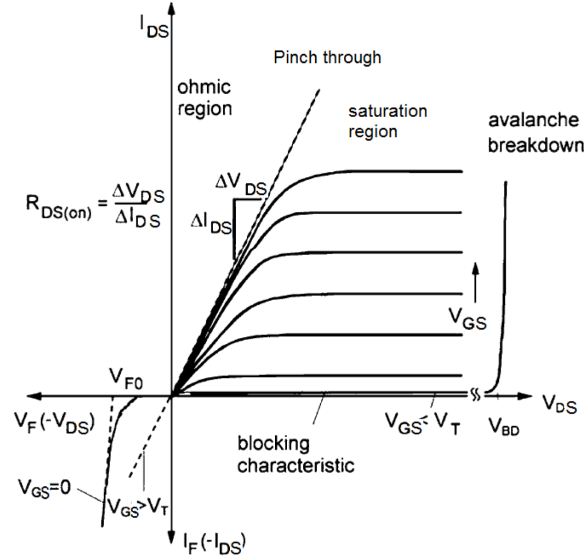
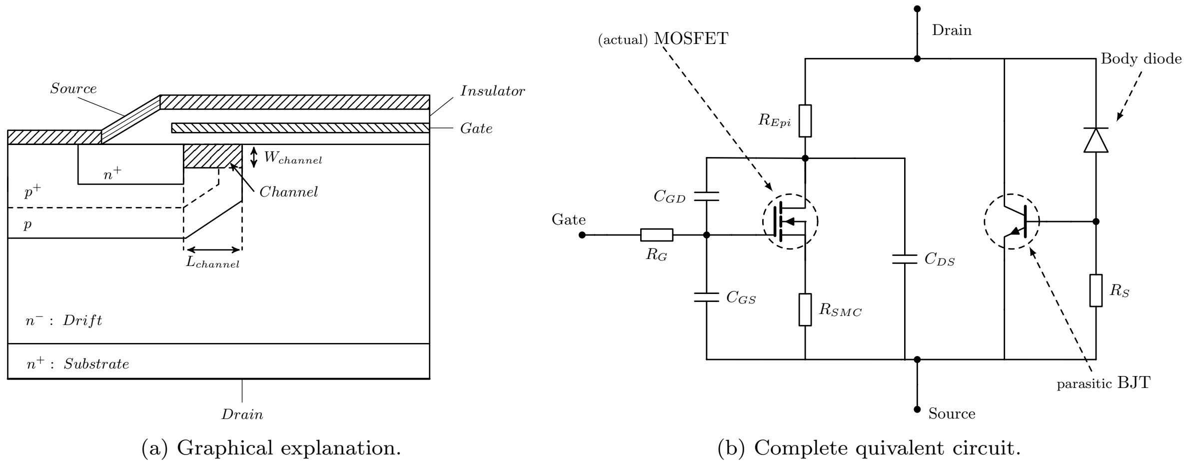


Fig. 1.8: I-V static characteristic curve of a MOSFET [13].

In the I-V curve of Fig. 1.8, a description of all static states in which the device operates is shown. In order to reduce the losses, the MOSFET operates in the ohmic region. But, when short-ciruit takes place, V_{DS} is very high and the device is driven into saturation, where high losses are dissipated.

To allow the conduction in the ohmic region, a voltage between the gate and the source must be applied, but at the same time the relation $V_{DS} < V_{GS} - V_{Th}$ must be fulfilled. In that case, as shown in Fig. 1.9 (a), in the p region a conducting channel that connects the drift with the n^+ region is formed.

An equivalent lumped model, Fig. 1.9 (b) , can be depicted in order to describe its behaviour in the ohmic region. Where $R_{SMC} = R_{CH} + R_{n+} + R_a + R_{FET}$.

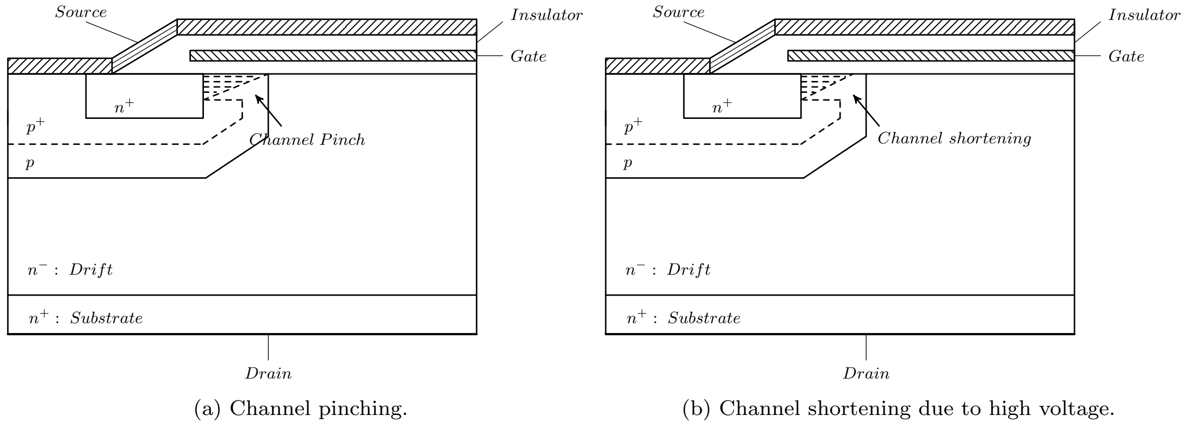


(a) Graphical explanation.

(b) Complete quivalent circuit.

Fig. 1.9: Device in the ohmic region.

But when the Drain Gate Source relation becomes $V_{DS} = V_{GS} - V_{Th}$, the pinch through voltage is reached. It defines the limit between the ohmic and saturation regions. Graphically, as shown in Fig. 1.10 (a), the channel becomes pinched. Further increase of V_{DS} leads to channel shortening Fig. 1.10 (b).



(a) Channel pinching.

(b) Channel shortening due to high voltage.

Fig. 1.10: Graphical explanation of a device entering the saturation region.

During short-ciruit, $V_{DS} \gg V_{GS} - V_{Th}$ and the drain current becomes saturated. In that case, in Eq. 1.1 I_{DS} is determined for the pinch off voltage: $V_{DS} = V_{GS} - V_{Th}$.

$$I_{DS} = \kappa \cdot [V_{GS} - V_{Th}] \tag{1.9}$$

Once this condition has been reached, the current becomes clamped, it could be modelled as a temperature-dependant current source. The temperature dependency is given by the electron mobility.

In [14,15] it is depicted that during short-ciruit, the highest electric field is located on the higher part

of the drift region. In this area as explained in [13], a Junction Field Effect Transistor (JFET) effect appears. Additionally, the highest heat generation takes place in this area [15] and as shown in [16] the highest temperature is reached in the JFET region.

1.1.4 Dynamic behaviour

In this work the switching procedure differs from the typical turn-on/off. During turn on into a short-ciruit, there is no drop of the voltage after having the current reached its load value. In Fig 1.11 the equivalent switching model is shown [11].

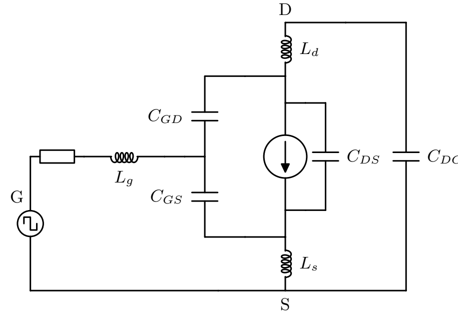


Fig. 1.11: Simplified switching model.

Where L_g, L_d and L_s are the lead inductances of the packaging. The waveforms by which the device turns on are shown in Fig. 1.12.

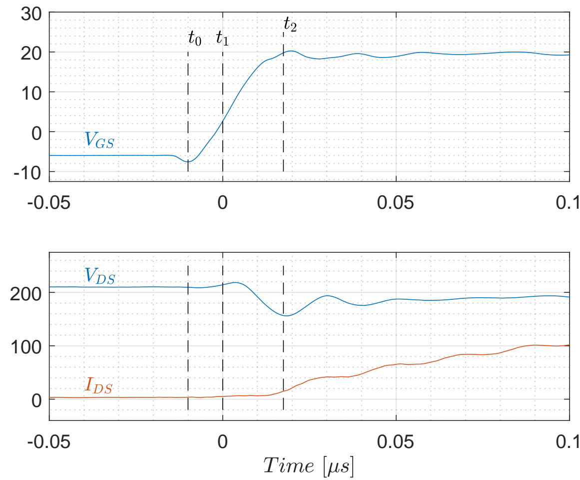
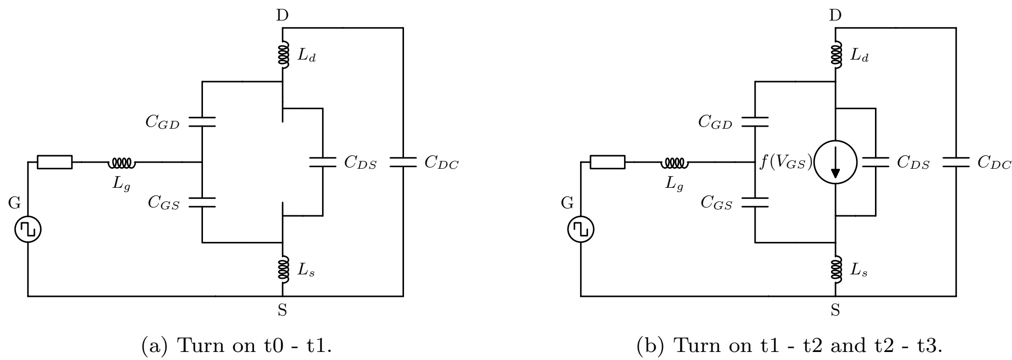


Fig. 1.12: Turn on waveforms.

As can be observed in Fig. 1.12, two main periods can be identified, t0 - t1 and t1 - t2. In Fig. 1.13, the equivalent circuit to which these periods related is shown.



(a) Turn on t0 - t1.

(b) Turn on t1 - t2 and t2 - t3.

Fig. 1.13: Equivalent circuits during switching .

The period shown in Fig. 1.13(a), t0 - t1 in Fig. 1.12 corresponds to the turn on delay time. During that time, C_{GD} and C_{GS} are charged and it corresponds to the time needed for V_{GS} to reach V_{Th}.

In 1.13(b) the second region is modelled. It corresponds to the charging of C_{GD} and C_{GS} until their corresponding voltage. By contrast with normal switching, V_{DS} does not decrease and the device enters the saturation region.

1.2 The short-ciruit in power electronic systems

In power electronic circuits, a short-ciruit can occur in different ways, the most common ones are the so-called type I and type II [3].

1.2.1 Short circuit type I

The short-circuit is noted as type I, also termed hard-switching fault (HSF), takes place when the switching device turns into a pre existing short-ciruit. Fig. 1.14, illustrates the typical current and voltage waveforms under a short-circuit type I condition. The dissipated energy during that period is very high and because of that, the mobility μ_n decreases. Therefore, the current decreases with increasing short-circuit time. The time that the device can withstand this state is limited [17].

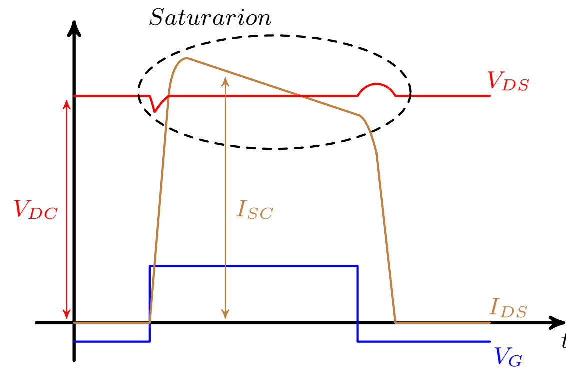


Fig. 1.14: Waveforms during short - circuit Type I.

This is the type of short-circuit that will be adopted in this project. An analysis in more detail follows in the Section 1.3.

1.2.2 Short circuit type II

Type II short-circuit, also termed failure under load (FUL), takes place during the normal conduction mode. The device behaves normally, then suddenly, a short-circuit happens and it sees the full DC-link. The typical waveforms during this type of short-circuit are shown in Fig. 1.15

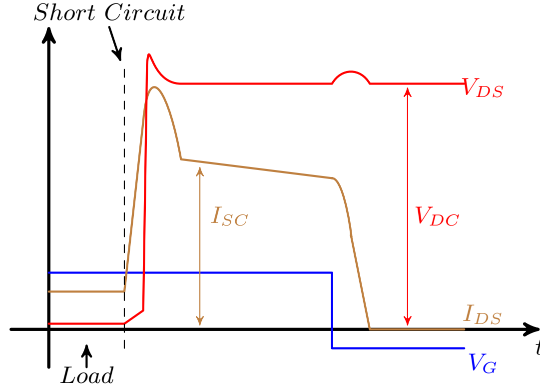


Fig. 1.15: Waveforms during short - circuit type II.

As can be seen in Fig. 1.15, in the beginning, the device is in the ohmic region, driving the load current with a low voltage drop. Then, the short-circuit occurs, the device sees the full DC-link and it is driven into saturation. In this region, both current and voltage are high and the dissipated energy is significant. As the Type I, short-circuit current (I_{SC}) decreases with time.

1.3 SiC MOSFET failure in short-circuit type I

In this work, the behaviour of SiC MOSFET under short-circuit Type I is studied. The prior-art work found in the literature regarding short-circuit robustness of SiC MOSFETs will be evaluated and compared.

1.3.1 Failure modes

First, a brief introduction of the common failure modes which can be found in the literature [14,16–20] is shown.

Two dominant failures have been experienced so far: a thermal runaway delayed failure and a sudden gate-breakdown failure.

- The delayed failure mode takes place a certain amount of time after the device turned off, two examples can be found in Fig. 1.16 and 1.17. This failure mode presents two cases, three terminal short-ciruit (GS and DS) and gate-source short-ciruit. The first case is shown in Fig. 1.16, where t_{sc} is the short-ciruit time and V_{pt} stand for the protection signal.

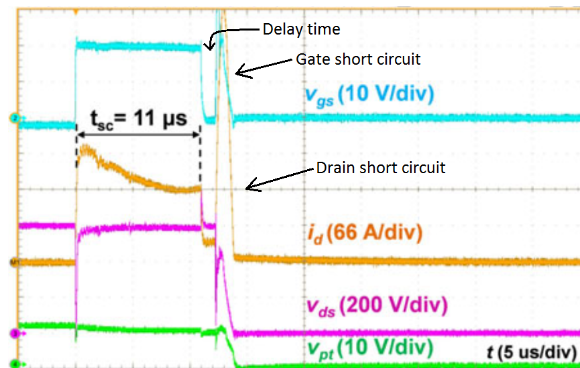


Fig. 1.16: CREE 1G [21], V_{DS} = 600 V and T_{case} = 200 ℃. Delayed failure with short-circuit of the gate-source and drain-source terminals. t_{sc} is the short-circuit time and V_{pt} stand for the protection signal. [14]

As can be seen in Fig. 1.16, the gate signal goes back to its off state, and apparently the device is turned off. However, after a 5 μs delay time, suddenly, both the gate-source and drain-source terminals become short-circuited. This type of failure has been termed by the authors as *SC: DS & GS [d]*.

The second case, in which only the gate-source terminals become short-ciruited is shown in Fig. 1.17.

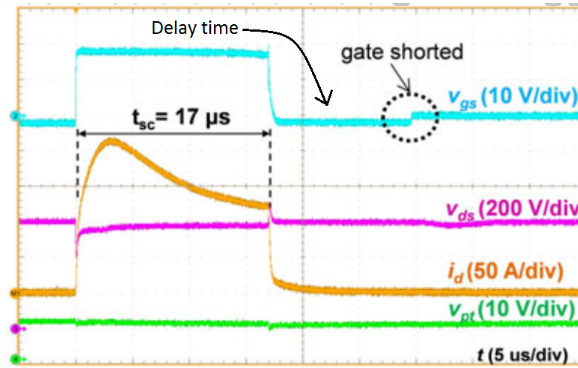


Fig. 1.17: ROHM [22], V_{DS} = 600 V and T_{case} = 200 ℃. Delayed failure with only short-circuit of the gate-source terminal [14].

In Fig. 1.17 after 17 μs the gate signal returns to its off state, turning off the device. But 12 μs after having returned to its off state a short-circuit of the gate-source terminals occurs. In contrast with the first case, the drain-source terminals do not become short-circuited and the device can withstand the applied voltage. According with [17], this second type of failure can be considered as a *soft failure*. This second type of failure was termed as *SC: GS [d]* by the authors.

- In the second failure mode, shown in Fig. 1.18, the gate-source and drain-source become short-ciruited instantly.

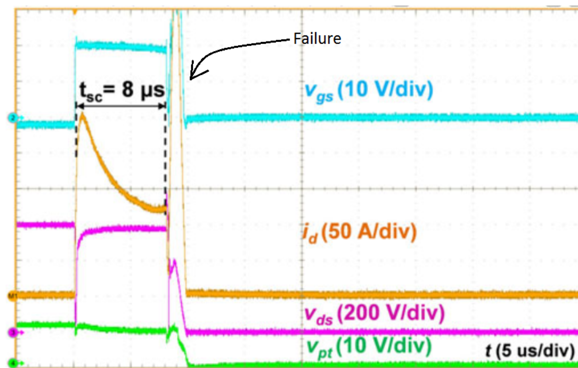


Fig. 1.18: CREE 2G [10], V_{DS} = 600 V and T_{case} = 200 ℃. Short-circuit at turn off with the short-circuit of the gate-source and drain-source terminals [14].

Fig. 1.18 shows the case were the three terminals are short-circuited. A protection signal allows to turn off the current. This third type of failure has been termed by the authors as *SC: DS & GS*.

1.3.2 Short-circuit withstand time and critical energy

When analysing the short-circuit behaviour of a given device, two parameters are basic. The short-ciruit withstand time (SCWT) and the critical energy (E_{sc}), given by Eq. 1.10. It depicts the dissipated energy during the short-circuit.

$$E_{sc} = \int_{t_0}^{t_{sc}} (V_{DS} \cdot I_{DS})\, dt \tag{1.10}$$

In the literature [14, 16–20, 23] usually 1st and 2nd generation CREE and ROHM discrete devices are evaluated. Additionally, in [18], the short-ciruit capability of SiC MOSFET modules is investigated. In Table 1.3 the basic characteristics of these most tested discrete devices is given.

Device	V_{BD} [kV]	$R_{DS\ on}$ [mΩ]	I_{DS} [A] $T_j = 100$ °C	Ref.
CMF20120, 1G CREE	1.2	80	24	[21]
C2M0080120D, 2G CREE	1.2	80	20	[10]
SCT2080KE, Rohm	1.2k	80	28	[22]

Table 1.3: Basic characteristics of the discrete SiC MOSFETS.

By collecting the data from different authors [14, 17, 20] it is possible depict a correlation between the SCWT and E_{sc}. In Fig. 1.19 the correlation is shown for $T_{case} = 25$ °C and $V_{DS} = 600$ V.

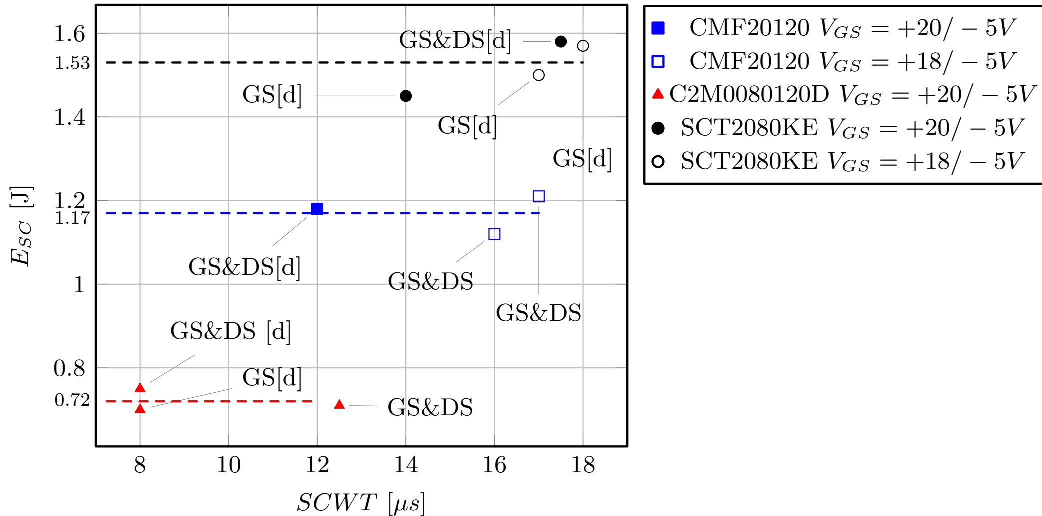


Fig. 1.19: SCWT and ESC for $T_{case} = 25$ and $V_{DS} = 600$ V [14, 17, 20].

From Fig. 1.19, it can be observed that devices of the same type exhibit approximately the same critical energy. Additionally, the SCWT may also be ranged. However, it is not possible to establish a specific SCWT for each device, e.g. 2G CREE varies from 8 to 12 μs. This may be both a sign of variation in the production process or differences in the test setup used by the authors.

It is also interesting to observe the withstand capability of the devices at different gate voltage levels. As shown in Fig. 1.19, the 1G CREE device with lower gate voltage depicts a 4 μs increase in SCTW, the ROHM device presents a similar behaviour. This agrees with the fact that a lower gate bias corresponds with a lower saturation current, and therefore the energy dissipated in the device is reduced [20].

Additionally,it can also be observed a trend of the ROHM MOSFETs towards a delayed break down with short-ciruit of the gate-source terminals. On the other hand, CREE devices appear to typically have a three terminals short-circuit.

In Fig. 1.20 the short-circuit withstanding capability at higher temperature and higher DC-link is shown. The arrow indicates the direction of more demanding test condition.

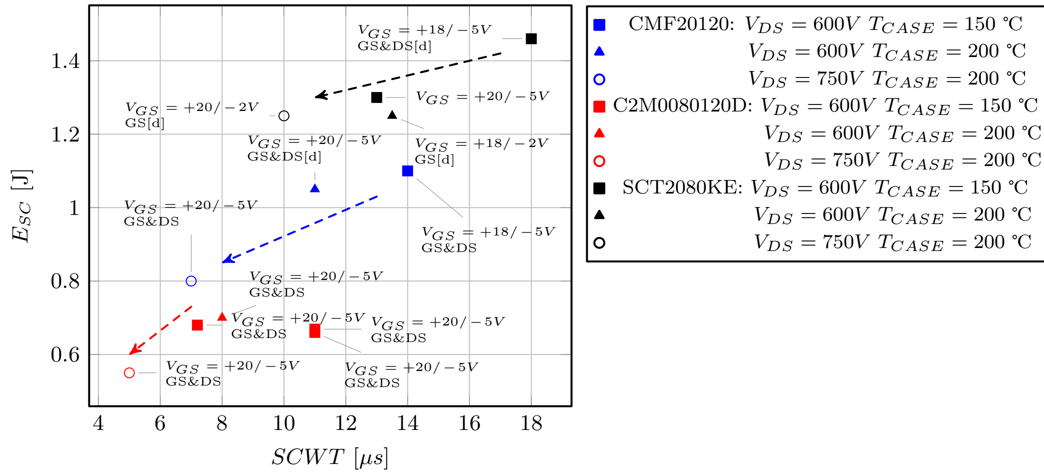
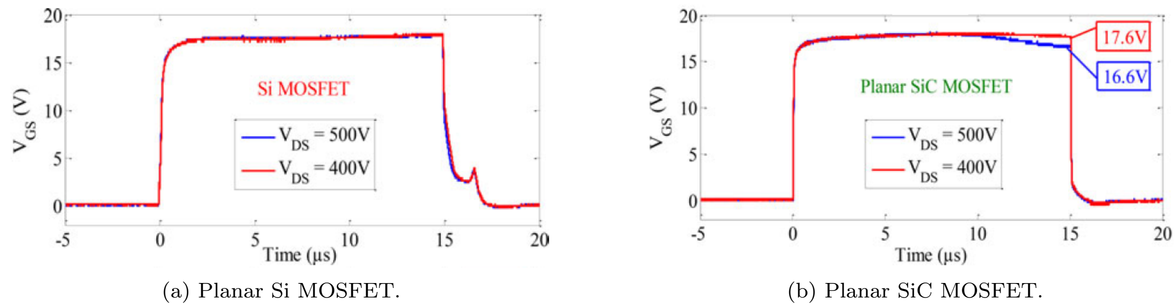


Fig. 1.20: SCWT and ESC at high case temperature and drain-source voltage. [14, 17, 20]

The tests results shown in Fig. 1.20 describe a trend towards the reduction of both SCWT and critical energy with the increase of case temperature and DC-link voltage.

1.3.3 Gate Reliability

It is interesting to observe that towards the end of sufficiently long short-circuit pulses the gate voltage decreases a few volts. As shown in, Fig. 1.21 this is a phenomenon that was not experienced in Si MOSFETs and it is observed both in discrete devices and in power modules [18, 23]. According to [23], the gate oxide thickness of SiC MOSFET is thinner than those of Si, which may be a reason for this phenomena.



(a) Planar Si MOSFET.

(b) Planar SiC MOSFET.

Fig. 1.21: Gate behaviour comparison during short-ciruit with $V_{DS} = 400$ and 500 V [23].

A concern exist on for the *Fowler –Nordheim tunnelling* process as responsible for the decrease of gate voltage. It is a quantum process by which electrons tunnel through a barrier in the presence of a high

electric field [24–27]. Thus, a current flow through the gate would decrease V_{GS}.

In [23], the behaviour of the of V_{GS} is specifically studied. A distinction between two different SiC MOSFET structures is done, planar and shielded planar. The CMF10120D presents a planar structure, by contrast, the SCT2080KE presents a shield planar structure. It is shown that the ΔV_{GS} ($\Delta V_{GS} = V_{GS,\ supply\ measured} - V_{GS,\ end\ of\ pulse}$) of a device with shielded planar structure is lower than with planar structure. Additionally, in the case of the planar device, ΔV_{GS} was observed to increase proportionally with V_{DS}.

1.3.4 Thermal Properties and Influence of the case temperature

As pointed out in Fig. 1.20 incrementing the case temperature decreased the survivability of the device, both in terms of E_{sc} and SCWT.

Different methods to determine the heat distribution and temperature at the junction may be found. In [14, 28] analytical methods to determine the junction temperature are developed. It is calculated that the peak junction temperature is in the order 1300 ℃. This extremely high temperature greatly increased the thermally generated current, which might be a possible cause of failure. Alternatively, the high temperature may degrade the material properties of the device leading to destruction [14,28]. Because the short-ciruit time is in the order of few μs, the heat may not have enough time to propagate to the case. This makes the device behaviour independent of external cooling [14].

Alternatively, in [16, 29] the thermal distribution is determined by Finite Element Methods (FEM). It allows for a simulation in which it is possible to determine the heat distribution inside the device. It is found that the highest temperature may reached in the FET region, with temperatures over 2000 K at breakdown.

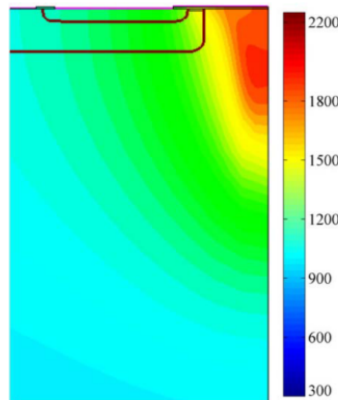


Fig. 1.22: Simulated temperature distribution $T_{SC} = 18.5\ \mu s$ ($V_{DS} = 400$ V; $V_{GS} = 18$ V; $T_{case} = 27$ ℃; temperature scale in K) [29]

However, both methods require a complexity in terms of methods and knowledge of semiconductor properties. In [30] it is proposed to solve the problem by the resolution of a thermal network. In Fig. 1.23 a thermal modelling of a MOSFET of three thermal layers with their corresponding thermal resistances and capacitances is shown.

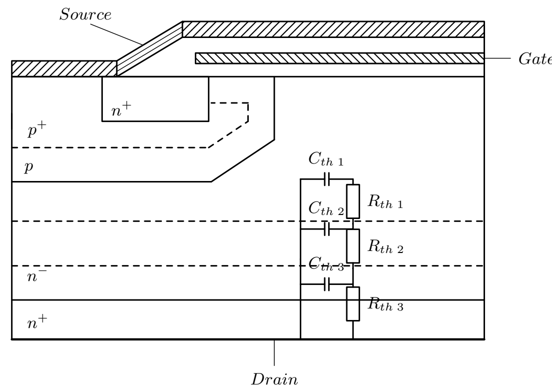


Fig. 1.23: Cauer thermal modelling of a MOSFET with three layers.

Where $R_{th\ k}$ is the thermal resistance and $C_{th\ k}$ is the thermal capacitance of the corresponding layer. Assuming that the losses are only produced on the first layer, as shown in Fig. 1.24, an electro-thermal model may be designed to comprehend electrical losses and temperature.

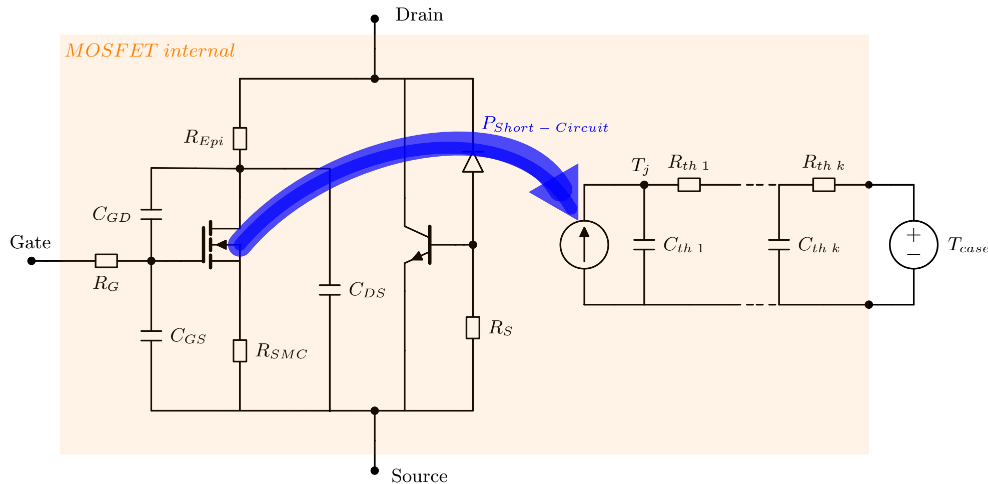


Fig. 1.24: Thermal network proposed by [30] to estimate the junction temperature (Tj).

The model shown in Fig. 1.24 shows the case of a clamped case temperature (T_{case}). The resolution of such a circuit allows for a an estimation of the junction temperature.

1.3.5 Hole current

It was aforementioned, that the internal structure of the MOSFET has an intrinsic BJT which, if activated, leads to the destruction of the device. In contrast with the switching of a MOSFET, bipolar devices i.e. BJT and IGBT present a tail current during turn off. Thus in the switching of a MOSFET one would not expect such behaviour. However, the short-ciruit results presented by Romano et al. [16, 29], Fig. 1.25, show an unexpected tail current in I_{DS}.

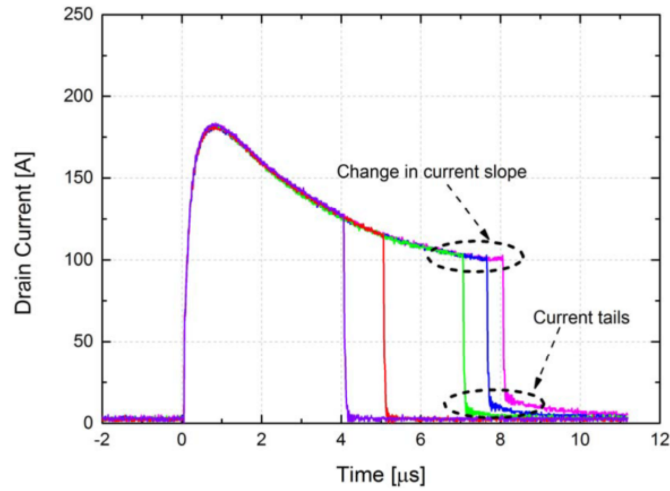


Fig. 1.25: Short circuit waveforms, V_{DS} = 600 V, V_{GS} = 19 V and T_{case} = 75 ℃. [29]

According to [29], the abnormal behaviour observed during turn off, may associated to a partial activation of the parasitic BJT. To understand the behaviour of hole current a FEM simulation is done by [29], Fig. 1.26.

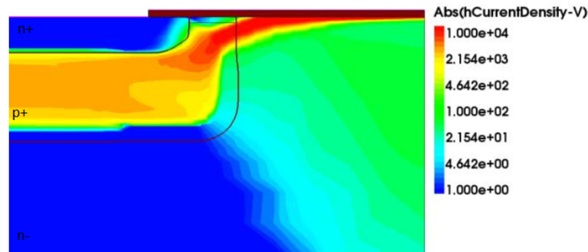


Fig. 1.26: Hole current density simulation. V_{DS} = 400 V, V_{GS} = 18 V, at T_{sc} = 18 μs, capture at 18.3 μs and current density scale in $A \cdot cm^2$.[29]

As can be observed in Fig. 1.26 , in the p+ region a lateral hole current flow is observed. The results suggest that because of this current flow, the parasitic BJT may be activated thus generate a current tail at turn off.

1.4 Project motivation

Silicon Carbide switching devices are becoming increasingly popular as the devices of choice by designers. Hand in hand with the introduction of such devices comes the need to assess their reliability on extreme conditions such as short-ciruit. The studied literature shows that SiC MOSFETs still face challenges when subjected to short-ciruit test. However, much of the effort has been directed to the comparison of the behaviour of devices from different manufacturers and component generations. Thus, there is a lack of work directed towards the relation between static characteristics and short-ciruit behaviour. Moreover, one should be aware that SiC devices are in continuous development, and their short-ciruit behaviour may vary over time which may make the available literature obsolete.

This work originates from the need to fill the lack of information in regards to a relation of static and short-circuit behaviour. In this sense, it is considered that addressing and identifying the differences between devices of the same model may be an appropriate method to focus this work. In this way it is possible avoid differences introduced by the internal structure found on devices by diverse manufacturers. Additionally, to keep up with modifications and improvements that may have been introduced, the latest devices have been tested.

1.5 Objective

This work aims to present the results of short-ciruit testing in an accurate and easy to understand manner. In order to achieve it, trends and correlations are pointed out. The objective of the report is to show weak points and identify challenges which SiC technology still faces in the field of short-circuit withstand capability. In this sense static and dynamic testing of the devices is performed. The problem was bounded with the identification by static testing, of devices that presented a distinctive parameter may influence the short-circuit behaviour.

1.6 Problem Formulation

From the objective, the following question may be developed,

Do differences in individually measured drain-source leakage (I_{DSS}) between different SiC MOSFETs of the same model affect the short-ciruit behaviour in terms of short-circuit waveform, withstand time and energy?

1.7 Scope and Limits of the project

The scope and limits of the project allow the reader to understand what is ought to be expected from this project. In this sense, which tasks have been performed and which ones fall outside the amplitude of the project.

Inside

- This project has mainly been directed towards the evaluation of real devices, therefore much experimental results should be expected.

  In this sense, static characterization for a wide range of variables at increasing temperatures hs been performed.

  Short circuit testing has been perform for a range of temperatures and DC-link voltages, this has make it possible to perform a description of the way the device is affected by the test parameters.

- In order to complement the obtained measurement results, the short-ciruit energy has been calculated and the junction temperature has been estimated.

Outside

- This work aims to assist the reader to observe and understand which are the current issues evolved in short-circuit behaviour of SiC MOSFETs. Therefore, a final or exact reason for which the devices fail should not be expected in this work.
- An alternative method to understand the affect of the short-circuit on the device parameters would have been to perform static test after each short-ciruit. However, since the purpose has been to investigate if a relation exist between leakage current and short-circuit this method was discarded.

Limits

Even though the project could be successfully completed, some factors were encountered which limited our access to a comprehensive evaluation into short-circuit breakdown.

For the static characterization, I would point out the limitation of the maximum temperature at which it could be performed. It would have been interesting to perform static characterization at higher temperature, the electrical parameters would have been more evident.

In regards to the short-circuit test, the behaviour of the MOSFET die could not isolated from the whole packaging. During the short-circuit, effects that may be associated with the packaging rather than with the transistor may have been experienced.

Additionally, for post-failure analysis of only electrical parameters could be evaluated. This difficults a comprehensive evaluation of the condition of the device.

1.8 Outline of the Master Thesis

The setup and hardware that was developed for testing is presented in Chapter 2. Additionally, the setup which was used and available at the E.T. Department is presented in Appendix B.

The presentation of the test results has been separated in two parts. Two different SiC MOSFET models were tested, a 1.2 kV 36 A and a 1.2 kV 90 A SiC MOSFET since their characteristics are not comparable, it was considered appropriate to analyse them on their own. In Chapter 3 the 36 A SiC

MOSFET is analysed and in Chapter 4 the 90 A device. Additionally, the conditions for static testing are given in the Appendix A.

Finally, because both devices displayed similar behaviour apart of individual conclusions in the corresponding chapter. A common conclusion which encompasses both devices is given in the last chapter, Chapter 5.

Chapter 2

Hardware developed for testing

The Non Destructive Tester (NDT) available at the Energy Technology (ET) laboratory is shown in Appendix B. It a flexible test ground for many topologies, therefore, a PCB had to be developed to adapt the TO - 247 footprint to the NDT connection.

2.1 Adapter

The Devices Under Tests (DUT) are a 1.2 kV and 36 A SiC MOSFET, C2M0080120D and a 1.2 kV and 90 A SiC MOSFET, C2M0025120D. Their basic characteristics are shown in Table 2.1.

Device	V_{BD} [kV]	$R_{DS\ on}$ [m Ω]	I_{DS}@ 25 ℃[A]	I_{DS}@ 100 ℃	named	Ref.
C2M0080120D	1.2	80	36	24	S1 - 4	[10]
C2M0025120D	1.2	25	90	60	S5 - 9	[31]

Table 2.1: Characteristics of the DUTs.

These present a TO - 247 footprint which needs to be adapted to the NDT. For this purpose a PCB had to be developed. This PCB should also have the footprint for the gate driver CGD15HB62P1 from CREE [32]. To perform fast switching, the inductance should be kept low. In this sense, differential planes are used for both the gate-source and the drain-source connection. In regard to the gate-source, a separate differential connection was traced to avoid the high current traces and reduce the inductive loop. For the drain source, apart of differential planes, a decoupling capacitor was added. The PCB which was developed and manufactured is shown in Fig. 2.1.

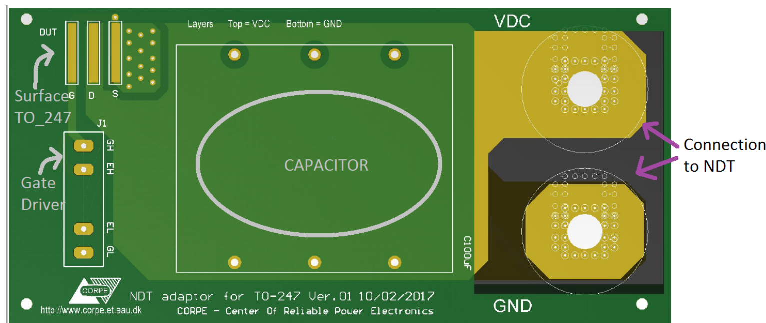


Fig. 2.1: Developed and manufactured NDT to TO - 247 PCB adapter.

To perform the test at a given temperature, a heat plate is attached to the DUT. It consists of a PTC heater [33] and a block of aluminum. A K - type thermocouple is attached to the aluminium block and fed back to a PID controller for temperature control [34]. In Fig. 2.2, the setup with the DUT, the current and voltage probes, driver and heat plate is shown. Note that the measurements are done after the capacitor.

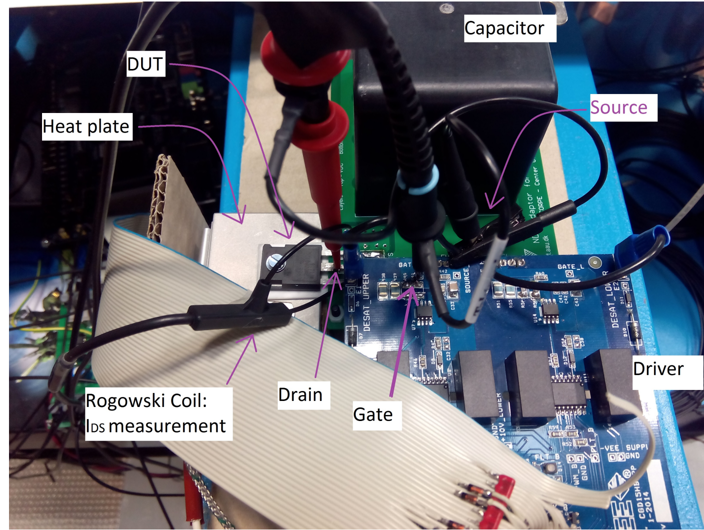


Fig. 2.2: Test setup with the DUT, heat plate, capacitor, driver and measurement probes.

2.2 Decoupling Capacitor

With the purpose of reducing the parasitic inductance and increase the raising of $\frac{dI_{DS}}{dt}$, Eq. 2.1, a capacitor is installed near the DUT.

$$\frac{V_L}{L\downarrow} = \frac{dI_L}{dt}\uparrow \tag{2.1}$$

In Table 2.2 the requirements for the capacitor are shown, these are estimated from the results observed in the literature. ΔV_{DS} is set at a 5% to avoid a high drop in the DC-link during short-circuit.

Variable	Requirement	Comments
V_{DC}	1.2 kV	Maximum DC link that the DUT can withstand
$I_{nominal}$	450 A	assumed $10 \cdot I_{Nominal}$
ΔV_{DS}	30 V	Maximum test voltage is expected: 600V, $600 \cdot 5\%$
t_{on}	10 μs	Maximum tested short-circuit time.

Table 2.2: Decoupling capacitor requirements.

These requirements are translated into Eq. 2.2.

$$C = \frac{I \cdot \Delta t}{\Delta V_{DS}} = \frac{450 \cdot 10 \cdot 10^{-6}}{30} = 150\ \mu F \tag{2.2}$$

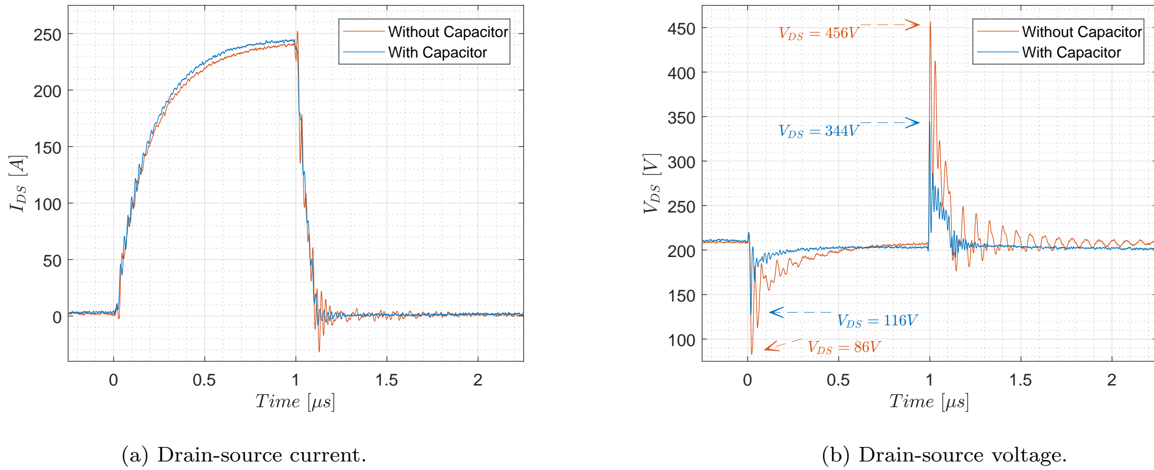
According to Eq. Eq. 2.2 a capacitor of 150 μF is needed. However, a component that could be installed in a PCB for 1.2 kV and 150 μF was not found in the market. The MKP1848C film capacitor from Vishay, Table 2.3, was the capacitor with the closest characteristics to the requirements

Part	Manufacturer	Capacitance	Voltage	expected t_{sc} at 600 V	Ref.
MKP1848C	Vishay	100 μF	1 kV	6.67 μs	[35]

Table 2.3: Characteristics of the installed decoupling capacitor.

According with Eq. 2.2, such a capacitor would allow a maximum short-circuit pulse of 6.7 μs for a V_{DS} = 600 V and a current of 450 A.

In Fig. 2.3, a comparison of I_{DS} (a) and V_{DS} (b) with and without decoupling capacitor and an increment of R_{GS} = 5 Ω to 10 Ω is shown.



(a) Drain-source current.

(b) Drain-source voltage.

Fig. 2.3: Comparison of electrical behaviour without and with decoupling capacitor, V_{DS} = 200 V and $t_{sc} = 1\mu s$.

As can be seen in Fig. 2.3(a) even if the gate resistance was decreased, the rise in I_{DS} does not differ significantly between both cases. On the other hand in Fig. 2.3(b), for the case of V_{DS}, the under and over voltage peaks are diminished. For example, during turn off, the over-voltage peak is a 24 % lower. This is an important aspect because switching at higher voltages could generate peaks that exceed the rated limit of the DUT (1.2 KV).

Having seen the results of this test, it was concluded that the addition of the capacitor was beneficial. Nevertheless, one should be aware that the DUT is not protected from the discharge of this capacitor.

Chapter 3

1.2 kV/ 36 A SiC MOSFET

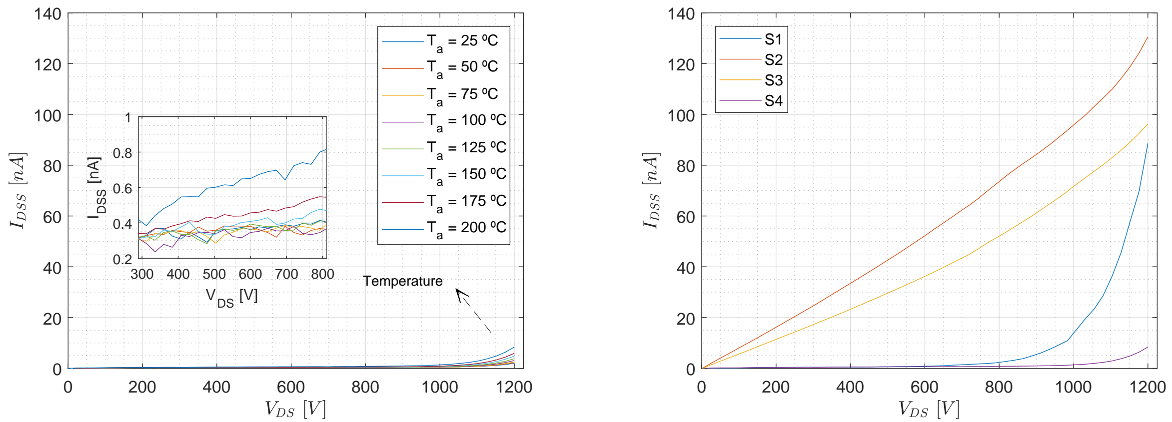
In this chapter the testing of the 1.2 kV/ 36 A SiC MOSFET is presented. Four devices of the same model have been tested, named as S1, S2, S3 and S4. First the static characterization is shown, then the dynamic testing afterwards a post processing of the results and finally, the conclusions.

3.1 Static testing

The static testing of the 1.2 kV/ 36 A SiC MOSFET, C0080120D, was performed at the ambient temperatures (T_a) of, 25, 50, 75, 100, 125, 150, 175 and 200 °C. Enough time is left for the DUT to heat up, and it is assumed that the junction temperature is equal to the ambient. Four samples have been tested, named S1 to S4. The testing conditions that the device analyser was programmed with are shown in Appendix A. The device analyser is the B1506A, and the setup is also shown in Appendix A.

3.1.1 Drain-source leakage current (I_{DSS})

The drain source leakage (I_{DSS}) current has been tested within range of V_{DS} = 0 - 1.2 kV with a gate-source voltage of 0 V. In Fig. 3.1(a), the measured I_{DSS} of S4 at increasing ambient temperatures is shown, in detail a zoom of the area of interest ($V_{DS} = 300 \ - \ 800V$) is presented. In Fig. 3.1(b) a comparison of the four devices S1 - 4 at T_a of 200 °C can be observed.



(a) Static test: drain-Source leakage current as a function of the temperature of S4.

(b) Static test: drain-Source leakage current, device comparison at T_a = 200 °C.

Fig. 3.1: Static test: drain-source leakage current.

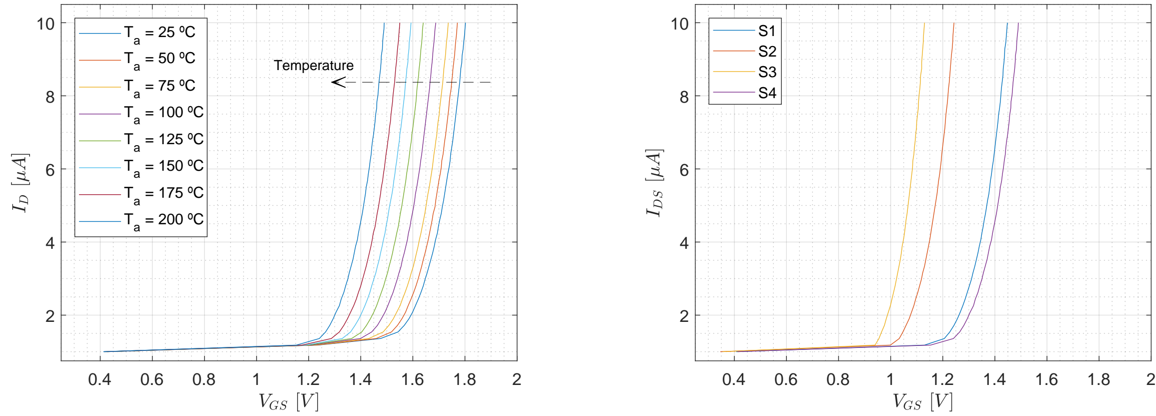
Two phenomena can be observed in Fig. 3.1(a). First, the drain-source leakage current is proportional to the applied voltage. In the case of S4, it is especially noticeable for the 1 - 1.2 kV range. Second,

the leakage current is also a function of the ambient temperature, being especially noticeable when its the temperature is above 175 ℃. For example, in the zoomed window, the leakage current at V_{DS} = 600 V and 200 ℃ is 1.6 times higher than at 25 ℃.

The results shown in Fig. 3.1(b), are very interesting because they show a significant difference on the current values of the different devices at high temperature. It should be mentioned that the leakage current value did not exceed the maximum stated by the manufacturer in the datasheet, (100 μA) [10]. The static testing depicts an 83 times higher leakage current of S2 in comparison with S4 at $V_{DS} = 600$ V. In accordance with [14] these devices with higher leakage current may present lower short-circuit ruggedness.

3.1.2 Gate-source threshold voltage ($V_{GS\,Th}$)

The static testing of the threshold voltage ($V_{GS\,Th}$) is shown in Fig. 3.2. In (a) the $V_{GS\,Th}$ behaviour of S4 for increasing temperature is shown and in (b) the comparison of the 4 devices at T_a =200 ℃ can be observed.



(a) Gate-source threshold voltage of S4 as a function of the temperature.

(b) Device comparison of $V_{GS\,Th}$ at T_a = 200 ℃.

Fig. 3.2: Static test: gate-source threshold voltage.

As can be seen in Fig. 3.2(a), the threshold voltage decreases with increasing temperature. At 200 ℃ its value is a 25 % lower than at 25 ℃. In Fig. 3.2(b) a large variation of the threshold voltage between the four devices at 200 ℃ exists. The DUT named S4 presents the highest threshold voltage while S3 the shows the lowest.

In Fig. 3.3, the threshold voltages for the tested temperatures are included into one figure. The method to determine the threshold voltage is shown in Appendix A.

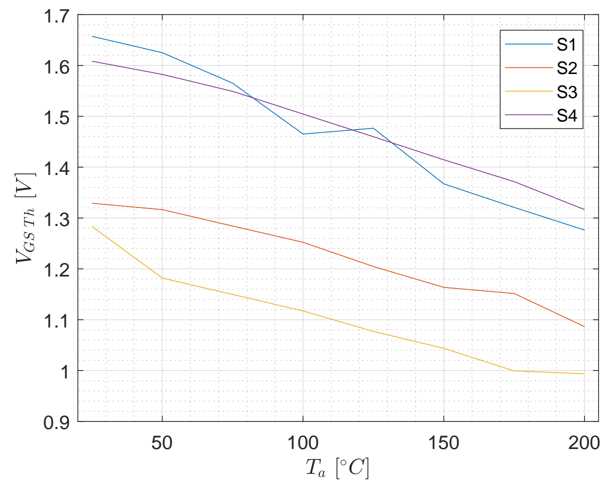


Fig. 3.3: Threshold voltage variation with increasing ambient temperature.

In agreement with the results in Fig. 3.2(b), in Fig. 3.3 it can be observed that S3 presents the lowest threshold voltage all temperatures.

3.2 Dynamic testing

To understand the behaviour and robustness of the 1.2 kV/ 36A SiC MOSFET during short-circuit and its relation with the drain-source leakage current, the devices were subjected to a wide range of tests. The influence of three parameters has been studied: short-circuit time, DC-link voltage and case temperature.

The gate drive characteristics are given in Table 3.1.

Variable	Value	Comment
V_{GS}	$+20/-5$ V	Recommended
R_G	10 Ω	Reduce the oscillations

Table 3.1: Gate drive characteristics.

3.2.1 Test procedure

Three 1.2 kV/ 36 A, C2M0080120D, devices have been tested, S1, S2 and S4. As it was shown previously in Fig. 3.1(b), they present the lowest and highest leakage current. Therefore, by choosing these devices it is intended to investigate whether a correlation between I_{DSS} and the short-circuit behaviour exists.

As shown in the next Diagram 3.4, S1 and S2 have been tested until destruction. On the other hand, S4 was tested up to DC-Link voltage $V_{DS} = 400$ V and case temperature, $T_{case} = 150$ °C.

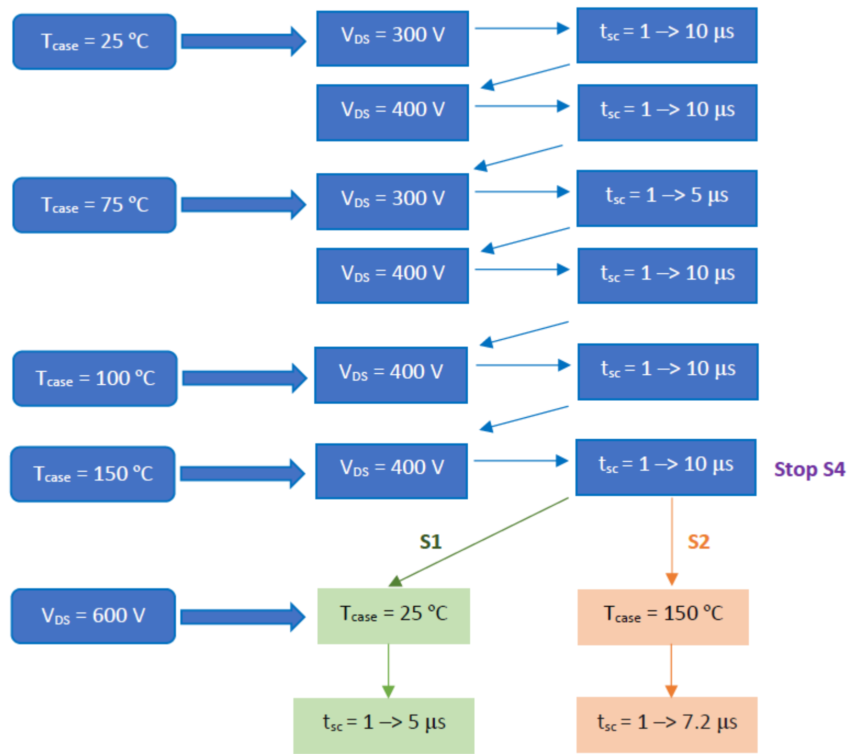
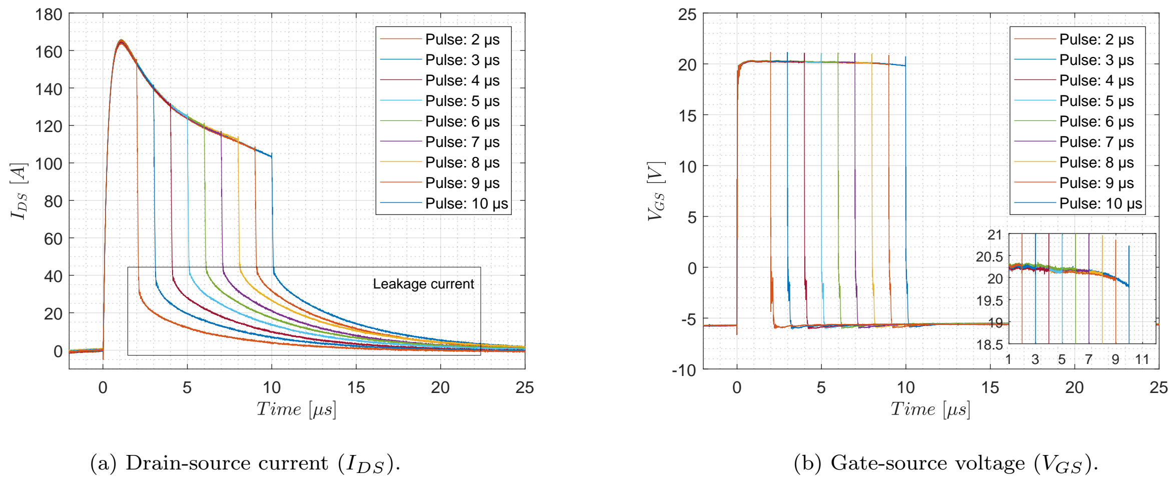


Fig. 3.4: Short-Cirucit test procedure followed for the 1.2 kV/ 36 A SiC MOSFETs. t_{sc} stands for the pulse length-

It should be commented, that enough time was left for the case temperature to diffuse to the junction. Therefore, it is assumed that the junction temperature is equal to the case.

3.2.2 Short-circuit time dependency

The short-circuit time dependency depicts the behaviour of the device with increasing pulses. In Fig. 3.5 the behaviour of S1 at T_{case} = 25 °C V_{DS} = 400 V and short-circuit pulse duration from 2 to 10 μs is shown. The short-circuit current (I_{DS}) waveform can be observed in (a) and the gate voltage (V_{GS}) can be seen in (b).



(a) Drain-source current (I_{DS}).

(b) Gate-source voltage (V_{GS}).

Fig. 3.5: Short-circuit waveforms of S1 for increasing pulse length at $T_{case} = 25$ ℃ and $V_{DS} = 400$ V.

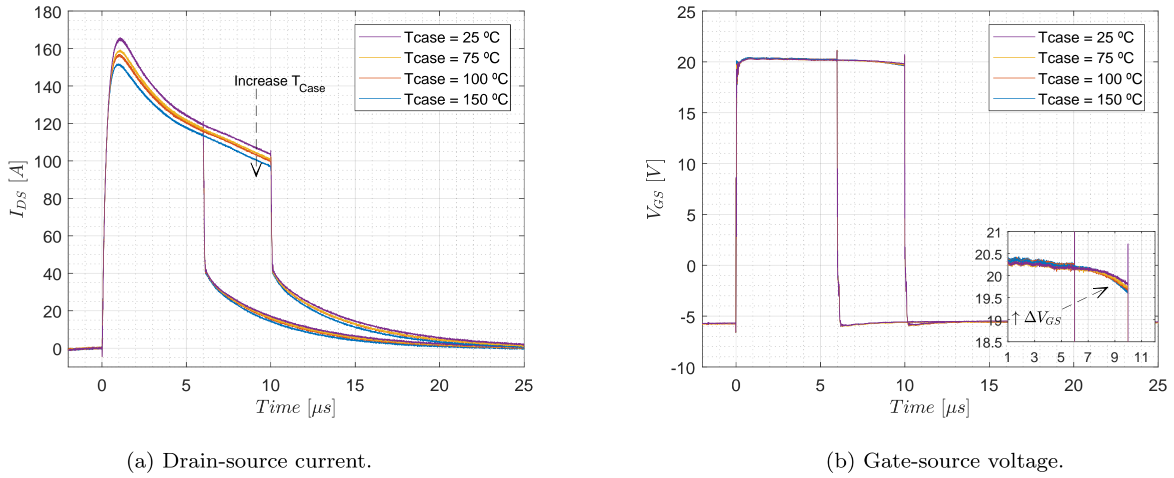
The results in Fig. 3.5 show that the device can withstand the typical 10 μs short circuit withstand time. As can be seen in (a), the device presents a peak I_{DS} of seven times its rated current, 170 A. After the initial peak, the current decreases, first (pulse = 2 $\rightarrow$ 5 μs) with a high slope and then (pulse = 5 $\rightarrow$ 10 μs) linearly with a slope of -4 $A/\mu s$. The high losses during the short-circuit produce a temperature increment which decreases the carrier mobility. In contrast with other works [14, 16, 17], the slope remains constant.

When the DUT is turned off, it presents a noticeable leakage tail current. The initial value of the leakage current increases for pulses of 2 to 5 μs, but after that, its value appears to be clamped at around 45 A.

In agreement with the studied works, in Fig. 3.5(b) the drop of the gate voltage is also observed for sufficiently long pulses. For example, for a pulse of 10 μs, the gate voltage has reduced 0.5 V from its original value.

3.2.3 Case temperature dependence

Silicon Carbide devices are expected to be used in high temperature applications [12] , therefore, its short-circuit behaviour over a range of temperatures should be evaluated. In Fig. 3.6 the behaviour for pulses of 6 and 10 μs, for $V_{DS} = 400$ V and $T_{case} = 25$, 75, 100 and 150 ℃ is shown. The drain-source current presented in (a) and the gate-source voltage waveform is shown in (b).



(a) Drain-source current.

(b) Gate-source voltage.

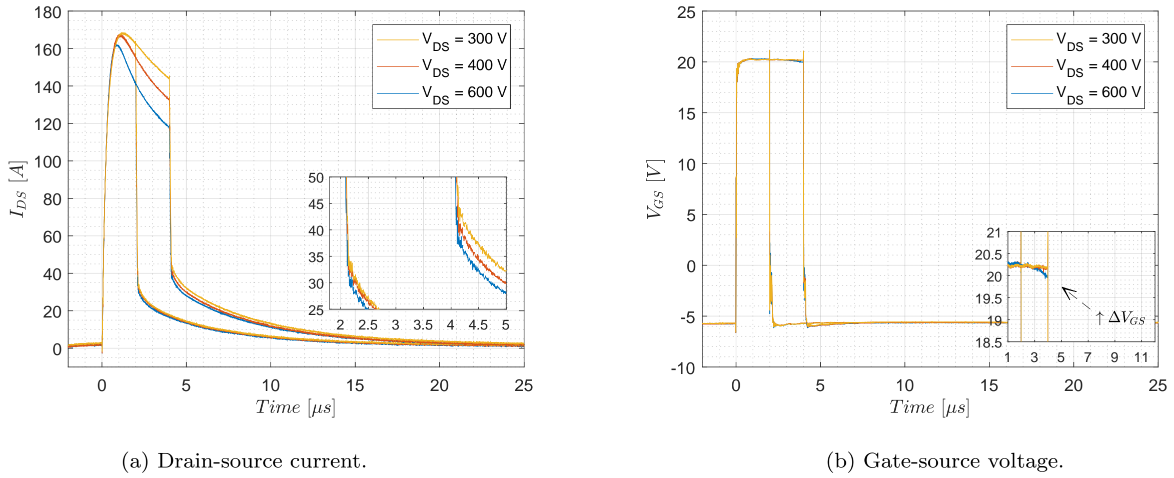
Fig. 3.6: Temperature comparison of S1 for T_{case} = 25, 75, 100 and 150 ℃ and $V_{DS} = 400\ V$ with short-circuit pulses of 6 and 10 μs.

In Fig. 3.6(a) it can be observed a decrease of short-circuit current with increasing case temperature. This is in agreement with a reduction of electron mobility due to higher temperature.

In Fig. 3.6(b), it should be observed that the temperature dependency of the gate level is significant during long short-circuit pulses. For example, for a pulse of $t_{sc} = 10\ \mu s$ and at a case temperature of $T_{case} = 150$ ℃ the voltage drop is $\Delta V_{GS} = 0.65$ V, a 25 % higher than at 25 ℃.

3.2.4 DC-link voltage dependence

Up to this point, test results were shown for $V_{DS} = 400$ V, quite below the nominal voltage of the DUT, usually around two-thirds the breakdown voltage. In Fig. 3.7 the DC link voltage dependence of S1 is depicted for $V_{DS} = 300$, 400 and 600 V. T_{case} is in all cases 25 ℃, and the pulse length is 2 and 4 μs. In (a) I_{DS} is presented and in (b) V_{GS}.



(a) Drain-source current.

(b) Gate-source voltage.

Fig. 3.7: Comparison for increasing DC-link voltage V_{DS} = 300, 400 and 600 V of S1 at the case temperature of T_{case} = 25 ℃ with pulses of t_{sc} = 2 and 4 μs.

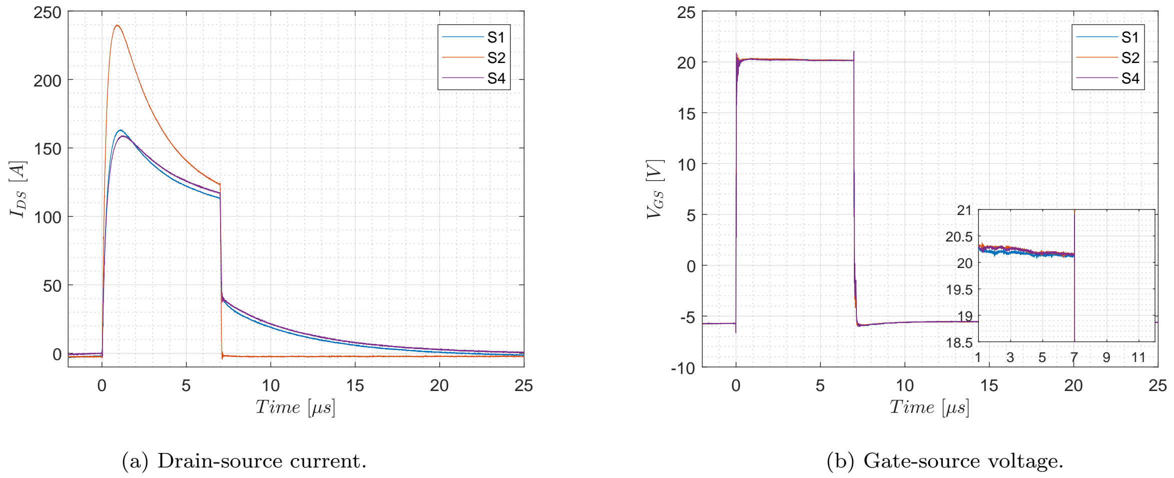
As can be observed in Fig. 3.7(a) increasing V_{DS} is implies higher dissipated power, therefore, the saturation current decreases. This is in agreement with the previous results. However, it is interesting to observe that the initial value of leakage current is lower at higher DC voltage. This contrasts with the results shown for the static characterization in Fig. 3.1, were higher voltage implied higher leakage current.

On the other hand, in Fig. 3.7(b) it should be noted the appearance of a drop in the gate voltage, for the DC-link of V_{DS} = 600 V at 4 μs.

3.2.5 Device comparison

The comparison of the different devices subjected to the same test conditions is presented for two case temperatures: in Fig. 3.8 for T_{case} = 25 ℃ and Fig. 3.9 for 100 ℃.

In Fig. 3.8, the DC-Link voltge is V_{DS} = 400V and the pulse length is t_{sc} = 7 μs.



(a) Drain-source current.

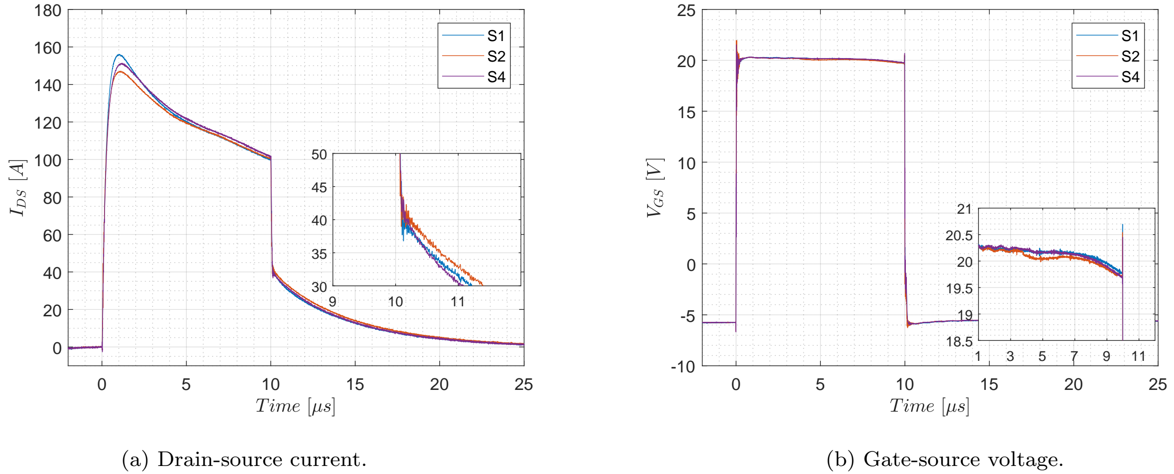
(b) Gate-source voltage.

Fig. 3.8: Devices S1, 2 and 4 comparison for T_{case} = 25 ℃ and V_{DS} = 400 V. The pulse length is 7 μs.

The results of Fig. 3.8(a) show and interesting behaviour. On one hand, S2 presents a higher short-circuit peak of I_{DS} = 240 A and no leakage current after turn off. By contrast, S2 and S4 present a reduced peak , though not the same and both present a high leakage current.

On the other hand, in Fig. 3.8(b) the behaviour described by the gate-source does not show differences between the tested devices.

In Fig. 3.9, the case temperature is increased to T_{case} = 100 ℃ the test voltage is V_{DS} = 400 V and the pulse is t_{sc} = 10 μs.



(a) Drain-source current.

(b) Gate-source voltage.

Fig. 3.9: Devices S1, 2 and 4 comparison for T_{case} = 100 ℃ and V_{DS} = 400 V. Short circuit pulse of 10 μs.

The measurements obtained for I_{DS} in Fig. 3.9(a) contrasts with those in Fig. 3.8(a). Interestingly, in this case, S2 behaves similarly to S1 and S4. Additionally, it has the lowest saturation current.

In regards to the drain-source leakage current, S2 presents a 5% (measured at $Time = 10.5\mu s$) higher

leakage current than S1 and S4. The higher leakage current is in agreement with the results of the static test, however, the difference is much lower than that shown in Fig. 3.1(b).

Fig. 3.9(b) shows an interesting behaviour of S2, at 3.75 μs a sudden reduction of $\Delta V_{GS} = 0.1$ V is measured. This phenomenon is not observed neither in S1 or S4. Even though S2 appears to become degraded, towards the end of the pulse, when ΔV_{GS} increases, S2 gate does not appear to be more leaky than S1 or S4.

3.2.6 Gate-source drop

A reduction of the gate voltage with increasing pulse length is observed in the three tested devices. It is a sign that current flows through the gate, in Fig. 3.10 the drop as a function of the temperature measured at $Time = 10$ μs and for an applied voltage of $V_{DS} = 400$ V is shown.

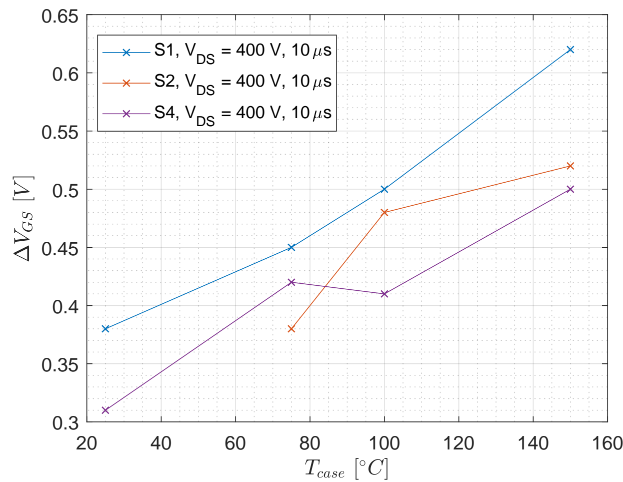


Fig. 3.10: Gate voltage drop (ΔV_{GS}) for S1, 2 and 4 for the drain-source voltage of 400 V, data taken at $Time = 10$ μs.

It can be observed in Fig. 3.10 that the gate drop is proportional with temperature. Additionally, S1 presents the highest drop at all tested temperatures.

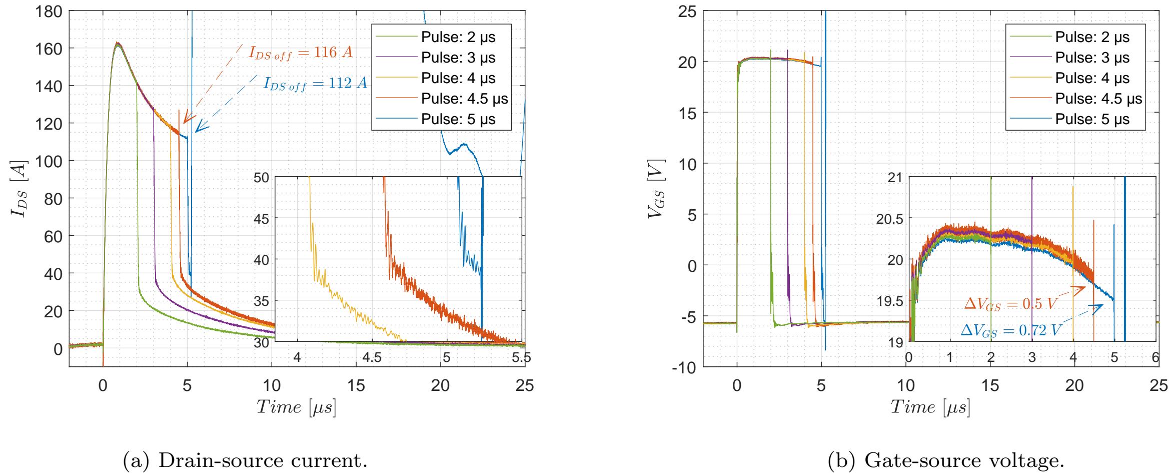
3.2.7 Degradation and destruction

As previously commented, in order to investigate the degradation and the destruction mechanism, S1 and S2 have been pushed to their limits. In both cases failure occurs with a DC-link voltage of $V_{DS} = 600$ V. However, the case temperature at which destruction was induced varied and so did the breakdown procedure.

Breakdown of the 1.2 kV/ 36 A, S1, at $T_{case} = 25$ ℃ and $V_{DS} = 600$V.

The breakdown of the 1.2 kV/ 36 A S1 MOSFET occurs at a case temperature of $T_{case} = 25$ ℃ and DC-Link of $V_{DS} = 600$ V. As can be observed in Fig. 3.11, the breakdown happens suddenly with a

pulse length of 5 μs.



(a) Drain-source current.

(b) Gate-source voltage.

Fig. 3.11: Breakdown of S1, at V_{DS} = 600 V and with T_{case} = 25 ℃.

In Fig. 3.11(a) the drain-source current is depicted. As can be observed, the breakdown is delayed 1.5 μs after turn off. At that point, the leakage current is approximately I_{DS} = 39 A. The short-circuit withstand time is lower than that observed, at the test same condition, in the state of the art .

In (b) it can be observed the decrease of the gate voltage, which at the short-circuit instant is ΔV_{GS} = 0.72 V.

The final state of the DUT is shown in Fig. 3.12

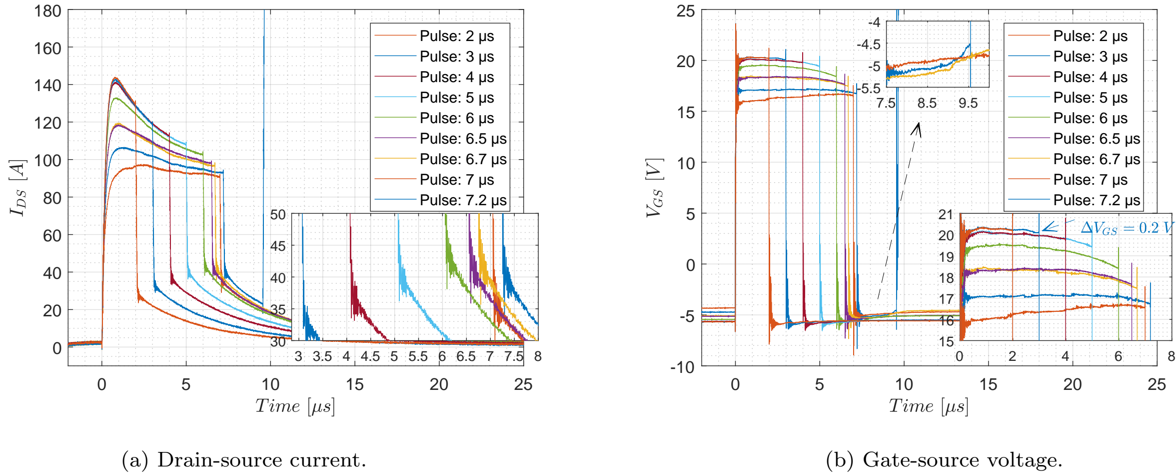
Fig. 3.12: State of the device after the breakdown.

As it can be observed, the device has exploded and the chip is left visible. The exposed part corresponds

to the source pad. The three leads remained attached to the package. After being dissembled from the PCB, three terminal short-circuit was measured. This failure mode has also been observed in the state of the art.

Breakdown of the 1.2 kV/ 36 A, S2, T_{case} = 150 ℃ and V_{DS} = 600V.

The destruction of S2 happened at $T_{case} = 150$ ℃ and a pulse of 7.2 μs. In contrast with the previous case, as can be seen in Fig. 3.13 it suffers a progressive degradation. Already at a pulse of 3 μs the gate dropped from raising to fall. In the 7.2 μs pulse, the breakdown is delayed, 2 μs after the turn off. At that instant, the drain-source current is $I_{DS} = 25$ A.



(a) Drain-source current.

(b) Gate-source voltage.

Fig. 3.13: Breakdown of S2, at $V_{DS} = 600$ V and case temperature of $T_{case} = 150$ ℃.

In Fig. 3.13(a) the progressive degradation of the device is noticed by a progressive reduction of the drain-source saturation current. In regards to the leakage current, it behaves similarly to the previous tests, and its initial point is approximately the nominal current.

In the gate-source voltage (V_{GS}), Fig. 3.13(b) the progressive degradation of the gate oxide is noticeable. With a pulse of 3 μs, before the degradation of the device, the gate drops $\Delta V_{GS} = 0.2$ V at turn off. But afterwards, for longer pulses, the whole gate drops, from rise to fall. Progressively, V_{GS} decreases up to approximately $V_{GS} = 16$ V. Additionally, during off state, a variation of the gate-source voltage level can be observed. This is a clear indication that current is flowing through the gate oxide pad during on and off states. This breakdown mode was not observed in the state of the art.

Similarly to S1, S2 shown in Fig. 3.14, also suffers an explosion leaving the chip visible. The three pads are also short-circuited.

Fig. 3.14: State of S2 after breakdown.

3.2.8 Short Circuit Energy analysis

The energy dissipated during the short-circuit may assist in understanding the short-circuit behaviour and its limit. In this case, the short-circuit energy density is analysed. The die are is given in [36], the approximate active area is $A_{Die} \approx 0{,}0788\ cm^2$.

S1 short-circuit energy analysis

As shown in Fig. 3.11, the destruction of S1 occurs just after turn off, at $T_{case} = 25$ ℃, with $V_{DS} = 600$ V and with a pulse of 5 μs and at that point $\Delta V_{GS} = 0.72$ V. In Fig. 3.15 the short-circuit energy of the tests at $V_{DS} = 400$ and 600 V is shown.

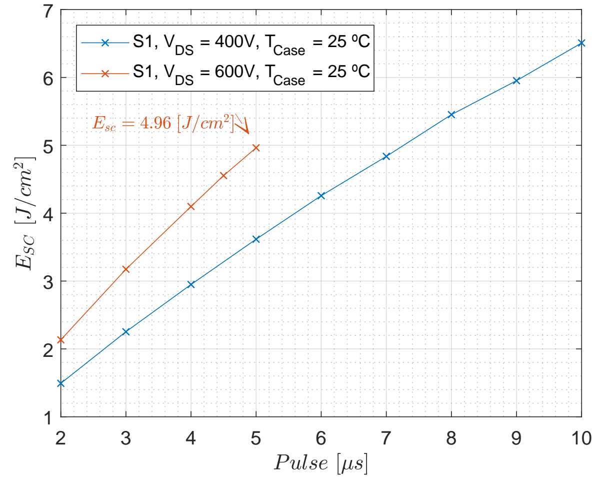


Fig. 3.15: S1 short-circuit energy with increasing short-circuit pulse length.

As it would be expected, in Fig. 3.15, with increasing short-circuit pulse and DC-link voltage, the short-circuit energy increases. It can be seen that at the breakdown instant, the short-circuit energy is $E_{SC} = 4.96\ J/cm^2$, much lower than that calculated in the state of the art. It should be observed, that the maximum short-circuit energy which is reached at $V_{DS} = 400$ V and pulse length of 10 μs, is

a 25 % higher than when the device fails at 600 V and 5 μs.

S2 short-circuit energy analysis

The breakdown of the second 1.2 kV/ 36A SiC MOSFET, S2, occurs at T_{case} = 150 ℃. A gradual reduction of the gate voltage for the DC-link voltage of 600 V after the 3 μs short-circuit pulse, was shown in Fig. 3.13. In Fig. 3.16 the short-circuit energy for T_{case} = 150 ℃ and test voltages of V_{DS} = 400 and 600 V is shown. Connected by lines are those pulses in which gate degradation was not observed.

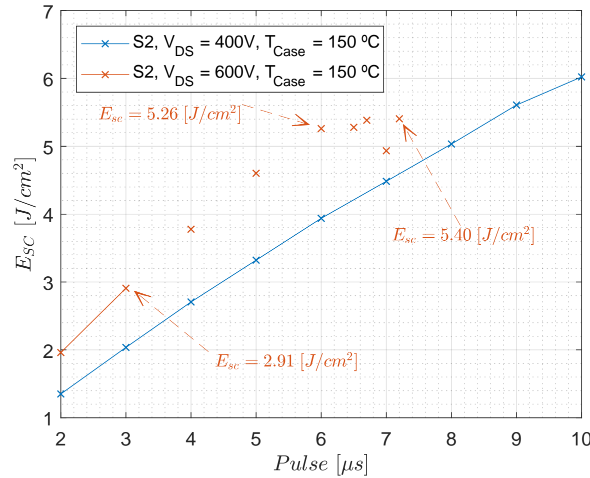


Fig. 3.16: Calculated short-circuit energy for S2 at increasing short-circuit time.

In Fig. 3.16 as in Fig. 3.15, except after the 6 μs pulse, when the gate is heavily degraded, the short-circuit energy is both proportional to the pulse length and voltage. In Fig. 3.13(b) it could be observed that the degradation happens after the pulse of 3 μs. That point corresponds to a short-circuit energy E_{SC} = 2.91 J/cm^s, half the maximum energy at V_{DS} = 400 V. After the 6 μs pulse the short-circuit energy oscillates around 5.25 J/cm^2.

3.2.9 Junction Temperature analysis

Depending on the case temperature, two different failure mechanisms were observed. On one hand, S1 failed suddenly at for a case temperature of T_{case} = 25 ℃. By contrast, S2 at a temperature of T_{case} = 150 ℃ presented progressive gate degradation before failure. Fig. 3.15 and 3.16 show that S2 fails at a much lower E_{sc} than S1. Having that the case temperature differs, it may be interesting to get an idea of the junction temperature at which failure occurs.

Maerz et al. [30] present a method to simulate the junction temperature. As explained in Section 1.3.4, it consist in slicing the semiconductor in layers so as to solve its internal Cauer network. It is assumed that the first layer depicts the junction temperature. The thermal capacitances and resistances associated with each layer are provided by CREE in the Spice simulation model [37].

S1 thermal analysis at breakdown

In Fig. 3.17 the temperature evolution of the first four layers nearest to the junction of S1 is shown. The test voltage is $V_{DS} = 600$ V, the pulse length is 5 μs and the case temperature is $T_{case} = 25$ ℃.

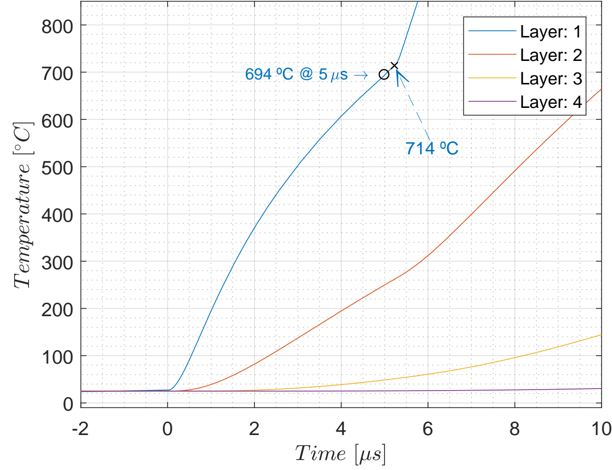


Fig. 3.17: S1 estimated temperatures for the breakdown pulse, $V_{DS} = 600$ V, pulse length 5 μs and $T_{case} = 25$ ℃.

In Fig. 3.17 it can be observed that the main temperature increment occurs in the first two terms of the Cauer network, this is in agreement with [14]. It is interesting to note that at the turn off instant, $Time = 5$ μs, the first layer temperature is $T_{Layer1} = 694$ ℃. But at breakdown $Time = 5.22$ μs, because energy is still being dissipated, its temperature has risen to $T_{Layer1} = 714$ ℃. The simulated junction is in the order of magnitude of the results in [30]. However, this value is much lower than the results obtained by FEM analysis in [14, 16].

S2 thermal analysis at degradation

S2 shows progressive degradation at $T_{case} = 150$ ℃. In Fig. 3.18 the temperature behaviour for the first four layers at the 3 μs pulse of is shown. This is the pulse length after which gate degradation appears.

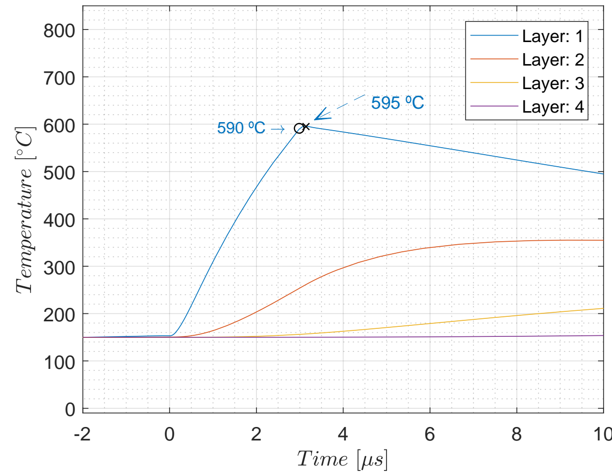


Fig. 3.18: S2 estimated temperatures for a DC-link voltage of $V_{DS} = 600$ V, pulse length 3 μs and $T_{case} = 150$ ℃.

In Fig. 3.18, the simulation of the temperature increment shows a maximum temperature 595 ℃. When comparing Fig. 3.18 against Fig. 3.17 it is interesting to observe that even if the case temperature of the second device (S2) is higher than S1, its junction temperature for the pulse which generates degradation is lower.

3.3 Conclusion

The static characterization and dynamic testing of 1.2 kV/ 36 A SiC MOSFETS has been performed. On one hand, for the static characterization, the gate-source threshold voltage ($V_{GS\ Th}$) and drain-source leakage current (I_{DSS}) tests have been carried out. With the purpose of relating the leakage current to the short-circuit behaviour, the devices with highest and lowest leakage current were chosen. These devices were able to withstand short-circuit pulses of up to 10 μs at DC-link voltage of $V_{DS} = 400$ V for a temperature range of $T_{case} = 25$ to 150 ℃. At a DC-link of $V_{DS} = 600$ V breakdown of the tested devices was experience for short-circuit pulses of under 10 μs.

During short-circuit test, a very high drain-source leakage current, in the order of the nominal current, was observed after turn off. Due to this high leakage current value, it is found difficult to perform a correlation between the short-circuit waveform and the static measurement of the drain-source leakage current.

Two different breakdown modes have been experienced at the DC-link voltage of $V_{DS} = 600$ V. On one hand, at $T_{case} = 25$ ℃ the breakdown occurs suddenly for a pulse length of 5 μs and delayed 1.22 μs after turn off. In this case, the gate voltage reduction at turn off is $\Delta V_{GS} = 0.72$ V, the short-circuit energy is $E_{sc} = 3.75\ mJ/m^2$ and the simulated junction temperature is 714 ℃. On the other hand, a second breakdown mode is experienced at $T_{case} = 150$ ℃. In this second mode, a progressive and permanent reduction of the whole gate-source voltage pulse was measured before breakdown. The pulse before degradation is 3 μs long, for this case, the gate has dropped $\Delta V_{GS} = 0.2$ V. The short-circuit energy is $E_{sc} = 2.91\ J/cm^2$ and the estimated junction temperature is $T_j = 594$ ℃.

Chapter 4

1.2 kV/ 90 A SiC MOSFET

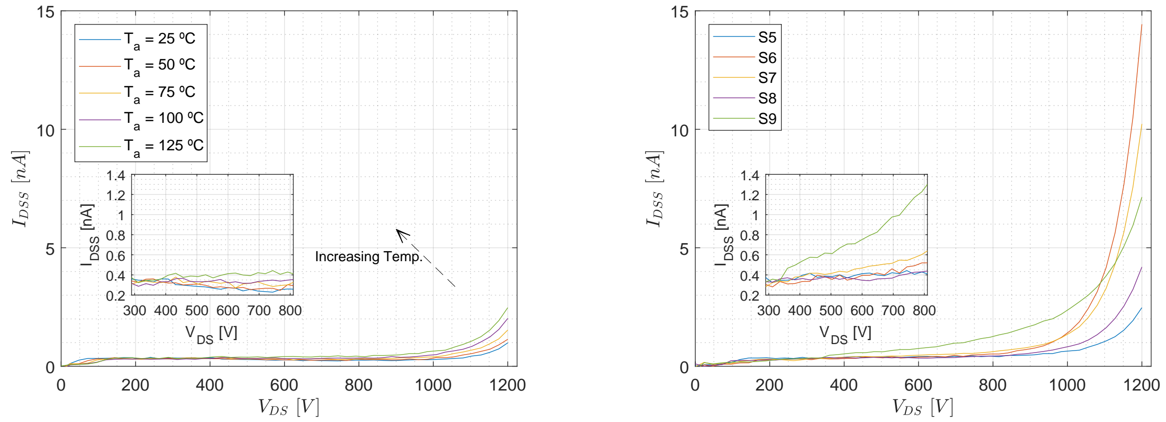
In this chapter the results of the higher rated SiC MOSFET model rated 1.2 kV/ 90 A SiC MOSFETs, C2M0025120D, from CREE is presented. Five devices are examined, named S5 - 9. Static testing of the devices was performed, of which two where selected to perform short-circuit testing.

4.1 Static characterization

In the static characterization, the drain-source leakage current (I_{DSS}), gate-source threshold voltage ($V_{GS\,Th}$), gate-source leakage current (I_{GSS}) and transfer characteristics ($V_{GS} - I_{DS}$) have been determined. For this purpose the B1506A curve tracer and Opt F10 fixture from Keysight is used. The test conditions and setup are presented in Appendix A. The range of tested temperatures is from T_a = 25 up to 125 ℃, where T_a is the ambient temperature which is assumed to be equal to the junction temperature.

4.1.1 drain-source leakage current (I_{DSS})

For the testing of I_{DSS} the gate-source voltage is set to 0 V. In Fig. 4.1(a) the drain source leakage current of S5 as a function of the temperature is shown. In Fig. 4.1(b) a comparison of the 5 devices at T_a = 125 ℃ is presented.



(a) Drain-source leakage current as a function of temperature for the 1.2 kV/ 90A SiC MOSFET (S5).

(b) Comparison of drain-source leakage current for different devices with T_a = 125 ℃.

Fig. 4.1: Static test results: drain-source leakage current.

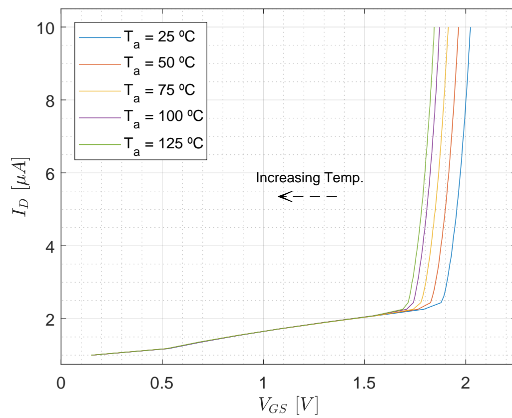
The results shown in Fig. 4.1(a) demonstrate that the leakage current increments with temperature and voltage. In the case of S5, this happens when V_{DS} is over 1000 V, however in the voltage region

of interest (300 to 800 V) a mild increment of leakage current can be observed.

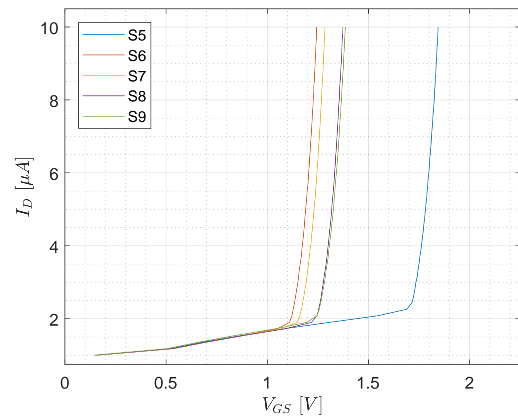
In Fig. 4.1(b) a comparison of the devices at T_a = 125 ℃ is presented. In the region of interest, it can be observed that S9 is the device showing the highest leakage current of the set. On the other hand, when reaching the device breakdown voltage, in this case V_{DS} = 1.2 kV S6 becomes the leakiest. Therefore, it is not possible to clearly state which is the least leaky device in the region of interest. But since S5 is the least leaky at 1.2 kV, it has been considered as the least leaky of the set.

4.1.2 Gate-source threshold voltage ($V_{GS\,Th}$)

Fig. 4.2(a) presents the threshold voltage variation corresponding with S5 as a function of the temperature, and (b) shows the characteristics of the five devices at 125 ℃.



(a) S5, threshold variation with temperature.



(b) Comparison of the threshold voltage at T_a = 125 ℃.

Fig. 4.2: Static testing results: gate-source threshold voltage.

Similarly, to the 36 A devices, Fig. 4.2(a) shows that the threshold voltage of S5 decreases with temperature. As can be observed in Fig. 4.2(b) a significant difference in threshold voltage exist between the five devices, presenting S5 the highest threshold voltage and S6 the lowest. In Fig. 4.3 all threshold voltages as a function of temperature are included into one figure.

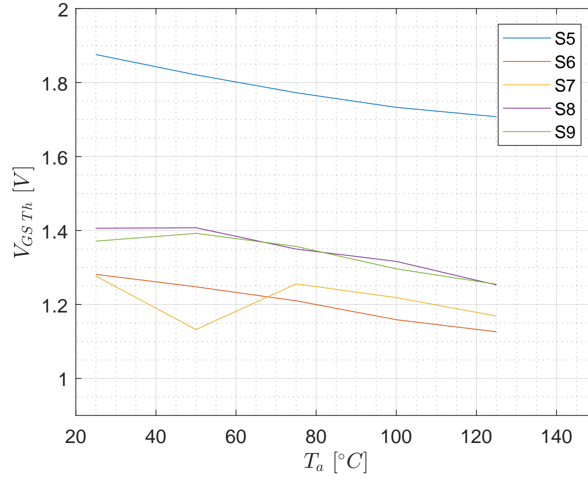
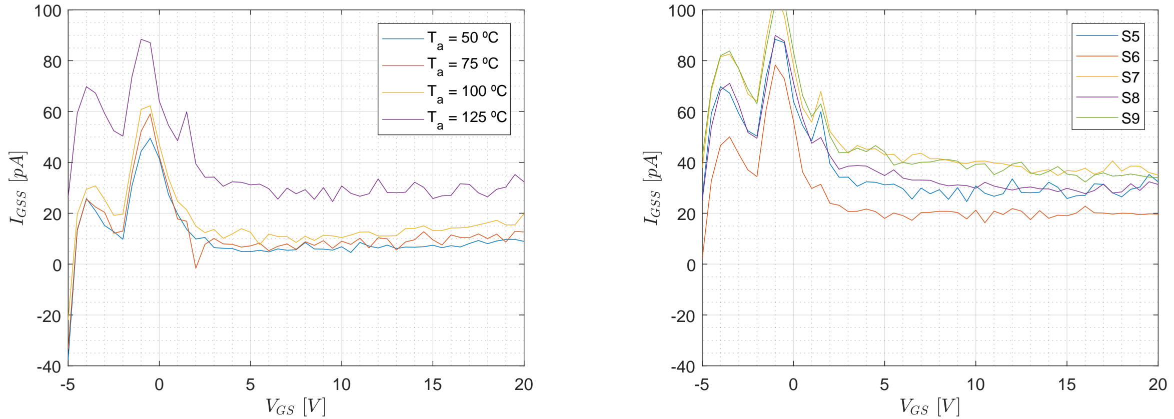


Fig. 4.3: S5 - 9 threshold voltage variation with increasing temperature.

The results depicted in Fig. 4.3 show two significant threshold voltage ranges. On one hand S5 with a threshold range from 1.85 to 1.7 V, which is 1.5 times higher than S6. On the other hand, S6 - 9, in which for example, S9 ranges from 1.35 to 1.25 V

4.1.3 Gate-source leakage current (I_{GSS})

The gate leakage current plays also an important role in the short-circuit reliability. In order to determine I_{GSS} only as a function of the gate voltage, V_{DS} is kept to 0V. In Fig. 4.4(a) the gate leakage of S5 for $T_{air\ flow}$ = 50 - 125 °C is shown. In (b) the comparison of the 5 devices at 125 °C is shown.



(a) S5, gate-source leakage current increase with temperature.

(b) Comparison of the gate-source leakage current at T_{case} = 125 °C.

Fig. 4.4: Static testing gate-source leakage current measurement.

In the DUT's datasheet one can find that the maximum I_{GSS} is 600 nA with T_{case} = 25 °C, V_{GS} = 20

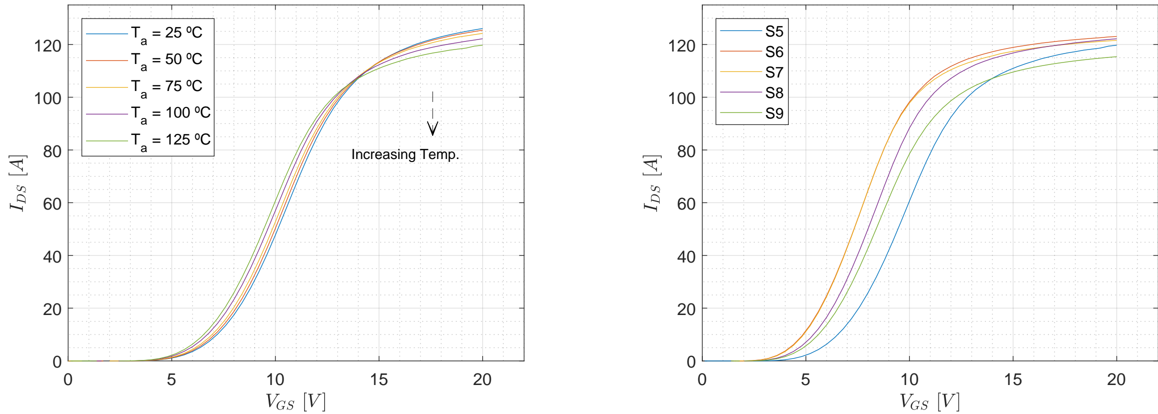
V and V_{DS} = 0 V. The results in Fig. 4.4 shown that even at the highest temperature, the maximum gate-source leakage current does not exceed the value specified in the datasheet.

Two interesting phenomena can be observed in Fig. 4.4(a). In the V_{GS} = 5 - 20 V range, the gate leakage current does not increase with higher applied voltage. A peak is observed at V_{GS} = 0 V in all devices. The second observation to is that the leakage current remarkably increases when the DUT is tested at a temperature of 125 ℃.

In Fig. 4.4(b) a comparison of I_{GSS} among the five devices (S5 - S9). At V_{GS} = 20 V, S6 is the device with the lowest leakage current, it has a 40 % lower gate source leakage current than its counterparts.

4.1.4 Transfer characteristics ($V_{GS} - I_{DS}$)

The transfer characteristics give an insight of the behaviour of the MOSFET during short-circuit. It has been obtained for V_{DS} = 20 V. In Fig. 4.5(a), the transfer characteristics of S5 as a function of the temperature are shown and in (b) the behaviour of the devices at 125 ℃.



(a) Transfer characteristics of S5 as a function of the temperature.

(b) Transfer characteristics comparison for the different devices at T_a = 125 ℃.

Fig. 4.5: Result of static test: transfer characteristics.

The results in Fig. 4.5(a) show the two typical regions which can be found in any semiconductor device. On one hand, a Negative Temperature Coefficient (NTC, resistance is inversely proportional to temperature) behaviour from V_{GS} = 5 - 13 V is observed. This implies that with increasing temperature, the current increases and with it the losses, a positive feedback leading to destruction of the device. On the other hand, from V_{GS} = 15 - 20 V the device presents a Positive Temperature Coefficient (PTC, resistance is proportional to temperature) behaviour. Therefore, at V_{GS} = 20 V, the internal heat generation will provoke a decrease of the saturation current due to the degradation of the electron mobility. This is in accordance with the current behaviour observed in the state of the art, where it is shown that the saturation current decreased with temperature.

Fig. 4.5(b) shows a comparison of the test devices at constant temperature. As it can be observed, S9 presents the lowest forward current at V_{GS} = 20 V and V_{DS} = 20 V.

4.2 Dynamic testing

With the purpose of studying the influence of the drain-source leakage current on the short-circuit behaviour, the dynamic testing of S5 and S9 has been performed. These devices are the ones with, respectively, the lowest and highest drain-source leakage current(I_{DSS}). Similarly to the 36 A devices, the testing has been performed for different short-circuit pulse lengths, drain-source voltages and case temperatures. The gate drive characteristics which are shown in Table. 4.1 are in accordance with the datasheet.

Variable	Value	Comment
V_{GS}	$+20/-5$ V	Recommended.
R_G	10 Ω	Reduce turn-off overshoot.

Table 4.1: Gate drive characteristics.

4.2.1 Test Procedure

The procedure followed for the testing is described in Diagram 4.6. As can be observed, the maximum tested voltage is 600 V. At this voltage level, the standard 10 μs short-circuit could not be reached.

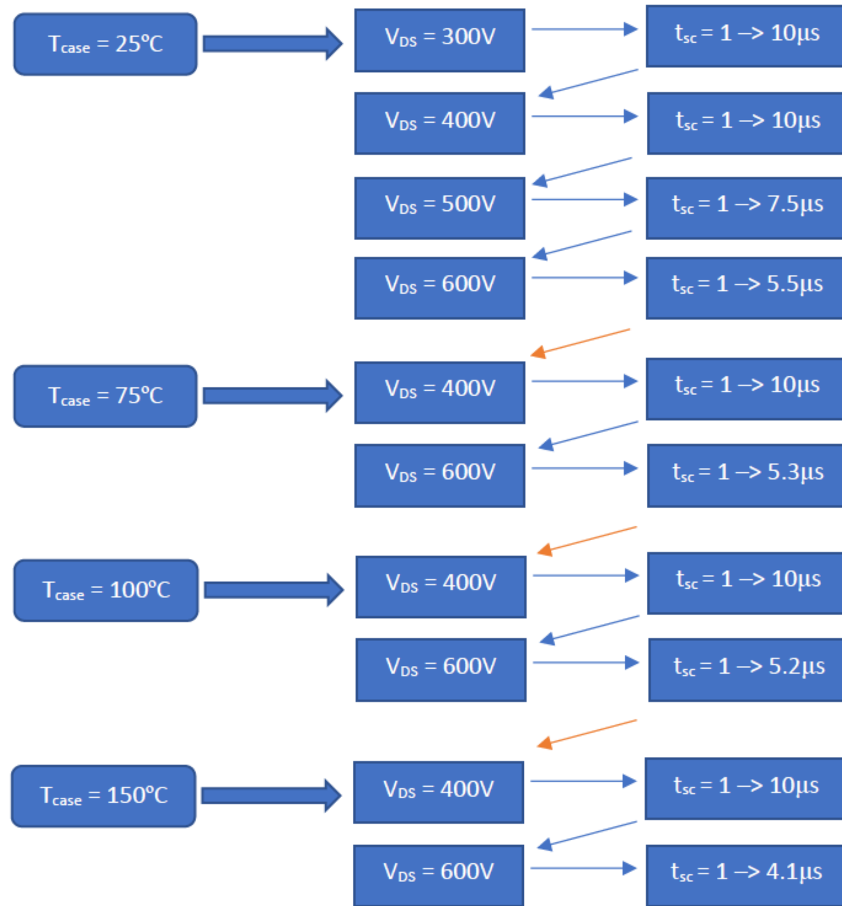


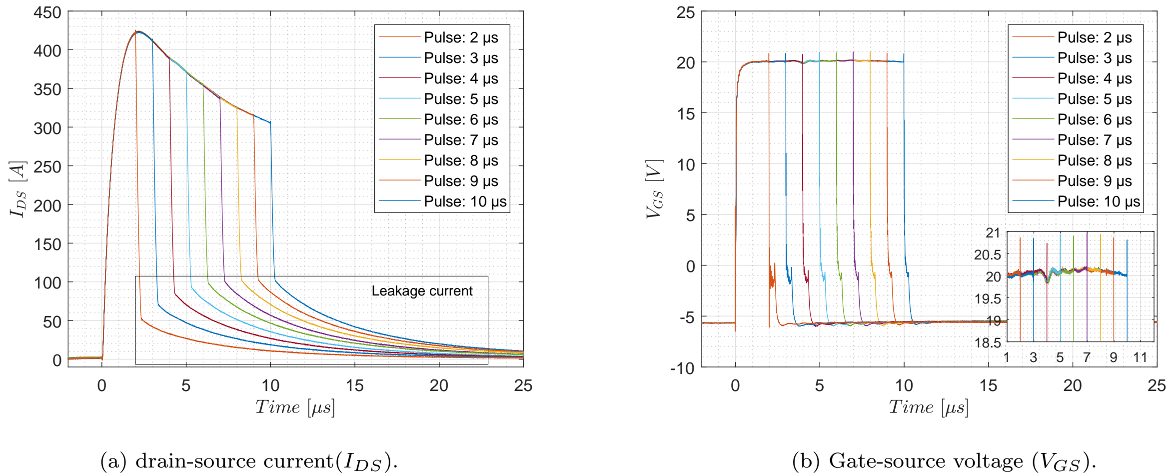
Fig. 4.6: Procedure followed during the short-circuit testing of the 1.2 kV/ 90 A devices (S5 and S9). t_{sc} stands for the pulse length-

As it can be observed, this testing procedure consist on gradually applying harsher test conditions to the DUT. One can argue that this repetitive short-circuit activity could lead to failures due to accumulated damage. But in order to compare different devices, this procedure was considered valid.

It should be mentioned that because enough time was waited, the initial junction temperature is assumed to be equal to the case temperature T_{case}.

4.2.2 Short-circuit time dependence

The maximum short-circuit withstand time is an essential characteristic that needs to be assessed. In Fig. 4.7 the behaviour of S5 at 400 V and T_{case} = 25 ℃ is shown, while the short-circuit time is incremented gradually.



(a) drain-source current(I_{DS}).

(b) Gate-source voltage (V_{GS}).

Fig. 4.7: Short circuit waveforms of the 1.2 kV/ 90 A SiC MOSFET, DUT: S5, V_{DS} = 400 V and T_{case} = 25 °C.

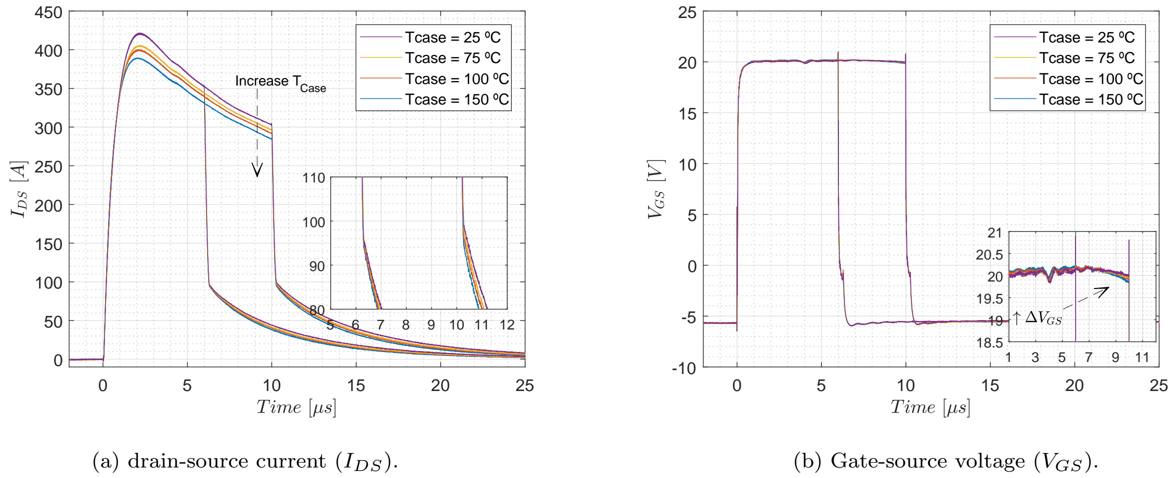
As can be seen in Fig. 4.7(a) The short-circuit saturation current of the 1.2 kV/ 90 A SiC MOSFET is 425 A, 4.7 times its nominal value. Due to the heating of the device and reduction of the electron mobility, the short-circuit current decreases at a rate of $-15\ A/\mu s$.

It is also very interesting to observe the large measured drain-source leakage current at turn off, which increases with short-circuit pulse length. Its maximum value appears to be stabilized at 100 A, approximately the rated current, for pulses of at least 7 μs.

On the other hand, when observing the gate one should note 2 phenomena. First, oscillations of the gate around its on state value can be observed. Specially at 4 μs when the signal suddenly decreases 0.75 V, to continue a damped oscillation. Secondly, it should be pointed out a slight and progressive gate source reduction towards the end of long pulses.

4.2.3 Case temperature dependence

To investigate the behaviour of these devices at a harsher environment such as high case temperature, testing at T_{case} = 25, 75, 100 and 150 °C has been performed.



(a) drain-source current (I_{DS}).

(b) Gate-source voltage (V_{GS}).

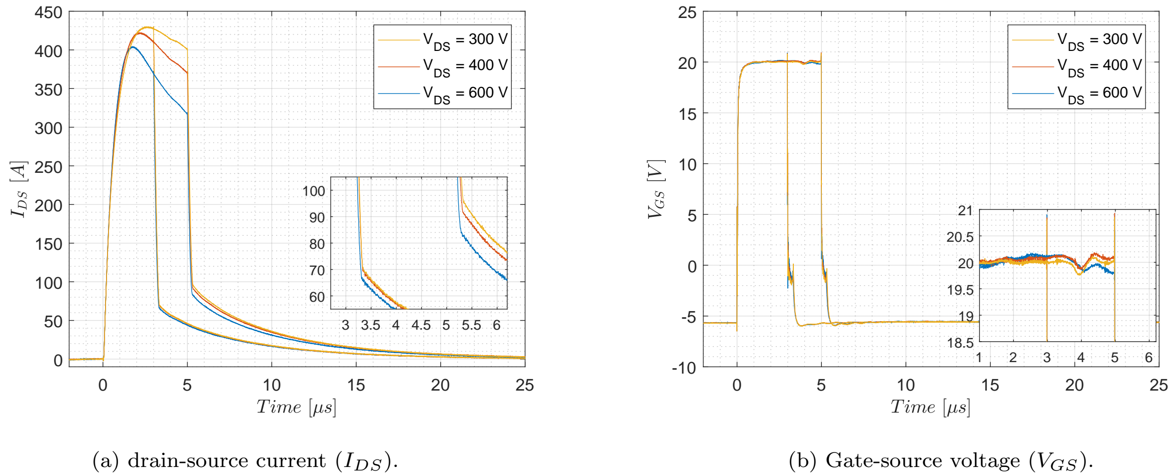
Fig. 4.8: Case temperature dependency of DUT S5 at V_{DS} = 400 V for the short-circuit pulses of 6 and 10 μs

As it would be expected, in Fig.4.8(a), increasing case temperature decreases the mobility of the electrons reducing the saturation current. Interestingly, this is also observed for the tail current, where for higher case temperature the leakage current is lower.

On the other hand, it can be observed in (b), that for pulses with a length over 7 μs, a higher case temperature has an impact on V_{GS}.

4.2.4 DC-link voltage dependence

Typically, the nominal voltage of these devices is 80% of its rated value. In Fig. 4.9, S5 is analysed at T_{case} = 25 ℃ and pulses of 2 and 5 μs for V_{DS} = 300, 400 and 600 V.



(a) drain-source current (I_{DS}).

(b) Gate-source voltage (V_{GS}).

Fig. 4.9: DC-Link voltage dependency of S5 at T_{case} = 25 ℃ for short-circuit pulses of 6 and 10 μs.

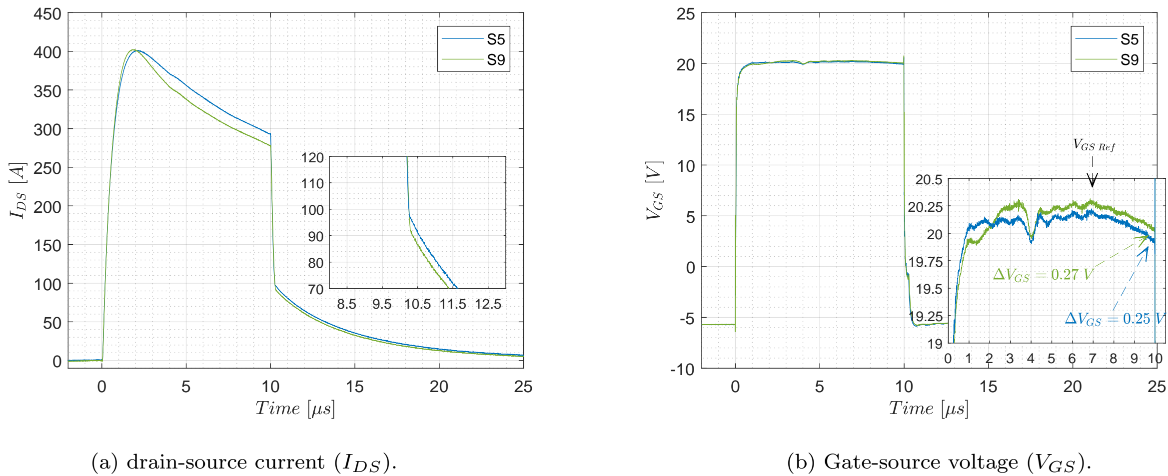
In Fig. 4.9(a), the behaviour of the drain-source current with increasing DC-link voltage is shown. It is possible to observe that higher voltage, leads to lower saturation current. Increasing V_{DS} leads to higher dissipated energy and therefore, the electron mobility is reduced. This has an impact reducing the saturation current. Additionally, the rate at which the saturation current decreases is higher.

In the zoom in Fig. 4.9(a), one should observe that with higher DC-link voltage, the initial saturation current decreases. Additionally, its tail current is also lower at V_{DS} = 600 V than at 300 V. This phenomena is also experienced in S9, the other tested device. However, it contrasts with the results of static characterization shown in Fig. 4.1, where higher V_{DS} implied higher saturation current.

Concerning the gate-source voltage, a significant ΔV_{GS} is noticeable for V_{DS} = 600 V. At 4 μs and V_{DS} = 600 V the gate voltage is V_{GS} = 19.8 V, on the other hand, at 400 V the gate voltage is V_{GS} = 20.1 V.

4.2.5 Device comparison

The comparison of the two tested 1.2 kV/ 90 A MOSFETs, S5 and 9 devices, at the same test conditions is shown in Fig. 4.10. The test conditions are T_{case} = 100 °C, V_{DS} = 400 V and t_{sc} = 10 μs. In (a) I_{DS} is shown and in (b) the gate-source voltage is presented.



(a) drain-source current (I_{DS}).

(b) Gate-source voltage (V_{GS}).

Fig. 4.10: Device S5 and 9 comparison with T_{case} = 100 °C V_{DS} = 400 V and t_{sc} = 10 μs.

The comparison of the devices at the same conditions shows differences between S5 and 9. When analysing the current behaviour, Fig. 4.10(a), it can be appreciated differences in the magnitude of the peak and time at which it is reached. For S5, $I_{DS\ Peak}$ = 400 A and $t_{sc\ Peak}$ = 2.1 μs. By contrast, for S9, $V_{DS\ Peak}$ = 402 A and $t_{sc\ Peak}$ = 1.8 μs. The second feature is the slope at which I_{DS} decreases. On one hand S5, presents a slope of $(\Delta I_{DS})/(\Delta t_{sc}) = -15.1 A/\mu s$ and S9 has a slope of $(\Delta I_{DS})/(\Delta t_{sc}) = -18.3 A/\mu s$.

By contrast with the static drain-source leakage current measurement (Fig. 4.1(b)), in Fig. 4.10(a) a higher leakage current is observed for S5 than for S9.

In Fig. 4.10(b), it can be observed that S9 exhibits a higher on-voltage than S5, but when it comes to

ΔV_{GS} drop, both devices behave similarly.

4.2.6 Gate-source drop

The drop in the gate towards the end of long short-circuit pulses is a parameter of concern for the device ruggedness. It indicates that current flows through the gate, which is supposed to be an insulator. In Fig. 4.11, the observed ΔV_{GS} for S5 and S9 is shown. For V_{DS} = 400 V, ΔV_{GS} is taken at 10 μs, it should be mentioned that for S9, at T_{case} = 150 ℃ de device was degraded, so, that data point was discarded. At V_{DS} = 600 V, ΔV_{GS} is taken at 5 μs, for S5 data is available for T_{case} = 25, 75 and 100 ℃. For S9 the available data is for T_{case} = 25 and 75 ℃.

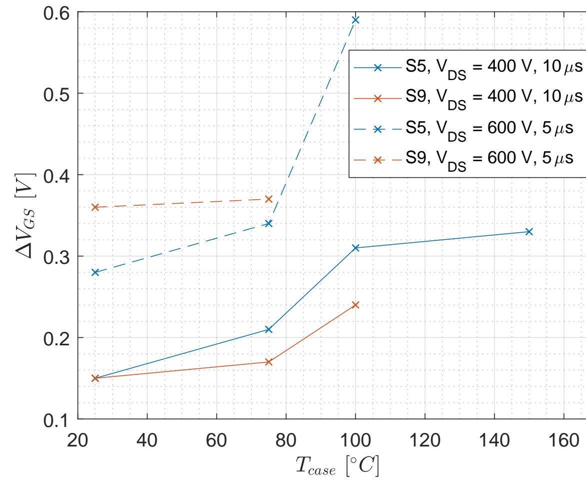


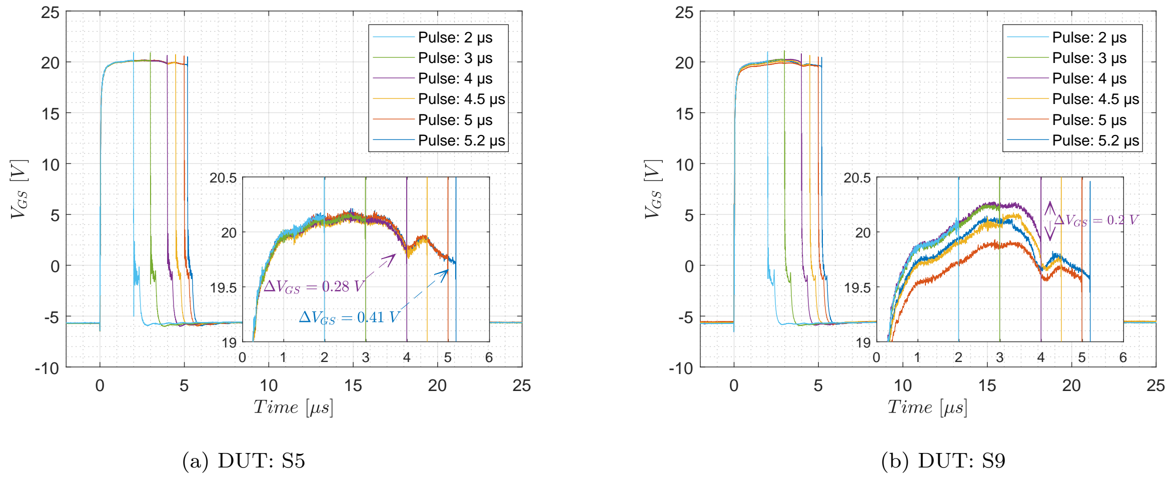
Fig. 4.11: Gate voltage drop (ΔV_{GS}) for S5 and S9 for the drain-source voltage of 400 and 600 V, data taken at 10 μs and 5 μs respectively.

The results in Fig. 4.11 show two opposite behaviour of ΔV_{GS}. On one hand, for V_{DS} = 400 V, S5 presents a higher voltage drop than S9. By contrast, at 600 V it is S9 which shows a higher ΔV_{GS}. However, in both cases, ΔV_{GS} is both proportional to the case temperature and applied voltage.

4.2.7 Degradation at T_{case} = 100 ℃

Before observing the results of the degradation it should be stressed that the test procedure for S5 and S9 has been identical.

In Fig. 4.12 the gate behaviour of S5 (a) and S9 (b) at T_{case} = 100 ℃ and V_{DS} = 600 V is shown.



(a) DUT: S5

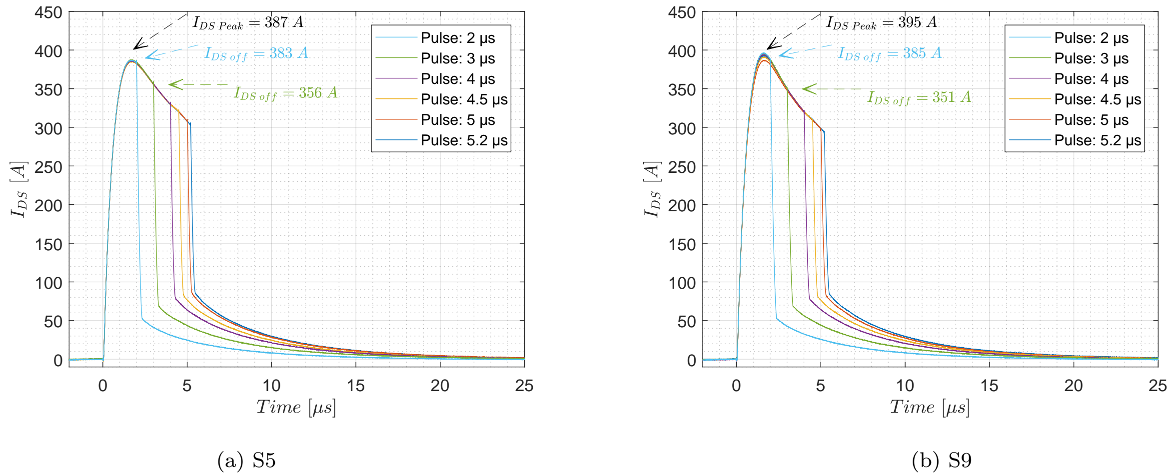
(b) DUT: S9

Fig. 4.12: Gate voltage measurement, V_{DS} = 600 V and T_{case} = 100 ℃.

In Fig. 4.12(a), the gate-source waveform of device S5 is shown with increasing short-circuit pulse. As discussed earlier, the gate voltage drop is more evidenced as soon as the short-circuit pulse is increased. In particular, the S5 device exhibits a voltage drop of 0.28 V at 4 μs and a voltage drop of 0.41V at 5.2 μs.

The gate-source voltage waveform of S9 with increasing pulse length is shown in (b). Its behaviour is similar to S5 for pulses of up to 4 μs. However, with a pulse of 4.5 μs, the measured gate voltage drops throughout the whole pulse. With increasing short-circuit time, the whole gate voltage pulse decreases gradually. This result indicates permanent gate oxide degradation.

The comparison of the behaviour of S5 and S9 drain-source current at the same conditions is presented in Fig. 4.13.



(a) S5

(b) S9

Fig. 4.13: I_{DS} measurement, V_{DS} = 600 V and T_{case} = 100 ℃

At first sight, the drain-source current of both S5 and S9 behave very similarly. The peak of S5 is a 3 % higher than S9. In accordance, as can be observed the rate at which current decreases is slightly

higher. But it can be observed in Fig. 4.13(b) that for the 5 μs the saturation current reaches a slightly lower peak. This is probably due to the drop of the gate voltage due to degradation

4.2.8 Degraded S9, static characterization

Further tests were carried out up to T_{case} = 150 °C, V_{DS} = 600 V and 4 μs. Following the trend of the results shown in Fig. 4.12 and 4.13, S5 did not show gate degradation. On the other hand, as could be observed in Fig. 4.12(b), S9 gate level continued permanently decreasing up to V_{GS} = 19 V before testing was stopped.

Having observed that S9 suffered degradation but not complete destruction, in order to observe if and how its electrical characteristics had varied, its static characterization was performed.

Gate-Source

The constant decrease of the gate-source voltage indicated a current flows through that path. Measurement with multimeter showed a R_{GS} = 105,8 Ω at room temperature.

Gate-Drain

In contrast with the gate-source measurement, when the gate-drain resistance is measured with a multimeter it displays *OL*, open loop, this indicates the insulation between these pins is not degraded.

Drain-Source

The measurement of the drain-source resistance displayed *OL*, open loop. However, it is possible to determine the behaviour of the drain-source leakage (I_{DSS}) current with the device analyser. In Fig. 4.14, I_{DSS} is measured at the ambient temperature range from 25 to 125 °C with V_{GS} = 0 V.

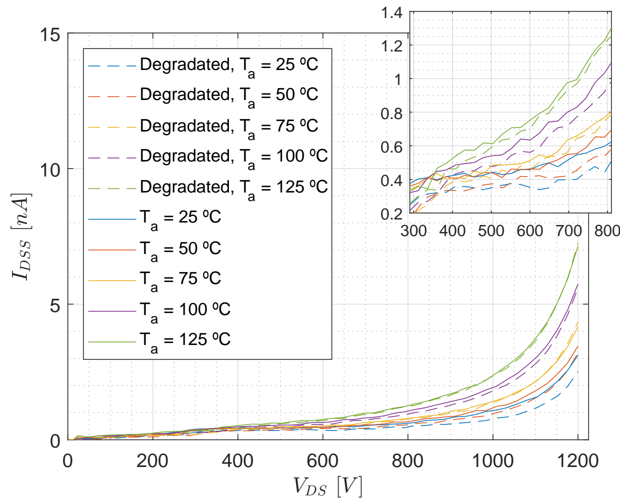


Fig. 4.14: drain-source leakage comparison of S9 with V_{GS} = 0 V.

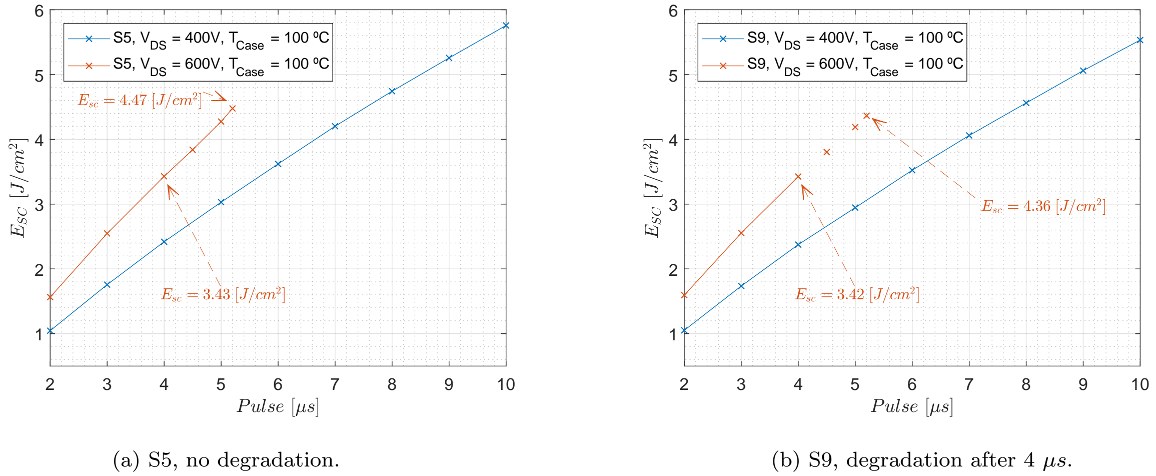
Analysing in detail it can be observed that the measured leakage current of the degraded device is very similar to a new device. However, at $T_{air\ flow}$ = 25 and 50 °C, the degraded device presents a slightly

lower leakage current.

4.2.9 Short-Circuit Energy analysis

Clear differences were observed in Fig. 4.12 and Fig. 4.13 between the 1.2 kV/ 90 A S5 and 9 devices. Understanding the energy dissipated by each of the devices may give additional information to evaluate the differences between them. To calculate the short-circuit energy density, the die area is approximately 0,23 cm^2 [38].

In Fig. 4.15 the comparison of E_{sc} at T_{case} = 100 ℃, temperature at which the initial degradation was observed, is shown. In (a) S5 is presented, and in (b) S9.



(a) S5, no degradation.

(b) S9, degradation after 4 μs.

Fig. 4.15: Calculated short-circuit energy (E_{sc}), for V_{DS} = 400 and 600 V, T_{case} = 100 ℃.

At V_{DS} = 400 V, the energy dissipated by S5 (a) at all short circuit times is slightly higher than S9, for example, at 10 μs it is a 4 % higher. Observe that at 600 V and 4 μs, instant at which the initial degradation takes place, both devices dissipate the same energy.

4.2.10 Junction Temperature analysis

In the introduction it was commented that to simulate the temperature inside the device, the semiconductor could be sliced in several layers. As explained in the introduction, Section 1.3.4, each single layer features a thermal resistance and capacitance. Therefore by solving the corresponding Cauer thermal network it is possible to estimate their temperatures. CREE provides a spice model with a thermal network of 14 layers for their C2M0025120D discrete MOSFET [37]. In Fig. 4.16 the simulation of the temperature evolution for the first 5 layers of S5 for V_{DS} = 600 V, T_{case} = 100 ℃ and a 4 μs pulse can be observed.

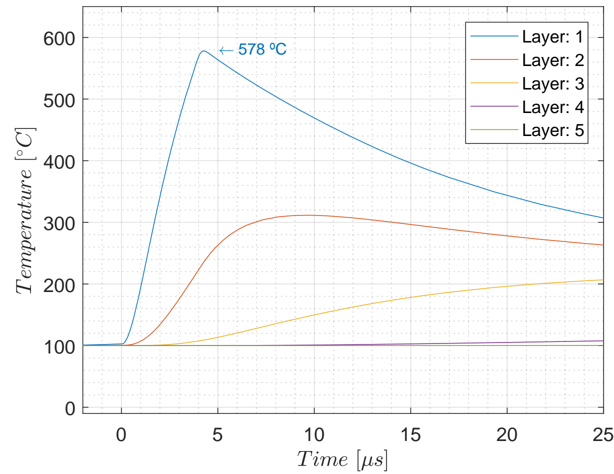


Fig. 4.16: Simulation of layer temperatures of S5, for V_{DS} = 600 V, T_{case} = 100 ℃ and a 4 μs pulse.

As can be observed in Fig. 4.16, a significant temperature increment is only simulated for the first three layers. This is in agreement with the results shown by Wang et al. [14]. The maximum temperature is $T_{Layer:1}$ = 578 ℃. It should mentioned that the results obtained by this method may not be completely accurate, but for comparison purposes are considered acceptable.

In Fig. 4.17 a comparison of the temperature behaviour of the first layer of S5 and 9 for two DC-link voltages is shown. It is assumed that the first layer is shows the junction temperature. The test conditions are: case temperature T_{case} = 100 ℃, for V_{DS} = 400 V a pulse of 10 μs and for V_{DS} = 600 V a 4 μs pulse.

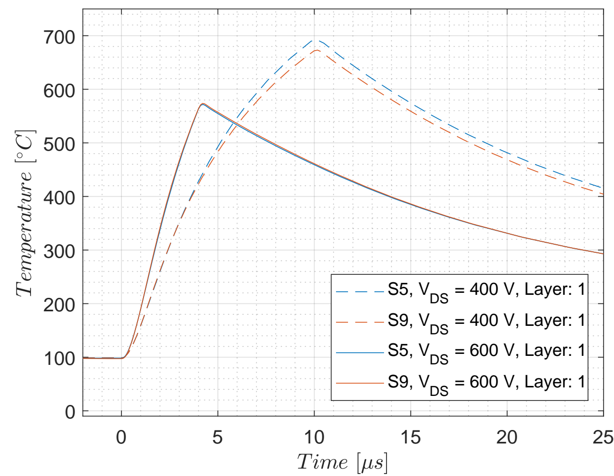


Fig. 4.17: First layer temperature evolution for S5 and S9 at a case temperature T_{case} = 100 ℃; for V_{DS} = 400 V a pulse of 10 μs and for V_{DS} = 600 V a 4 μs pulse.

The simulation of the junction temperature shows that the slope of temperature increment for V_{DS} = 600 V is higher than at 400 V. On the other hand, in agreement with Fig. 4.15 a higher temperature is reached at 400 V than at 600 V. At 400 V, S5 reaches a temperature 25 ℃ higher than S9. By contrast, at 600 V, both devices follow similar heating trajectories.

4.3 Conclusion

The static characterization and short-circuit testing of 1.2 kV/ 90 A SiC MOSFETS from CREE was performed. In the static characterization, the devices were tested for drain-source leakage current (I_{DSS}), gate-source threshold voltage ($V_{GS\ threshold}$), gate-source leakage current (I_{GSS}) and transfer characteristics ($V_{GS} - I_{DS}$). From these devices, those whose drain-source leakage current (I_{DSS}) was the highest and lowest were chosen for short-circuit testing.

When performing the short-circuit testing, the 1.2 kV/ 90 A devices could withstand at V_{DS} = 400 V short-circuit pulses of 10 μs at case temperatures ranging from 25 to 150 ℃. It should be commented that after turn off, a very high leakage current tail was measured. At its initial instant, it was of about the rated current. On the other hand, at a DC-link voltage of 600 V it is not possible to reach 10 μs short-circuits, pulses were kept under 5.5 μs. In this study permanent degradation was observed for the device with higher statically measured leakage current.

The purpose of selecting the devices S5 and S9 for short-circuit testing was to lay the ground for a correlation between the leakage current and short-circuit behaviour. It was observed that the high leakage current was inversely proportional to V_{DS} and T_{case}. This contrasts with the results of static testing were I_{DSS} showed a proportional behaviour to temperature and voltage. This rises doubts on the feasibility of a correlation between the statically measured I_{DSS} and short-circuit behaviour. However, it should be commented that the device with lower leakage current did not degrade.

It is interesting to note that at T_{case} = 100 ℃ a higher short-circuit energy is reached at V_{DS} = 400 V and 10 μs than at V_{DS} = 600 V and 4 μs (Fig. 4.15). Note that for one of the devices degradation is observed at V_{DS} = 600 V and 4 μs.

Finally, a simulation of the temperature behaviour at the the junction is performed. On one hand it shows that a higher temperature is reached at V_{DS} = 400 V and 10 μs than at V_{DS} = 600 V and 4 μs. However, the rate of temperature increment is higher in the later case.

Chapter 5

General conclusion and future work

In this last section, a general conclusion that comprehends the results observed for the 1.2 kV 36 A and 90 A SiC MOSFETs is given. Additionally, the future work which may follow this report is presented.

5.1 General conclusion

In this study two different SiC MOSFET models, a 1.2 kV 36 A and a 90 A, of the same manufacturer were evaluated against short-circuit. With the purpose of analysing the correlation between the static measurement of the drain-source leakage current and the short-circuit behaviour, several devices of each model were tested in a device analyser. The devices with highest and lowest leakage current were chosen for short circuit testing.

Both SiC MOSFET models displayed a very high leakage after turn off, which was in the order of the rated current. This high leakage current and the short-circuit results were not in complete agreement with static measurement. It difficulted the possibility of relating the static test drain-source leakage current with the short-circuit behaviour.

Regarding the short-circuit withstand capability, both MOSFET models where tested a at range of temperatures from T_{case} = 25 to 150 ℃. At a DC-link of 400 V, all the tested devices were able to withstand 10 μs short circuits pulses. By contrast, at 600 V a short circuit pulse of 10 μs could not we reached. At this voltage, the DUTs either failed suddenly or a permanent and gradual decrease of the whole gate voltage pulse was observed. This latter phenomena occurs for both 36 and the 90 A models when the case temperature is over T_{case} = 100 ℃.

5.2 Future work

In order to continue with the investigation on the cause for early short-circuit failure, among other possible ideas, two tasks may be considered for following works.

On one hand, to gain more information about the devices, the 36 A MOSFETs should also be characterised for gate-source leakage current and transfer characteristics. Having observed during testing, that the gate-source voltage decreased towards the end of long pulses. It may be indicated to choose the devices with the highest and lowest for short circuit test. The results of this test may assist to understand if the gate ruggedness affects the short-circuit behaviour.

On the other hand, with the purpose of understanding how and if the device is damaged after a short circuit. It may be worth to perform static characterization of the DUT after each test. This procedure may be specially applied at demanding test conditions.

Appendix A

Appendix: Static characterization

A.1 Setup

The static characterization is performed to determine the static characteristics of the different devices and relate them to dynamic testing. For this purpose, the B1506A Power Device Analyser from Keysight which is available at the Energy Technology department is used [39]. As can be seen in Fig. A.1, to characterize the device at diverse temperatures, a thermostream Temtronic TP 4500 [40] is attached to the Power Device Analyser fixture.

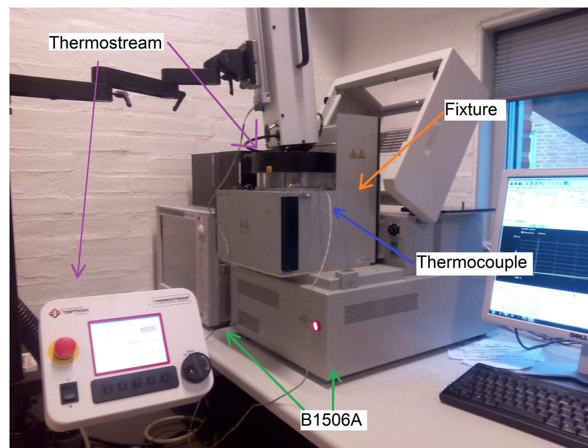
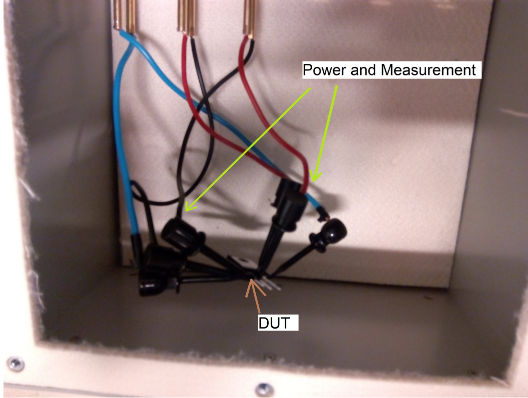
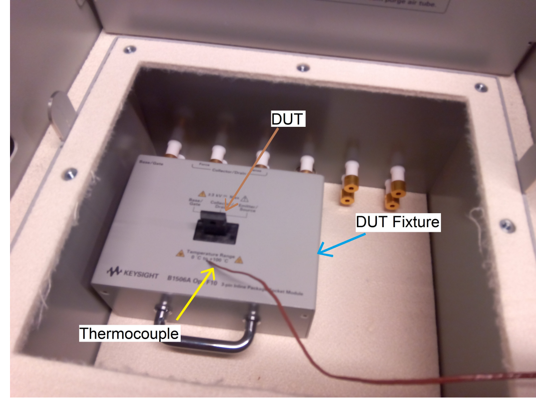


Fig. A.1: General layout of the static test setup.

In Fig. A.1, it can be observed that the thermostrean is directly attached to the fixture, providing a flow of air in the order of few litres per second at the desired temperature. The temperature inside the fixture is monitored by a T type thermocouple. In Fig. A.2 (a) and (b) the interior of the fixture are shown. Two arrangements where used, (a) attachment with mini hooks and (b) with a fixture. It should be mentioned that as shown in (b) the thermocouple is not attached to the Device Under Test(DUT). This means that the measured temperature is approximately the DUT temperature.



(a) The device is characterized using mini hooks, tested temperature range is 0 - 200 °C.

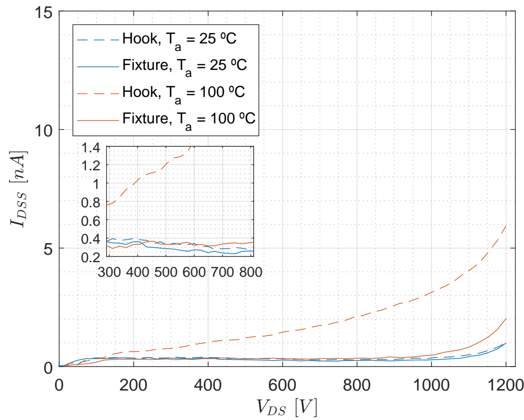


(b) The device is characterized with the Opt F10 fixture from Keysight at a temperature range of 0 - 125 °C.

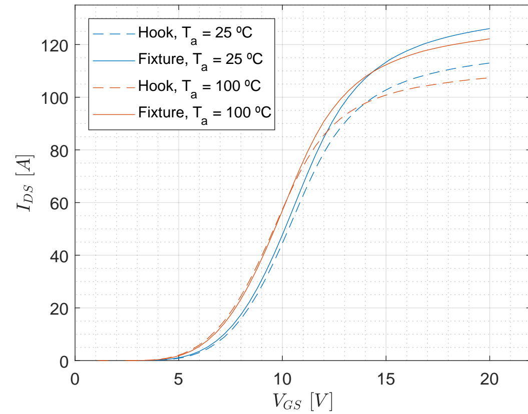
Fig. A.2: Interior of the fixture shown in Fig. A.1. The DUT are the SiC MOSFETs with TO - 247 packaging.

In order to characterize the devices at a wide temperature range, the C2M0080120D [10] devices were tested with the setup shown in Fig. A.2(a). However, the contact resistance and inductance that the hooks may add to the measurement raised concerns over the quality of the measurement.

In Fig. A.3 the comparison of measurement with hooks and fixture of the C2M0025120D [31] at the temperature range of $T_a = 25$ and 100 ℃ is shown. In (a) the drain source leakage current is depicted and in (b) the transfer characteristics.



(a) Drain-Source leakage current (I_{DSS}).



(b) Transfer characteristics.

Fig. A.3: Comparison between hook and fixture measurement

In Fig. A.3 (a), it can be observed that at $T_a = 100$ ℃ a higher drain source leakage current is measured with the hooks than with the fixture. By contrast, in (b), the crossing point and the final reached current is higher with the fixture than with the hook. It was considered that the results obtained with the fixture to be more trustworthy than those obtained with the hooks. Therefore, it was decided to perform the static characterisation of the C2M0025120D with the fixture instead of the hooks.

A.2 Tested Variables

A.2.1 Drain-source leakage current (I_{DSS})

According to Reigosa et al. [41] thermal runaway is considered to be a common failure in silicon devices at high temperatures in off state. Additionally, in the introduction it was reported that this type of failure was also being observed in SiC MOSFETS. In Si devices, as a rule of thumb, the leakage current is expected to increase by a factor of 2 when the temperature increases 11 ℃. Therefore, it is intended to observe whether a correlation between this term and short-circuit behaviour can be performed.

A.2.2 Gate-source threshold voltage ($V_{GS\,Th}$)

During short circuit a high about of energy is dissipated, thus the device heats up fast. This temperature increase, causes the reduction of the gate threshold voltage. A low threshold voltage may cause the unintended triggering of the device [42].

The method to determine the threshold voltage is graphically shown in Fig. A.4. It corresponds to S1 at $T_a = 25$ ℃.

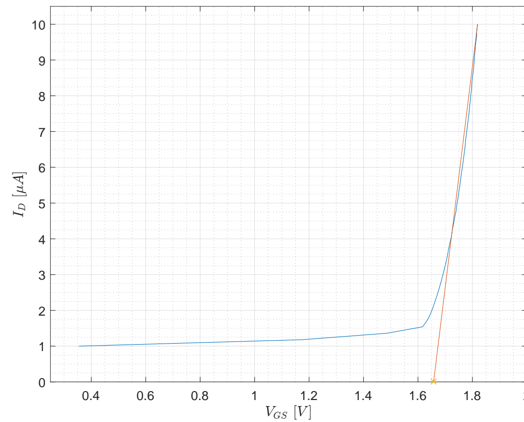


Fig. A.4: Threshold voltage determination.

As can be observed, the I_{DS} trace is extended, the crossing point at which $I_D = 0$ A is where the threshold voltage is considered to be located. In the case of Fig. A.4, at $V_{GS\,threshold} = 1.65$ V.

A.2.3 Gate-source leakage current (I_{GSS})

As commented in the introduction, a voltage drop towards the end of the pulses was observed during short circuits. The reduction of gate-source voltage is a sign of current flowing through the gate. By this test it is intended to understand how does this term vary with temperature.

A.2.4 Transfer characteristics (V_{GS} − I_{DS})

The transfer characteristics depict de behaviour of I_{DS} as a function of V_{GS} with a constant drain source voltage, in this case ($V_{DS} = 20$ V). It depicts whether at a given condition the device will behave with Negative Thermal Coefficient (NTC) i.e. reducing its resistance with temperature, or Positive Thermal coefficient (PTC) i.e. increasing its resistance.

A.3 Test conditions for C2M0080120D

The test conditions for the C2M0080120D are shown in Table A.1 for the and drain-source leakage current and in Table A.2 for the gate-source threshold voltage.

Drain Source leakage current (I_{DSS})

Variable	Comment	Value	Minimum	Maximum
V_{GS}	-	0 V	-	-
I_{GS}	compliance	250 μA	-	-
V_{DS}	-	-	0 V	1.2kV
I_{DS}	compliance	10 μA	-	-

Table A.1: Drain source current leakage, test conditions and compliance.

Gate source threshold voltage ($V_{GS\,Th}$)

Variable	Comment	Value	Minimum	Maximum
V_{GS}	compliance	10 V	-	-
I_{GS}	-	-	1 μA	10 μA
V_{DS}	compliance	10 V	-	-
I_{DS}	-	-	10 μA	250 μA

Table A.2: Gate source threshold voltage, test conditions and compliance.

A.4 Test conditions for C2M0025120D

The test conditions for the second device are given in the next Table A.3 I_{DSS}, Table A.4 $V_{GS\,Th}$, Table A.5 I_{GSS} and Table A.6 V_{GS} - I_{DS}.

Drain Source leakage current (I_{DSS})

Variable	Comment	Value	Minimum	Maximum
V_{GS}	-	0 V	-	-
I_{GS}	compliance	250 μA	-	-
V_{DS}	-	-	0 V	1.2 kV
I_{DS}	compliance	10 μA	-	-

Table A.3: Drain source current leakage, test conditions and compliance.

Gate source threshold voltage ($V_{GS\,Th}$)

Variable	Comment	Value	Minimum	Maximum
V_{GS}	compliance	10 V	-	-
I_{GS}	-	-	1 μA	10 μA
V_{DS}	compliance	10 V	-	-
I_{DS}	-	-	10 μA	250 μA

Table A.4: Gate source threshold voltage, test conditions and compliance.

Gate Source leakage current (I_{GSS})

Variable	Comment	Value	Minimum	Maximum
V_{GS}	-	-	-5 V	20 V
I_{GS}	compliance	600 nA	-	-
V_{DS}	-	0 V	-	-
I_{DS}	compliance	8 mA	-	-

Table A.5: Gate source leakage current, test conditions and compliance.

Gate source threshold voltage (V_{GS} $-$ I_{DS})

Variable	Comment	Value	Minimum	Maximum
V_{GS}	-	-	0 V	20 V
I_{GS}	compliance	1 A	-	-
V_{DS}	-	20 V	-	-
I_{DS}	compliance	135 A	-	-

Table A.6: Transfer characteristics, test conditions and compliance.

Appendix B

Appendix: Short-circuit test setup

The discrete SiC MOSFETs are tested at the Non Destructive Tester (NDT) available at the Energy Technology department [18].

B.1 Test setup

In Fig. B.1 the setup is shown, the diagram to which the tester relates is in Fig. B.2.

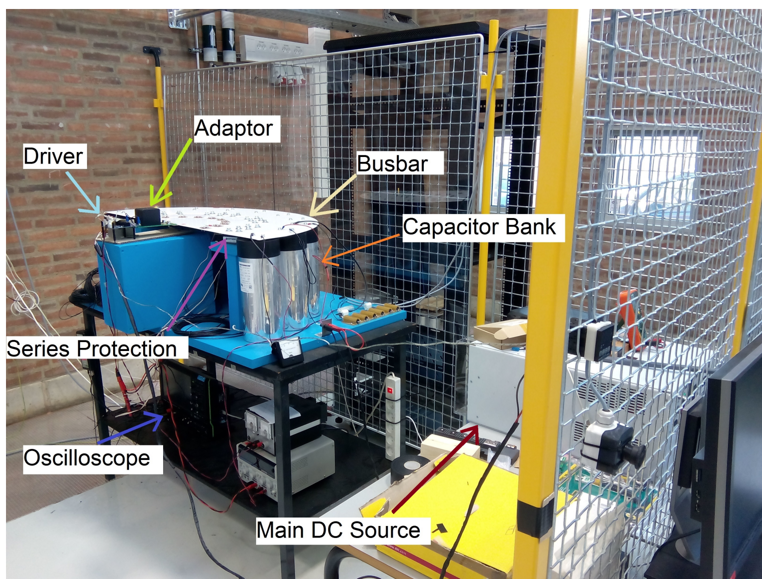


Fig. B.1: NDT tester available at the E.T. department.

As can be observed in Fig. B.1 and in the diagram in Fig. B.2, the NDT tester consists of: the *main* DC Source (V_{DC}), a capacitor bank (C_{DC}), a Series Protection (SP) switch to break the short-circuit in case of breakdown and a busbar of 30.5 nH [43]. Additionally C_{small} is added directly on the PCB for decoupling.

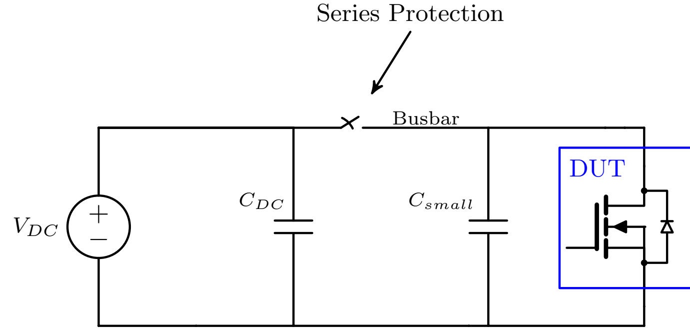


Fig. B.2: Diagram of the setup for NDT available at the laboratory. If the series protection is closed, and the gate of the DUT is enabled, the tested device sees the full DC link.

In Fig. B.3 the waveforms by which the gates of the Series Protection and DUT are driven is shown.

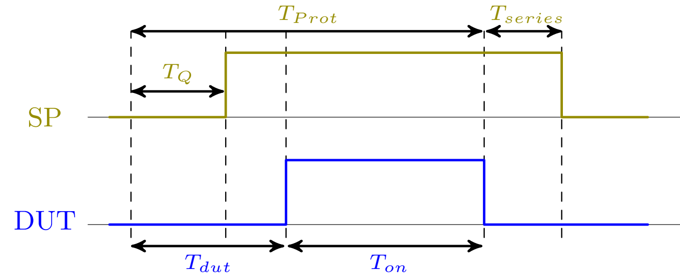


Fig. B.3: Gate waveforms of both the Series Protection (SP) and DUT.

T_{on} in Fig B.3, corresponds to the short circuit time. T_{series} is an amount of time before turning off the system. It is left to observe if a delayed the short circuit happens. As can be seen, the SP is turn on first. After a certain time, the DUT is turned on and the SC happens. An example of such timing procedure is shown in Table B.1.

	T_Q	T_{Prot}	T_{DUT}	T_{Series}	T_{on}
time [ns]	100	50000	50000	2000	1000

Table B.1: Timing for a 1 μs short − circuit.

The reason to leave such prolonged periods in comparison with T_{on} is to allow C_{small} to get charged.

B.2 Hardware

The hardware used for setting the test condition is shown in Table B.2. In Table B.3, the measurement equipment is shown.

Device	Brand	Model	Ref.
Main DC source	Magna – Power Electronics	TS 6U	[44]
Driver DC source	GW Instek	GPS - 4303	[45]
Driver	CREE Inc.	CGD15HB62P1	[32]
FPGA	Terasic Technologies Inc.	DE2 - 115	[46]
Temperature Controller	Omrom Corp.	E5CB	[34]
Enclosure Heating	DBK Technology Ltd.	HPG-2/22-75X35-100-240	[33]

Table B.2: Test conditioning.

Device	Brand	Model	Ref.
Oscilloscope	Teledyne Lecroy	HDO 6104-MS	[47]
High Voltage Probe	Teledyne Lecroy	PPE6KV	[48]
Voltage Probe	Tektronix	TP0200	[49]
Rogowski coil	PEM	CWT Ultra-mini	[50]

Table B.3: Measurement equipment.

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