AALBORG UNIVERSITY

MASTER THESIS PROJECT

Investigation of a STATCOM Modular Multilevel Converter under unbalanced conditions

Department of Energy Technology

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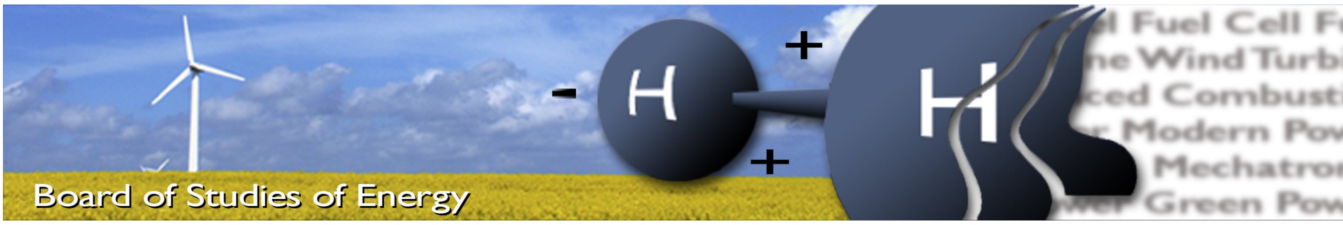

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SYNOPSIS:

The advancements of Multilevel Converter technology have brought the beginning of a new era in the FACTs industry and the Modular Multilevel Converter has received the attention of researchers in the last decade. The present Thesis focuses on the development of an advanced control system of a Modular Multilevel Converter aimed for a STATCOM application. The performance of the proposed control scheme under internal and external unbalances is evaluated via extensive simulations combined with experimental sessions. Finally, an enhanced control system is employed for the effective mitigation of current harmonics, with the STATCOM acting as an active filter.

Georgios Tsolaridis

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Georgios Tsolaridis
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Nomenclature

$\hat{i}_{c1}$	Fundamental component of circulating current
ϕ_1	Angle of fundamental component of output current vector
ϕ_c	Angle of fundamental component of circulating current vector
$\hat{P}_n$	Peak of oscillating term of the active power
$\hat{Q}_n$	Peak of oscillating term of the reactive power
$\hat{v}_1$	Peak of the phase voltage
ω	Fundamental frequency in radians per second
ω_{samp}	Sampling frequency in radians per second
ϕ^+	Phase of positive sequence PCC voltage vector
ϕ_I^+	Phase of positive sequence current vector
ϕ^-	Phase of negative sequence PCC voltage vector
ϕ_I^-	Phase of negative sequence current vector
θ_0	Phase of zero sequence PCC voltage vector
bw	Controller's bandwidth
C_{eq}	Equivalent pole-to-pole capacitance
C_{sm}	Submodule's capacitance
$f_{s_{eff}}$	Effective Switching frequency
f_s	Switching frequency
I^+	Magnitude of positive sequence current vector
I^-	Magnitude of negative sequence current vector
i_c	Circulating current
i_l	Lower arm's current
i_s	Output current
i_u	Upper arm's current
i_{c0}	DC component of circulating current
i_{sm_l}	Individual lower arm submodule's current
i_{sm_u}	Individual upper arm submodule's current
L_{arm}	Arm inductance
m	Modulation index
N	Number of submodules per arm
n_l	Lower arm's insertion index

n_u	Upper arm's insertion index
p	Instantaneous active power
P_0	Average active power
p_Δ	Instantaneous arm difference power
p_Σ	Instantaneous leg power
$p_{u_{arm}}$	Instantaneous power of upper arm
q	Instantaneous reactive power
Q^+	Magnitude of positive sequence reactive power
Q^-	Magnitude of negative sequence reactive power
Q_0	Average reactive power
R_{arm}	Arm resistance
t_r	Controller's rise time
T_{samp}	Sampling time
V^+	Magnitude of positive sequence PCC voltage vector
V_g^+	Magnitude of positive sequence grid voltage vector
V^-	Magnitude of negative sequence PCC voltage vector
V_g^-	Magnitude of negative sequence grid voltage vector
v_{cl}^Σ	Sum capacitor voltages of lower arm
v_{cu}^Σ	Sum capacitor voltages of upper arm
V_0	Magnitude of zero sequence PCC voltage vector
v_a	Converter phase-a voltage
v_c	Internal voltage
V_{dc}	Pole-to-pole voltage
$v_{l_{arm}}$	Voltage of lower arm
v_{sm}	Submodule's voltage
v_s	Output voltage
$v_{u_{arm}}$	Voltage of upper arm
V^{+*}	Voltage reference of the positive sequence PCC voltage vector
V^{-*}	Voltage reference of the negative sequence PCC voltage vector
W_Δ	Energy Difference between the upper and lower arm
W_Σ	Leg Energy

Chapter 1

Introduction

The increasing requirements of the modern lifestyle when it comes to the power quality have been the main reason of the wide usage of Flexible AC Transmission Systems (FACTS). Apart from that, the growth of FACTS market can be attributed to factors such as the growing markets of electric utility and renewable systems as well as the on-growing demand for energy savings and maximum energy efficiency in a world that relies more and more on electricity [4]. The FACTS market share is split between big power system companies like ABB, General Electric, Siemens, Alstom and Mitsubishi to mention just a few. In fact, the market share is growing with increasing ratio and it is expected to surpass the $\$1.000M$ landmark, before 2020, as can be depicted on the figure on the left hand side [1].

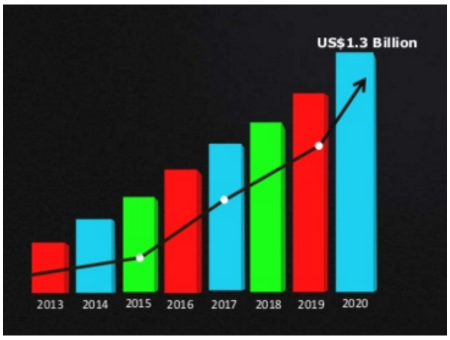

FIGURE 1.1: Global Facts Market [1].

1.1 Why STATCOM Technology?

The great majority of the loads that are used in real world applications are inductive and it is rather unlikely that the utility grid will be presenting a unity power factor if no action is taken. Inductive and capacitive loads absorb or produce reactive power respectively. Reactive power needs to be compensated since its presence increases the conduction losses of a given system without increasing the active power and usually leads to poor voltage regulation.

Thyristor based reactive compensation is a technology that is used in utility grids since the 1970s. The basic principle of these devices is the control of the susceptance of the reactor by controlling the firing angle of the thyristors. This type of reactive power compensation is commonly known as static VAR compensator (SVC) and finds many applications in modern power grids due to its fast response and high performance [5]. Usually, a capacitor bank comprised by multiple capacitors is used along with a thyristor bridge. Combining multiple capacitor banks gives an extra flexibility to control the inserted reactive power in steps, therefore ensuring a smoother performance. The technology is commonly referred to as Thyristor Switched Capacitor (TSC). If there is a need to compensate a capacitive load, then instead of a capacitor bank, a reactor bank is used, but the operating principle remains the same. This setup is usually referred to as Thyristor Controlled Reactors (TCR) [6].

The development of Voltage Source Converters (VSC) signified the beginning of a new era for the power grid. VSC technology became a basic part of FACTS and found its application on reactive power compensation with the emergence of the STATic synchronous COMpensator (STATCOM), initially introduced in the nineties [7]. STATCOM became immediately one of the most representative members of FACTS family as its technology is widely used in modern power grids due to its excellent dynamic performance, fast response time, design flexibility and small footprint due to the small number of needed passive components.

1.2 Why Multilevel Converter Technology?

In addition to the above, medium and high voltage grid applications, require the use of power devices with a high blocking voltage rating. Silicon technology however seems to have reached its full potential regarding voltage rating, with the highest available rating for a Si IGBT on the market being 6.5 kV. SiC devices promise higher blocking voltages due to superior material properties in comparison to conventional Si devices but at present their technology is relatively immature and they are not expected to substitute their Si counterparts in the near future, at least for large scale applications [8].

One popular solution that was adopted in the previous decades was the connection of a transformer in the output of the converter in order to scale up the voltage before connecting it to the grid. However these transformers are usually bulky and expensive, making their use unattractive [3].

Another attractive solution could be the series connection of power devices. The series connected devices would ideally share the total voltage between them and the total voltage rating of the setup could be increased. However, the unavoidable differences between the intrinsic parameters of the power devices cause voltage imbalances and therefore lead to reliability issues. The problem can be solved with various auxiliary circuits that slow down the switching transients but this would increase the cost of the setup along with decreasing its efficiency [9].

In addition to the aforementioned problem, modern power grid codes and regulations have become stricter over the past years regarding $\%THD$ and power quality requirements [5]. Consequently, the adoption of multilevel converters appears as the most promising solution since these topologies can produce an AC voltage that increases with increased number of levels while reducing the harmonic injection without increasing the voltage rating of the power devices [10].

Two of the most widely discussed multilevel topologies in literature are the Diode Clamped Multilevel Inverter (DCMLI), which is also called Neutral Point Clamped Converter (NPC) when only 3 levels are used, and the Flying Capacitor Multilevel Inverter. Both of these topologies are capable of producing high quality AC waveforms [11]. An analytic comparison can be found in [12]. A short description of these topologies can be found in Appendix A.

Among the multilevel converter topologies used in FACTS, the Modular Multilevel Converter (MMC) has been the most promising and encountered a huge amount of focus by researchers due to its superior properties. This topology offers excellent harmonic performance and combines low switching frequencies with high reliability, modularity and design flexibility [13].

Firstly, due to the high quality output AC voltage, the MMC is usually associated with the absence of low order passive filters. These filters are usually bulky and their performance often depend on the operating conditions and the impedance of the network, making their design challenging. Moreover, the MMC topology offers the possibility to the manufacturer to extend the topology according to the needs of the customer. This modularity is a unique characteristic that in the long run results in reduced production cost [5]. In addition, the MMC can effectively switch with a lower frequency, even with fundamental frequency, resulting in reduced switching losses. The use of low frequency in this case compromises neither the dynamic performance of the system nor the final output waveform since the effective switching frequency (switching frequency seen at the AC waveform) is directly proportional to the number of levels used.

Moving on, the MMC family is usually classified in four different configurations described thoroughly in [13]:

- Single Star Full-Bridge (SS-FB)
- Single Delta Full-Bridge (SD-FB)
- Double Star Half-Bridge (DS-HB)
- Double Star Full-Bridge (DS-FB)

This report focuses on the Double Star Half-Bridge configuration. A small discussion along with the relevant schematics of all the configurations can be found in Appendix A. The importance of the DS-HB and its attractiveness from a performance as well as from an economic point of view, in a large scale STATCOM application over the widely used SD-FB has been highlighted in a complete study that can be found in **Publication A**.

1.3 Thesis Objectives

In this M.Sc Thesis report, the focus is laid on the theoretical design and implementation of an advanced and complete control system aimed for the reliable operation of the MMC under internal and external unbalanced conditions in a STATCOM application. The designed control system is initially tested with simulations and finally with extensive experiments.

Moreover, the capability of the configuration to mitigate voltage sags and fault conditions that generally arise from the AC side should be investigated and the proposal of a preferred injection strategy for the application is intended. However fault conditions will not be tested in the experimental setup. Finally, the MMC's capability to mitigate higher harmonic components and compensate by a proper injection strategy should also be investigated through simulations and experiments.

1.4 Limitations

In the experimental part of the conducted work, certain limitations were involved. A newly developed, small scale MMC setup was used for the first time in Aalborg University. The reliability of the setup at its initial development stage was relatively low and faults usually occurred. To ensure safety, the prototype was used at a power level equal to half of its rated power. Apart from that, the initial unavailability of the setup did not permit the study of fault conditions on the AC side, in time.

1.5 Main Contributions

The original contributions of the Thesis are listed below:

- A comparison of the losses and related costs of the SD-FB and DS-HB configuration was conducted, exhibiting the advantages of the DS-HB configuration in a STATCOM application when negative sequence reactive power is controlled. This analysis can be found in **Publication A**.
- A cost effective way to reduce the necessary submodule's capacitance with the injection of a second order circulating current was investigated and its results are demonstrated in **Publication B**, in close collaboration with group PED2-940.
- An intuitive and easy to implement decoupled arm energy balancing method was introduced.
- An improved injection strategy during asymmetrical voltage sags was presented. The improved strategy takes into consideration the effect of the zero component of the voltage in the calculations of the voltage references, in contrast to previous studies.
- A complete structure for the effective mitigation of higher order current harmonics in the MMC was developed. A mathematical analysis linked the presence of harmonics in the output current with the harmonics of the circulating current.
- The complete control structure of the MMC for the STATCOM application was implemented on a dSPACE environment for future usage in Aalborg University.

1.6 Outline of the Thesis

The report at hand is structured as follows. In Chapter 2, the governing equations of the MMC configuration are discussed and the fundamentals for the design of the control system are set. In Chapter 3, the complete control system of the MMC is presented and its performance in eliminating internal unbalances is shown through extensive simulations. In Chapter 4, external unbalances are investigated and two different injection strategies are studied thoroughly through simulations. In each case, the ability of the designed control system to keep the MMC balanced is highlighted. In Chapter 5, extensive experimental sessions prove the validity of the control system in a small scale MMC operating as a STATCOM. Finally in Chapter 6, a discussion of the main conclusions of the Thesis work is carried out and future work proposals are made.

Chapter 2

Overview of the Governing Dynamics of the MMC

In this chapter a fundamental analysis of the Modular Multilevel Converter used as a STATCOM is presented. The operating principles are explained and all the relevant quantities will be defined. The dynamics of the system are analyzed with the focus being laid on the energy variations that affect the internal balance of the converter. The mathematical model will form the backbone of the control strategies that will be presented in Chapter 3. The reader is encouraged to refer to the Nomenclature for all the relevant symbols.

2.1 MMC Fundamentals and Operating Principles

A three phase MMC in Double Star configuration is illustrated in Figure 2.1. The submodules used are consisted of two identical switches, forming a half-bridge, connected to a capacitor that will be referred to from now on as submodule's capacitor C_{sm}. The submodule chain is consisted of N identical submodules connected in series as shown in the schematic. The arm inductors L_{arm} are shown as well in the schematic and are connected between the converter output and the submodule chain. An equivalent arm resistor R_{arm} is also included to account for the inductor's parasitic resistance as well as the on-resistance of the switches. As a result, R_{arm} is variable and usually difficult to be determined. Its value is small and can be neglected for the shake of simplicity. By definition, a submodule is considered to be bypassed when the lower switch is conducting and inserted when the upper switch is conducting.

The output of the converter is connected to the three phase grid. For the shake of the analysis, the DC-link is considered to be formed by an equivalent capacitance. This equivalent capacitance is actually the capacitance that is formed by the connection of the C_{sm}. This capacitance is now split into two parts and the middle point is grounded. In reality, in the STATCOM application, the two neutral points of the star connection will be floating but this imaginary grounded point will simplify the extracted mathematical model.

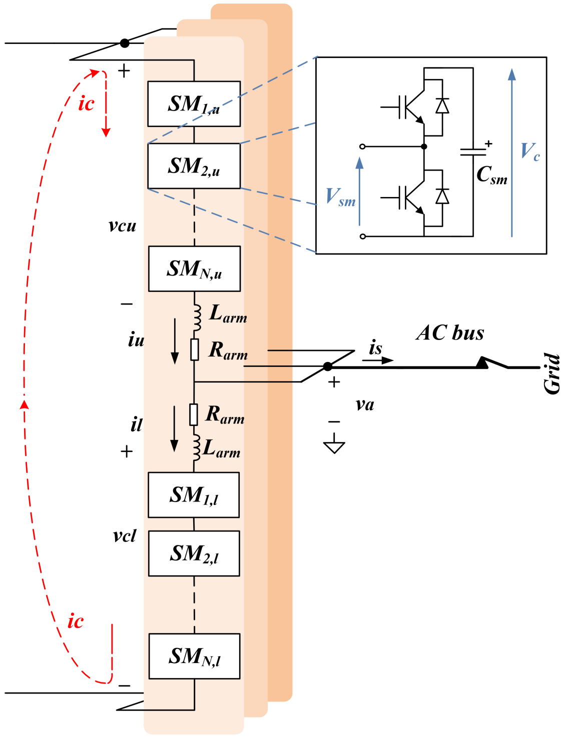

FIGURE 2.1: Schematic of the MMC.

The phase-a output voltage (v_a) of the converter is considered to be the reference in this analysis, with all the other phase shifts being calculated with reference to this. Due to symmetry, only the analysis of phase-a leg will be shown. The output converter voltage and current are then defined as:

$$v_a = \hat{v}_1 \cdot cos(\omega t) \tag{2.1}$$

$$i_s = \hat{i}_1 \cdot cos(\omega t + \phi_1) \tag{2.2}$$

The currents that are flowing inside the arms of the converter are defined in such a way that when they are positive and the submodule is inserted, C_{sm} is charging whereas when they are negative, C_{sm} is discharging. Using Kirchhoff's current law (KCL) in Figure 2.1:

$$i_s = i_u - i_l \tag{2.3}$$

The circulating current i_c is defined as the current that flows inside converter legs, without affecting the output current i_s. This current is defined as the mean value of the upper and lower arm legs:

$$i_c = \frac{i_u + i_l}{2} \tag{2.4}$$

In the case of a STATCOM, where there is no DC-link capacitor connected between the neutral points of the Double Star, the three phase average i_c current is obviously zero. However in the next chapters it will be shown that each leg's current could have a DC component that is different than zero, providing that the sum of the instantaneous values add up to zero. Apart from that, the circulating current is usually associated with a number of harmonics that also derive from the control method that is being used, and will be further analyzed later on.

The combination of Equation 2.3 and Equation 2.4 give rise to the following set of equations that describe the arm currents as a function of the output and the circulating current:

$$\begin{cases} i_u = i_c + \frac{i_s}{2} \\ i_l = i_c - \frac{i_s}{2} \end{cases} \tag{2.5}$$

Until this point, no discussion was made about the effect of the modulation in the system. In order to simplify the calculations, the assumption that the switching frequency is approaching infinite is made [14]. In this way, the modulation indexes can be assumed to be varying with the fundamental component only. Based on this simplified model, the insertion indexes of the upper and lower arm can be defined as:

$$\begin{cases} n_u = \frac{1}{2}(1 - m \cdot cos(\omega t)) \\ n_l = \frac{1}{2}(1 + m \cdot cos(\omega t)) \end{cases} \tag{2.6}$$

The above defined indexes take discrete values in the interval $[0,1]$. The total voltage inserted by the upper arm (v^{Σ}_{cu}) and the one inserted by the lower arm (v^{Σ}_{cl}), can now be expressed as a function of the insertion indexes.

$$\begin{cases} v^{\Sigma}_{cu} = n_u \cdot N \cdot v_{sm} \\ v^{\Sigma}_{cl} = n_l \cdot N \cdot v_{sm} \end{cases} \tag{2.7}$$

Assuming that all of the submodules are controlled to the same value, the submodule's voltage is usually taken as:

$$v_{sm} = \frac{V_{dc}}{N} \tag{2.8}$$

At this point, setting up the voltage equations for the upper and lower arm will prove to be very useful for understanding the control strategies that should be applied to the output as well as to the internal current controllers. From the Kirchhoff's law of voltages (KVL):

$$\begin{cases} v_a = \frac{V_{dc}}{2} - v^{\Sigma}_{cu} - R_{arm} \cdot i_u - L_{arm} \cdot \frac{\partial i_u}{\partial t} \\ v_a = -\frac{V_{dc}}{2} - v^{\Sigma}_{cl} + R_{arm} \cdot i_u + L_{arm} \cdot \frac{\partial i_l}{\partial t} \end{cases} \tag{2.9}$$

After proper manipulation, the sum of these equations will give insight for the control strategy that should be implemented to drive the output current:

$$\frac{L_{arm}}{2} \cdot \frac{\partial i_s}{\partial t} = \frac{v^{\Sigma}_{cl} - v^{\Sigma}_{cl}}{2} - v_a - \frac{R_{arm}}{2} \cdot i_s \tag{2.10}$$

Equation 2.10 shows that the difference of the inserted voltage of the lower and upper arm is responsible for controlling the output current. This differential voltage term will be referred to from now on as the output voltage:

$$v_s = -\frac{v_{cl}^{\Sigma} - v_{cu}^{\Sigma}}{2} \tag{2.11}$$

It should be also pointed out, since it will prove to be important in the control chapter that follows, that the effective inductance that is seen from the output is $\frac{L_{arm}}{2}$ and the effective resistance is $\frac{R_{arm}}{2}$.

On the other hand, subtracting equations 2.9 will give insight for the control strategy of the circulating current:

$$L_{arm} \cdot \frac{\partial i_c}{\partial t} = \frac{V_{dc}}{2} - \frac{v_{cl}^{\Sigma} + v_{cu}^{\Sigma}}{2} - R_{arm} \cdot i_c \tag{2.12}$$

Equation 2.11 shows that the sum of the inserted voltage of the lower and upper arm is responsible for controlling the circulating current. In contrast to the output current, the effective inductance and resistance that the circulating current sees is L_{arm} and R_{arm} respectively. Similarly to the previous definition of the output voltage v_s, the internal voltage v_c will be defined hereby as:

$$v_c = \frac{v_{cl}^{\Sigma} + v_{cu}^{\Sigma}}{2} \tag{2.13}$$

The final step to complete the fundamental analysis is the extraction of the insertion indexes defined before, as a function of the reference voltages. If v_s^* is the reference output voltage generated by the output current controller as pointed out before, and v_c^* is the internal voltage reference generated by the circulating current controller, then the insertion indexes n_u and n_l are found to be:

$$n_u = \frac{v_c^* - v_s^*}{V_{dc}} \tag{2.14}$$

$$n_l = \frac{v_c^* + v_s^*}{V_{dc}} \tag{2.15}$$

2.2 Internal Energy Dynamics

In order to ensure complete balance of the converter, the internal dynamics have to be studied and a controller that ensures balanced operation both under ideal and non-ideal conditions has to be implemented based on the governing equations. Therefore, it is crucial to investigate the internal energy variations that occur in the studied configuration. This investigation will be used in the next chapter in order to design the internal controllers of the system.

Equations 2.1 and 2.2, defined the output current of the converter and the phase voltage respectively. As explained in the previous section, the DC component of the three phase circulating current is zero, but each phase may contain a DC component as long as the sum of the instantaneous values are zero. In general, the DC component of the circulating current is responsible for moving active power from one phase leg to the other and its fundamental component is responsible for active power transfer between the upper and the lower arm inside one converter leg [15]. Based on these and assuming that a proper harmonic mitigation strategy is used, in order to cancel out all the higher harmonics, the circulating current can be defined as:

$$i_c = i_{c0} + \hat{i}_{c1} \cdot cos(\omega t + \phi_c) \tag{2.16}$$

Substituting equations 2.2 and 2.16 in Equation 2.5, the upper and lower arm currents are found:

$$i_u = i_{c0} + \hat{i}_{c1} \cdot cos(\omega t + \phi_c) + \frac{\hat{i}_1}{2} \cdot cos(\omega t + \phi_1) \tag{2.17}$$

$$i_l = i_{c0} + \hat{i}_{c1} \cdot cos(\omega t + \phi_c) - \frac{\hat{i}_1}{2} cos(\omega t + \phi_1) \tag{2.18}$$

The arm voltage of the upper and lower arm, based on Figure 2.1 can be expressed as:

$$v_{u_{arm}} = \frac{V_{dc}}{2} - v_a = \frac{V_{dc}}{2} - \hat{v}_1 \cdot cos(\omega t) \tag{2.19}$$

$$v_{l_{arm}} = \frac{V_{dc}}{2} + v_a = \frac{V_{dc}}{2} + \hat{v}_1 \cdot cos(\omega t) \tag{2.20}$$

Assuming that the instantaneous voltage of the submodules can be represented by a constant DC voltage source in series with an AC source, a simplified model of the MMC can be derived as explained in [16]:

$$p_{u_{arm}} = i_c \cdot \frac{V_{dc}}{2} - i_c \cdot v_a + \frac{i_s}{2} \cdot \frac{V_{dc}}{2} - \frac{i_s}{2} \cdot v_a \tag{2.21}$$

$$p_{l_{arm}} = i_c \cdot \frac{V_{dc}}{2} + i_c \cdot v_a - \frac{i_s}{2} \cdot \frac{V_{dc}}{2} - \frac{i_s}{2} \cdot v_a \tag{2.22}$$

The total power of each inverter leg as well as the power difference can be found based on the extracted equations 2.21 and 2.22, by addition and subtraction respectively. Adding the aforementioned equations and substituting the voltages and currents with their full expressions results in Equation 2.23 below:

$$p_\Sigma = i_{c0} \cdot V_{dc} + V_{dc} \cdot i_{c1} \cdot cos(\omega t + \phi_c) - \frac{\hat{v}_1 \cdot \hat{i}_1}{2} \cdot cos(\phi_1) - \frac{\hat{v}_1 \cdot \hat{i}_1}{2} \cdot cos(2\omega t + \phi_1) \tag{2.23}$$

The second and fourth term of the equation above are oscillating terms that have zero mean value over a fundamental cycle. On the other hand, the third term is associated with the AC output current. This term represents the active power that is flowing from the converter into the grid side and for a STATCOM it is negligible.

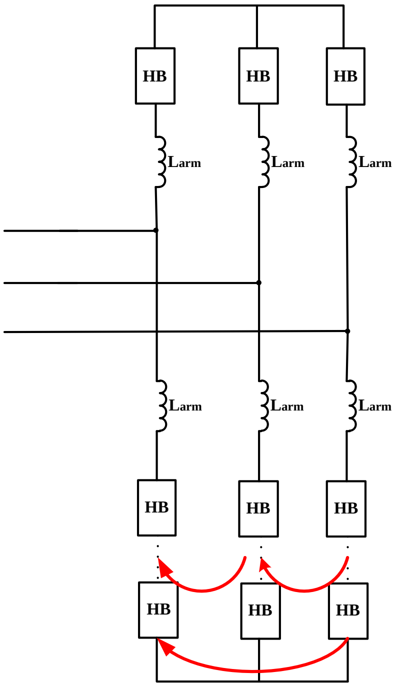

FIGURE 2.2: Leg Energy Balancing

The most interesting term of Equation 2.23 is the first one. The DC component of the circulating current is responsible for generating an equal amount of active power on the upper and lower leg. As a result it can be concluded that the total amount of energy in a converter leg can be controlled based on the DC component of the circulating current, as indicated in the figure on the left hand side. However, the sum of the three phase DC components should add up to zero:

$$i_{c0_a} + i_{c0_b} + i_{c0_c} = 0 \tag{2.24}$$

In other words, it can be concluded that by controlling the DC component of the circulating current in each phase of the converter, energy balance between the three legs can be achieved under ideal or non-ideal conditions. These findings will be used in the next chapter, in the energy balancing controller design section.

Going back to Equations 2.21 and 2.22, the power difference between the upper and lower arm can be found by subtracting the equations and substituting the terms with their previously defined forms:

$$p_{\Delta} = -2 \cdot i_{c0} \cdot \hat{v}_1 \cdot cos(\omega t) - \hat{v}_1 \cdot \hat{i}_1 \cdot cos(\phi_c) - \hat{v}_1 \cdot \hat{i}_1 \cdot cos(2\omega t + \phi_c) + \frac{V_{dc}}{2} \cdot \hat{i}_1 \cdot cos(\omega t + \phi_1) \tag{2.25}$$

The first, third and fourth term of the above equation are oscillating terms with an average value of zero, over one fundamental period so they are of no interest for the present analysis. On the other hand, the second term of Equation 2.25 is a DC term that is capable of redistributing the energy inside an arm as indicated by the figure on the right. The reason that the circulating current definition contained a first harmonic term should now be clear. The first harmonic of the circulating current is responsible for this inner leg distribution of energy. In other words, this term can be used in order to ensure balanced operation of the converter under ideal or non-ideal conditions. It should also be pointed out that the first harmonic is not generated naturally in an MMC configuration (see Chapter 5), so it should be ejected accordingly.

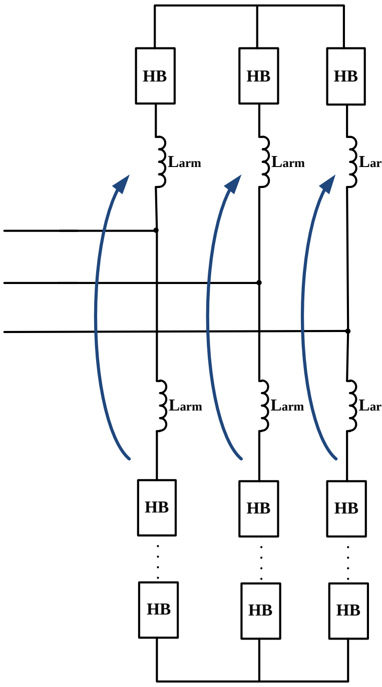

FIGURE 2.3: Arm Energy Balancing

However, one challenge that is commonly disregarded in the bibliography is that the injection of a current in one phase will have an impact on the other phases of the converter as well, since these phases will act as the return path. Based on these findings, a proper decoupled controller will be designed in the next chapter.

Chapter 3

Advanced Control Strategies

In the previous chapter the operating principles and the fundamental equations of the converter were analyzed. The dynamics that govern the operation of the converter topology form the basis for the implementation of the control strategies that will follow in this chapter. The chapter is divided in six sections. The first section presents a complete design procedure for the model that will be used in the simulations. After this, the implementation of the control system takes place. Figure 3.1 shows a complete overview of the control system that will be analyzed. In the following sections of the chapter, all the relevant control blocks shown in Figure 3.1 will be individually presented and their tuning process will be discussed, followed by a performance evaluation.

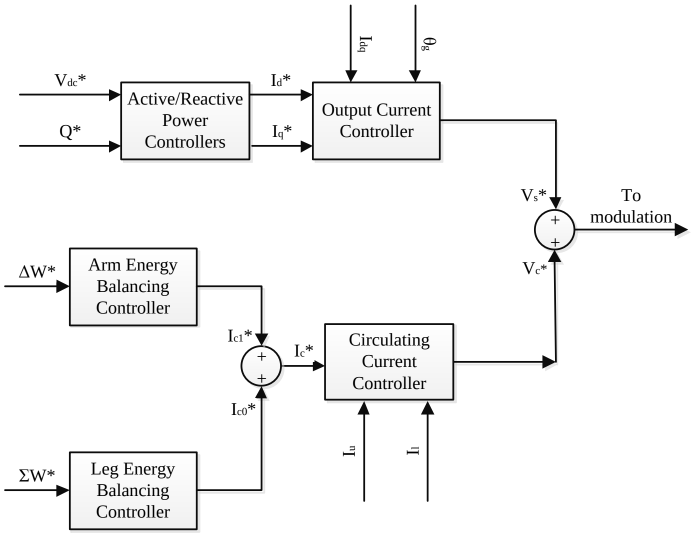

FIGURE 3.1: Overview of the STATCOM Control System.

3.1 Simulated System Specifications

The design of the simulated system is based on the procedure followed for the Double Star Half-Bridge configuration in **Publication A**. The simulated STATCOM is designed for a rated apparent power of 1 MVA and is connected directly to an AC grid of 6.6 kV through a line impedance that is assumed to be consisted of an inductance of 0.08 pu and a small resistance of 0.02 pu [17]. The base power used for these calculation is the rated power of the system (1 MVA) and the base voltage is the line to line RMS voltage (6.6 kV).

In addition to the above, the resulting total pole-to-pole voltage of the system can be found to be $V_{dc} = 14.2\ kV$ and the RMS current is calculated to be 87.5 A. For this application the Infineon FS50R17KE3 part number is chosen to be used [18]. The rated voltage of the device is 1.7 kV and the rated current 50 A. Designing for 100 FIT, each device should be blocking no more than 0.9 kV and therefore the number of cells per arm can be calculated to be 18, accounting for 10% redundancy [19].

Moving on, the choice of the switching frequency is crucial since a big switching frequency results in low converter efficiency but on the other hand, a small one is related with limited controller bandwidth and significant harmonic content in low frequencies.

TABLE 3.1: Device Parameters

Description	**Symbol**	**Value**
Submodule's RMS Current (A)	I_{sm}	44
IGBT Voltage Drop (V)	V_{ce}	2.2
Diode Forward Drop (V)	V_f	1.7
IGBT Turn On Losses (mJ)	E_{on}	20
IGBT Turn Off Losses (mJ)	E_{off}	32
Diode Reverse Recovery Losses (mJ)	E_{rr}	25

In this report, the choice of the switching frequency will be based on an approximation of the resulting efficiency of the system, with a 98.5% efficiency considered as an acceptable choice. The conduction and switching losses can be roughly approximated for various switching frequencies based on the table on the right. After an approximate expression is found, the efficiency is calculated for various frequencies and the result is plotted in Figure 3.2. The switching frequency choice in this report will be 270Hz that results in approximately 98.9% efficiency.

The submodule's capacitance choice is based on the analysis in [20]. The STATCOM requires the largest amount of stored energy when it is consuming reactive power. Accounting for 10% allowed

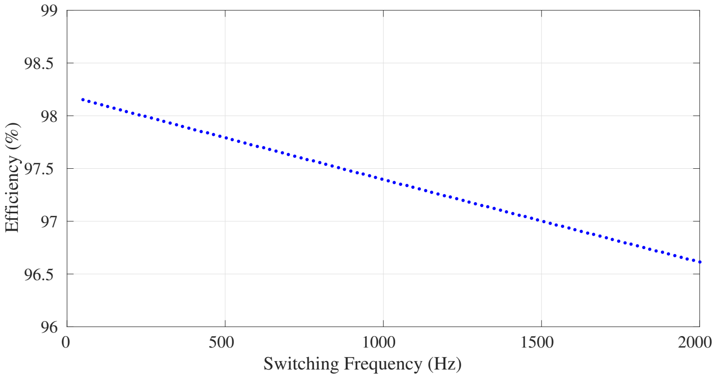

FIGURE 3.2: Converter estimated efficiency as a function of the switching frequency.

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capacitor voltage ripple and no third harmonic injection, the energy requirements are approximately 70 kJ/MVA. In the end, each cell should have a 2.1 nF capacitance connected in parallel to the half bridge.

TABLE 3.2: Simulated System Parameter Table

Description	**Symbol**	**Value**
Rated Power (MVA)	S	1
AC RMS Voltage (kV)	V_{ac}	6.6
Submodule's Voltage (kV)	V_{sm}	0.9
Submodule's Capacitance (mF)	C_{sm}	2.1
AC Grid Inductance (mH)	L_{ac}	11.1
Arm Inductance (mH)	L_{arm}	5
Switching Frequency (Hz)	f_s	270
Number of Submodules per arm	N	18
Pole-to-pole Voltage (kV)	V_{dc}	14.2
Effective Switching Frequency (kHz)	$f_{s_{eff}}$	4.8
Output RMS Current (A)	I	87.5

Finally, the arm inductance is a unique characteristic of the MMC and the choice of its value is usually made based on two main considerations: i) the circulating current suppression capability and ii) the fault current limiting capability of the inductance [21]. In this report however, the circulating current controller is responsible for the circulating current suppression and the focus is laid on the optimization of the control for this purpose. In addition to the above, a pole to pole fault that is usually considered as the worst fault condition is not a realistic scenario in the studied STATCOM configuration. An arm inductance of $0.03-0.04$ pu was used for a similar application in [22] and this choice results in the 5 mH value that will be used in the upcoming simulations. Table 3.2 summarizes the main parameters of the STATCOM configuration that will be used in the simulations.

3.2 Output Current Controller

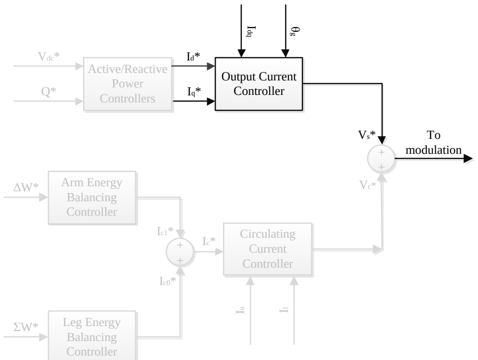

FIGURE 3.3: Output Current Controller.

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The analysis of the control system will start from the control of the output current i_s. The output current is the heart of the control system and the controller has to be designed with care since any instabilities in this loop may deteriorate the performance of the whole converter system. In this section, the Proportional-Resonant controllers (PR-controllers) used throughout this report will be introduced and a tuning process that takes into consideration both the performance as well as the stability of the system will be presented. The tuning process in this section as well as in the rest of the report will be made in the continuous Laplace domain (s-domain) but the method can be easily extended to the z-domain with appropriate manipulations.

In this report, the control of the output current is made in the stationary abc-frame, so the reference currents are sinusoidal in the fundamental frequency. These references are in the general case generated by the higher level controllers, as shown in the next section of this chapter. Conventional PI-controllers are not sufficient when the reference to be tracked down is not DC. On the other hand, PR-controllers are acting as bandpass filters tuned in specific frequencies, in this case in the fundamental frequency, in order to track down sinusoidal references. In fact, PR-controllers are general integrators tuned to have infinite gain at the desired frequency [23]. PI-controllers are tuned to have an infinite gain at 0 rad/s and therefore can be perceived as a specific case of the general case, where the desired frequency is zero. The transfer function of a PR-controller is depicted in Equation 3.1.

$$G_c(s) = K_p \cdot (1 + \frac{1}{T_r} \cdot \frac{s}{s^2 + (h\omega_1)^2}) \tag{3.1}$$

where K_p is the proportional gain that defines the dynamics of the controller, T_r is the time constant of the resonant part, that minimizes the tracking errors in the desired frequency, h is an integer and ω_1 is the fundamental frequency. It is clear now that if $h = 0$ the resonant part reduces to a simple integrator. This property of the PR-controllers will prove to be particularly useful when a reference with more than one frequencies needs to be tracked down as in Chapter 5 of the report at hand. Then the inclusion of multiple resonant parts connected in parallel, tuned in different frequencies, will prove to be effective, without increasing the complexity of the control system. Moreover, the controllers are sequence-decoupled, meaning that they can track down both positive and negative sequence components. This will prove to be convenient in Chapter 4.

The control of the output current is straightforward. An inspection of Equation 2.10 shows that the output voltage v_s defined as in Equation 2.11, is driving the output current i_s through an impedance with a resistive part $\frac{R_{arm}}{2}$ and an inductive part $\frac{L_{arm}}{2}$. The voltage at the converter side v_a can be treated from a control point of view as a disturbance to the system. Figure 3.4 shows the closed loop system for the control of the output current. The voltage at the converter side v_a is measured and fed-forward to the voltage reference that comes out of the PR-controller in order to improve the dynamic performance of the control system. The sum of those two according to Equation 2.11, form the reference output voltage v_s^*, that is fed to the modulation. The modulation inserts a time delay in the loop before giving rise to the output voltage v_s. The plant function then can be easily determined based on the previous findings as:

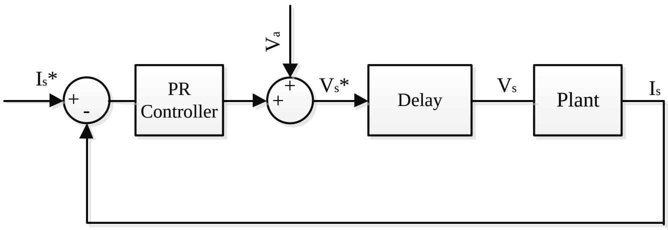

FIGURE 3.4: Output Current Controller Loop.

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$$\frac{I_s}{V_s} = \frac{2}{L_{arm} \cdot s + R_{arm}} \tag{3.2}$$

The time delay that the modulation inserts is difficult to be determined and depends strongly on the implementation of the control system in the DSP or the FPGA. In the usual case, the sampling frequency is two times higher than the switching frequency, and to be more precise for the case of MMC, two times higher than the effective switching frequency which accounts for all the submodules. The computational time delay can then be assumed to be in the magnitude of one sampling time, as it includes all the relevant communication delays and delays in the sensors. Therefore, in total the modulation can be associated with a time delay that is 1.5 times higher than the sampling time [24]. The delay block can be approximated with the following transfer function:

$$G_d(s) = e^{-s \cdot 1.5 \cdot T_{samp}} \tag{3.3}$$

In order to simplify the tuning process, the delay will not be initially considered and its effect on the loop's response and its stability will be evaluated in the end. Apart from that, R_{arm} is usually very small and therefore can be neglected at this point. As stated before the proportional part of the PR-controller is the one that defines the dynamic behavior of the control system. To further simplify the tuning process the resonant part can be neglected initially and the open loop transfer function is then given by Equation 3.4:

$$G_{cl}(s) = 2\frac{\frac{K_p}{L_{arm}}}{s + 2\frac{K_p}{L_{arm}}} \tag{3.4}$$

The bandwidth of the closed loop function is defined as the point where the bode diagram crosses $-3\ dB$ in magnitude and is related to the response of the system. For this simplified system the bandwidth bw will be:

$$bw = 2 \cdot \frac{K_p}{L_{arm}} \tag{3.5}$$

A high bandwidth translates into a low rise time and therefore a fast response and vice versa. For first order systems, according to general control theory the relation between the bandwidth bw and the rise time t_r is given by Equation 3.6 [25]:

$$t_r = \frac{\ln(9)}{bw} \tag{3.6}$$

Typically in voltage source converter applications, the rise time of the current loop is taken in the magnitude of milliseconds. The limitation for the upper limit of the bandwidth is imposed by the sampling time and a useful rule of thumb states that the bandwidth of the output controller has to be 10 times lower than the sampling angular frequency according to Equation 3.7:

$$bw < \frac{\omega_{samp}}{10} \tag{3.7}$$

This relation reveals also one of the properties of the MMC converter. Due to the inclusion of many submodules, the effective switching time and therefore the effective bandwidth of the system is increased without compromising the system's efficiency. This allows the current controller in an MMC configuration to be tuned to have ahigher bandwidth than the conventional Voltage Source Converters.

According to the above, the bandwidth of the controller can then be selected based on 3.8:

$$\frac{\ln(9)}{t_r} < bw < \frac{\omega_{samp}}{10} \tag{3.8}$$

For this system the minimum desired rise time can be selected to be 1 ms which gives rise to a bandwidth $bw = 2200\ \frac{rad}{s}$ which at the same time respects Equation 3.7. Based on the above, the proportional gain can be selected according to Equation 3.5.

The only thing left at this point is the selection of the resonant time constant T_r, which should minimize the tracking errors without deteriorating the stability of the system. The closed loop transfer function, including the resonant controller, after proper manipulations can be brought to the following form:

$$G_{cl}(s) = \frac{2K_p}{L_{arm}} \cdot \frac{s^2 + \frac{1}{T_r}\cdot s + \omega_1^2}{(s + 2\frac{K_p}{L_{arm}})\cdot(s^2 + \frac{1}{T_r}\cdot s + \omega_1^2) - \frac{s^2}{T_r}} \tag{3.9}$$

The above equation reduces to Equation 3.4 when $T_r \rightarrow \infty$. However, a big value would result in a very slow tracking of the static errors that the resonant part aims to eliminate. It can be proven useful to associate the time constant of the resonant part with the fundamental frequency that it is controlling. In this way, a generic and consistent way to tune all the resonant controllers can be deduced. Throughout this report, the resonant time constant will be taken according to Equation 3.10.

$$T_r = \frac{\pi}{h \cdot \omega_1} \tag{3.10}$$

To conclude, the bode plot of the complete open loop system, including the delay, before and after the inclusion of the resonant part are depicted in Figure 3.5. The phase margin of the loop without and with the resonant controller can also be depicted. It can be deduced that the inclusion of the resonant controller with the specified gain does not deteriorate the stability of the system.

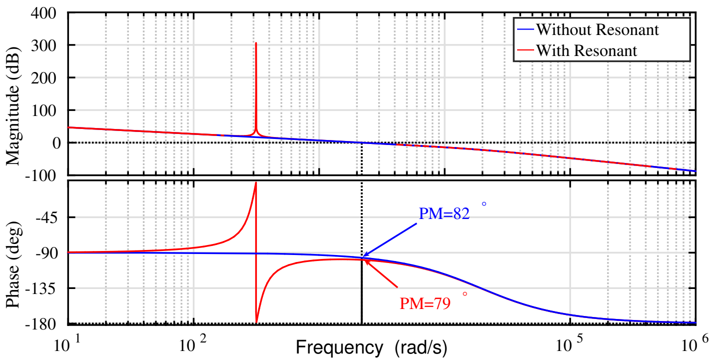

FIGURE 3.5: Output current controller open loop Bode plot.

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Finally, the performance of the output current controller in tracking down a sinusoidal reference is evaluated with simulations of the complete model. The reference of the current is changed at the time instance of 1 s from 0 to 20 A. It can be noticed that the dynamics are rather fast and the resonant part of the PR-controller minimizes the tracking error in approximately 50 ms.

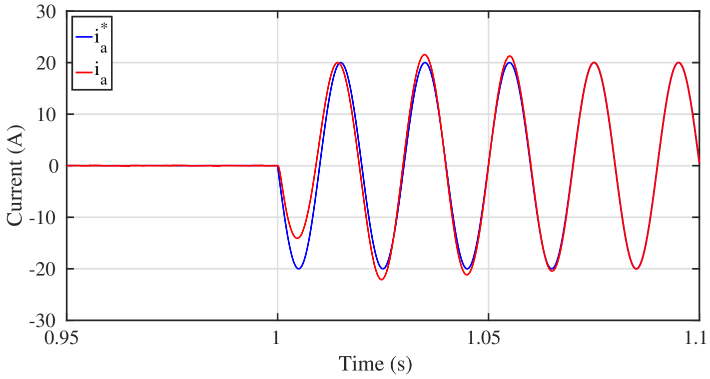

FIGURE 3.6: Output current controller response.

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3.3 Power Controllers

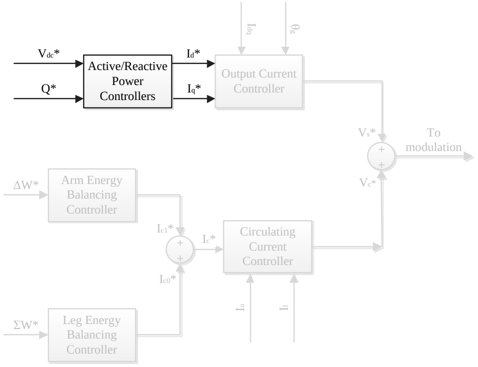

FIGURE 3.7: Active/Reactive Power Controllers.

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In this section, the active and reactive power controllers will be described. These controllers receive the reference active and reactive power that the STATCOM should provide to the grid and output the reference d and q current components that along with the angle that comes from the Phase Locked Loop (see Chapter 4), are fed to the output current controller. Due to the cascaded nature of the control system, basic control theory states that these controllers have to be tuned with a smaller bandwidth than the output current controller in order to not interact with it [25].

In the dq -synchronous frame system, the apparent power can be expressed as:

$$S = \frac{3}{2} \cdot (v_d + j \cdot v_q) \cdot (i_d - j \cdot i_q) \tag{3.11}$$

However, the PLL, as it will be described later on, aligns the vector with the dq-frame ensuring that the voltage vector is real and therefore setting its q-component to zero. In this way, the apparent power can be expressed as:

$$S = \frac{3}{2} \cdot v_d \cdot (i_d - j \cdot i_q) \tag{3.12}$$

As a consequence, the active and reactive power can be expressed as a function of the d and q current components:

$$\begin{cases} P = \frac{3}{2} \cdot v_d \cdot i_d \\ Q = -\frac{3}{2} \cdot v_d \cdot i_q \end{cases} \tag{3.13}$$

An inspection of the above shows that the d-component is responsible for the active power whereas the q-component is responsible for the reactive power. Furthermore, the current references can be simply generated in open loop by solving equations 3.13 for the d and q components respectively, assuming that P^* and Q^* are inputs of the system.

A small amount of active current needs to be drawn by the STATCOM to compensate for the unavoidable losses, giving rise to the i_d^*. In this application, due to the absence of a physical DC link, the aforementioned controller will be referred to from now on as pole-to-pole voltage controller. With C_{eq} being the equivalent pole-to-pole capacitor of the MMC, the power balance suggests:

$$\frac{\partial}{\partial t}(\frac{1}{2} \cdot C_{eq} \cdot V_{dc}^2) = \frac{3}{2} \cdot v_d \cdot i_d \tag{3.14}$$

C_{eq} is given by equation Equation 3.15, assuming that at every time instance the total number of submodules that are inserted is equal to N:

$$C_{eq} = \frac{3 \cdot C_{sm}}{N} \tag{3.15}$$

The pole-to-pole voltage controller is then shown in Figure 3.8. The plant function of the con-

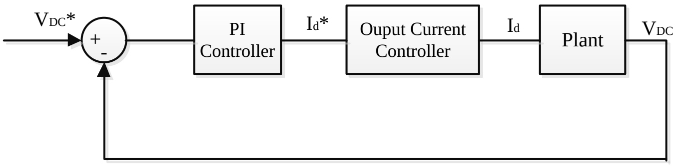

FIGURE 3.8: Pole-to-Pole Voltage Controller Loop.

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troller can be directly determined from the Laplace transformation of Equation 3.14:

$$\frac{V_{dc}}{i_d} = \frac{3 \cdot v_d}{2 \cdot V_{dc}} \cdot \frac{1}{C_{eq} \cdot s} \tag{3.16}$$

The system theoretically has a free integrator at the origin so there is no need for an integral part to eliminate the static errors. The stability of the pole-to-pole voltage is the first priority and therefore the controller need not be aggressive. The bandwidth of this controller is chosen to be tuned to have a small bandwidth in the region of 50 rad/s. In this way, it is ensured that there will be no interactions with the output current controller. It must be noted that the voltage v_d is generally not constant since it depends on the reactive power reference as noted in Equation A.2, but it can be assumed to be approximately equal to the peak of the phase voltage of the grid.

Taking into consideration all the above, the desired gain is found based on the root locus of the system. The open loop bode plot is then depicted below to prove the stability of the system. The theoretical settling time of the system was also found to be approximately 40 ms.

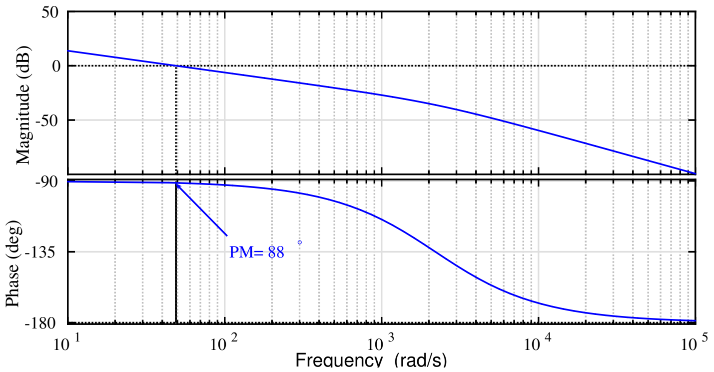

FIGURE 3.9: Pole-to-Pole voltage controller Open Loop Bode.

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Finally, a step change of 1% is applied in the pole-to-pole voltage at $t = 1s$, as shown in Figure 3.10 of the simulated system and the validity of the controller is evaluated. There are several things to notice in Figure 3.10. At first, the resulting step response exhibits small oscillations that arise probably due to the presence of the resonant parts of the output current loop. Moreover, the static errors are minimized due to the presence of the free integrator, despite the use of the P controller without the integral part. Finally, the step response is similar to the theoretically calculated, with the rise time being approximately 45 ms.

3.4 Circulating Current Controller

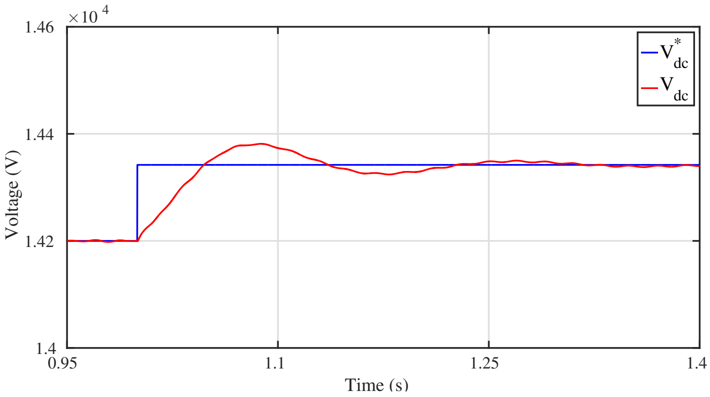

FIGURE 3.10: Pole-to-Pole Voltage controller Step Response.

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In this section the control of the circulating current will be presented. The circulating current is crucial for the efficient, balanced and reliable operation of the MMC since on the one hand, it needs to be suppressed in order to reduce the conduction losses of the power devices and on the other hand it is the mean to balance any unbalances introduced by internal (e.g impedance mismatches) or external (e.g. grid faults) causes and keep the voltage of the cell capacitors within their specified limits. In any other case, the efficiency of the system would drop along with its reliability since the voltage of the cell capacitors is also the blocking voltage of the power devices [26].

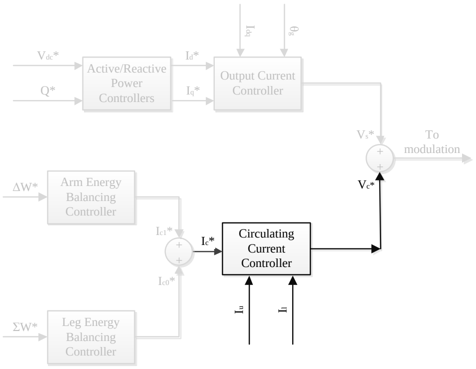

FIGURE 3.11: Circulating Current Controller.

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The circulating current was defined in Equation 2.4. In a STATCOM application, the DC component of this current should naturally be zero, since no active power is fed to the grid. The controller, as shown in Figure 3.11 takes the current reference from the energy balancing controllers and with a combination of compensators, uses the reference internal voltage that was described in the previous chapter as a mean to track down the aforementioned reference. However, the design of the controller is not straightforward, as the different components that the circulating current may present are not easily detected.

In section 2.2 the internal dynamics of the MMC were analyzed. The analysis of the difference between the upper and lower arm average power showed that a fundamental component of the circulating current could be used in order to exchange active power between each leg's arms. Similarly, the analysis for the sum of the energy of a leg has showed that a DC component can be utilized in order to redistribute the energy between the converter legs. Moreover, apart from the DC and fundamental components, the circulating current presents naturally a second order component as is derived analytically in Chapter 5 of the report at hand [15]. Therefore, the controller of the circulating current should include three parallel resonant parts. The corresponding block diagram is shown in Figure 3.12.

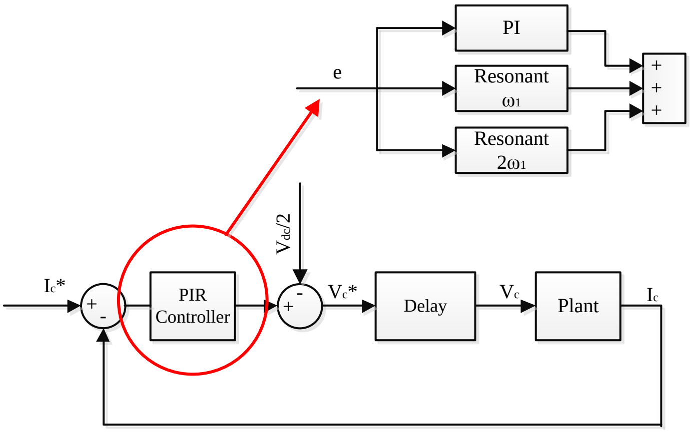

FIGURE 3.12: Circulating Current Controller Loop.

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An inspection of Equation 2.12 and 2.13 leads to the conclusion that the circulating current is being driven through an impedance with a resistive part of R_{arm} and an inductive part of L_{arm}, by the internal voltage v_c. If the term $\frac{V_{dc}}{2}$ is treated as a disturbance, the plant function is straightforward:

$$\frac{i_c}{v_c} = \frac{1}{L_{arm} \cdot s + R_{arm}} \tag{3.17}$$

The delay block that is depicted in Figure 3.12 was discussed in the previous section for the output current controller. Furthermore, the tuning method used for the output current controller can be followed for the circulating current controller as well, with the proportional term dominating the dynamics of the system while the integrators take care of the static errors in different frequencies. The circulating current controller can be tuned to be less aggressive than the output current controller, since its response is not as important for the system's performance. In this report, the bandwidth of the circulating current controller was selected for a rise time of 1.5 ms according to Equation 3.6.

The resonant controllers are tuned as described from Equation 3.10. In this way, the performance of all the parts in tracking down the reference is similar in terms of their respective periods. Since Equation 3.10 cannot be used for the DC part, it is tuned with the same gain as the fundamental part for simplicity.

The open loop bode plot of the complete system, including the associated delay and all the resonant parts is shown in Figure 3.13, in order to prove the stability of the circulating current controller.

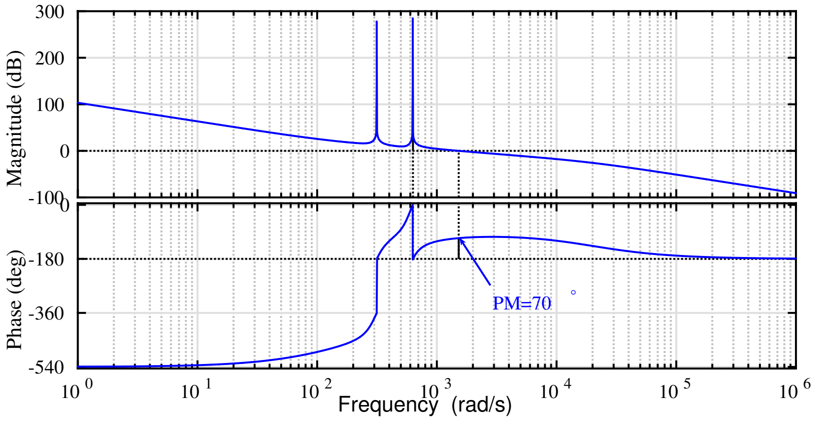

FIGURE 3.13: Circulating current controller open loop Bode plot.

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The performance of the controller in suppressing the circulating current under balanced conditions is depicted in Figure 3.14.

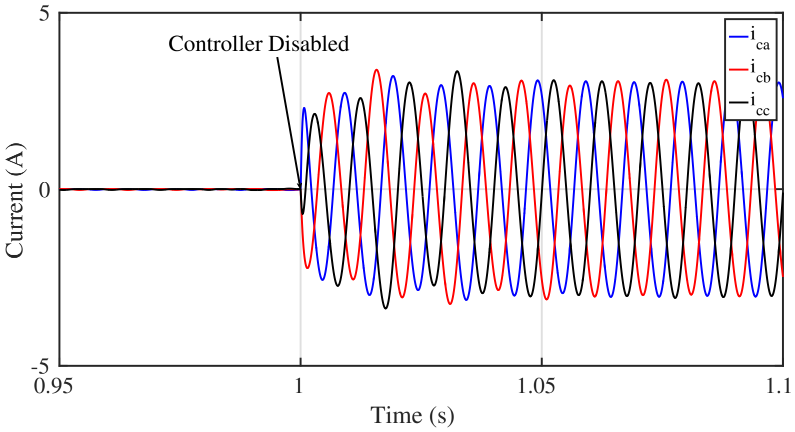

FIGURE 3.14: Circulating current controller - Suppression of second harmonic.

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The resonant part tuned at double the fundamental frequency is disabled at $t = 1s$, giving rise to a second order component. From this figure, the natural existence of the second order component in the circulating current is obvious, and it will be explained through analytical expressions in Chapter 5. It is also evident that under balanced conditions, the circulating current in STATCOM applications is zero, as noted before.

3.5 Arm Energy Balancing Controller

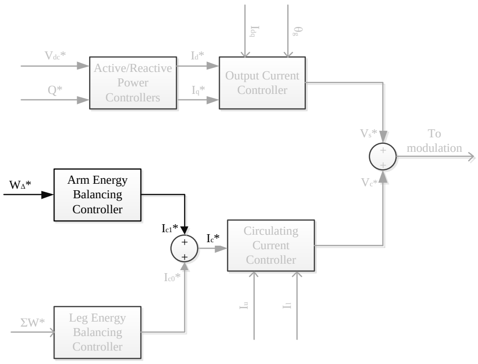

FIGURE 3.15: Arm Energy Balancing Controller.

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In this section, the arm energy balancing controller will be designed, implemented and its performance will be evaluated through simulations. As it is shown in Figure 3.15, the controller is taking the desired energy difference reference between the upper and the lower arm of each phase. It is clear that this difference in most cases will be set to zero, in order to achieve energy balance in between the arms of a converter leg. Under this condition and assuming that all the cell capacitances are identical, the energy balance will ensure that all the capacitors have the same average value. In other words, the arm balancing controller determines the value of the first harmonic of the circulating current that is needed in order to cancel any possible energy difference between the arms [15]. Finally, the circulating current controller generates the appropriate internal voltage reference that is fed to the modulation.

At this point Equation 2.25 will be revised. Neglecting for the time being the oscillating terms, and introducing the concept of energy difference, the equation can be rewritten as:

$$\frac{\partial W_\Delta}{\partial t} = -\hat{v}_1 \cdot \hat{i}_{c1} \cdot cos(\phi_c) \tag{3.18}$$

This equation states clearly that the first harmonic of the circulating current has to be in phase with the respective phase voltage in order to cause active power redistribution. The angle of the phase voltage however is known by the control system due to the action of the Phase Locked Loop (see Chapter 4). The complete closed loop of the arm energy balancing controller is shown in Figure 3.16. The dynamics of the circulating current controller are much faster than the outer arm

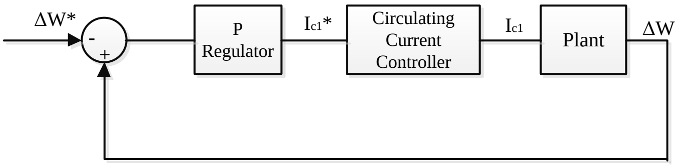

FIGURE 3.16: Arm Energy Balancing Controller Loop.

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balancing loop, so it can be assumed that the two controllers are independent from one another. Assuming that $cos(\phi_c) = 1$, the plant function of the controller can be directly determined by Equation 3.18:

$$\frac{W_\Delta}{\hat{i_{c1}}} = -\frac{\hat{v}_1}{s} \tag{3.19}$$

The closed loop transfer function of the circulating current controller was shown in the previous section and therefore it will be omitted hereby. The closed loop system contains a free integrator and therefore theoretically there is no need for the compensator to include a second one since the existent one should be capable of eliminating any possible steady state errors. A small integrator gain could be used however to eliminate small steady state errors in a realistic system [16].

The tuning of the P regulator will be based on the response and its stability. Since the arm energy controller is an outer loop, stability is the desired characteristic. A usual tuning technique that is used in these cases is based on the phase margin of the system. For this case, the phase margin is chosen to be 88° and the resulting settling time is approximately 30 ms. Revising again

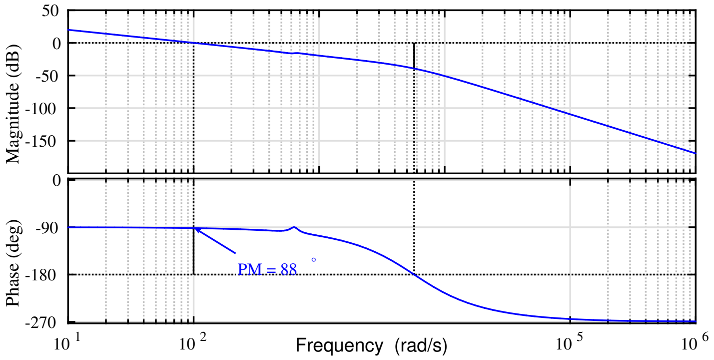

FIGURE 3.17: Arm energy balancing controller open loop bode.

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Equation 2.25, the energy difference between the upper and lower legs, naturally presents a large fundamental harmonic content and a relatively smaller second harmonic content. The average amount of differential energy is however what is important to be kept zero, so these terms were neglected in the analysis since they were not essential for the controller design. Nevertheless, a low pass filter (LPF) can be used in order to filter the measured differential energy as it is fed-back to the controller. However, the fundamental component is hard to be filtered effectively with an LPF. Two band-stop filters are connected in series instead, one tuned at $50Hz$ and one at $100Hz$. An ideal band-stop filter used in the simulations, in the Laplace domain follows the transfer function in Equation 3.20.

$$G_{BSF}(s) = \frac{s^2 + w_c^2}{s^2 + 2 \cdot w_c + w_c^2} \tag{3.20}$$

Moving on, a commonly disregarded issue, resulting from the usual implementation of the arm balancing controller is that injecting a fundamental active current in one phase, will affect the energy balancing of the other two legs. This means that the arm energy balancing controller cannot work independently for every phase if no action is taken. In [27], an arm energy balancing controller with the aforementioned problem was demonstrated. The controller did not ensure decoupled power flow as indicated in **Publication B**.

In contrast, the idea of a decoupled control was introduced in [28]. In this work, a way to decouple the problem by injecting a reactive current in the balanced phases, so that the average active power value stays unaffected, was presented. The control strategy used however is hard to be implemented, utilizing state space vectors.

At this point, a comprehensive and intuitive way to decouple the arm energy balancing controller is presented. This control method is easy to implement since it is based on basic vector theory. The idea however is the same with the one in [28], where the active current of one phase is combined with reactive currents in the other two phases in order for the arm balancing controller to be independent for each leg.

Due to the symmetry of the problem, only one case will be studied hereby, assuming that the arms of phase-a are unbalanced, so an active current in phase with phase-a voltage has to be injected in the circulating current. The reactive axes of phase-b and phase-c that could be combined to form a vector of phase-a are shown in the figure below. The reactive axis-b is named axis-qB- since it is shifted $-90°$ with respect to axis-b and the reactive axis-c is referred to as axis-qC+ since it is shifted $+90°$ with respect to axis-c. Due to the star configuration the three current vectors should have a sum of zero, and therefore form a triangular. The problem now becomes easy, since the only thing that needs to be determined is the magnitude of the vectors that should be applied. Based on basic trigonometry, the amplitude of the vectors of phase-b and phase-c are $\sqrt{3}$ times

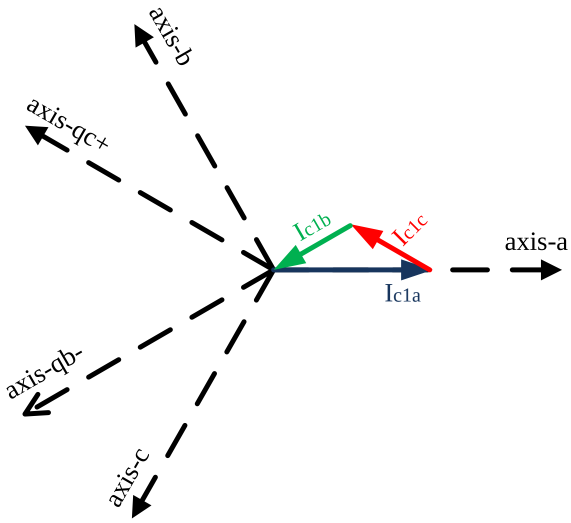

FIGURE 3.18: Arm energy balancing controller decoupling strategy.

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smaller than the vector of phase-a. In this way, the sum of the three imposed vectors is zero, but phase-a is getting active power whereas the other two phases are getting reactive power which does not shift the average of the capacitor voltages. The final commanded current reference for all phases assuming that a P-regulator is used, will be:

$$i^*_{c1_a} = K_p \cdot (e_a \cdot cos(\omega t) + \frac{1}{\sqrt{3}} \cdot e_b \cdot cos(\omega t + \frac{\pi}{2}) + \frac{1}{\sqrt{3}} \cdot e_c \cdot cos(\omega t - \frac{\pi}{2}) \tag{3.21}$$

$$i^*_{c1_b} = K_p \cdot (e_b \cdot cos(\omega t - \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} \cdot e_a \cdot cos(\omega t - \frac{7\pi}{6}) + \frac{1}{\sqrt{3}} \cdot e_c \cdot cos(\omega t - \frac{\pi}{6}) \tag{3.22}$$

$$i^*_{c1_c} = K_p \cdot (e_c \cdot cos(\omega t + \frac{2\pi}{3}) + \frac{1}{\sqrt{3}} \cdot e_a \cdot cos(\omega t + \frac{7\pi}{6}) + \frac{1}{\sqrt{3}} \cdot e_b \cdot cos(\omega t + \frac{\pi}{6}) \tag{3.23}$$

where e_a, e_b and e_c are the errors fed to the P-regulator of each phase.

Finally, the effectiveness of the proposed solution is evaluated through simulations. At first, an extreme and unrealistic test scenario is introduced where the upper arm of phase-a exhibits an impedance that is double the arm impedance of all the other arms. In this simulation, the upper arm of phase-a stores more energy than the lower, until the arm energy controller is introduced, as shown in Figure 3.19. The energy controller cancels the energy difference by moving active power from the upper leg to the lower leg bringing the system to balance, despite the extreme difference in the arm impedance.

Energy balance is translated into capacitor voltage balance. For an MMC system, it is crucial to keep the capacitor voltages balanced under all operating conditions. The following graph depicts

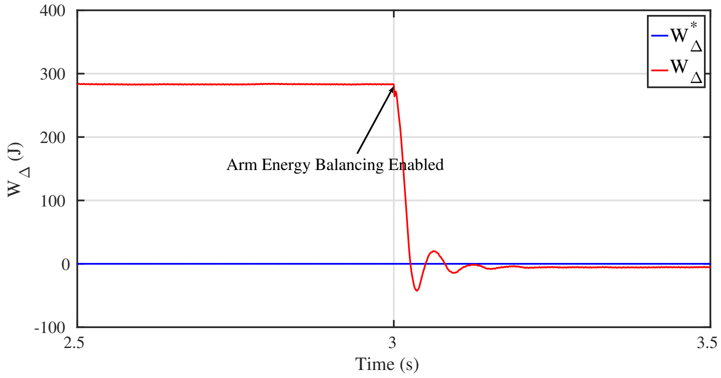

FIGURE 3.19: W_Δ under extreme internal unbalance.

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the instantaneous sum capacitor voltages, as well as the average sum capacitor voltages for phase-a, for the aforementioned test case scenario. It can be noted that the arm balancing controller acts by bringing the average sum capacitor voltage of the upper and lower leg to the desired value.

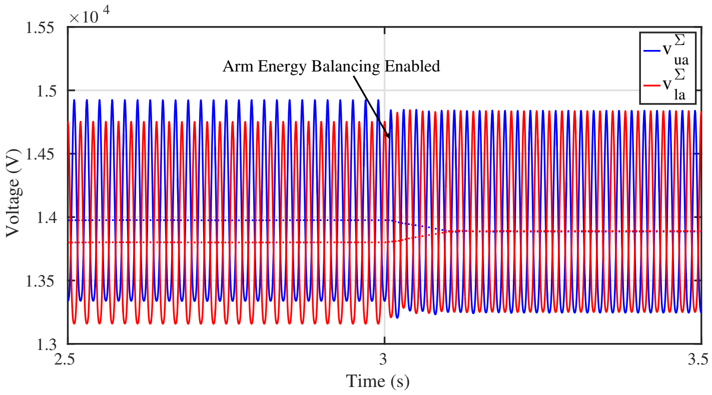

FIGURE 3.20: Phase-a sum capacitor voltages under extreme internal unbalance.

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Finally, the independent operation of the controller is proven hereby. In this simulation, a step change in the energy difference reference is applied for phase-a at the time instance of 1 s. The references of phase-b and phase-c remain however at zero. It can be depicted in Figure 3.21 that the arm energy controller reacts fast to the change in reference change, exhibiting a settling time of approximately 28 ms, which is also the theoretically calculated step response shown in the analysis before. A small overshoot is the result of the interaction between the various controllers of the system. It can be concluded that the other two phases are not affected by the generation of active power in phase-a since the controller forces the currents that are flowing in the legs of phase b and c to be purely reactive.

3.6 Leg Energy Balancing Controller

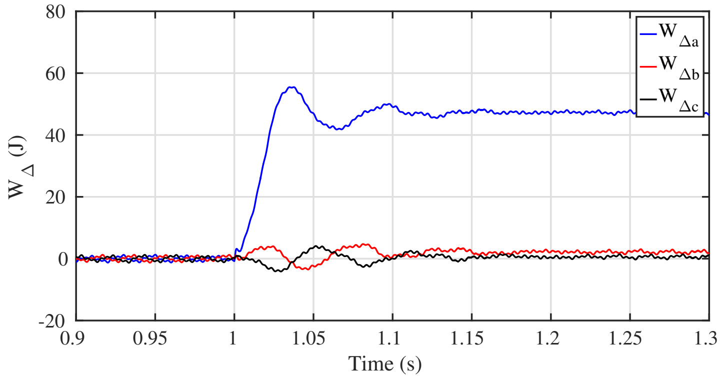

FIGURE 3.21: Arm energy balancing controller response under a step change in phase-a.

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In this section, energy balance between the three converter legs will be ensured through the use of the leg energy balancing controller that is highlighted in the figure on the right hand side. Having already ensured that the converter arms will be balanced, the energy balance between phase legs will make sure that the sum of the cell capacitor voltage will be the same for every phase. This controller is having as an input, the desired total stored energy, that can be easily calculated based on the total pole-to-pole voltage requirement. The total energy of the converter legs is measured and fed-back to the controller [29]. Assuming once again that all the capacitors are identical, energy balancing is translated into average voltage balancing, which is important for keeping the devices within their safe operational area.

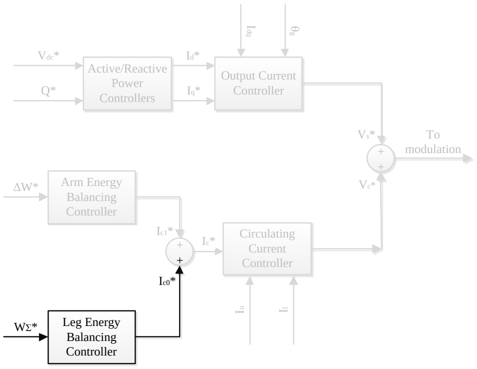

FIGURE 3.22: Leg Energy Balancing Controller.

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It is now time to revise Equation 2.23. Similarly to the arm balancing case, the oscillating terms are neglected for the time being and the concept of energy sum is introduced:

$$\frac{\partial W_{\Sigma}}{\partial t} = i_{c0} \cdot V_{dc} - \hat{v}_1 \cdot \hat{i}_1 \cdot cos(\phi_1) \tag{3.24}$$

The second term of the above equation is related to the energy that is flowing to the grid so it is not relevant with the internal dynamics of the converter system. However, the first term is a DC term that is related to the DC component of the circulating current. Based on this equation, it should be clear that the DC component of the circulating current is capable of exchanging active power between the legs of an MMC. As it was mentioned however before, the sum of the three instantaneous DC components of the circulating current should be zero. This means that the total energy stored in the converter legs can be redistributed between them in order to achieve energy balance, based on the injected DC component of the circulating current.

The DC component generated by the leg energy controller is fed to the circulating current controller that produces the appropriate internal voltage reference. The closed loop system diagram is shown in the schematic 3.23:

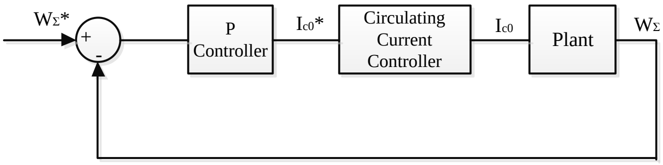

FIGURE 3.23: Leg Energy Balancing Controller Loop.

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The reference for the leg energy controller is the sum of the energy stored in the cell capacitors. The reference is calculated based on the equation below:

$$W_{\Sigma} = 2N \cdot \frac{1}{2} \cdot C_{sm} \cdot v_{sm}^2 \tag{3.25}$$

Since the leg balancing controller is an outer loop, it is tuned to have much slower dynamics in comparison to the circulating current controller. In this case, stability is the desired characteristic, so the tuning process will be based on the phase margin, just like the arm balancing controller. The plant function can be found by taking the Laplace transformation of Equation 3.24 and neglecting the term that is related to the output current:

$$\frac{W_{\Sigma}}{i_{c0}} = \frac{V_{dc}}{s} \tag{3.26}$$

Since the closed loop system has a free integrator, theoretically there is no need to include an integral part, so at this point the system will be tuned without one. However, in the realistic system, static errors are expected and a small integral part could be used in order to eliminate them [16]. The phase margin is set to 88° resulting in a rise time of approximately 30 ms. The bode diagram of the open loop system is depicted in Figure 3.24.

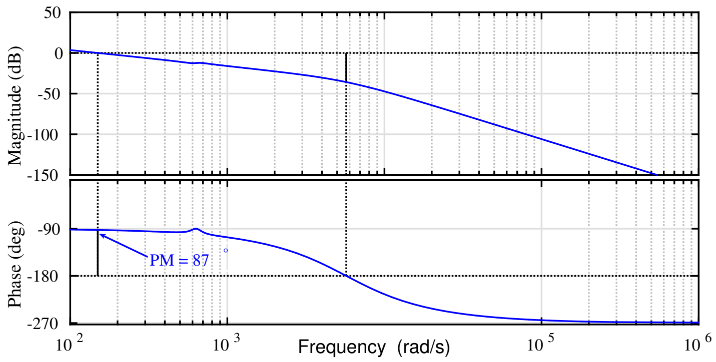

FIGURE 3.24: Leg energy balancing controller open loop bode.

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Revising Equation 2.23 once again, the neglected oscillating terms in the fundamental as well as in the second harmonic should be filtered out from the measured sum of the energy. The band-stop filters that were designed in the previous section are used in this part too.

Finally, the validity of the analysis is proven through simulation results, and the performance of the controller under leg unbalances is evaluated. Firstly, an extreme unbalance is introduced in the converter leg of phase-a. The impedance of each arm of phase-a is doubled, and the leg balancing controller is enabled at the time instance of 1.5s. Figure 3.25 depicts the total energy in the leg of phase-a: The impedance difference, causes phase-a to store more energy than the other

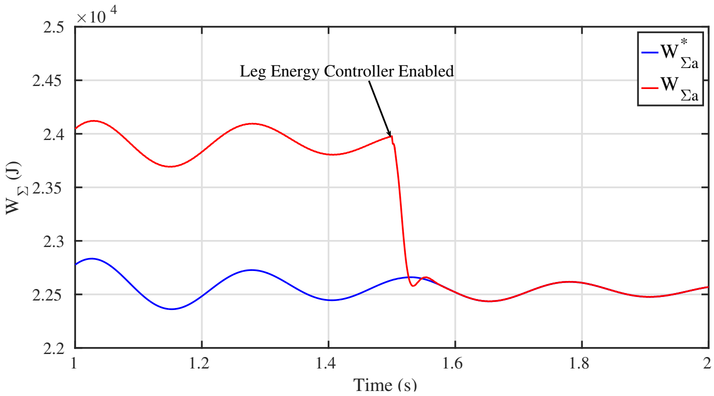

FIGURE 3.25: W_Σ under extreme internal unbalance in phase-a.

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two phases. When the leg balancing controller is introduced, the total leg energy of phase-a is brought to the calculated reference level. Figure 3.26 shows the sum of the capacitor voltages of the upper and lower arm of each leg, as well as their average value. Finally, as in the arm energy balancing controller case, the step response of the leg energy controller is assessed. In this simulation, phase-a at the time instance of 1.5 s is receiving a $+1000$ J command, whereas the other two phases a -500 J. The final result is plotted in Figure 3.27. As can be depicted in this figure, the rise time of the energy is around 27 ms, close to its theoretically calculated value.

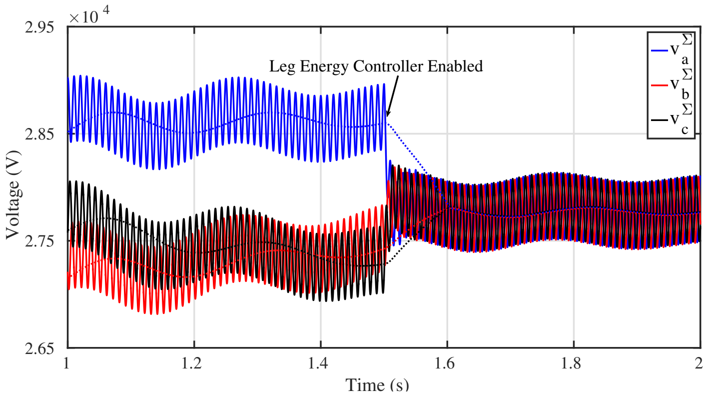

FIGURE 3.26: Sum capacitor voltages under extreme internal unbalance in phase a.

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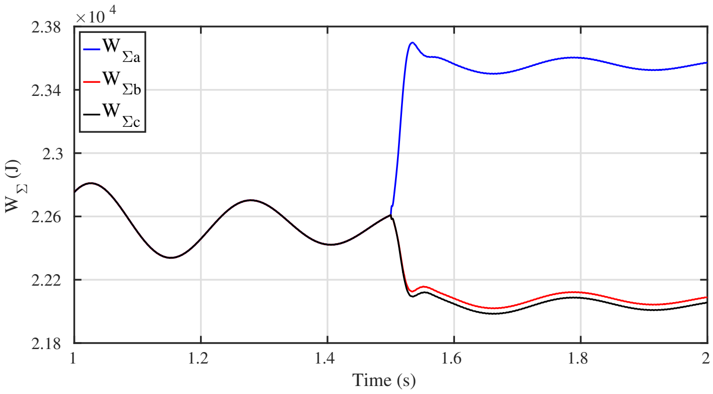

FIGURE 3.27: Leg energy balancing controller response under step change.

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Chapter 4

Control Strategies under External Unbalanced Conditions

Until now, the grid three-phase voltages were considered to be ideal in this report. However, asymmetrical conditions can arise in power grids either due to faults (line-to-ground fault, line-to-line fault etc.) or due to the sudden connection of asymmetrical loads that could cause temporary voltage sags in one phase (asymmetrical) or in all three phases (symmetrical). The effect of these voltage perturbations can be important since they could cause malfunction of the devices connected to the PCC and as a result economic losses [30].

Grid connected converters are known to be sensitive to external voltage disturbances since their control system's performance may deteriorate under distorted operating conditions. A STATCOM needs to not only ride through these faults without tripping but also be utilized in order to provide voltage support by injecting reactive power, reducing the possibility of a voltage collapse [31].

In this chapter, the Phased Locked Loop (PLL) will be designed and a way to extract the different symmetrical components (the foundations of the symmetrical components theory can be found in Appendix B) will be presented. After this, two injection strategies during asymmetrical grid faults will be discussed and their effectiveness will be demonstrated through simulation results.

4.1 Positive-Negative Sequence Extraction Method and Phase Locked Loop

The analysis of the Phase Locked Loop (PLL) and its tuning procedure has not been discussed intentionally up until this point, despite the fact that it is a fundamental part of the control system. The grid frequency, the voltage amplitude as well as the angle of the voltage space vector are crucial for the control system and have to be properly determined. Furthermore, as shown in Appendix B, unbalanced conditions can cause the emergence of negative sequence components in the system. For this reason, an extraction method based on a Double Second Order General Integrator (DSOGI) as discussed in [32], will be presented and the positive and negative components of the PCC voltage will be identified. Then, the PLL is tuned appropriately locking the output angle on the positive sequence voltage component.

At first it should be clear that Clarke's transformation can be used in both positive and negative sequence components without modifications, since it is not dependent on the direction of the rotational space vector. The voltage transformation from abc-frame to $\alpha\beta$-frame is depicted hereby:

$$\begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} = \underbrace{\frac{1}{\sqrt{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}}_{T_{\alpha\beta}} \cdot \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{4.1}$$

The positive and negative sequence $\alpha\beta$ voltage components can be expressed as:

$$\begin{cases} V_{\alpha\beta}^{+} = [T_{\alpha\beta}] \cdot [T_p] \cdot V_{abc} \\ V_{\alpha\beta}^{-} = [T_{\alpha\beta}] \cdot [T_n] \cdot V_{abc} \end{cases} \tag{4.2}$$

where $[T_p]$ and $[T_n]$ are matrices defined in Appendix B. After manipulations and matrix operations:

$$\begin{bmatrix} \vec{V}_\alpha^{+} \\ \vec{V}_\beta^{+} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & -\alpha_\perp \\ \alpha_\perp & 1 \end{bmatrix} \begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} \tag{4.3}$$

where $\alpha_\perp = 1\angle - \frac{pi}{2}$ which is an operator used to facilitate the expression of a quadrature signal. Similarly, the negative sequence components are expressed as:

$$\begin{bmatrix} \vec{V}_\alpha^{-} \\ \vec{V}_\beta^{-} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} 1 & \alpha_\perp \\ -\alpha_\perp & 1 \end{bmatrix} \begin{bmatrix} \vec{V}_\alpha \\ \vec{V}_\beta \end{bmatrix} \tag{4.4}$$

Examining carefully the above equations, it can be deduced that the extraction of the positive and negative sequence components, requires the generation of signals in quadrature to the α and β components of the measured PCC voltage. A simple method was presented in [32], utilizing two Second Order General Integrators with quadrature signal generating capability as signified in Figure 4.1. SOGI generally acts as a bandpass filter, tuned in the frequency of interest. In Figure 4.1,

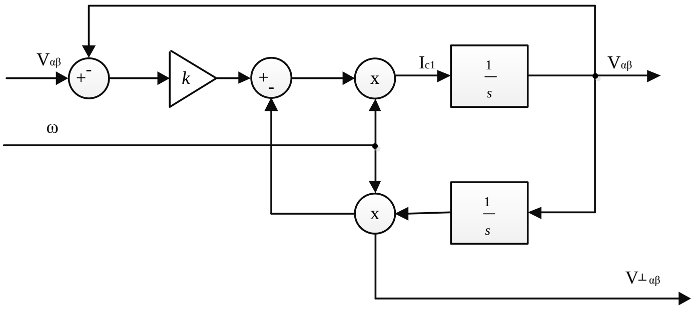

FIGURE 4.1: DSOGI with quadrature signal generation capability.

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ω is the fundamental frequency. In this way, any possible disturbances or harmonic components resulting from the grid side can be attenuated. The gain k is representing the bandwidth of the filter. The choice of this gain is a trade-off between filtering ability and response time. More about bandpass filters and their tuning procedure are discussed in Chapter 5. At this point, an optimum bandwidth gain is used as derived in [33] with the gain chosen to be $k = \sqrt{2}$. The overall extraction method for positive and negative sequence components is shown in Figure 4.2..

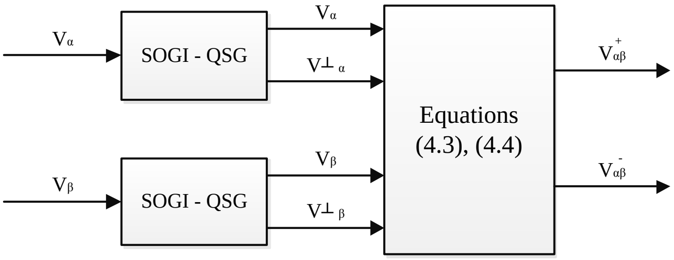

FIGURE 4.2: Positive-Negative Sequence Extraction method.

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The positive sequence of the $\alpha\beta$ voltage is then provided as an input to the PLL, which locks the angle of the positive sequence space vector. In this way, if the angle at the output of the PLL is used in the dq-transformations, the q-component of the positive sequence would be set to zero, verifying the assumptions taken in the power definitions of Chapter 3. The PLL's loop is shown in Figure 4.3. At first, the signal $sin(\gamma-\theta)$ is constructed based on Equation 4.5, where γ represents

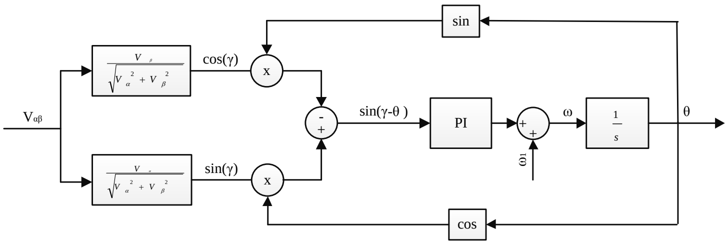

FIGURE 4.3: The Phase Locked Loop (PLL).

the desired reference angle and θ is angle at the output of the PLL.

$$sin(\gamma-\theta) = sin(\gamma)\cdot cos(\theta) - cos(\gamma)\cdot sin(\theta) \tag{4.5}$$

When this angle difference is small, then its sinus is close to zero so the assumption in Equation 4.6 can be taken:

$$sin(\gamma-\theta) \simeq \gamma-\theta \tag{4.6}$$

This angle difference is treated as the error that is fed to the PI controller. Since the plant contains a free integrator as shown in Figure 4.3, a P controller would be sufficient in tracking a constant phase angle. However, the angle is increasing linearly when a mismatch of frequencies exists and therefore a second integrator is needed. If the effect of the SOGI parts is neglected, then the closed loop transfer function can be derived as:

$$G_{PLL} = \frac{K_p\cdot s + K_i}{s^2 + K_p\cdot s + K_i} \tag{4.7}$$

The proportional gain is what defines the dynamics of the system. A high K_p, which acts as a bandwidth, may result in amplification of parasitic components. Usually the proportional gain is therefore chosen to be smaller than the fundamental frequency. In this report, the choice will be based on the settling time. Basic control theory suggests that a second order system the time constant is [25]:

$$\tau = \zeta\cdot\omega_n \tag{4.8}$$

Assuming that the system settles after 5 time constants and taking a settling time of 100 ms (five fundamental periods), the proportional gain is found. The integral gain can be chosen based on the maximum overshoot.

The effectiveness of the tuning procedure of the PLL is shown with a simple step response of $1Hz$ in Figure 4.4. The rise time is approximately 20 ms with the settling time being approximately $95ms$, close to the expected one.

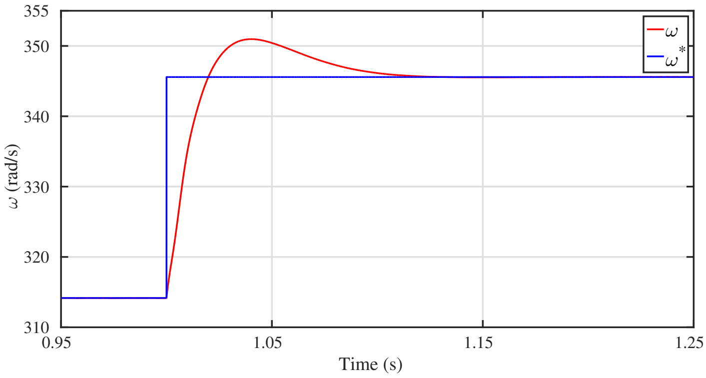

FIGURE 4.4: Step response of the PLL.

4.2 Control of Negative Sequence Reactive Power

Modern STATCOMs are required to control both the positive as well as the negative sequence reactive power due to the fact that many asymmetrical loads, such as arc furnaces, generate unbalanced currents [17]. One of the great advantages of the DS-HB STATCOM configuration is the fact that it can be used to control the negative sequence current without significant increase in the circulating current as explained in detail in **Publication A**. This ability will be highlighted through simulation results in this section.

Since the control of the output current was implemented in the *abc*-stationary frame with resonant parts, there is no need for changes in the control system as the resonant part will track down the $50Hz$ component regardless of the sequence of the phases [34]. The presence of unbalances results in active power oscillations that affect the V_{dc}, leading to oscillations with double the fundamental frequency.

Figure 4.5 depicts the current waveforms when 1pu of negative sequence reactive power is controlled.

I is shown that phase-c is leading phase-b by 120°. Figure 4.6 shows the phase voltages at the PCC, as well as the amplitude of the positive and negative sequence voltage space vector, as extracted based on the methods discussed in the previous section.

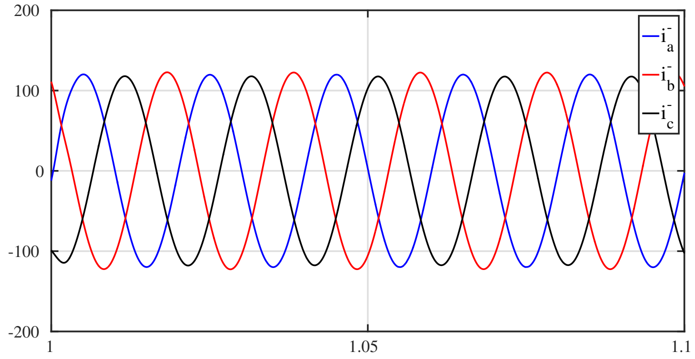

FIGURE 4.5: Output Currents with 1pu Negative Sequence Reactive Power.

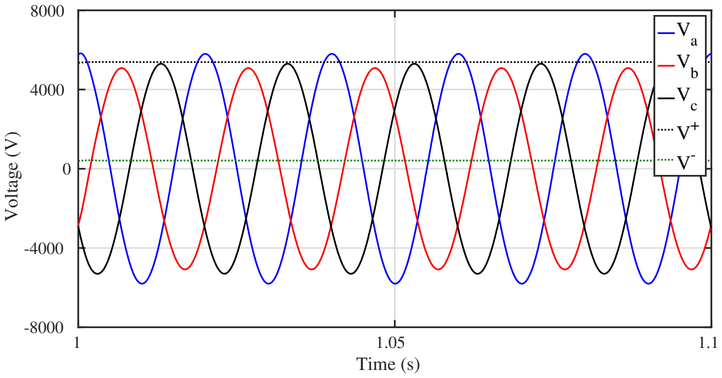

FIGURE 4.6: PCC Voltages with 1pu Negative Sequence Reactive Power.

The circulating currents of the three phases are shown in Figure 4.7. It can be deduced that a small DC component (20A) is used in order to control the full negative sequence, as expected. It can also be noticed that there is active power exchange between the leg of phase-c and the leg of phase-b, while the DC circulating current of phase-a is zero [35].

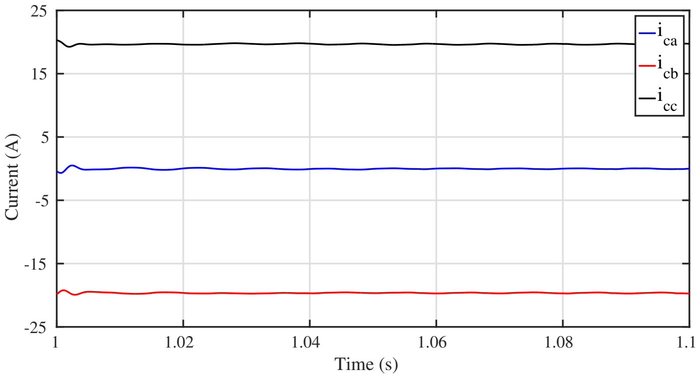

FIGURE 4.7: Circulating Currents with 1pu Negative Sequence Reactive Power.

Finally, Figure 4.8 verifies that the system remains balanced when the full negative sequence reactive power is controlled. The unbalanced currents result in different amplitudes in the voltage

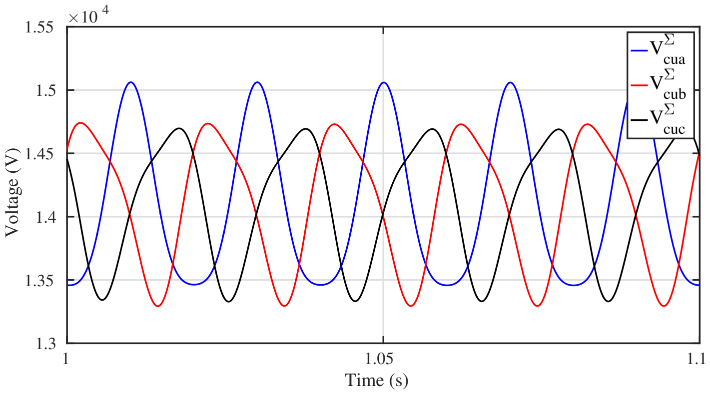

FIGURE 4.8: v^{Σ}_{cu} with 1pu negative sequence reactive power.

oscillations of the capacitors, but the mean value remains constant and equal to the mean value of the other phases.

4.3 Reactive Power Control for Voltage Sag Mitigation

Grid faults arise often in power systems and they can degrade the performance of the topology causing equipment failures and economic losses. Grid regulations usually do not have requirements for STATCOMs when faults in the AC side arise. However, a STATCOM can be utilized in order to support the grid voltage or enhance the stability of the system depending on its ratings and the strategy of injection. Various strategies exist and were explained in detail in [30].

In this section, two strategies will be discussed, both of them having as a main goal the support of the voltage at the PCC. The first strategy will inject maximum reactive current in positive sequence, respecting always the current ratings of the converter and increasing equally each phase voltage whereas the second strategy will provide more flexibility by the injection of positive and negative sequence currents.

4.3.1 Positive Sequence Injection

According to the instantaneous power theory [36], the presence of negative sequence components leads to active and reactive power oscillations with a double fundamental frequency component. The instantaneous active and reactive power can be expressed with the following set of equations [37]:

$$\begin{cases} p = P_0 + \hat{P}_1 cos(2\omega t) + \hat{P}_2 sin(2\omega t) \\ q = Q_0 + \hat{Q}_1 cos(2\omega t) + \hat{Q}_2 sin(2\omega t) \end{cases} \tag{4.9}$$

Applying the dq-transformations and taking into consideration both the positive and the negative sequence components, the power terms can be written in matrix form as follows:

$$\begin{bmatrix} P_0 \\ \hat{P}_1 \\ \hat{P}_2 \\ Q_0 \\ \hat{Q}_1 \\ \hat{Q}_2 \end{bmatrix} = \frac{3}{2} \begin{bmatrix} V_d^+ & V_q^+ & V_d^- & V_q^- \\ V_d^- & V_q^- & V_d^+ & V_q^+ \\ V_q^- & -V_d^- & -V_q^+ & V_d^+ \\ V_q^+ & -V_d^+ & V_q^- & -V_d^- \\ V_q^- & -V_d^- & V_q^+ & -V_d^+ \\ -V_d^- & -V_q^- & V_d^+ & V_q^+ \end{bmatrix} \begin{bmatrix} i_d^+ \\ i_q^+ \\ i_d^- \\ i_q^- \end{bmatrix} \tag{4.10}$$

Equation 4.10, suggests that there are six power terms to be controlled but only four independent variables. The problem then becomes a designer's choice. Many injection strategies have been developed and tested according to the needs of the power system, and in [30], an in-depth description and comparison was made while a flexible injection strategy was also developed.

Among the findings of the analysis was that despite the fact that a balanced positive sequence injection of currents does not mitigate the power oscillations, it allows for maximum reactive current injection and therefore maximum voltage support at the PCC. The reactive power reference after the detection of the fault will be the maximum possible, taking into consideration the current ratings of the converter system.

The maximum reactive power that the STATCOM can provide is given by Equation 4.11, assuming that the PLL is locked on the positive sequence d-component ($V_q^+ = 0$):

$$Q_{max}^* = \frac{3}{2} I_{max} \cdot V_d^+ \tag{4.11}$$

The maximum current I_{max} depends on the ratings of the converter system. When a voltage dip or a ground fault occurs, V_d^+ is reduced and therefore the maximum reference reactive power should be reduced in order for the current to respect its ratings. Based on the above, the current command will be purely in positive sequence with the i_d^+ generated from the pole-to-pole voltage controller and the i_q^+ generated based on Equation 4.11. In the following simulations, the fault duration will be assumed to be $300ms$ and a dead-band of 10% in the voltage is considered as proposed in [38]. The reactive power command is considered to be $0Var$ before the fault occurs.

Starting from a symmetrical voltage sag scenario, a reduction of 20% in all three phases of the system occurs at $t = 1s$. Figure 4.9 depicts the phase voltages before and after the three phase dip. It can be seen that since the dip is symmetrical, there is no negative sequence voltage while the positive sequence voltage rises from $0.8pu$ to $0.87pu$ approximately due to the injection of reactive power. Figure 4.10 verifies that the injection strategy does not result in currents higher than the rated ones. The current waveforms surpass the limits only during the transient as the PLL has not settled at the initial periods after the occurrence of the fault.

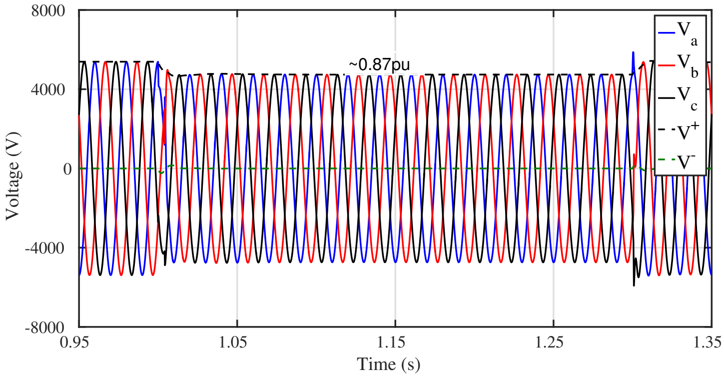

FIGURE 4.9: Symmetrical three-phase sag of 0.2pu - PCC voltages.

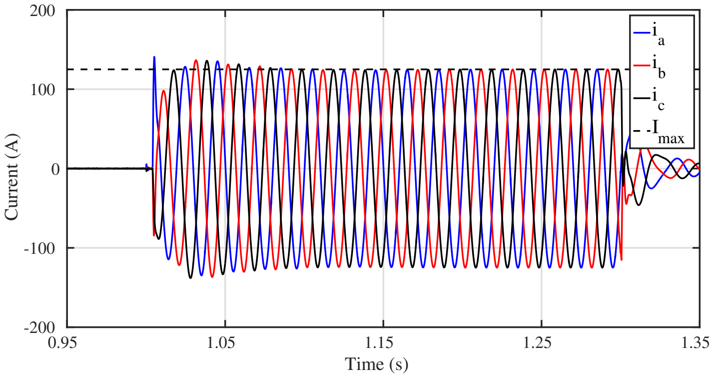

FIGURE 4.10: Symmetrical three-phase sag of 0.2pu - Line currents.

Figure 4.11, depicts the instantaneous active and reactive power provided to the grid. The power terms exhibit only average terms, as expected since there is no negative sequence present. It should also be highlighted that the maximum injected reactive power is less than the rated $1MVA$. In Figures 4.12, the internal balance of the MMC during this symmetrical fault is verified. More particularly, Figure 4.12 depicts the circulating current during the voltage sag and it can be seen that after the initial transient, it is suppressed to zero until the fault is cleared. The sum capacitor voltages of the upper leg is also depicted verifying that their average voltage remains constant.

The performance of the strategy is also tested in an asymmetrical single line-to-ground fault in phase-a, which is considered as the worst case scenario in grid applications. At first, the phase voltages at the PCC are depicted in Figure 4.13, where a significant amount of negative sequence voltage component is present, resulting in unbalances in the PCC voltages. The balanced injection

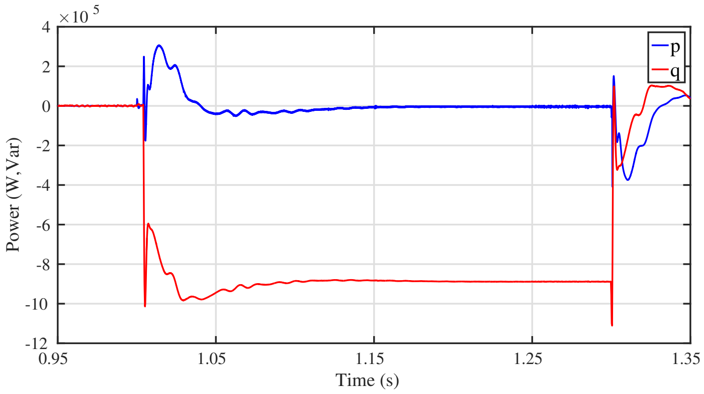

FIGURE 4.11: Symmetrical three-phase sag of 0.2pu - Active and reactive power.

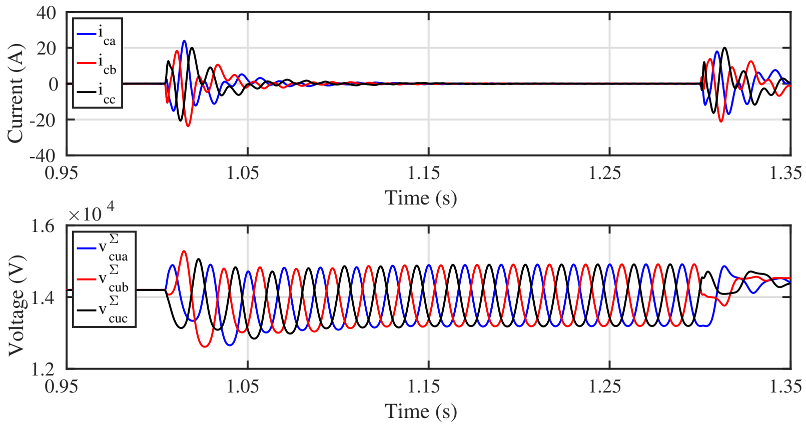

FIGURE 4.12: Symmetrical three-phase sag of 0.2pu - i_c and v_{uc}^{Σ}.

increases the voltage amplitude of all phases equally. Figure 4.14 verifies that with this method, the currents are symmetrical, balanced and inside their rated limits.

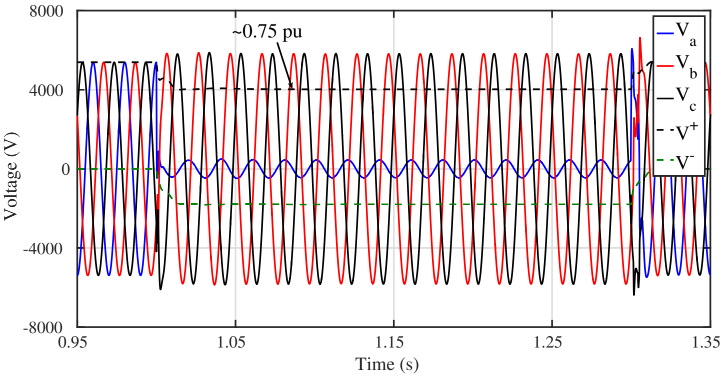

FIGURE 4.13: Single line-to-ground fault - PCC voltages.

Figure 4.15 depicts the active and reactive power. It can be seen that the existence of a high negative sequence component leads to huge oscillations in the active and reactive power, as this method fails to mitigate the issue, since it does not reduce the presence of the negative sequence voltage vector.

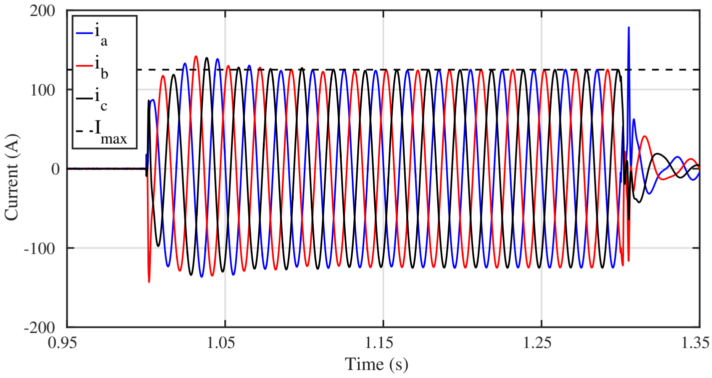

FIGURE 4.14: Single line-to-ground fault - Line currents.

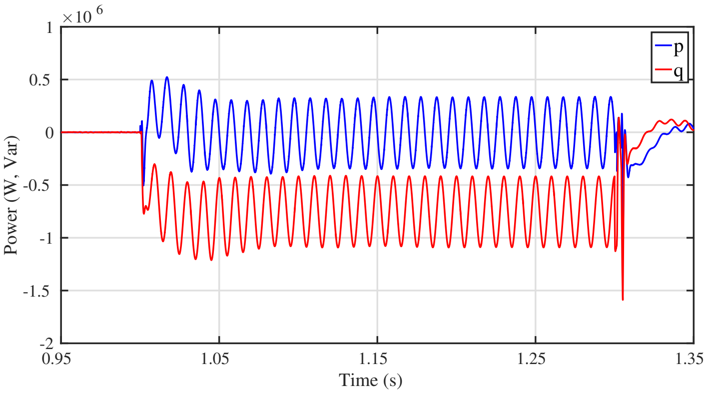

FIGURE 4.15: Single line-to-ground fault - Active and Reactive Power.

The internal balance of the MMC configuration is depicted again in Figure 4.16. The mean value of the capacitor voltages remains constant due to the existence of a dc circulating current, that arise due to the presence of the negative sequence voltage vector. An exchange of active power can be noticed between the two "healthy" phases.

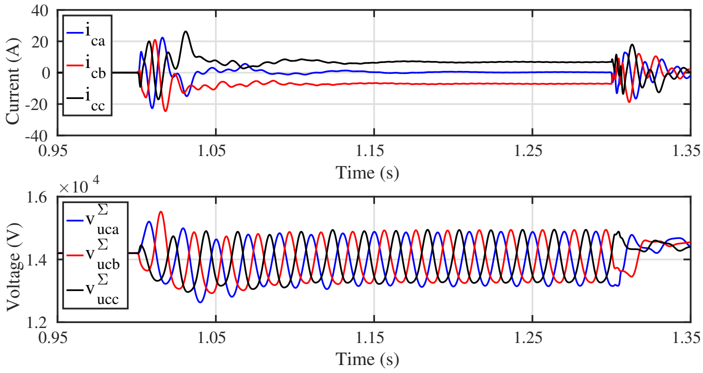

FIGURE 4.16: Single line-to-ground - i_c and v^{Σ}_{uc} with energy controllers.

To conclude, in order to stress out the importance of the energy balancing controllers in keeping the system balanced under asymmetrical grid faults, Figure 4.17 shows the circulating current and arm capacitor voltages when the energy controllers are disabled. it can be seen that the capacitor voltages are drifting away from their commanded average value. This result is unacceptable since it would lead to the disconnection of the converter due to the over-voltage experienced by the submodules of phase-b in this simulated case.

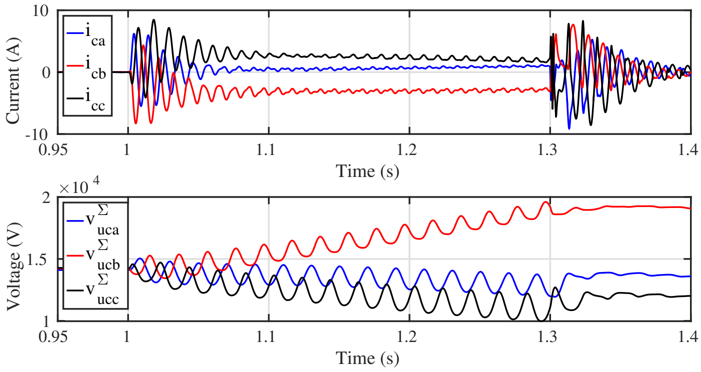

FIGURE 4.17: Line to ground fault - i_c and v^{Σ}_{uc} without energy controllers.

4.3.2 Mixed Sequence Injection respecting Phase Voltage Limits

In case of voltage sags it is very important for a STATCOM to manage to keep the voltages of all individual phases within their specified limits. The required voltage at the PCC however depends on the application. The requirements for this report will be chosen to be as follows [39]:

$$\begin{cases} V_{max} = 1.1\text{p}u \\ V_{min} = 0.85\text{p}u \end{cases} \tag{4.12}$$

As it was shown in the previous section, the balanced positive sequence injection increases the amplitude of all phases equally. This however may have severe effects for the "healthy" phases in the case of asymmetrical faults and could possibly affect sensitive equipment that is connected at that point. This problem can be noticed in Figure 4.18. In this figure, maximum positive sequence injection is considered for a system, with a two times higher $\frac{X}{R}$ ratio than the previously studied one. In this case an asymmetrical sag in phase-a (0.7 pu) and phase-b (0.8 pu) occurs, while phase-c is unaffected. The positive sequence injection restores the positive sequence of the voltage at 1 pu as it was before the occurrence of the fault while increasing the amplitude of phase-a to the minimum acceptable level of 0.85 pu. However, the magnitude of phase-c increases unacceptably to approximately 1.16 pu.

The example above shows that a more analytic approach could prove to be beneficiary for voltage sag mitigation, respecting the voltage limits as they were previously set. The injection approach

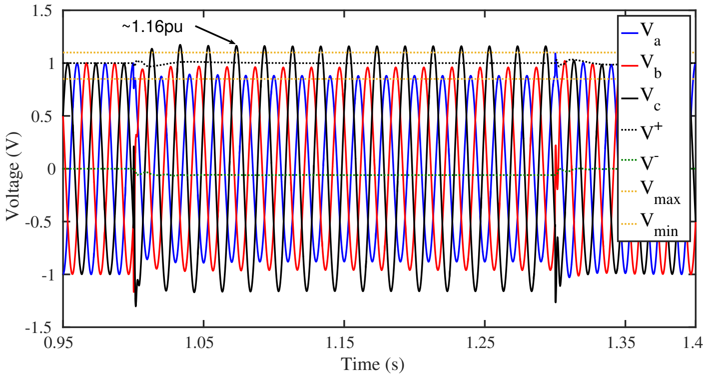

FIGURE 4.18: Asymmetrical voltage sag - Positive sequence injection.

that will be followed in this report was firstly introduced in [39] and it is reformed in this section in order to take into consideration the effect of the zero sequence component of the voltage.

Due to the action of the PLL, the voltage vector of the positive sequence is locked on the d-axis as previously described as in Equation 4.13. As a result the phase angle of the positive sequence voltage vector is considered to be $\phi^+ = 0$.

$$V^+ = \sqrt{V_d^{+2} + V_q^{+2}} = V_d^+ \tag{4.13}$$

Similarly, the magnitude and the phase angle of the negative sequence component can be calculated as shown in Equations 4.14 and 4.15. The extraction of the d and q components of the negative sequence voltage vectors were described previously.

$$V^- = \sqrt{V_d^{-2} + V_q^{-2}} \tag{4.14}$$

$$\phi^- = \tan^{-1} \frac{V_q^-}{V_d^-} \tag{4.15}$$

It is important at this point to understand the concept of voltage support and how the injection of positive and negative sequence current increases the voltage at the PCC. In order to do so, the schematic of Figure A.1 is considered and the positive sequence voltage at the grid side can be calculated as:

$$V_g^+ = V^+ - \omega \cdot L \cdot I^+ \tag{4.16}$$

This equation reveals that the injection of a positive sequence current, results in a voltage at the PCC that is higher than the voltage of the grid side and as a result the voltage sag is reduced. Similarly, for the negative sequence component:

$$V_g^- = V^- + \omega \cdot L \cdot I^- \tag{4.17}$$

Equation 4.17 reveals that the injection of negative sequence current, reduces the negative sequence voltage at the PCC that as a result reduces the unbalance between the phase voltages at the PCC in comparison to the one at the grid.

The positive and negative sequence reactive power can then be calculated as:

$$Q^+ = \frac{3}{2} \cdot \frac{V^+(V^+ - V_g^+)}{\omega L} \tag{4.18}$$

$$Q^- = \frac{3}{2} \cdot \frac{V^-(V_g^+ - V^-)}{\omega L} \tag{4.19}$$

The current references can then be extracted from Equation 4.20.

$$\begin{cases} I^+ = \frac{2}{3}\frac{Q^+}{V^+} \\ \\ I^- = \frac{2}{3}\frac{Q^-}{V^-} \end{cases} \tag{4.20}$$

The phase voltage with the maximum amplitude and the one with the minimum one have to be identified firstly and then their references will be set to the maximum and minimum limits that were defined in Equation 4.12. The phase voltage vectors can be expressed as a combination of the positive, negative and zero sequence components as shown in Appendix B. Given that the reference angle is considered to be the angle of the d-component of the voltage, the amplitudes of the voltages can be expressed as follows:

$$V_a = V^+ + V^- \cos\phi^- + V_0 \cos\theta_0 \tag{4.21}$$

$$V_b = V^+ + V^- \cos(\frac{2\pi}{3} + \phi^-) + V_0 \cos(\frac{2\pi}{3} - \theta_0) \tag{4.22}$$

$$V_c = V^+ + V^- \cos(\frac{4\pi}{3} + \phi^-) + V_0 \cos(\frac{4\pi}{3} - \theta_0) \tag{4.23}$$

The zero component is generally a rotating vector that is similar for all phases. Its magnitude and its angle are determined as shown in Figure 4.19. The input of the SOGI is the instantaneous value of the zero component. The SOGI generates a voltage component that is exactly the same as the input and one that is lagging 90°. This is then transformed to dq-reference frame with the feedback angle of a PLL that locates the angle of the d-component of the zero sequence component. Finally, the angle θ_0 is the difference of the reference angle of the system with the PLL's output angle. The magnitude of the zero sequence component is calculated based on Equation 4.24:

$$|V_0| = \sqrt{{v_0}^2 + {v_0^\perp}^2} \tag{4.24}$$

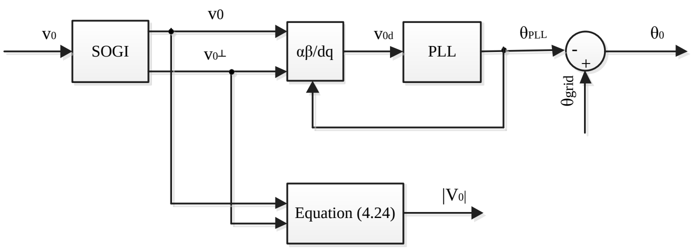

FIGURE 4.19: Zero Component Detection.

Since all the components of equations (4.21) - (4.23) are determined, the phases with the maximum and the minimum amplitude can be found. The references for the positive and negative sequence components of the voltage can then be generated based on Equation 4.25 and Equation 4.26.

$$V^{-*} = \frac{(V_{max} - V_{min}) \cdot (\cos(i_{max}\frac{2\pi}{3} - \theta_0) - \cos(i_{min}\frac{2\pi}{3} - \theta_0))}{\cos(i_{max}\frac{2\pi}{3} + \phi^-) - \cos(i_{min}\frac{2\pi}{3} + \phi^-)} \tag{4.25}$$

$$V^{+*} = V_{max} - V^{-*}\cos(i_{max}\frac{2\pi}{3} + \phi^-) - |V_0|\cos(i_{max}\frac{2\pi}{3} - \theta_0) \tag{4.26}$$

In the above equations, i_{max} and i_{min} is the index of the phase with the maximum and minimum voltage respectively. These references can then be used to calculate the commanded positive and negative sequence reactive power.

In order to complete the injection strategy, the saturation limits for the positive and negative sequence reactive power have to be determined. The strategy followed here assumes equal priority to both positive and negative sequence components but can be as well adapted depending on the application [40]. It has to be noted however, that the currents that result from this injection strategy are not symmetrical and therefore, the saturation limits have to be adjusted for the phase with the maximum current.

The phase current amplitude in contrast to the voltage will be the combination of a positive and negative sequence component without the presence of a zero sequence. Based then on the basic geometrical law of cosines, the amplitude of each phase's current can be found as can be deduced

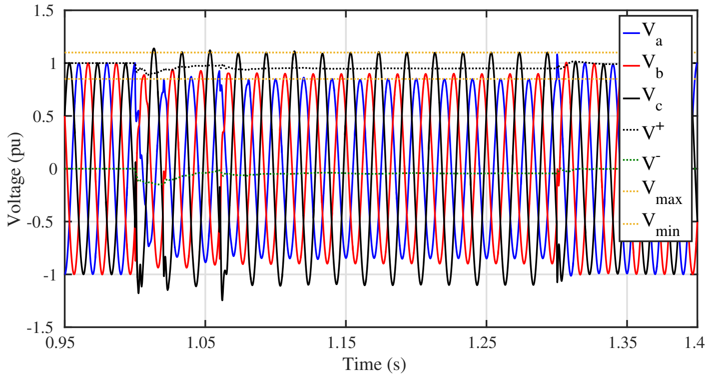

FIGURE 4.20: Asymmetrical voltage sag - PCC voltages.

by the following equations:

$$I_a = \sqrt{I^{+2} + I^{-2} + 2I^+I^- \cos\left(\frac{\phi_I^+ - \phi_I^-}{2}\right)} \tag{4.27}$$

$$I_b = \sqrt{I^{+2} + I^{-2} + 2I^+I^- \cos\left(\frac{2\pi}{3} + \frac{\phi_I^+ - \phi_I^-}{2}\right)} \tag{4.28}$$

$$I_c = \sqrt{I^{+2} + I^{-2} + 2I^+I^- \cos\left(\frac{4\pi}{3} + \frac{\phi_I^+ - \phi_I^-}{2}\right)} \tag{4.29}$$

Based on the above equations and following the same extraction process that was followed for the voltage, the phase with the maximum current amplitude I_{max} can be found. Finally, the reactive power saturation can be set as in [40]:

$$Q^+_{max} = Q^+ \cdot \frac{I_{rated}}{I_{max}} \tag{4.30}$$

$$Q^-_{max} = Q^- \cdot \frac{I_{rated}}{I_{max}} \tag{4.31}$$

The asymmetrical voltage sag shown in Figure 4.18 will be simulated with the aforementioned injection strategy. Firstly, the voltages at the PCC are shown in Figure 4.20. From Figure 4.20, it can be deduced that the injection strategy manages to keep the phase voltages at the PCC inside the previously specified limits while providing the needed reactive power to support the grid. More particularly, phase-a which experienced the higher sag, is increased up until the minimum limit while at the same time, the unaffected phase-c voltage rises to the maximum limit. In this way, all three phases are kept within the limits. In order to do so, the injection strategy employs asymmetrical currents as shown in Figure 4.21. The current amplitudes in this case are significantly lower than the rated current. As it was shown in Figure 4.20, the injection strategy reduces the unbalance between the phases and therefore, reduces the negative sequence voltage vector amplitude. This results in the reduction of the active and reactive power oscillations as shown in Figure 4.22.

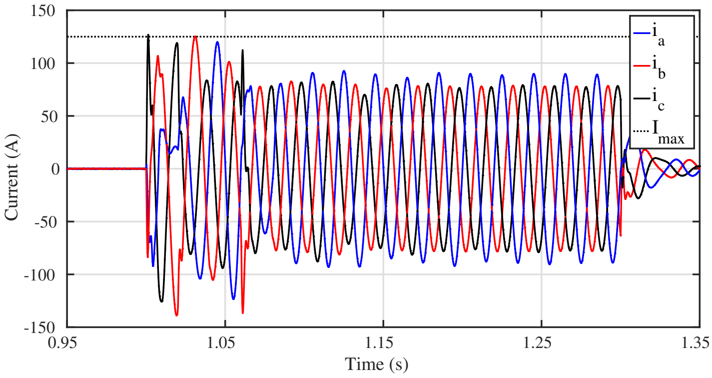

FIGURE 4.21: Asymmetrical voltage sag - Line currents.

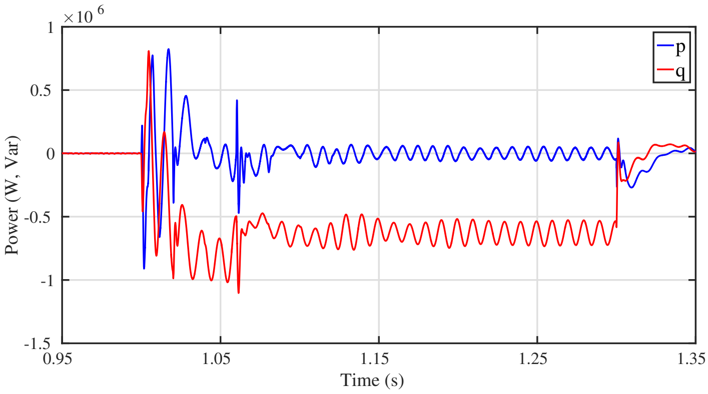

FIGURE 4.22: Asymmetrical voltage sag - Active and reactive power.

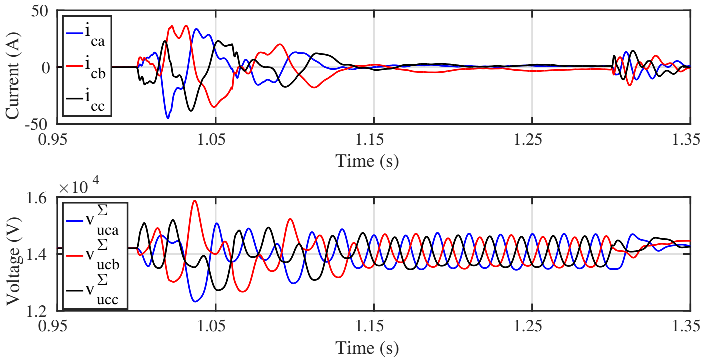

FIGURE 4.23: Asymmetrical voltage sag - i_c and v_{uc}^{Σ}.

It should also be noted that the total injected reactive power is lower than the rated one, since the goals of the injection are achieved without the need for maximum reactive power injection. Finally, Figure 4.23 shows the circulating current as well as the internal capacitors instantaneous voltages of the upper arm. The later figure proves that despite the injection of asymmetrical currents, the internal balance is ensured. It can also be seen that the capacitors of phase-a exhibit a significantly higher ripple due to the fact that the current of phase-a is higher. The average DC value however remains constant for all three phases.

Chapter 5

Harmonic Mitigation

A major problem in modern power systems is the pollution of power quality due to the introduction of harmonic content by various power electronic based loads. The current harmonics can cause voltage flicker and other undesired phenomena, such as malfunction of electronic equipment. One of the biggest challenges of the grid operators is to keep the power quality standards high, by limiting the Total Harmonic Distortion (THD) in the PCC voltage and the line currents [41].

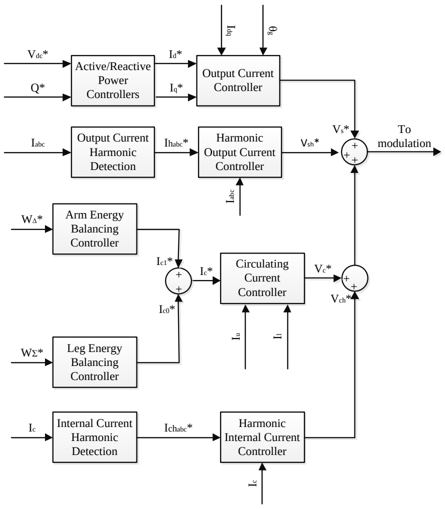

FIGURE 5.1: Overview of the STATCOM Control System including Harmonic Mitigation.

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A common solution is the harmonic mitigation using VSCs. VSCs employ an enhanced control system in order to detect and compensate for the current harmonics in the PCC, acting as active filters [42]. In this chapter, the performance of the MMC STATCOM topology in the mitigation of current harmonics up to the 13th order will be evaluated. An interesting study of the performance of the MMC in the mitigation of harmonics can be found on [43]. That study however does not take into consideration the induced harmonic content in the internal converter current. Naturally the chapter will be divided into two main section: i) the control strategy for the mitigation of the output current harmonics and ii) the control strategy for the mitigation of the internal current harmonics. Figure 5.1, shows the overview of the STATCOM control system including the harmonic mitigation strategies.

5.1 Output Current Harmonic Mitigation

The focus of this section will be laid on the detection and mitigation of the harmonic components of the output current controller, as shown in Figure 5.2. Usually, power electronic based loads are the cause of harmonic current present in the lines of a power system [44]. Most commonly, voltage source converters aim to mitigate the 5th, 7th, 11th and 13th order harmonics, since these ones are usually the ones with the higher amplitude.

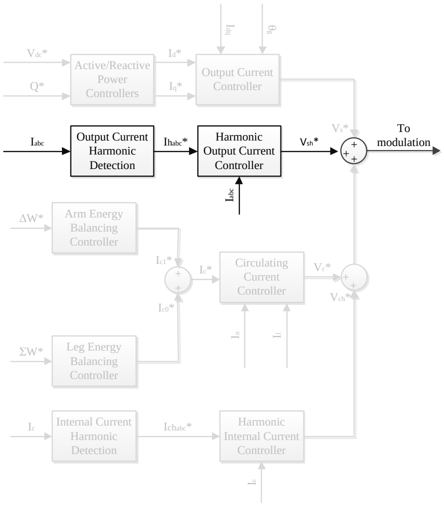

FIGURE 5.2: Overview of the STATCOM Control System including Harmonic Mitigation.

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The measured output current, shown in the block diagram in Figure 5.2, is fed to the harmonic detection block which will be analyzed right after. This block then generates the reference harmonic current that should be injected to the grid by the STATCOM in order to compensate for the current harmonics and keep the THD of the current waveforms as well as of the voltage waveforms at the PCC, as low as possible.

Regarding the detection methods, various techniques have been investigated. The methods usually split into two main categories: i) the selective detection methods that detect the magnitude of each harmonic individually and ii) the non-selective methods that simply split the current into fundamental and non-fundamental component [45]. In this report, bandpass filters will be employed in order to properly detect each harmonic order individually.

The band-pass filters that will be used in the simulations are designed in the Laplace domain. The general transfer function of a band-pass filter is:

$$G_{BPF}(s) = \frac{H_0 \cdot B \cdot s}{s^2 + B \cdot s + \omega_0^2} \tag{5.1}$$

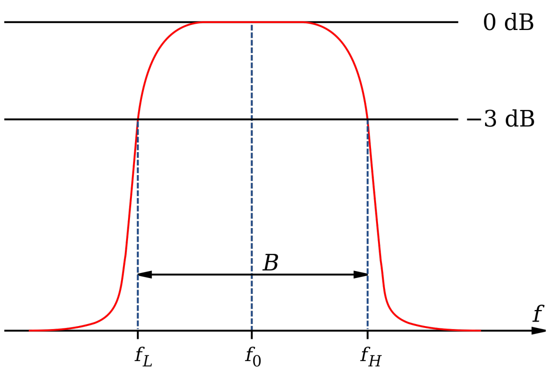

FIGURE 5.3: General band-pass filter [2].

In the above equation, parameter H_0 is the gain of the filter that is usually set to 1, B is the bandwidth of the filter and ω_0 is the center frequency that is desired to be selected through the filter. The frequency response of an ideal band-pass filter is shown in Figure 5.3 and is described by Equation 5.1. The ideal band-pass filter would have a flat pass-band region without inserting any attenuation or gain to the frequencies inside its bandwidth region while efficiently attenuating all the other frequencies. The bandwidth of the filter by definition is measured between the half power points, as shown in the figure on the right hand side [2].

In the application under study, the harmonic current source is assumed to be injecting $5th$, $7th$, $11th$ and $13th$ order harmonics. In order to detect these components in the measured current, the band-pass filters are designed with a center frequency:

$$f_0 = n_h \cdot 50 \tag{5.2}$$

where n_h corresponds to the order of the respective harmonic. The bandwidth of the filters is tuned to be $B = 50\ Hz$. Taking the fifth harmonic as an example, this means that the half power points with $-3\ dB$ attenuation are set at $225\ Hz$ and $275\ Hz$ according to the definitions. The frequency response of the magnitude and the phase of the four designed band-pass filters are shown in the figures below.

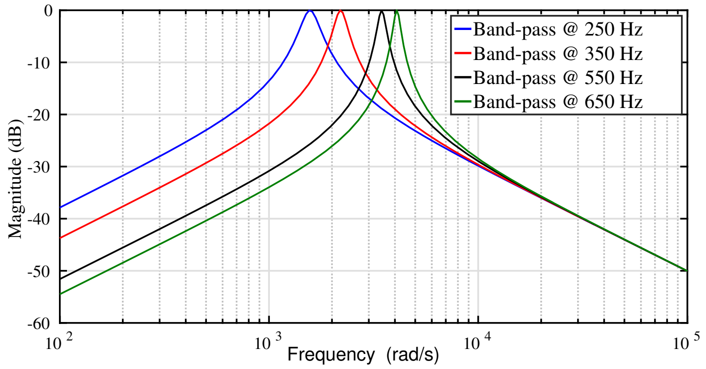

FIGURE 5.4: Band-pass filters frequency response: Magnitude.

There are a couple of things worth noting regarding the bode diagrams of the band-pass filters. Firstly, from the phase diagram of the frequency response, it can be deduced that the designed

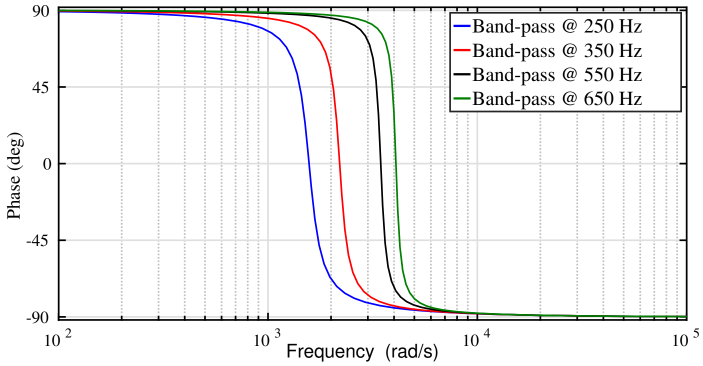

FIGURE 5.5: Band-pass filters frequency response: Phase.

band-pass filters do not affect the phase of the center frequency. This consists one of the desired characteristic of the band-pass filter. On the other hand, the designed filters are not ideal and therefore despite having zero gain in the center frequency, they do not provide full attenuation to the neighbouring harmonics. An inspection of the magnitude of the frequency response reveals that the band-pass filter of the $5th$ order, provides approximately 10 dB attenuation on the $7th$ harmonic. Similarly, the same filter provides a 25 dB attenuation to the fundamental component.

In order to avoid the aforementioned problem and improve the selectivity of the designed filters, two actions are taken. At first, a band-pass filter with a center frequency of 50 Hz and a small bandwidth of 10 Hz is designed and its output is subtracted from the measured current. In this way the input of the band-pass filters will see only the higher harmonic content of the measured current. Secondly, the outputs of the filters are fed-back to the input and are subtracted from the inputs of the other filters as shown in Figure 5.6. The reference outputs are then fed to the harmonic output current controller in order to be compensated [44].

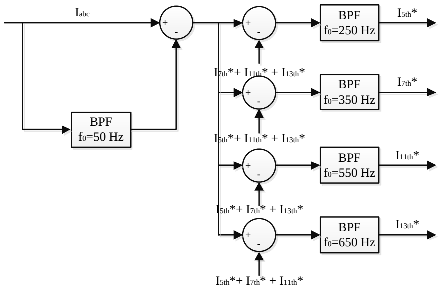

FIGURE 5.6: Harmonic detection strategy for the output current.

The output current controller was described in detail in Chapter 3. The harmonic output current controller is operating in parallel with the output current controller of the fundamental harmonic as can be seen in Figure 5.1. Since the control is implemented in the abc-frame with PR controllers, the harmonic output current controller block includes four resonant controllers in parallel, tuned at the desired frequencies of 250 Hz, 350 Hz, 550 Hz and 650 Hz respectively.

These resonant controllers now have to deal with higher harmonics in comparison to the fundamental resonant controller so their resonant gains have to be tuned to be faster. The tuning process of the resonant part of the fundamental controller was based on the fundamental frequency since this was the frequency that it aimed to follow. Thinking in exactly the same way, the resonant parts of the harmonic output current controller are chosen as:

$$K_{R_n} = n_h \cdot K_{R_1} \tag{5.3}$$

where K_{R_1} is the fundamental resonant gain, K_{R_n} is the resonant gain of the n_{th} harmonic and n_h is the order of the harmonic component. The simulation results in the last section of the chapter validate the proposed control strategy.

5.2 Internal Current Harmonic Mitigation

The injection of harmonic current in the output has an impact on the circulating current, since it increases its harmonic content. This harmonic content can be of significant magnitude, affecting the performance and the efficiency of the system.

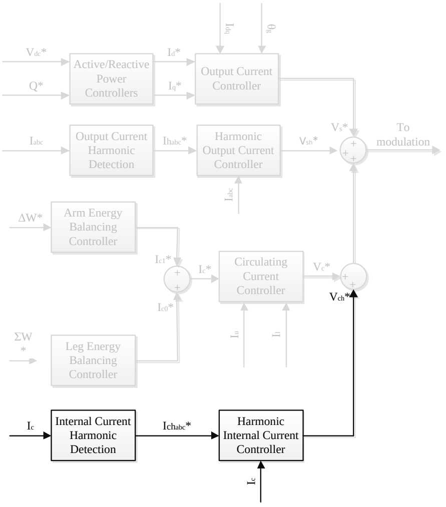

FIGURE 5.7: Internal Current Harmonic Mitigation.

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As a direct consequence of the above, suppressing the circulating current that results from the extra injection of current becomes of major importance for the MMC converter. Since the detection strategies and the compensation methods were described in the previous section, the remaining challenge that needs to be dealt with at this section is the determination of the resulting internal current harmonics due to the extra current injection. To do so, an analytic approach to the problem follows, investigating the effect of the current harmonics on the circulating current. Once the expected harmonic content of the circulating current is found, a compensation method is applied to suppress it. Since the circulating current is defined as the mean value of upper and lower arm currents within a converter leg, in order to identify the impact that the harmonic content of the output current will have in the circulating current, it is enough to look at the variations of the sum arm voltages that drive this current [15]. Equation 2.7 defined the total voltage of the upper arm and lower arm, inserting the concept of submodule's voltage (v_{sm}). Equation 2.8 however disregarded the variations in the capacitor voltages. More precisely, the submodule's voltage can be found by integrating the submomdule's current i_{sm} according to the equation:

$$v_{sm} = \frac{1}{C_{sm}} \cdot \int i_{sm} dt \tag{5.4}$$

On average however the submodule's current can be expressed as a function of the insertion index of the upper or lower leg respectively:

$$\begin{cases} i_{sm_u} = n_u \cdot i_u \\ i_{sm_l} = n_l \cdot i_l \end{cases} \tag{5.5}$$

Substituting Equation 5.5, Equation 5.4 and Equation 2.6 in Equation 2.7 the sum capacitor total voltages of the upper and lower arm can be expressed as:

$$v_{cu}^{\Sigma} = N \cdot \frac{1 - m \cdot cos(\omega t)}{2} \cdot \frac{1}{C_{sm}} \cdot \int \frac{1 - m \cdot cos(\omega t)}{2} \cdot i_u dt \tag{5.6}$$

$$v_{cl}^{\Sigma} = N \cdot \frac{1 + m \cdot cos(\omega t)}{2} \cdot \frac{1}{C_{sm}} \cdot \int \frac{1 + m \cdot cos(\omega t)}{2} \cdot i_l dt \tag{5.7}$$

Summing the above equations and re-arranging them:

$$v_{cu}^{\Sigma} + v_{cl}^{\Sigma} = \frac{N}{2C_{sm}} \int (n_u \cdot i_u + n_l \cdot i_l) dt - \frac{N}{2C_{sm}} \cdot m \cdot cos(\omega t) \int (n_u \cdot i_u - n_l \cdot i_l) dt \tag{5.8}$$

At this point some assumptions to simplify the analysis will be made. The circulating current will be assumed to be 0, since the focus of the current analysis is the impact of the output current on the internal dynamics. Moreover, the output current will be assumed to have a fundamental component and a $5th$ harmonic component, in order to simplify the analysis. The conclusions of this analysis however can be extended for n_{th} order harmonics in the output current.

Based on the above the upper and lower arm currents can be written as:

$$i_u = \frac{\hat{i}_1}{2} \cdot cos(\omega t) + \frac{\hat{i}_5}{2} \cdot cos(5\omega t) \tag{5.9}$$

$$i_l = -\frac{\hat{i}_1}{2} \cdot cos(\omega t) - \frac{\hat{i}_5}{2} \cdot cos(5\omega t) \tag{5.10}$$

Based on these definitions the terms $n_u i_u + n_l i_l$ and $n_u i_u - n_l i_l$ of Equation 5.8 can be expressed as:

$$n_u i_u + n_l i_l = -m \cdot \hat{i_1} \cdot cos^2(\omega t) + -m \cdot \hat{i_5} \cdot cos(\omega t) cos(5\omega t) \tag{5.11}$$

Having in mind that:

$$cos(a) \cdot cos(b) = \frac{1}{2}(cos(a-b) + cos(a+b)) \tag{5.12}$$

Equation 5.11 can be re-written as:

$$n_u i_u - n_l i_l = \frac{-m \cdot \hat{i_1}}{2} + \frac{-m \cdot \hat{i_1}}{2} \cdot cos(2\omega t) + \frac{-m \cdot \hat{i_5}}{2} \cdot cos(4\omega t) + \frac{-m \cdot \hat{i_5}}{2} \cdot cos(6\omega t) \tag{5.13}$$

Since the integration does not change the frequency component of the trigonometric terms, the sum of the arm voltages, according to Equation 5.13 will have a $2nd$, a $4th$ and a $6th$ component.

The other integral term of Equation 5.8 is found to be:

$$n_u i_u - n_l i_l = \hat{i_1} \cdot cos(\omega t) + \hat{i_5} \cdot cos(5\omega t) \tag{5.14}$$

Taking a moment to inspect Equation 5.8 and having in mind that:

$$cos(a) \cdot sin(b) = \frac{1}{2}(sin(a-b) + sin(a+b)) \tag{5.15}$$

The second term of Equation 5.8 will again result in a harmonic content of $2nd$, $4th$ and a $6th$ component.

Concluding this analysis, the main outcomes are listed hereby:

- The sum of the voltage variations of the arms contains the same harmonic content as the circulating current, so Equation 5.8 can be used to determine the expected harmonic content of the circulating current.
- The $2nd$ harmonic component appears naturally in the circulating current, due to the presence of the fundamental current. This is a finding commonly encountered in previous research and until this point of the report, it was not mentioned. The circulating current controller needs therefore to include a resonant controller tuned at 100 Hz to suppress the resulting circulating current. This effect was taken into consideration in the development of the circulating current controller in Chapter 3.
- It was found that only even harmonics appear on the circulating current due to the odd harmonics of the output current.

- The $5th$ harmonic output current results in the appearance of a $4th$ and $6th$ harmonic in the circulating current. However, the $6th$ is a zero component harmonic and due to the nature of the STATCOM that does not include a DC-link, the zero sequence components are naturally eliminated from the current waveforms.
- The previous finding can be generalized. An n harmonic order component in the output current will produce either $n-1$ or $n+1$ component in the circulating current. For example, the $5th$ harmonic produces a $4th$ harmonic component whereas the $7th$ produces an $8th$ etc.

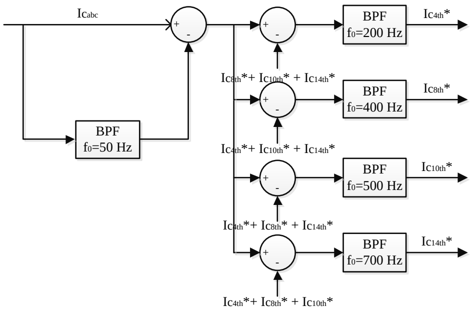

FIGURE 5.8: Harmonic detection strategy for the circulating current.

Based on the above findings, the harmonic detection strategy can be depicted in Figure 5.8. The detection strategy as mentioned before is identical with the one followed for the output current, with the band-pass filters being tuned with the same bandwidth but different center frequencies, as depicted in the figure on the left hand side. An extra band-pass filter with smaller bandwidth is also designed here to effectively remove the fundamental component of the circulating current that may result from the arm energy balancing controller. A DC component is also expected in the circulating current due to the leg energy balancing controller, but this component is expected to be well attenuated by the band-pass filter, so no action is taken hereby.

Just like in the harmonic output current case, the outputs of the harmonic detection are fed to the harmonic internal current controller that is comprised by several resonant controllers tuned at the respective frequencies. The resonant controllers are tuned as described in the previous section.

5.3 Simulation Results

In this section, simulation results prove the validity of the aforementioned study in the mitigation of current harmonics. In this simulation study, a harmonic current source is connected to the PCC in order to emulate the behavior of a diode rectifier load that injects current harmonics in the power system. This current source is generating 5th, 7th, 11th and 13th harmonic components, as can be seen in Figure 5.9.

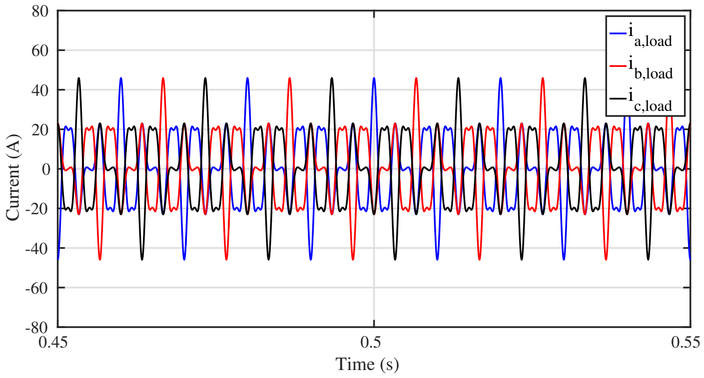

FIGURE 5.9: Load Harmonic Currents injected to the PCC.

Figure 5.10 depicts the three phase line currents. The output harmonic controller is enabled at 0.5 s. It can be seen that before that instance, the line currents are distorted due to the presence of the non-linear load. The controller however compensates for the harmonic currents and after 0.5s the line currents have a significantly lower harmonic content. It should be noted that after enabling the harmonic mitigation, the lower harmonics are fully compensated, while the 13th order is not. If a higher bandwidth was chosen for the output current controller, then the complete compensation of this component would be possible as well.

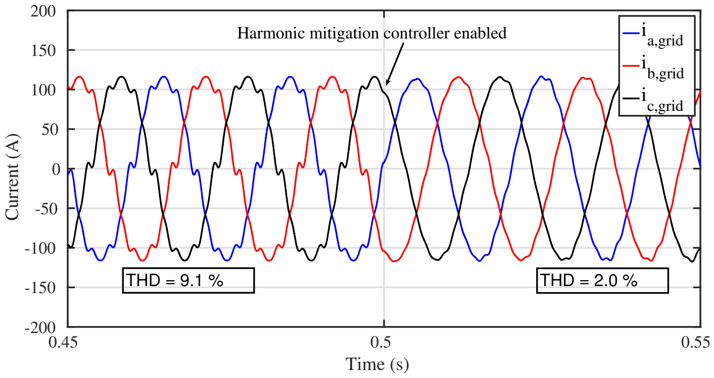

FIGURE 5.10: Line Currents when a harmonic current source is connected.

For completeness, the current flowing into the STATCOM is shown in Figure 5.11. It is clear that the STATCOM even before enabling the harmonic mitigation controller, acts as a shunt filter, absorbing a big part of the harmonic load, due to its relatively low impedance. Furthermore, the mitigation of the voltage harmonics at the PCC is crucial for the proper operation of the system. A distorted voltage at that point will mean that all the other loads connected to the PCC will see a distorted input. As it can be deduced from Figure 5.12, the voltage harmonics are well mitigated by the introduction of the harmonic controller, resulting in almost sinusoidal voltages.

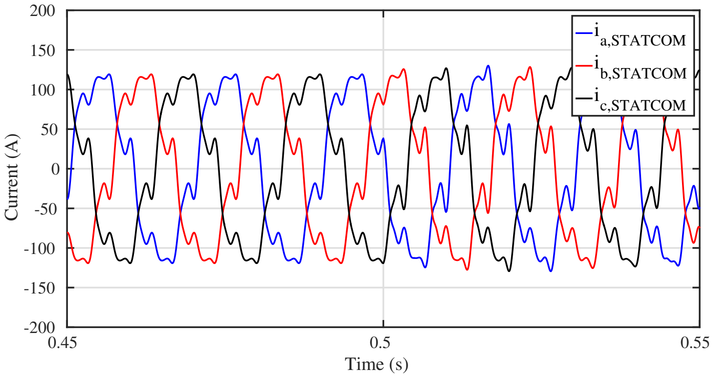

FIGURE 5.11: Arm Currents when a harmonic current source is connected.

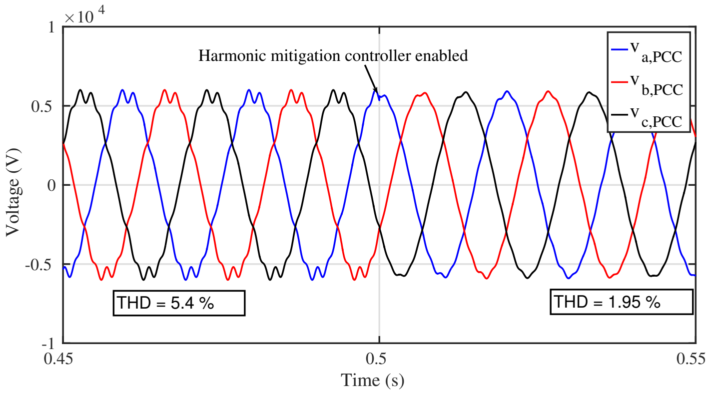

FIGURE 5.12: PCC voltage when a harmonic current source is connected.

Since the system is balanced, the arm energy controller as well as the leg energy controller do not inject any circulating currents in the system, and the expected circulating current is therefore zero. In the previous section it was shown however, that the extra harmonics in the arm currents will introduce an extra circulating current that may have an impact on the performance and efficiency of the converter.

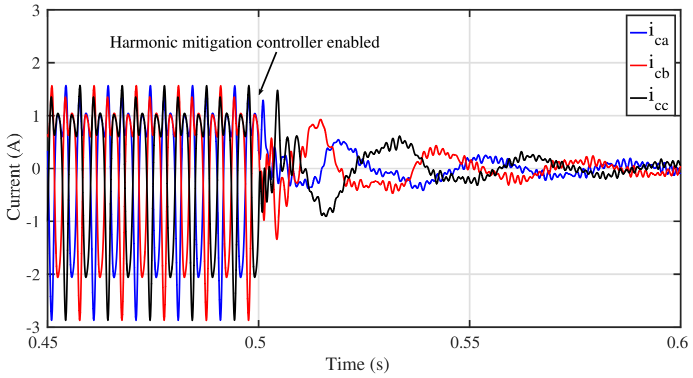

FIGURE 5.13: Circulating current when a harmonic current source is connected.

The internal harmonic controller, as can be depicted in Figure 5.13, is mitigating the circulating current harmonics, bringing the circulating current of all three phases to zero.

Chapter 6

Experimental Results

In order to prove the validity of the analysis of the MMC controllers, extensive experimental results are presented in this chapter. The experimental results were recorded in the MMC laboratory of Aalborg University, working with a small scale MMC configuration, shown on the picture on the right. The control of the setup was implemented in dSPACE and the modulation technique that was used throughout the experiments was the basic sorting algorithm, as firstly presented in [46].

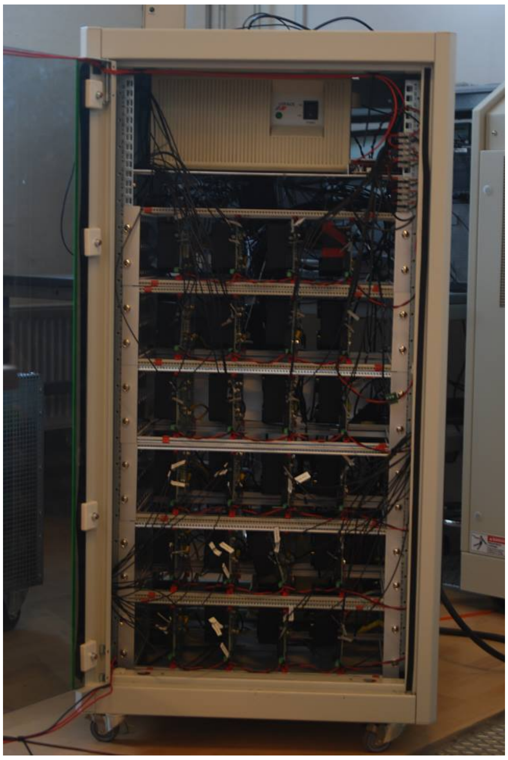

FIGURE 6.1: The MMC prototype with four submodules per arm in Aalborg University.

The output of the converter is connected to a three-phase AC source through a 2.5 kVA transformer of type Dyn11 with a turns ratio transformation equal to $1/\sqrt{3}$. The parameters of the setup and the operating conditions of the experiments are shown on Table 6.1.

This chapter is structured as follows. Firstly, the ability of the configuration to control positive and negative sequence reactive power is shown in steady state. After this, the energy balancing controllers are validated and the improvement in the performance of the converter with their use is highlighted. Finally, the ability of the configuration to control high order current harmonics, using a relatively low switching frequency, is experimentally demonstrated and its ability to operate as an active filter while providing reactive power is evaluated.

TABLE 6.1: Parameters of Experimental Setup

Description	**Symbol**	**Value**
Rated Power (kVA)	S	2.5
Operating AC RMS Voltage (V)	V_{ac}	150
Rated Submodule's Voltage (V)	V_{SM}	200
Operating Pole-to-pole Voltage (V)	V_{dc}	300
Submodule's Capacitance (mF)	C_{SM}	4
Arm Inductance (mH)	L_{arm}	20
Number of Submodules per arm	N	4
Transformer Turns Ratio	n	1:$\sqrt{3}$

6.1 Reactive Power Control

At first, the converter is injecting positive sequence reactive power to the grid, acting as a capacitor. The pole-to-pole voltage is set to 300 V and the grid's phase RMS voltage is set to 150 V. The reference of the q-component current on the converter side, in positive sequence is then set to $i_q^* = 6A$ resulting to a reactive power of approximately 1.2 kVA. It must be noted that the converter is operated close to half of its rated power for safety reasons.

Figure 6.2 depicts the instantaneous active and reactive power as measured on the grid side. As expected the converter draws a small amount of active power, in order to compensate for the losses and keep the pole-to-pole voltage constant. Due to the absence of a negative sequence component, the instantaneous active and reactive power are constant.

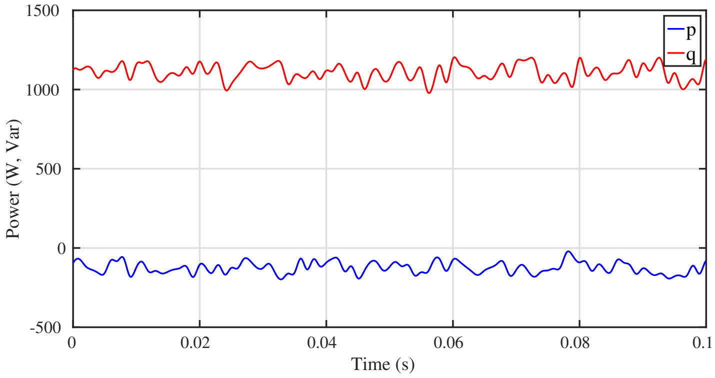

FIGURE 6.2: Positive Sequence Reactive Power Control - p and q.

The three phase output currents in the *abc* - reference frame are depicted in Figure 6.3, as measured on the secondary side of the transformer. It should be noted that part of the distortion of the current waveforms in all the experimental graphs is due to the insufficient sampling of the dSPACE control desk, when recording the waveforms.

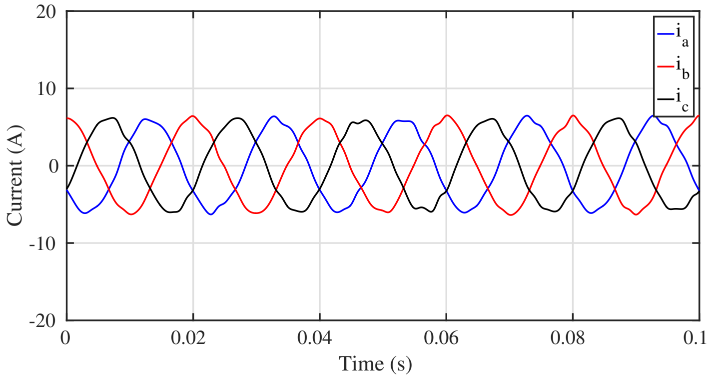

FIGURE 6.3: Positive Sequence Reactive Power Control - Output Currents.

In Figure 6.4, the circulating current is depicted. As noted several times throughout the theoretical analysis of the configuration, the expected circulating current when no active power is controlled, is zero. However, a small second harmonic component is naturally expected as shown analytically in Chapter 5. This component can be noticed in the figure below. The circulating current controller is disabled in this case as the current amplitude is very small.

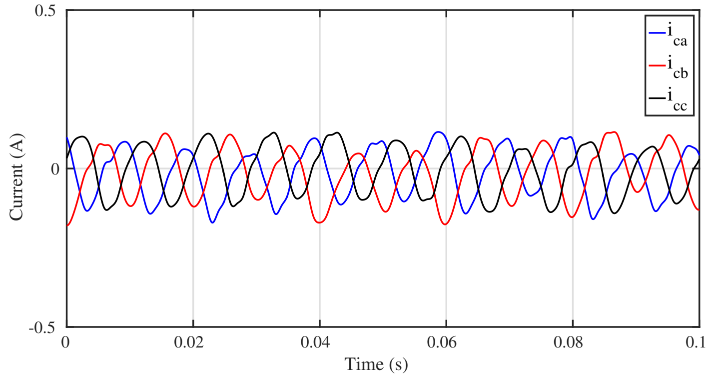

FIGURE 6.4: Positive Sequence Reactive Power Control - Circulating Currents.

Moving on, a negative sequence q-component current is injected under the same operating conditions as before. The reference of the positive sequence d-component of the current is still produced by the pole-to-pole voltage controller while the other three current component references are introduced as:

$$\begin{cases} I_q^+ = 0 \\ I_d^- = 0 \\ I_q^- = 6\text{A} \end{cases} \tag{6.1}$$

Figure 6.5 depicts the instantaneous active and reactive power. The presence of the negative sequence results in large oscillations as expected by Equation 4.10.

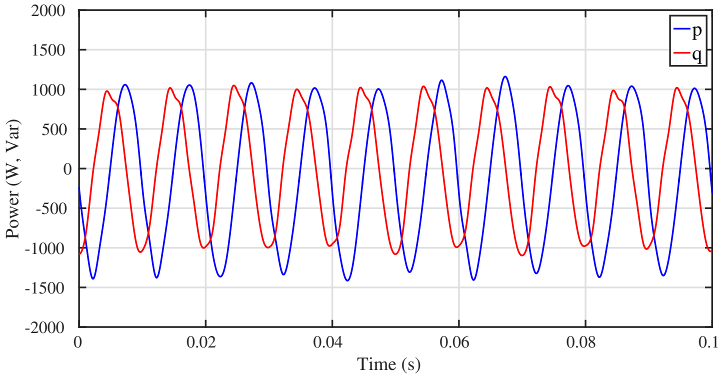

FIGURE 6.5: Negative Sequence Reactive Power Control - p and q.

Figure 6.6 shows the output currents injected to the AC source with the previously described conditions. It can be noticed that phase-c leads phase-b as expected when negative sequence current is controlled. It should also be noticed that the currents in this case are unbalanced.

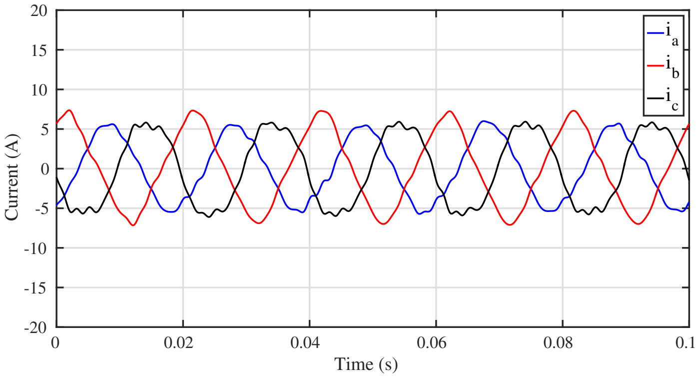

FIGURE 6.6: Negative Sequence Reactive Power Control - Output Currents.

Figure 6.7 depicts the circulating current when negative sequence current is injected. It can be deduced that apart from the second order harmonic, the circulating currents of each phase contain a DC component as well. It is very important however to note that this component is small in comparison to the total current and therefore the total RMS value of the current is barely affected by its presence.

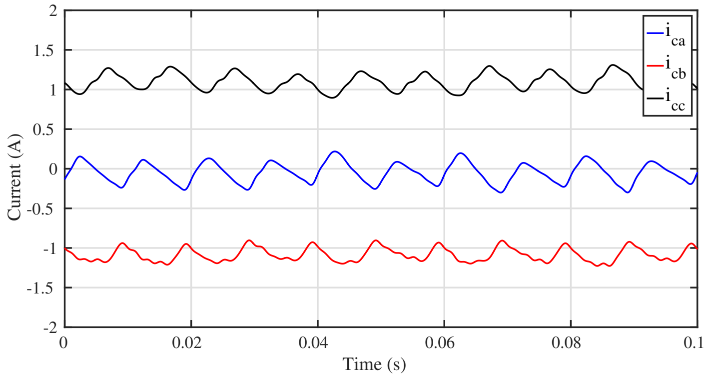

FIGURE 6.7: Negative Sequence Reactive Power Control - Circulating Currents.

To conclude the analysis, mixed positive and negative sequence reactive current is injected. The reference of the positive sequence d-component of the current is still produced by the pole-to-pole voltage controller while the other three current component references are introduced as:

$$\begin{cases} I_q^+ = 3\text{A} \\ I_d^- = 0 \\ I_q^- = 3\text{A} \end{cases} \tag{6.2}$$

Figure 6.8 shows the instantaneous active and reactive power for this injection case. It can be noticed that the presence of negative sequence produced large oscillations whereas the positive sequence current is responsible mainly for the average value of the reactive power.

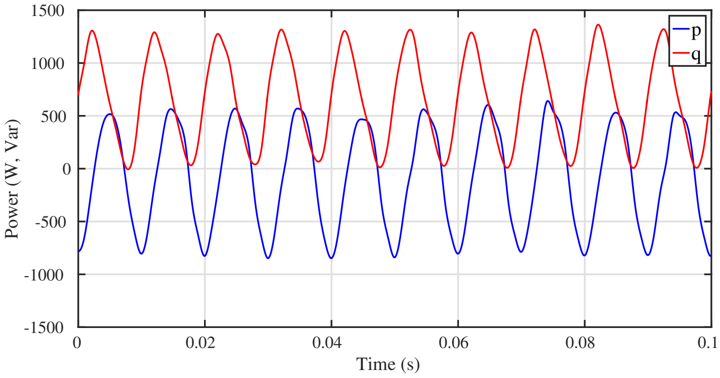

FIGURE 6.8: Mixed Sequence Reactive Power Control - p and q.

Figure 6.9 shows the output currents injected to the AC source with the previously described conditions.

Finally, the circulating currents of the three legs of the converter for the mixed sequence current injection are shown in Figure 6.10. Once again the circulating current is composed by a small

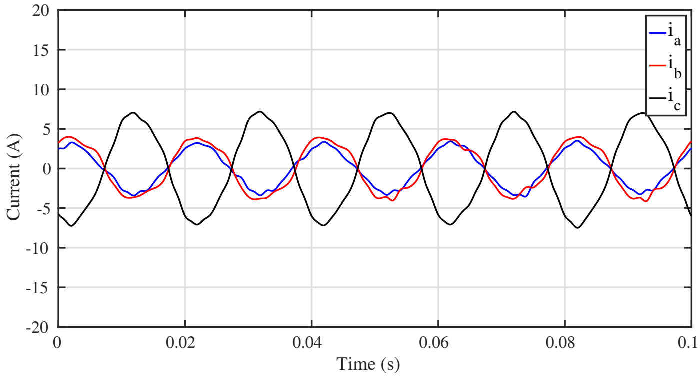

FIGURE 6.9: Mixed Sequence Reactive Power Control - Output Currents.

natural second order harmonic as well as a DC component due to the presence of the negative sequence current.

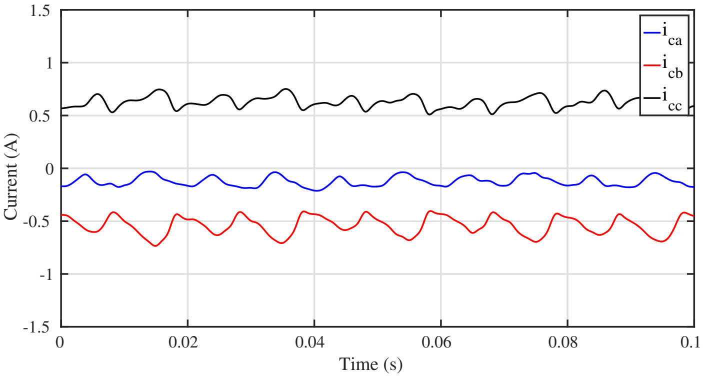

FIGURE 6.10: Mixed Sequence Reactive Power Control - Circulating Currents.

6.2 Energy Balancing Controllers

In this section, the leg energy balancing as well as the decoupled arm energy balancing controller will be verified through experimental results. The gains of the energy controllers are tuned in the same way as was described in Chapter 3 of the report at hand.

Firstly, Figure 6.11 depicts the action of the leg energy balancing controller. It can be seen that initially the difference between the total leg energies is very small as the mismatch between the parameters of the converter is very small. However, after enabling the energy controller, the aforementioned energy difference is eliminated.

After this, a step change of 10% is applied in phase-a as shown in Figure 6.11. The leg energies of phase-b and phase-c are reduced accordingly as well in order to keep the total stored energy

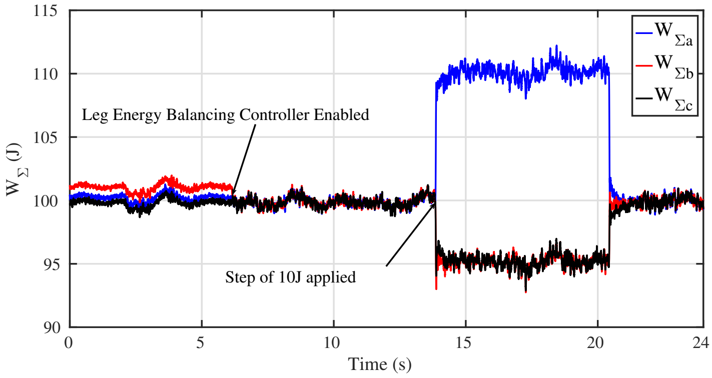

FIGURE 6.11: Leg Energy Balancing Controller - W_{Σ}.

of the converter constant. It can be deduced that the energy controller manages to exchange power between the converter legs as expected, with the help of a DC component of the circulating current.

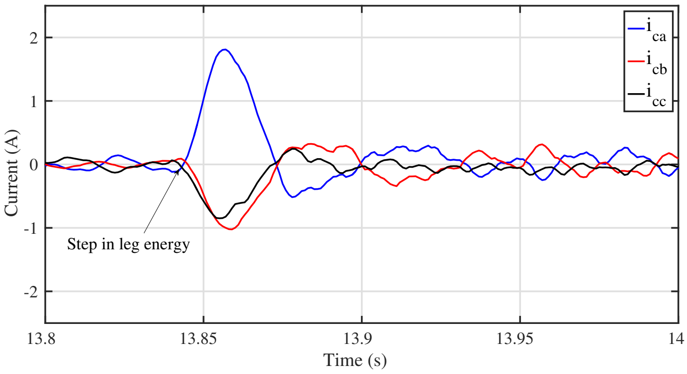

FIGURE 6.12: Leg Energy Balancing Controller - Circulating Current

Figure 6.12 depicts the circulating current at the moment of the step change. It can be deduced that the leg energy controller imposes a positive DC reference in the circulating current of phase-a and a negative one in phases b and c. After the energy of phase-a reaches its reference, the circulating current of each phase returns to zero.

In addition to the above, the average value of the sum capacitor voltages of the upper leg, during the energy change, are depicted in Figure 6.13. Initially the average total capacitor voltage of every phase is equal to total pole-to-pole voltage ($300V$). When the energy step change is imposed, the average value of the voltage of the capacitors of phase-a is increased, as expected.

Moving on, the decoupled arm energy balancing controller is tested experimentally. In Chapter 3, it was shown that this controller can be used in order to exchange active power between the arms of a specific converter leg without affecting the other legs. Any mismatches between the energy

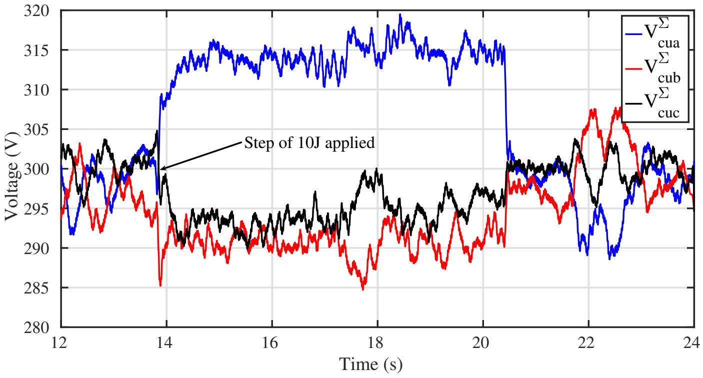

FIGURE 6.13: Leg Energy Balancing Controller - Sum capacitor average voltage (upper leg)

levels of the arms can then be eliminated with the use of the first harmonic of the circulating current.

Figure 6.14 depicts the energy difference between the upper and lower arm of each phase.

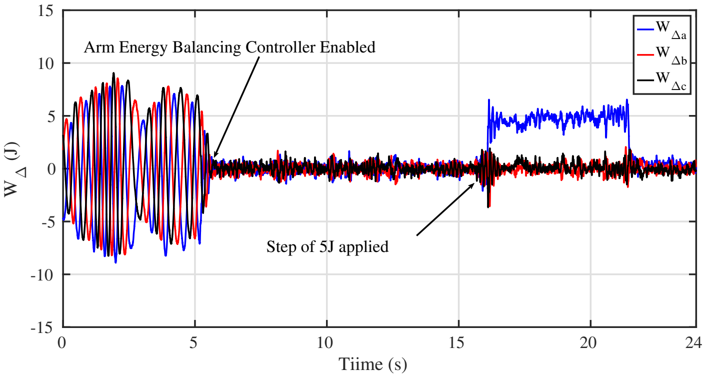

FIGURE 6.14: Arm Energy Balancing Controller - W_{Δ}.

Initially, the controller is disabled and the energy difference between the arms oscillates. After enabling the controller, the energy difference is controlled to zero as indented to, stabilizing the system. After this, a step energy change of 5 J is applied between the arms of phase-a while at the same time the energy difference references for phases b and c remain zero. As can be depicted in Figure 6.14, energy is moved from the lower to the upper arm of phase-a without affecting the other phases, proving the decoupling concept that was analyzed in Chapter 4.

Figure 6.15, depicts the average sum capacitor voltages of the upper and lower arm. It should be clear that on the one hand the voltage of the capacitors follows the energy difference profile and on the other hand, independent control of the voltage level of each arm can be achieved with the developed controller.

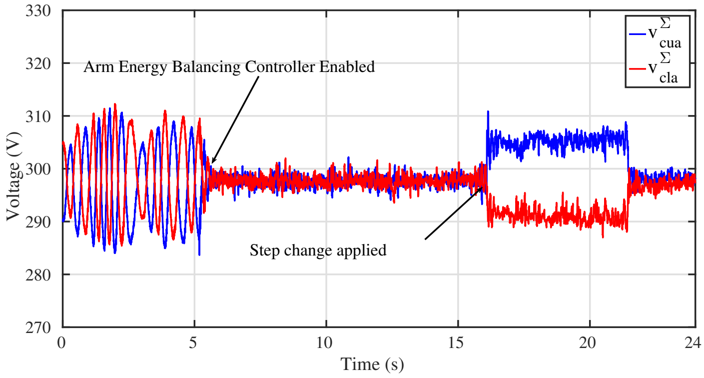

FIGURE 6.15: Arm Energy Balancing Controller - Sum capacitor average voltage (phase-a) .

6.3 Harmonic Injection

As highlighted in Chapter 5, it is usually required from a STATCOM to inject high ordered harmonic currents to the grid in order to compensate for the existent harmonic currents present at the PCC, caused by non-linear loads. One of the most important aspects of the MMC configuration is its increased bandwidth that allows the control of higher ordered harmonics with relatively low switching frequency. In order to demonstrate the aforementioned advantage of the MMC, in this section the ability of the control system to follow a higher ordered harmonic current will be exhibited.

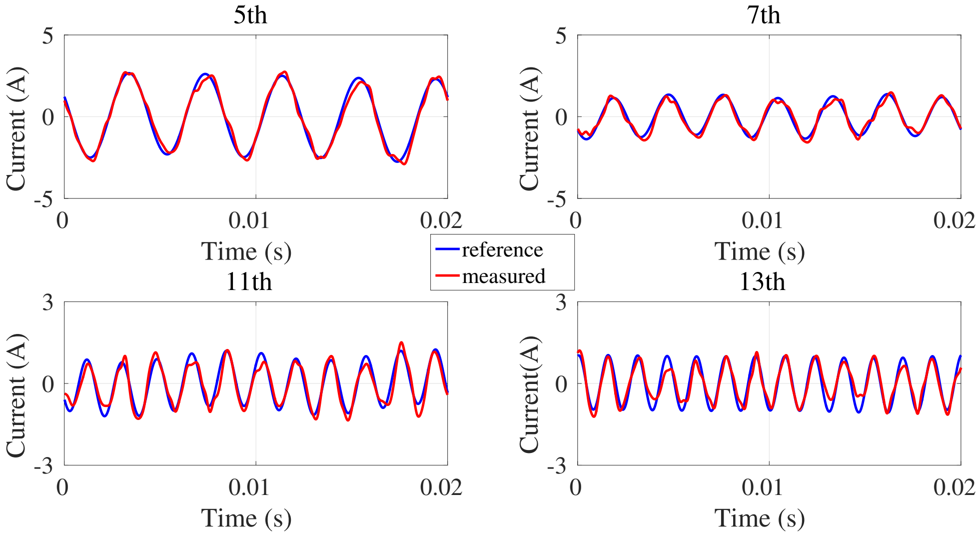

FIGURE 6.16: Harmonic Output Current Injection.

Figure 6.16, shows the performance of the current controller in the control of $5th$, $7th$, $11th$ and $13th$ order harmonic. It should be noted that in all cases, the magnitude of the injected current shown is the maximum that could be controlled without saturating the voltage reference. The harmonic output current controller used is identical to the described one in Chapter 5, so no further discussion is made hereby. From Figure 6.16 it can be deduced that the developed controller follows with high accuracy the $5th$ and $7th$ harmonic order reference. The high accuracy is deteriorated in the $11th$ and $13th$ case, due to the presence of oscillations in the reference that likely result from oscillations of the pole-to-pole voltage. These oscillations can be noted in the figure above. The result however can be considered sufficiently accurate.

6.4 Harmonic Compensation

In this section, the complete current harmonic compensation procedure will be applied, in order to detect and compensate the high harmonics injected to the AC source by a diode bridge load, as shown in Figure 6.17. The DC output of the load is connected to a resistive load of 200 Ω. The harmonic currents that are drawn by a diode rectifier were analyzed in [47].

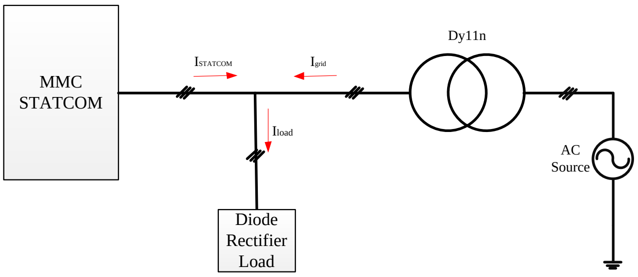

FIGURE 6.17: Schemmatic of experimental setup for harmonic mitigation.

The grid currents are sensed and fed to the MMC STATCOM control system. The detection of the harmonic components is made in the dq-reference frame and the positive and negative components are extracted with the appropriate rotation. After this, a second order Low-Pass-Filter (LPF) is used to extract the DC component that corresponds to the desired frequency component in the abc-reference frame.

The detection method as well as the reference frame transformation however are usually associated with time delays arising from the sampling frequency. In the work of [24] the time delays are well explained. Moreover, the trade-off between the filter's response and its

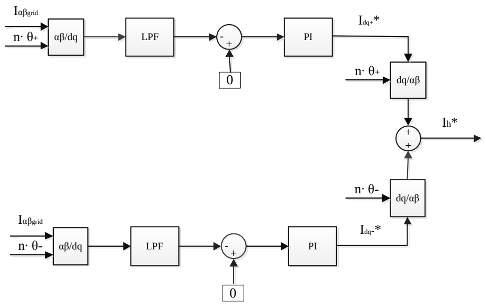

FIGURE 6.18: Control System for the generation of harmonic reference currents.

attenuation is well-known [2]. These two effects on the detection method are discussed in detail in [43], where a comparison of different detection methods is conducted and the limitations of the active filtering procedure are highlighted. In order to compensate for the unavoidable errors, the output of the LPF is compared with zero, which is the desired harmonic content in the grid currents. The formulated error is then passed through a PI. The proportional gain is set to 1 while the integral gain can be set to a small value in order to maximize the stability of the method and avoid unnecessary transients. In the end, the integral part reduces the error by gradually eliminating the harmonic components of the currents, provided that the output current controller can follow the reference with precision.

Figure 6.19, depicts the currents of phase-a when no compensation is applied. The STATCOM in this case operates at $1.1kVA$, injecting $5A$ current to the grid. Due to the high impedance of the MMC, the harmonic currents flow mostly towards the grid side, resulting in a huge distortion of 26%.

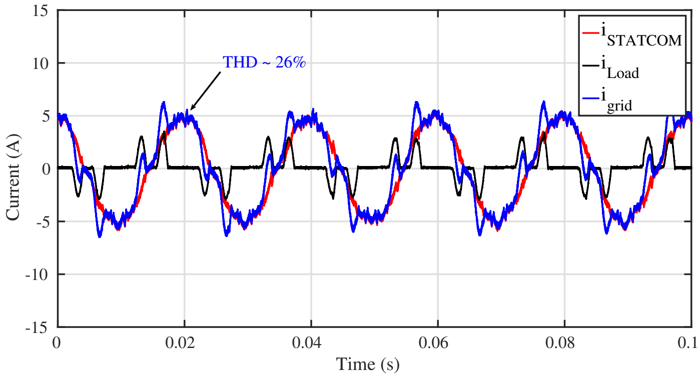

FIGURE 6.19: Currents without harmonic compensation.

Figure 6.20, depicts the current waveforms after the application of the compensation. It can be seen that the STATCOM currents are now distorted, while the THD of the grid currents has been reduced to 9%. The switching frequency in this case was measured (sorting algorithm) to be approximately 1 kHz.

A comparative graph in Figure 6.21, depicts the grid currents before and after the application of the harmonic compensation in the time domain.

Finally, Figure 6.22 depicts the result of the Fast Fourier Transformation of the grid current waveforms before and after the application of the harmonic compensation. It can be deduced that the injection strategy eliminates completely the 5th, 7th, 11th and 13th component.

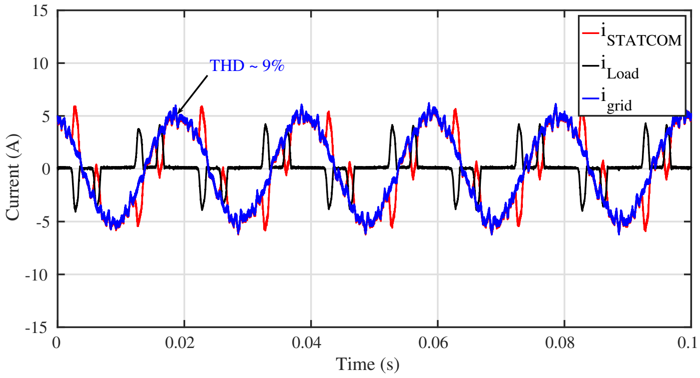

FIGURE 6.20: Currents with harmonic compensation.

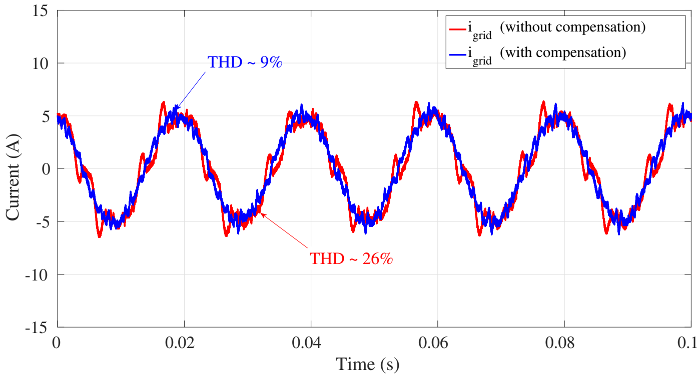

FIGURE 6.21: Grid currents comparative graph.

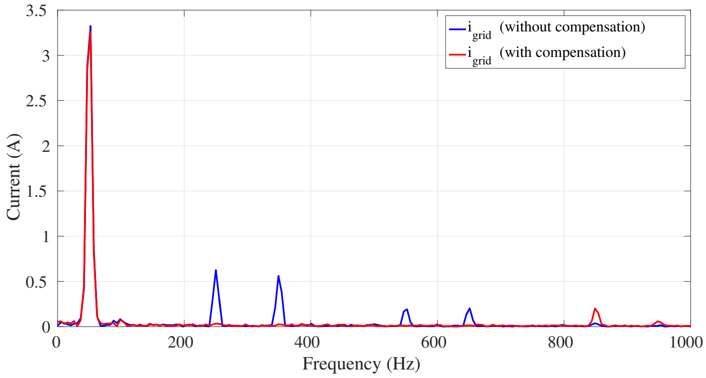

FIGURE 6.22: Grid currents comparative graph - FFT.

Chapter 7

Conclusions and Future Work

In this final chapter of the report, the conclusions of this work are drawn and future work proposals are suggested. The conclusions summarize the main outcomes of the conducted research since these are the points that the reader should focus on. The time limitations that unavoidably exist in semester projects did not permit a more detailed analysis and therefore research proposals are suggested for future researchers on the topic.

7.1 Conclusions

Some of the main conclusions of the Thesis are listed hereby:

- Initially, a comparison between the losses and associated costs in the development of a large scale STATCOM with full negative sequence control capability, showed that the DS-HB configuration, despite the higher initial cost, proves to be beneficiary in comparison to the commonly used SD-FB.
- The inclusion of the energy balancing controllers facilitated the independent control of each arm's voltage levels, which might prove to be useful in certain applications. Nevertheless, the internal control scheme that was developed, is able to eliminate any possible energy level differences that may arise due to the unavoidable mismatches of the system's parameters (device parameter spread, aging of equipment, manufacturing spread etc.).
- An intuitive method to implement a decoupled arm energy controller was presented. The inclusion of this particular controller improved greatly the performance of the experimental setup, as can be seen in Figure 6.14.

- The current controller was developed with the use of PR-controllers. This proved beneficiary in the control implementation since the developed controllers can track down a sinusoidal signal with a certain frequency regardless of its sequence, something that reduced greatly the complexity of the control system.
- The proposed internal balancing control scheme was proven via simulations efficient in keeping the MMC balanced when asymmetrical grid faults arise. In the worst case scenario of a single line-to-ground fault, the necessity of energy balancing controllers was depicted in Figures 4.16 and 4.17.
- An improved injection strategy during asymmetrical grid faults was studied. The injection strategy takes the effect of the inevitable zero sequence voltage component into account, in contrast to the previous studies and tries to keep the phase voltages within their specified limits.
- A connection between the harmonics of the output current and its effect on the circulating current was established in [15]. When the STATCOM is used as an active filter for harmonic compensation, the findings of the study should be taken into account in order to minimize the effect of the circulating current harmonics on the system's efficiency. These findings were backed via analytic calculations and simulations in Chapter 5.
- In the experimental part, the efficiency of the MMC in mitigating higher ordered current harmonics with a relatively low switching frequency was demonstrated. The increased bandwidth of the MMC due to its modularity allowed for the control of current harmonics up to the 13th order, demonstrating great performance as shown in Figure 6.22.

7.2 Future Work

The present Thesis investigated internal and external unbalanced conditions. However, external unbalances due to voltage sags and AC grid faults were not tested experimentally. This is obviously one of the most important research topics. Despite the fact that the simulation results indicate that the proposed MMC control strategy can ensure the internal balance of the setup, experimental tests should take place in order to indicate possible problems related to the internal balance.

Furthermore, due to the high value of the arm inductance used in the experimental part, the circulating current was inevitably very low, as shown in Chapter 6. This is of course one desired characteristic for a real application but for research purposes, tests in a setup with a lower arm inductance could prove useful from an academic point of view.

Last but not least, the current Thesis used time averaged models to describe the dynamics of the system. However, the modulation technique is of major importance in an MMC system, mainly due to the fact that it can be set to be much lower than in conventional topologies without compromising the efficiency of the control system. Nevertheless, important details are left out of the current analysis and their inclusion could give further insight of the operation of the control scheme and the dynamic performance of the system.

Appendix A

Review of STATCOM technology

A.1 STATCOM Operating Principle

STATCOM belongs to the general family of dynamic shunt compensators and is currently the most widely accepted and reliable way for controlling and compensating the reactive power present in utility power grids. Its operation is based on the theory of Voltage Source Converters. STATCOM controls the reactive power by controlling the amplitude and the phase of the voltage at its output and therefore it does not use any passive component (capacitor/reactor banks) [11].

Ideally STATCOM controls reactive current in such a way that reactive power is exchanged between the phase legs without transferring any active power. For simplicity, the converter can be seen as an ideal voltage source behind and inductor connected to the grid as shown in Figure A.1.

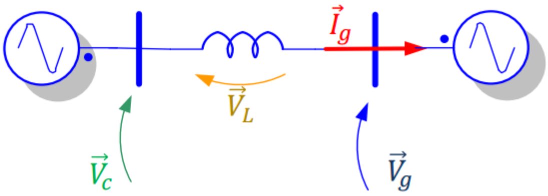

FIGURE A.1: Simplified STATCOM Schemmatic.

The resulting power equation at the grid end is given by:

$$Q = \frac{V_g}{\omega L}(V_{con} cos\delta - V_g) \tag{A.1}$$

The voltage of the grid V_g is taken with a reference phase angle and δ is the angle of the converter voltage vector. The phase angle difference is responsible for the active power flow between the two voltage sources whereas the difference of the magnitudes of the converter voltage V_{con} and the grid's voltage V_g is responsible for the reactive power flow. When V_{con} is in phase with the grid's voltage Equation A.1 is simplified:

$$Q = \frac{V_g}{\omega L}(V_{con} - V_g) \tag{A.2}$$

From this equation it is easy to see that depending on the amplitude of the converter's voltage, STATCOM can either produce reactive power, acting as a capacitor ($V_{con} > V_g$) or can absorb reactive power acting as an inductor ($V_{con} < V_g$). When these two voltages are equal then there is no exchange of reactive power whatsoever. The vector diagrams below show this operation in a more comprehensive way.

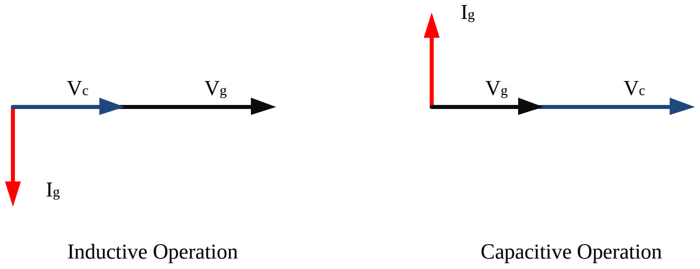

FIGURE A.2: STATCOM simplified vector diagram.

A.2 Popular Multilevel Converter Topologies

Two of the most widely discussed multilevel topologies in literature are the Diode Clamped Multilevel Inverter (DCMLI), which is also called Neutral Point Clamped Converter (NPC) when only 3 levels are used, and the Flying Capacitor Multilevel Inverter. Both of these topologies are capable of producing high quality ac waveforms. An analytic comparison can be found in [12].

The DCMLI topology splits the total DC voltage in multiple stages depending on the number of levels used (N-1 voltage stages for N levels). The blocking voltage of each devices is clamped by diodes as shown in the relevant schematic below. One reported advantages of this topology is its ability to control negative sequence reactive power and therefore support the grid during fault conditions [3]. On the other hand, the number of power devices used is increasing due to the clamping diodes that are used.

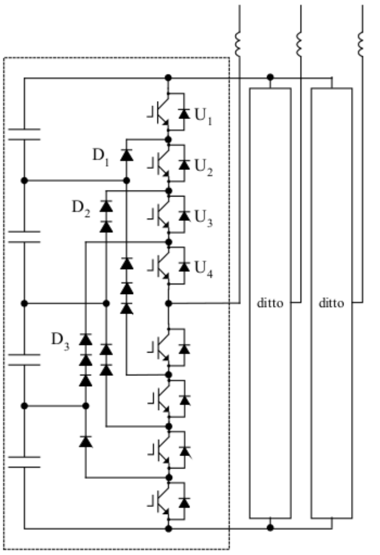

FIGURE A.3: DCMLI Structure [3].

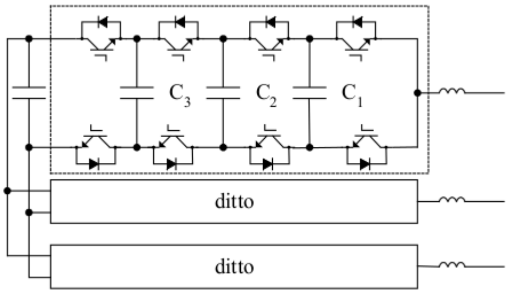

FIGURE A.4: FCMLI Structure [3].

The FCMLI uses multiple capacitors on the DC link side, depending again on the number of levels that are used. The capacitors are shown in figure A.4. These capacitors are charged on different voltage levels and the difference defines the voltage steps of the produced AC waveform [12]. In contrast to the DCMLI topology, the FCMLI topology ensures the clamping of the voltage of each power device with the use of the capacitors, so it does not require clamping diodes. Furthermore, the topology has the ability as well to control negative sequence current. However, when low switching frequency is used, the size of the capacitors increase.

A.3 The MMC family

As noted in the introduction, the MMC family is usually classified in four different configurations:

- Single Star Full-Bridge (SS-FB)

- Single Delta Full-Bridge (SD-FB)
- Double Star Half-Bridge (DS-HB)
- Double Star Full-Bridge (DS-FB)

This report focuses on the Double Star Half-Bridge configuration but at this section a small discussion of all the configurations will take place. It should also be noted that these configurations can be found in the bibliography with different names.

Starting from the Single Star Full-Bridge, its structure can be depicted in Figure A.5. This configuration is utilizing a chain series of H-bridges, per each leg, while the three phase legs are connected in star. As can be seen in the figure, an arm inductor is used to connect each phase to the grid, in the PCC.

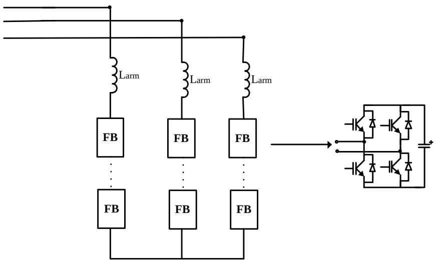

FIGURE A.5: Single Star Full-Bridge Structure.

One major disadvantage related to the operation of this configuration is that it needs the insertion of a zero sequence voltage equal to the phase voltage, when a negative sequence current is present, regardless of the amplitude of this current [48]. In order to be able to generate negative sequence current therefore, the converter's voltage rating has to be doubled [35]. This characteristic makes it unsuitable for modern STATCOM applications, where there is the need for controlling both the positive as well as the negative sequence reactive current. However, due to its high practicability, this configuration finds many applications in modern FACTS [3].

The Single Delta Full-Bridge (SD-FB) configuration is depicted in Figure A.6. This configuration is comprised by multiple Full Bridge cells connected in series, forming a delta branch. The connection to the PCC is achieved through a common mode inductor.

Similar to the SS-FB configuration, the SD-FB requires over-rating of the converter in order to achieve control of negative sequence reactive power [35]. In this case however, the current's rating should be increased according to the needs, since a zero sequence current needs to be injected to control the possible unbalance. In contrast to the SS-FB case, the amplitude of the injected zero

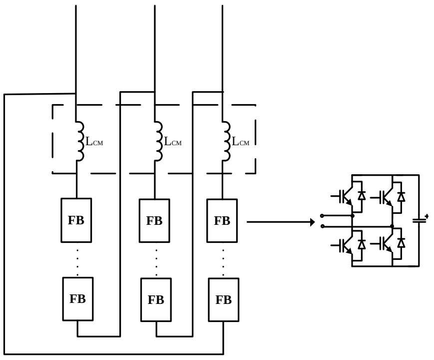

FIGURE A.6: Single Delta Full-Bridge Structure.

sequence current is proportional to the amplitude of the negative sequence current. Therefore, the needed current depends on the unbalance. Nevertheless, in order to control a $1pu$ negative sequence current with this configuration, an injection of $1pu$ zero sequence current is needed. This current will be circulating inside the delta connected branches, increasing the current flowing through the power devices.

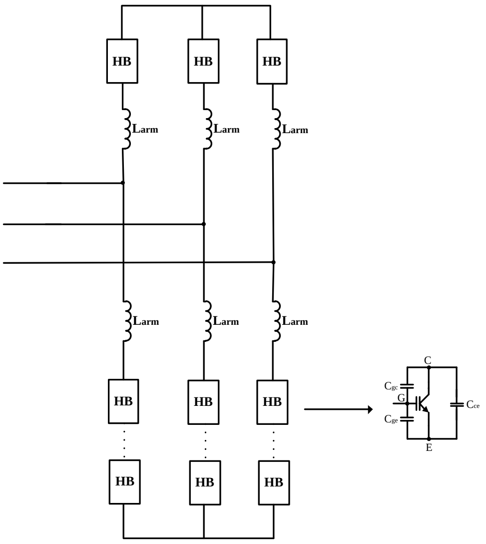

FIGURE A.7: Double Star Half-Bridge Structure.

As mentioned before, the focus of this report lies on the Double Star Half-Bridge (DS-HB) configuration which is depicted in Figure A.7. In this configuration, multiple half bridge cells are connected in series to form an arm. The topology is consisted of six arms in total, one upper and one lower arm per phase. The arms are connected through an arm inductor to the PCC and to the grid.

An advantage of this configuration that makes it attractive for STATCOM applications, is the fact that it can control the full negative sequence current ($1pu$) without the need to over-rate that converter's voltage or current. This is due to the presence of the circulating current, that flows between the converter's legs and exchanges energy between them. In this way, this zero-sequence current with proper control strategies, can be used to balance possible unbalances between the cells.

Finally, if the half-bridge modules are replaced by H-bridges, the DS-HB configuration becomes the DS-FB configuration. This configuration combines the advantages of the previous ones but is usually associated with high development cost and low practicability [3].

Appendix B

Symmetrical Components Theory

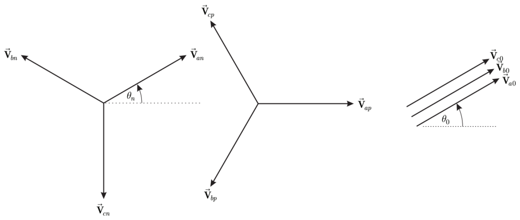

FIGURE B.1: Symmetrical components.

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According to basic symmetrical components theory, during asymmetrical conditions, every voltage or current can be expressed as a combination of positive, negative and zero sequence vectors [48]. These vectors are indicated and defined according to Figure B.1. The positive sequence phase voltages are can be written as in Equation B.1, taking the angle of the positive sequence phase-a voltage as a reference.

$$\begin{cases} u_{ap} = \hat{V}^{+} \cdot cos(\omega t) \\ u_{bp} = \hat{V}^{+} \cdot cos(\omega t - \frac{2\pi}{3}) \\ u_{cp} = \hat{V}^{+} \cdot cos(\omega t - \frac{4\pi}{3}) \end{cases} \tag{B.1}$$

In the general case, the negative sequence components have a different amplitude and are phase shifted with respect to the positive sequence, as shown in Figure B.1.

$$\begin{cases} u_{an} = \hat{V}^{-} \cdot cos(\omega t + \theta_n) \\ u_{bn} = \hat{V}^{-} \cdot cos(\omega t - \frac{4\pi}{3} + \theta_n) \\ u_{cn} = \hat{V}^{-} \cdot cos(\omega t - \frac{2\pi}{3} + \theta_n) \end{cases} \tag{B.2}$$

It should be noted that the positive sequence voltage vector is rotating in counter-clockwise direction whereas the negative sequence voltage vector in clockwise direction based on the above definitions. Finally, the zero-sequence set of voltages is expressed as in Equation B.3.

$$\begin{cases} u_{a0} = \hat{V}_0 \cdot cos(\omega t + \theta_0) \\ u_{b0} = \hat{V}_0 \cdot cos(\omega t + \theta_0) \\ u_{c0} = \hat{V}_0 \cdot cos(\omega t + \theta_0) \end{cases} \tag{B.3}$$

The three phase voltages can then be expressed as a combination of the positive, negative and zero sequence components as follows:

$$\begin{cases} \vec{V}_a = \vec{V}_{ap} + \vec{V}_{an} + \vec{V}_{a0} \\ \vec{V}_b = \vec{V}_{bp} + \vec{V}_{bn} + \vec{V}_{b0} \\ \vec{V}_c = \vec{V}_{cp} + \vec{V}_{cn} + \vec{V}_{c0} \end{cases} \tag{B.4}$$

By proper projection of the vectors and introducing the operator $\alpha = 1\angle\frac{2pi}{3}$ the phase voltage vectors can be expressed as a function of the sequence components in matrix form:

$$\begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \alpha^2 & \alpha & 1 \\ \alpha & \alpha^2 & 1 \end{bmatrix} \begin{bmatrix} \vec{V}_{ap} \\ \vec{V}_{an} \\ \vec{V}_{a0} \end{bmatrix} \tag{B.5}$$

After mathematical manipulations, and since the matrix in Equation B.5 is invertible, the symmetrical components can be expressed as a function of the phase voltages in matrix form as shown in Equations B.6, B.7, and B.8.

The positive sequence components are shown in Equation B.6:

$$\begin{bmatrix} \vec{V}_{ap} \\ \vec{V}_{bp} \\ \vec{V}_{cp} \end{bmatrix} = \underbrace{\frac{1}{3} \begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix}}_{T_p} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{B.6}$$

Proper manipulation and solving for negative sequence components yields:

$$\begin{bmatrix} \vec{V}_{an} \\ \vec{V}_{bn} \\ \vec{V}_{cn} \end{bmatrix} = \underbrace{\frac{1}{3} \begin{bmatrix} 1 & \alpha^2 & \alpha \\ \alpha & 1 & \alpha^2 \\ \alpha^2 & \alpha & 1 \end{bmatrix}}_{T_n} \begin{bmatrix} \vec{V}_a \\ \vec{V}_b \\ \vec{V}_c \end{bmatrix} \tag{B.7}$$

Finally, the zero sequence components could be expressed as:

$$\begin{bmatrix} \vec{V}_{a0} \\ \vec{V}_{b0} \\ \vec{V}_{c0} \end{bmatrix} = \underbrace{\frac{1}{3} \begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}}_{T_0} \begin{bmatrix} \vec{V}_{a} \\ \vec{V}_{b} \\ \vec{V}_{c} \end{bmatrix} \tag{B.8}$$

Losses and cost comparison of DS-HB and SD-FB MMC based large utility grade STATCOM

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Abstract— **Among the various multilevel converter topologies used in medium and high voltage grid applications, the Modular Multilevel Converter (MMC) has been the most promising since it combines good harmonic performance with low switching frequency and high reliability. A major concern however for inverter designers has been the associated cost due to the need for a large number of power devices and capacitors.**

This paper focuses on the application of MMC in transformer-less STATic synchronous COMpensators (STATCOMs). Initially, the double-star half bridge (DS-HB) and the single-delta full bridge (SD-FB) configurations are presented. Their specific components are designed in an analytical way followed by loss estimation. Finally, a comparison of the necessary components gives an insight of the total cost associated with each configuration.

Keywords— MMC STATCOM, HVDC, losses analysis, cost comparison

I. INTRODUCTION

Medium voltage and high voltage grid applications require the use of power devices with high blocking voltage capability. However high power devices are not commercially available for voltage ratings higher than 6.5 kV [1]. One possible solution would be the use of a transformer connected to the output of the inverter. These transformers are usually expensive and bulky, increasing significantly the cost of the system [1]. Consequently, multilevel topologies appear as the most promising solution for grid applications.

Among the various multilevel topologies that have been researched, the Modular Multilevel Converter (MMC) is considered as the next generation converter for medium and high voltage grid STATCOM applications. It combines excellent harmonic performance and low switching frequency with high reliability and design flexibility. In addition, high power quality is a major concern nowadays with the grid codes requiring efficient control of both positive-sequence and negative-sequence reactive power. In particular, the control of negative sequence reactive power is a crucial power quality requirement when non-linear loads, like arc furnaces, are present.

The MMC family is usually classified into four different configurations, described thoroughly in [2]:

- Single-Star Full Bridge (SS-FB);
- Single-Delta Full Bridge (SD-FB);
- Double-Star Half Bridge (DS-HB);
- Double-Star Bridge Cells (DS-FB).

The SS-FB configuration's ability to control negative-sequence reactive current is limited by the voltage rating of the converter, since it requires the injection of a zero-sequence voltage equal to the phase voltage [3]. This need for overdesigning the voltage rating by a factor of two makes it unsuitable for modern STATCOM applications. In addition, the DS-FB, despite its superiority over the other configurations, is usually not recommended due to the large number of power devices needed and its low practicability [1]. On the other hand, the SD-FB and the DS-HB appear as very attractive solutions for STATCOM applications due to their ability to control both positive and negative sequence reactive power in a large operating range [2].

In this paper, the SD-FB and DS-FB configurations will be initially presented and their components will be analytically designed for a STATCOM application that is able to control *1 pu* negative-sequence reactive power. A loss calculation will follow, based on the power device manufacturer's datasheets. Finally, a comparison of the necessary components and the associated capital and operational expenditures will take place. The final purpose of this work is to point at the preferred MMC configuration choice for large utility grade STATCOM applications.

II. MMC CONFIGURATIONS

The SD-FB configuration in a STATCOM application was evaluated in [4]. The complete circuit configuration is shown in Fig. 1, where the MMC is connected through the inductors L_{ac} to the three-phase grid. Multiple single-phase H-bridge cells are cascaded to form a branch. The three branches are connected in a delta configuration through the coupled inductors L_{CM}. As mentioned in the introduction, one advantage of this configuration is that the circulating current can be used to allow energy exchange between the phase legs

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and thereby can be used under unbalanced conditions. However, this configuration can only control the full negative sequence reactive power (*1pu*) when it is designed for a current rating of *2 pu*, since a zero-sequence component current equal to the negative sequence injected current, needs to circulated between the delta connected branches [5].

Fig. 2 depicts the DS-HB configuration in a STATCOM application. In this case, multiple bidirectional chopper cells, are cascaded to form a converter arm. The upper and lower arms of each phase are connected through two arm inductors to the PCC. The performance of this topology was evaluated in [2]. As in the SD-FB configuration, the presence of the circulating current makes the DS-HB configuration very attractive for STATCOM applications. Furthermore, in contrast to the SD-FB, the DS-HB can be used to control the full negative-sequence reactive power (*1pu*) without increasing the conduction losses of the system and without the need to over-design the converter's components. The circulating current between the converter legs for this configuration is negligible in comparison to the negative sequence current that is injected. Thus, the total arm current is not a function of the negative sequence current as in the SD-FB topology.

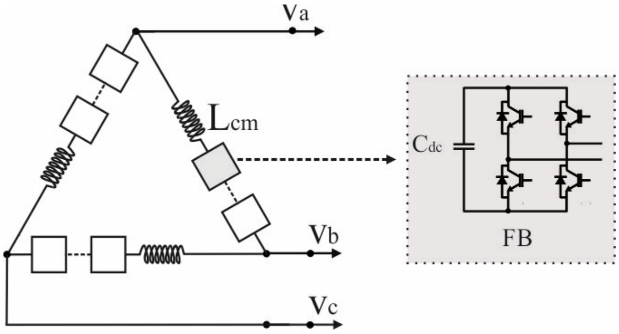

Figure 1: Single Delta – Full Bridge STATCOM configuration

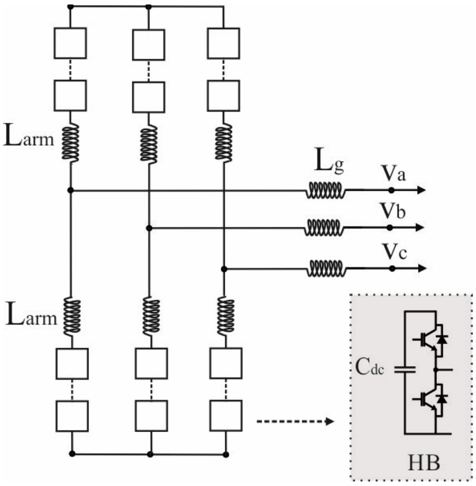

Figure 2: Double Star – Half Bridge STATCOM configuration

III. TOPOLOGIES DESIGN

A. Number of submodules

Although in both studied topologies, no physical dc-link is present, the methodology used in traditional 2L-VSC can be adapted. The necessary effective dc-bus voltage is calculated and it is divided by the submodule's (SM) capacitor voltage, obtaining the number of SM per arm/branch.

The calculation of the minimum dc-bus voltage is based on the following points [1]:

- Output impedance of STATCOM is considered 8 % with a variation of 5 % around this value;
- Grid voltage can change 5 %;
- DC-bus voltage presents in the worst case 10 % of ripple and a constant error of 3 % in steady-state.

Based on these assumptions, the maximum voltage synthetized by the STATCOM is given by:

$$V_s = 1.05 \times (1 + 0.08 \times 1.05)V_g = 1.139V_g \tag{1}$$

where V_s is the line voltage synthetized by the STATCOM and V_g is the PCC line voltage. Considering a modulation factor equal to 1.104 [1], for delta topology:

$$\lambda_{max} = \frac{\sqrt{2}V_s}{1.104 \cdot (0.97 - 0.1)V_{dc,\Delta}} \tag{2}$$

where λ_{max} is the maximum modulation index of the converter. For Double-Star topology, the maximum modulation index is defined as:

$$\lambda_{max} = \frac{2}{\sqrt{3}} \frac{\sqrt{2}V_s}{1.104 \cdot (0.97 - 0.1)V_{dc,DY}} \tag{3}$$

Considering the IGBT's switching frequency equal to 360 Hz and 1.5 μs for the minimum on-time and dead-time, it is possible to obtain a maximum modulation index of $\lambda_{max} = 0.9968$. Therefore, the dc-voltage necessary for each topology is:

$$V_{dc,\Delta} = 55.45kV \tag{4}$$

$$V_{dc,DY} = 64.16\ kV. \tag{5}$$

An Infineon IGBT part number (FF600R17) of 1.7kV-600A, is chosen for this application. The operating voltage is chosen to be 0.9kV [6], and 10% of SM redundancy is added [7]. Thus, the number of SM per branch in Delta topology is:

$$N_\Delta = 68, \tag{6}$$

and the number of SM per arm in Double-Star topology is:

$$N_{DY} = 79. \tag{7}$$

B. Capacitor design

The cell capacitance selection is a trade-off between sub-module voltage requirements and capacitor size. The total cell capacitance is generally defined between 30–45 kJ per MVA of converter, and a methodology to calculate the capacitance value, based on energy storage requirements is presented in [8].

For delta topology, the methodology proposed by [1] is used. The dc bus voltage ripple becomes maximum when a purely reactive current flows. Therefore:

$$\int_0^{\frac{T}{4}} V_{rms} I_{rms} sin(2\omega t) = \frac{1}{2} C\left(V_{dc,\Delta max}^2 - V_{dc,\Delta min}^2\right) \tag{8}$$

where V_{rms} is the RMS value of the ac voltage per submodule and I_{rms} is the RMS current. This way, the submodule capacitance can be calculated by:

$$C_{dc,\Delta} = \frac{V_{rms} I_{rms}}{2\omega V_{dcsm,\Delta} \Delta V_{dc,\Delta}} \tag{9}$$

Considering the converter's parameters shown in Table I, the SM capacitor value in Delta topology is $C_{dc,\Delta} = 38.5mF$. For Double-Star topology, reference [6] proposes a methodology based on minimum storage energy requirements. Thus, the submodule capacitance can be determined by:

$$C_{dc,2Y} = \frac{2NE_{nom}}{V_{dc,DY}^2} \tag{10}$$

where E_{nom} is the nominal energy storage per arm.

Considering the system injecting nominal reactive power into the grid with the maximum modulation index, the required nominal energy storage in the converter per transferred VA is approximately, 42 kJ/MVA [8]. This way, the nominal energy storage by arm is given by:

$$E_{nom} = \frac{42\, kJ/MVA \cdot 100MVA}{6} = 700\ kJ \tag{3}$$

Using this value of nominal energy storage by arm, the necessary capacitance per submodule is found to be $C_{dc,DY} = 26.2mF$.

C. Inductor design

In MMC topologies, inductors are placed in the converter arms to suppress transients in the circulating [9] and limit fault currents [10]. For grid-connected applications, suitable values of the arm inductors could very well be in the range of 0.1 p.u. In DS-HB topology a value of 28 % for the arm inductor is chosen, as used in [8]. In SD-FB topology, a common mode inductor of 37 % is used while the ac link inductor is 8 % [4].

IV. LOSSES ANALYSIS

At this point, an estimation of the switching losses will be made for the configurations that were designed in the previous sections. The devices are considered to be operating with a junction temperature of 125°C. The gate resistance is considered to be 1 Ω and the gate bias is ±15 V.

The loss estimation is based on a simple model that takes into account the instantaneous current flowing through the submodule and data found in the device datasheet, as shown in Fig. 3. It should be noted that in the case of the SD-FB, unipolar PWM is considered.

The IGBT's voltage drop as well as the diode's forward voltage drop is expressed as a function of the current, resulting in the total conduction losses of each cell as shown in Fig. 3. Similarly, the turn on and turn off along with the reverse recovery energy losses are expressed as a function of the current, resulting in the switching losses of the IGBT and diode respectively [6]. Due to the symmetry ensured by PS-PWM, the result can be extended for all the submodules. The current is considered to be sinusoidal, leading 90˚ the phase voltage.

TABLE I. SPECIFICATIONS OF MMC INVERTER

	Topologies		
	Description	***DS-HB*** [a]	***SD-FB*** [b]
N	Number of SM	79 (\arm)	68 (\branch)
C_{dc}	SM capacitance (mF)	26.2	38.5
L_{arm}	Arm inductor	9.7 mH (28% [a])	-
L_{cm}	Common mode inductor	-	6.4 mH (37% [b])
L_g	AC-link inductor	-	1.4 mH (8% [b])
S	Rated power (MVA)	100	200
V_{SM}	Sub-module voltage (kV)	0.9	0.9
f_{sw}	Switching frequency (Hz)	360	360
f	Grid frequency (Hz)	50	50
f_{swe}	Effective switching frequency (kHz)	56.88	48.96
V_{grid}	Grid voltage (kV)	33	33
I_g	Injected nominal current	1750	3500
I_{SM}	SM RMS current (A)	875	2020
IGBT	IGBT in parallel	2	4

[a] 33kV, 100MVA, and 50-Hz base; [b] 33kV, 200MVA, and 50-Hz base;

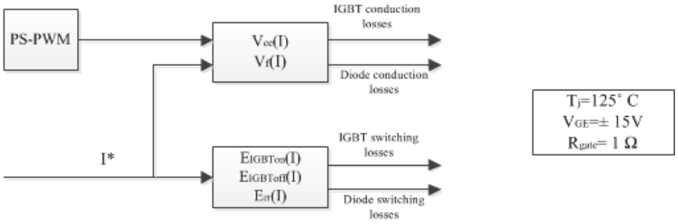

Figure 3: Model Based Loss Estimation

The switching losses depend on the operating conditions and the amount of negative sequence current injection. As noted before, the DS-HB uses a small amount of DC circulating current in order to control the negative sequence current. This means that in all cases, *1 pu* power is translated into *1 pu* current for the DS-HB configuration. On the other hand, the SD-FB configuration requires the injection of a zero sequence component equal to the amount of negative sequence current [5], increasing the switching losses. Table II depicts the losses when *1 pu* positive sequence reactive power is exchanged with the grid.

TABLE II. LOSS COMPARISON FOR *1PU* POSITIVE SEQUENCE INJECTION

	Conduction Losses (kW)	***Switching Losses (kW)***	***Total Losses (kW)***
DS-HB	750.8	141.6	892.4
SD-FB	782.9	272.1	1055

Table II shows that even when no negative sequence current is exchanged, the efficiency of the DS-HB configuration is slightly higher (99.11% instead of 98.96%) than the SD-FB. This is however normal since the SD-FB converter was overdesigned by a factor of two in order to be able to control full negative sequence reactive power.

Fig. 4 breaks down the losses into IGBT and diode losses for the two configurations. The conduction losses are similar in both cases, but due to the higher number of IGBT and diode parts, the amount of the devices that switch is higher in the SD-FB configuration, leading to higher switching losses.

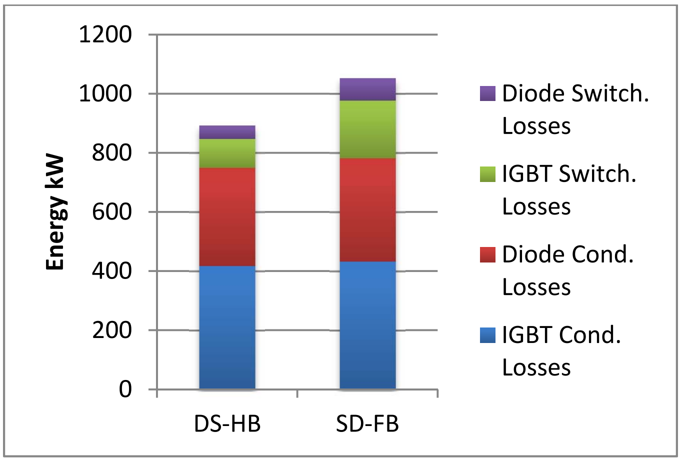

Figure 4: Losses of IGBT and Diode comparison for 1 pu positive sequence reactive power injection.

In Fig. 5 the switching losses of the two compared topologies are shown as a function of the negative sequence reactive power Q_n, respecting always that the total exchanged reactive power is: $Q_p + Q_n = 1\,pu$, with Q_p being the positive sequence reactive power.

As can be deduced by Fig. 5, the total losses in the case of the DS-HB are independent of the amount of exchanged negative sequence reactive power, due to the negligible circulating current that is needed in order to keep each phase balanced. On the other hand, the total current needed in the SD-FB is increasing linearly with the increase of the negative sequence reactive power. As a result, the conduction losses increase, reducing the efficiency of the converter system. Particularly in the case of 1 pu negative sequence reactive power, the efficiency of the SD-FB configuration drops to approximately 98%. It should be noted that this analysis accounts only for the losses of the switches and does not take into consideration the losses on the arm inductors, which are considered to be ideal.

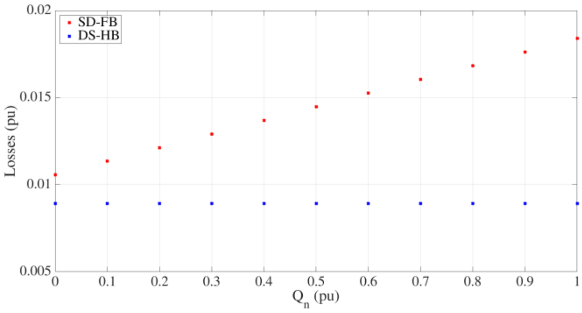

Figure 5: Loss Comparison as a function of Q_n.

Concluding the loss analysis section, Table III depicts the losses when *1 pu* negative sequence reactive power is exchanged with the grid. As expected the high current results in almost double losses for the SD-FB configuration.

TABLE III. LOSS COMPARISON FOR FULL NEGATIVE SEQUENCE INJECTION

	Conduction Losses (kW)	***Switching Losses (kW)***	***Total Losses (kW)***
DS-HB	750.8	141.6	892.4
SD-FB	1596	285.6	1881.6

V. COST ANALYSIS

In this section, an estimation of the total cost of the two compared configuration will take place. The total cost will be broken down to capital expenditure (CAPEX) and operational expenditure (OPEX). The initial cost is based on the number of components required and the price per part number. For the current analysis the cost of the power electronic modules as well as the price of the capacitor banks will be considered, since all the other components are considered to account only for a small percentage of the total cost.

An overview of the most important components that each configuration utilizes is shown in Table IV. The DS-HB requires less power modules but on the other hand has greater energy storage requirements. For the completeness of the analysis, the number of gate driver units, current sensors and voltage sensors is also included, although these components only account for a minor part of the total cost.

For a more detailed evaluation of the cost, the capacitors have to be chosen carefully for each configuration. As pointed out in the section III.B, the two configurations were designed with low cost power modules. This choice however has led to large energy storage requirements, making the capacitor cost dominant. It should be clarified that in this paper *1 unit* is equivalent to *1000 £*. From now on, all costs will be measured in units.

TABLE IV. SPECIFICATIONS OF MMC INVERTER

Component	**Quantity**	
	DS-HB	***SD-FB***
IGBT	1896	3264
Gate Drive Unit	948	816
Capacitor [kJ]	4200	3183
Current Sensor	6	3
Voltage Sensor	3	3

Aluminum Electrolytic Capacitors are chosen for this application [11]. The rated voltage of the chosen capacitors is *500 V* so two of them need to be connected in series. The resulting capacitance drops then to *3.4 mF*. For the DS-HB configuration 16 capacitors are required per submodule while for the SD-HB configuration 22 of these capacitors are required per submodule. The initial cost per submodule is then normalized and calculated as shown in Table V.

TABLE V. COST PER SUBMODULE

Component	**Quantity**	
	DS-HB	***SD-FB***
Module Cost (units)	0.48	1.92
Capacitor Cost (units)	1.4	1.93
Total Cost (units)	**1.88**	**2.85**

In the case of the SD-FB, it is worth noting that the development cost of one submodule is shared equally between the cost for the power module and the capacitors, despite the fact that low cost power modules were used. On the other hand, in the DS-HB configuration, the capacitor cost is by far the dominant one.

Fig. 6 gives an insight of the capital expenditure of the two configurations as well as the cost distribution between the power module and the capacitors for each case. It is very interesting to notice that the DS-HB configuration despite the significantly lower power device cost, resulted in approximately 14% higher CAPEX due to the high energy storage requirements that account for 75% of its CAPEX.

The operational cost, especially for large utility grade applications, is significant. The analysis of the operational cost (OPEX) will be based on the cost per kilowatt-hour along with the operational losses. In the case of the DS-HB the operational cost is independent of the amount of negative sequence injection while the SD-FB operational cost will increase linearly as the negative sequence reactive power is increased.

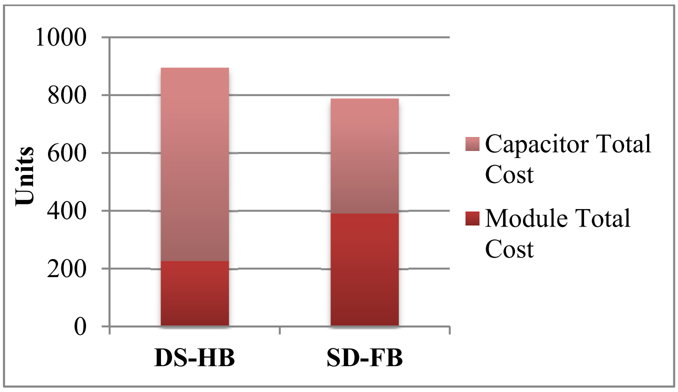

Figure 6: Total capital expenditure comparison of the discussed configurations.

The average price per kilowatt-hour is taken according to official statistics for 2015 for the countries inside the Eurozone (~0.12 €/kWh) and is then converted to units. The expected lifetime of the converter system is assumed to be 10 years of operation with the rated power and a duty factor of 10%.

Fig. 7 adds the operational cost (OPEX) of the two configurations to the previously extracted capital expenditure (CAPEX). In this graph the STATCOM is assumed to be providing only positive sequence reactive power which is the best case scenario for the SD-FB configuration.

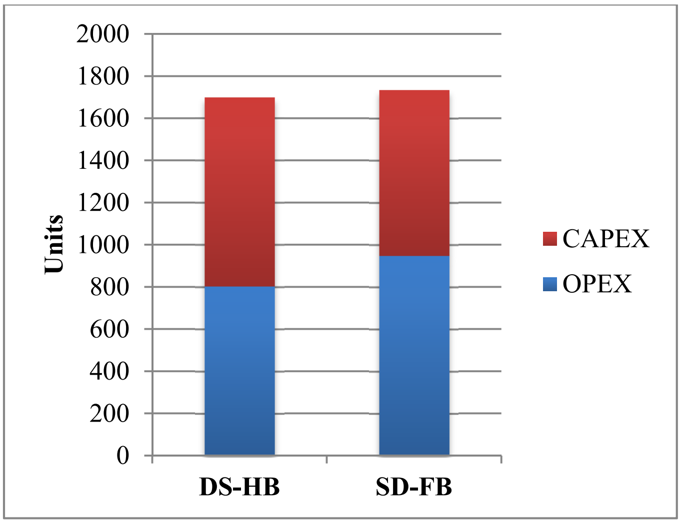

Figure 7: Total cost comparison of the discussed configurations for 10 years operation with rated power.

It is clear in Fig.7 that the higher losses in the SD-FB configuration increase the operational cost that finally even with the best case scenario of injecting only positive sequence current, the total cost of this configuration is slightly higher in comparison to the DS-HB converter. A more realistic scenario of injection would result in further increase in the operational cost of the DS-FB converter, as discussed previously.

Finally, Fig. 8 shows the total cost in units as a function of the time in years for both configurations. It can be seen that in the best case scenario when only positive sequence injection is considered, the DS-HB becomes more profitable after approximately 7.5 years of operation.

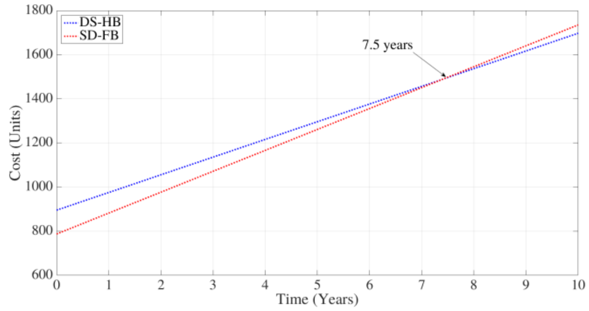

Figure 8: Total cost comparison per year.

VI. DISCUSSION

In this paper, an in depth comparison of the DS-HB and SD-FB configuration in their application as large utility grade STATCOMs, able to control *1 pu* negative sequence reactive power, was made. It should be highlighted that the current analysis used a low-cost 1.7kV commercial IGBT. These devices are known for their low price/MVA ratio, their low switching times that allow higher maximum modulation indexes and lower switching losses in comparison to their MV counterparts. On the other hand, this choice leads to the need for large capacitors that as shown in the cost analysis section, dominate the capital expenditure of the discussed topologies

A final evaluation of the two topologies in terms of losses and cost is shown in radar diagram form in Fig. 9 that follows. In this Figure, PSI stands for positive sequence injection and NSI for negative sequence injection.

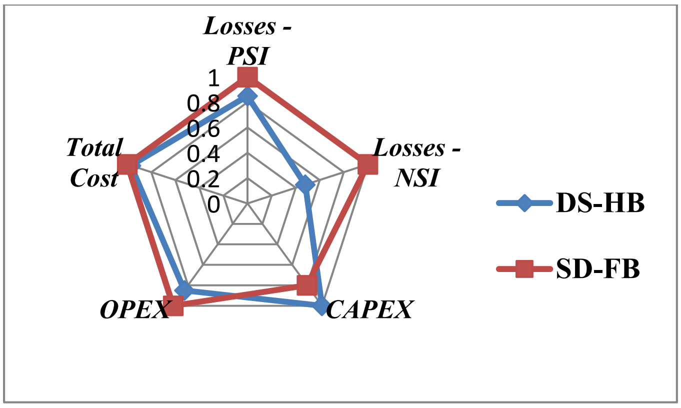

Figure 9: Performance evaluation of the discussed configurations

Based on the conducted analysis it can be concluded that the DS-HB is the preferred topology for a STATCOM application when the full negative sequence current needs to be exchanged with the grid. Finally, it should be highlighted that many components that are associated with the CAPEX were left outside of the cost analysis and may significantly increase the initial cost. The exact estimation of the total cost however was outside of the scope of this paper that aimed to compare the discussed topologies.

REFERENCES

[1] K. Fujii, U. Schwarzer, R.W. de Doncker, "Comparison of Hard-Switched Multi-Level Inverter Topologies for STATCOM by Loss-Implemented Simulation and Cost Estimation," *in Power Electronics Specialists Conference*, pp.340–346, 2005.

[2] M. Hagiwara, R. Maeda and H. Akagi "Theoretical Analysis and Control of the Modular Multilevel Cascade Converter Based on Double-Star Chopper-Cells (MMCC-DSCC) ", *Conf. Rec. IPEC-Sapporo*, 2010.

[3] Betz R, Summers T.: "Introduction to Symmetrical Components and their use in STATCOM Applications", ResTech Pty Ltd School of Electrical Engineering and Computer Science University of Newcastle, Australia 2009.

[4] M. Hagiwara, R. Maeda and H. Akagi "Negative-Sequence Reactive-Power Control by a PWM STATCOM Based on a Modular Multilevel Cascade Converter (MMCC-SDBC)", *Energy Conversion Congress and Exposition (ECCE), IEEE*, pp. 3728-3735, 2011.

[5] E. Behrouzian, M. Bongiorno and H. Z. De La Parra, "Investigation of negative sequence injection capability in H-bridge multilevel STATCOM," *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, Lappeenranta, 2014, pp. 1-10.

[6] Infineon IGBT, *FF600R17ME4*.

[7] N. Ahmed, L. Angquist, A. Antonopoulos, L. Harnefors, S. Norrga, H.S. Nee, "Performance of the modular multilevel converter with redundant submodules", in *Industrial Electronics Society*, 2015

[8] K. Ilves, S. Norrga, L. Harnefors, and H.-P. Nee, "On energy storage requirements in modular multilevel converters", *IEEE Trans. Power Electron., vol. 29, no. 1*, pp. 77–88, Jan. 2014.

[9] J. Kolb, F. Kammerer, and M. Braun, "Dimensioning and design of a modular multilevel converter for drive applications", in *Proc. 15th Int. Power Electron. Motion Control Conf.*, pp. 1–8, 2012.

[10] Q. Tu, Z. Xu, H. Huang, and J. Zhang, "Parameter design principle of the arm inductor in modular multilevel converter based HVDC", in Proc. *International Conference on Power System Technology*, pp. 1–6, 2010.

[11] Kemet, ALS 30/31 Series, *ALS30A682NT500*.

Capacitor voltage ripple reduction and arm energy balancing in MMC-HVDC

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***Abstract*—Modular Multilevel Converters are emerging and widely used in HVDC applications. However, the submodule capacitors are still large and the energy balancing under unbalanced conditions is a challenge. In this paper, an analytical model focusing on the energy stored in the capacitors and voltage variations is utilized in order to achieve better performance. By injecting a second order harmonic component into the circulating current, the energy variation and consequently the capacitor voltage ripple is reduced allowing for a capacitor size reduction. At the same time, an arm energy balancing controller has been proposed which uses the first harmonic of the circulating current in order to keep the energy balance of the leg under internal unbalanced conditions.**

Keywords - Modular Multilevel Converter(MMC), High-voltage direct-current(HVDC), capacitor voltage ripple, circulating current, arm balancing, second harmonic injection, energy controller.

NOMENCLATURE

The upper and lower arms of the converter in Fig.1, are denoted with the subscripts u and l respectively. An expression which is valid for either of the arms is denoted with the subscript u, l.

M	Number of phases
m	Phase index for phases a,b,c
L_{arm}	Arm Inductance
R_{arm}	Parasitic arm resistance
v_d	DC-link voltage
i_d	DC-link current
$i_{u,l}$	Arm currents
i_s	Output current
i_c	Circulating current
v_s	Output voltage (driving i_s)
v_c	Internal voltage (driving i_c)
ω	Fundamental angular frequency
ϕ_i	Load angle
i_{c1m}	fundamental frequency component of i_c
i_{c2m}	second harmonic component of i_c
$\Delta v^{\Sigma}_{c_{u,l}}$	Arm voltage ripple

I. INTRODUCTION

Modular Multilevel Converters (MMCs) have gained researcher's attention due to their ability to handle high voltage and power ratings. VSC HVDC is getting increasingly important for integrating renewable energy sources such as large offshore wind farms, providing flexible interconnection between two weak AC grid network using back-to-back configuration, or simply transmitting power using underground cables [1].

MMCs provide several advantages in comparison to the conventional converter systems, featuring modular design, high efficiency and low harmonic distortion at the output side. Analytical investigations have been carried out notifying the effects of the internal dynamics of the MMC, specifically on the sum capacitor voltages and circulating current as well as on the output leg power [2] [3]. An important point to consider is the circulating current within each phase-leg of the MMC, which if it is not properly controlled, it can have adverse impact on semiconductor ratings, losses as well as on the magnitude of the capacitor voltage ripple.

This paper focuses on an cost effective approach of reducing the capacitor voltage ripple. A strategy of injecting an AC second harmonic component in the circulating current is proposed to ensure the reduction of energy variation between the upper and lower arm. An arm balancing strategy is also implemented to effectively keep the system balanced under unbalanced conditions.

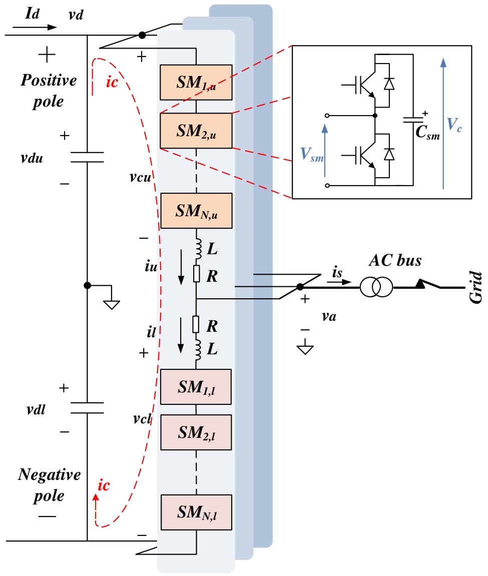

Fig. 1: Three-phase schematic of MMC.

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II. BASICS OF MMC

An MMC consists of several series connected submodules, that can be referred as cells, as it is illustrated in Fig.1. There are two arms per phase, which are referred as the upper and lower arms. The upper arms of the M phases are connected to the positive pole and similarly the lower arms are connected to the negative pole of the DC link. The arm inductors installed on each arm of the MMC functions as a filter to attenuate the high-frequency harmonics in the arm currents and to limit the rate of current rise during faults. [1].

The symmetric configuration yields:

$$v_{du} = v_{dl} = \frac{v_d}{2} \tag{1}$$

and as shown in Fig.2 the output and circulating current are defined as:

$$i_s = i_u - i_l \qquad \text{and} \qquad i_c = \frac{i_u + i_l}{2} \tag{2}$$

By manipulating the above introduced two equations a relation between the arm currents with the output and circulating currents can be deduced as:

$$i_u = \frac{i_s}{2} + i_c \qquad \text{and} \qquad i_l = -\frac{i_s}{2} + i_c \tag{3}$$

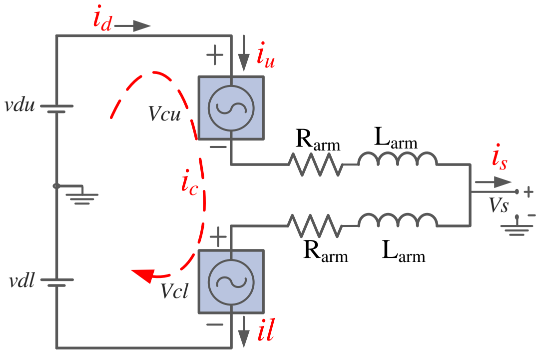

Fig. 2: Average Model of MMC

Under balanced conditions, in order to obtain a constant DC bus voltage and to keep the converter losses and RMS value of the arm currents low, the mean values of the circulating current should only contain a DC component inferring [8]:

$$\overline{i_u} = \overline{i_l} = \overline{i_c} = \frac{i_d}{M} \tag{4}$$

By analyzing the mathematical model and applying Kirchhoff's Voltage Law to each arm of three phases of MMC, the AC side voltage equation yields to:

$$v_a = \frac{v_d}{2} - v_{cu} - R_{arm} i_u - L_{arm} \frac{di_u}{dt} \tag{5}$$

$$v_a = -\frac{v_d}{2} + v_{cl} + R_{arm} i_l + L_{arm} \frac{di_l}{dt} \tag{6}$$

By adding (5) and (6), the output voltage can be defined as:

$$v_s = \frac{v_{cl} - v_{cu}}{2} \tag{7}$$

Similarly, by subtraction of (5) and (6), the internal voltage can be expressed as:

$$v_c = \frac{v_d - v_{cl} - v_{cu}}{2} \tag{8}$$

After proper manipulation of the equations, the sum and difference of the instantaneous power can be expressed as:

$$\frac{dW_\Sigma}{dt} = 2v_c i_c - v_s i_s \qquad \text{and} \qquad \frac{dW_\triangle}{dt} = v_c i_s - 2v_s i_c \tag{9}$$

Assuming the circulating current to a DC value and considering v_s and i_s to be perfect sinusoidal signals:

$$\frac{dW_\Sigma}{dt} = v_d i_c - \frac{\hat{V}_s \hat{I}_s}{2} \cos\phi_i - \frac{\hat{V}_s \hat{I}_s}{2} \cos(2\omega t - \phi_i) \tag{10}$$

$$\frac{dW_\triangle}{dt} = \frac{v_d \hat{I}_s}{2} \cos(\omega t - \phi_i) - 2\hat{V}_s i_c cos(\omega t) \tag{11}$$

Further, integrating (10) and (11) and considering balanced conditions, where the input DC power equals the total phase output AC power(neglecting losses), the equations can be simplified to:

$$W_\Sigma = \frac{C{v_d}^2}{N} - \triangle W_\Sigma \qquad \text{and} \qquad W_\triangle = W_{\triangle 0} + \triangle W_\triangle \tag{12}$$

After some more mathematical manipulations, the sum and the difference of the capacitor voltages in a leg can be expressed as [2]:

$$v_c^\Sigma = v_{cu}^\Sigma + v_{cl}^\Sigma = 2v_d + \frac{N}{Cv_d} \triangle W_\Sigma \tag{13}$$

$$v_c^\triangle = v_{cu}^\Sigma - v_{cl}^\Sigma = \frac{N}{Cv_d} \triangle W_\triangle \tag{14}$$

III. MINIMIZATION OF ENERGY VARIATION IN THE LEG

The power in the leg of a MMC should have a zero average value over one fundamental cycle in order to keep the capacitor average voltages constant, implying that the entire power from the DC bus is transferred to the AC bus within one cycle. However, considering the leg power equation from (10), it is observed that in order to obtain a zero average power, the two DC terms have to be equal, ensuring the balance between the DC and AC average power [3].

$$I_{c0m} = \frac{\hat{V}_{sm} \hat{I}_{sm}}{2 \cdot v_d} \tag{15}$$

As stated in (10), the instantaneous leg power is composed of three terms, where the first two refers to the DC and AC active power components per phase respectively and the third term represents an instantaneous oscillating power component with the second harmonic ($\frac{\hat{V}_s \hat{I}_s}{2} \cos(2\omega t - \phi_i)$), which needs to be canceled out for (10) to be zero. This can be achieved by injecting an alternating current with negative sequence to

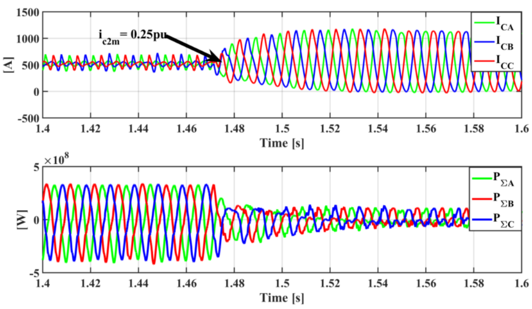

Fig. 3: (a) Circulating Current (b) Instantaneous leg Power.

the reference of the circulating current control as shown in Fig.(3) [6].

The generic form of the injected negative sequence current can be expressed as:

$$i_{c2m} = \hat{I}^{-}_{c2m} cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi^{-}_{c2}) \quad (16)$$

Thus, the total circulating current will be:

$$i_{cm} = I_{c0m} + i_{c2m} \quad (17)$$

Substituting (17) in (10) and solving for $\hat{I}^{-}_{c2m}$ yields to:

$$\frac{dW_\Sigma}{dt} = 2\cdot v_c I_{c0m} + 2\cdot v_c \hat{I}^{-}_{c2m} cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi^{-}_{c2}) - [\frac{\hat{V}_{sm}\hat{I}_{sm}}{2} cos\phi_i + \frac{\hat{V}_{sm}\hat{I}_{sm}}{2} cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi_i)] \quad (18)$$

$$\hat{I}^{-}_{c2m} = \frac{\hat{V}_{sm}\hat{I}_{sm} 2cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi_i)}{2\cdot v_c cos(2\omega_1 t + \frac{2\pi(m-1)}{3} - \phi^{-}_{c2})} \quad (19)$$

In order to eliminate the second order harmonic terms and have an amplitude of $\hat{I}^{-}_{c2m}$ constant, the injected second harmonic signal angle is chosen to be equal to the load angle (ϕ_i=ϕ^{-}_{c2}), resulting in:

$$\hat{I}^{-}_{c2m} = \frac{\hat{V}_{sm}\hat{I}_{sm}}{2\cdot v_d} \quad (20)$$

The effect of the injected negative sequence current can also be seen in the sum capacitor voltage ripple. Substituting (17) in (11), and with mathematical manipulations shown below, it can be observed that the magnitude of the fundamental component of $v^{\triangle}_c$ is reduced as expressed in (14):

$$\frac{dW_\triangle}{dt} = v_c \cdot \left\{ \hat{I}_{sm} cos(\omega_1 t - \frac{2\pi(m-1)}{3} - \phi_i) \right\} - 2\cdot \hat{V}_{sm}\cdot I_{c0m} cos(\omega_1 t - \frac{2\pi(m-1)}{3}) - \hat{V}_{sm}\cdot \hat{I}^{-}_{c2m} cos(3\omega_1 t - \phi^{-}_{c2}) - \hat{V}_{sm}\cdot \hat{I}^{-}_{c2m} cos(\omega_1 t - \frac{2\pi(m-1)}{3} - \phi^{-}_{c2}) \quad (21)$$

Thus, on further integration of (21) energy imbalance equation can be obtained as:

$$W_\triangle = W_{\triangle 0} + \triangle W_\triangle \quad (22)$$

Choosing (ϕ_i=ϕ^{-}_{c2}) as above and from the aforementioned equation of (22), information about $\triangle W_\triangle$ can be extracted as expressed below:

$$\triangle W_\triangle = \left\{ \frac{v_d\cdot \hat{I}_{sm}}{2\omega_1} - \frac{\hat{V}_{sm}\cdot\hat{V}_{sm}\cdot\hat{I}_{sm}}{\omega_1\cdot v_d} - \frac{\hat{V}_{sm}\cdot\hat{V}_{sm}\cdot\hat{I}_{sm}}{2\omega_1\cdot v_d} \right\} \left\{ sin(\omega_1 t - \frac{2\pi(m-1)}{3}) \right\} \quad (23)$$

The ripple equation for the upper and lower arm capacitor voltages can be given by:

$$\Delta v^{\Sigma}_{cu} = \frac{N}{2Cv_d}(\Delta W_\Sigma + \Delta W_\Delta) \quad (24)$$

$$\Delta v^{\Sigma}_{cl} = \frac{N}{2Cv_d}(\Delta W_\Sigma - \Delta W_\Delta) \quad (25)$$

Since, $\triangle W_\triangle$ is directly proportional to $\Delta v^{\Sigma}_{cu,l}$ as seen in (24) and (25), it can be concluded that the injected second harmonic signal is not only useful in eliminating the double frequency oscillating term from the leg power, but also is able to reduce the capacitor voltage ripple.

A simulation model of the converter topology presented in Fig.1 with the parameters shown in Table III has been built in PLECS in order to validate the above presented mathematical analysis. The effect of the suppression of the AC components from the circulating current are presented in Fig.4(b).

Parameters	Notation	Value
P(MW)	Active Power	1000
N_{arm}	Submodules/arm	40
V_{dc}(kV)	Direct voltage	640
C_{sm}(mF)	Capacitance	1.25
L_{arm}(mH)	Arm Inductance	20
V_g(kV)(l-l)rms	Alternating voltage	400
f(Hz)	Rated frequency	50

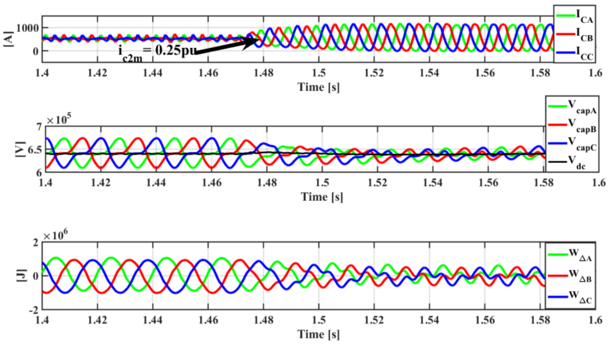

Fig. 4: (a) Circulating Current (b) Upper arm capacitor voltages (c) Leg energy difference.

It is to be noted that the amplitude of second harmonic injected current as shown in (20) and assuming $\hat{V}_{sm} = \frac{v_d}{2}$ is around 0.25 times the peak value of output current($\hat{I}_{sm}$) which is considered to be the optimum injected current. Relating

($\hat{I}_{sm}$) with respect to i_c, it can be seen from Fig.6 and from mathematical calculations based on (2) and (3) that with the injected i_{c2m}, the rms value of the arm currents increases by 7% of the peak output current i.e from($0.40pu$ to $0.47pu$) which can be validated in Fig 5. This results in a minor increase in the stress and rating of the switches in the submodules due to an increase in the conduction losses, thus inferring an increase in the operational cost and decrease in efficiency.

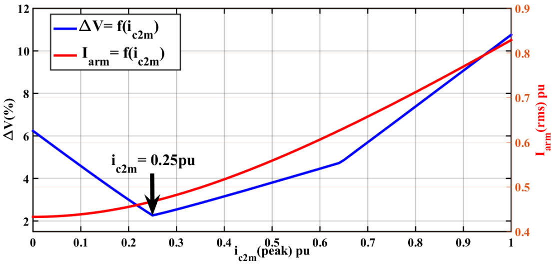

Fig. 5: Voltage ripple and arm currents as a function of (i_{c2m})

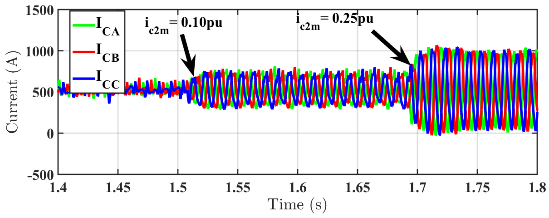

Fig. 6: Circulating current with and without injection of (i_{c2m})

From (26) it can be noted that by injecting a circulating current equivalent to 0.25pu of peak output current the second harmonic component term i.e (ΔW_{Σ}) from (24) and (25) can be eliminated inferring that the $50Hz$ ripple in the cell capacitors only depends on ΔW_{Δ}. Thus, voltage ripple as a function of the injected circulating current can be expressed as:

$$\Delta V = \frac{N}{Cv_d} \cdot \frac{v_d \hat{I}_s}{2\omega}[(X - 0.25)sin(2\omega t) + (0.5 - X)sin(\omega t) + \frac{X}{3}sin(3\omega t)] \quad (26)$$

where,

$$i_{c2m} = X \cdot \hat{I}_s \quad (0 < X \leq 0.25) \quad (27)$$

From the above proposed conjecture, the minimization of the energy variation and reduction in the voltage ripple of cell capacitors can be done as showcased in Fig.8. This makes possible more reduction in the capacitance value which could prove to be size and cost effective. A graph displaying voltage ripple as a function of capacitance can be seen in Fig.7 where the system was designed for 5% of voltage ripple as a common design requirement.

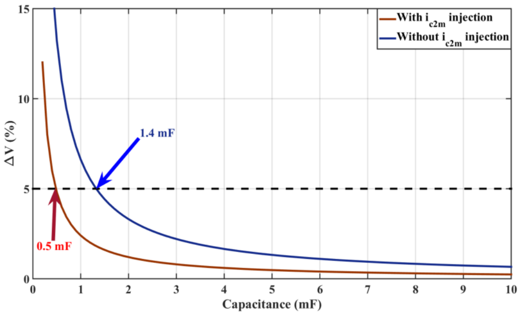

Fig. 7: Voltage ripple as a function of capacitance

Thus from the above information, an optimum solution can be obtained taking into consideration the voltage ripple as a function of efficiency i.e. (injection of i_{c2m}) on one hand and capacitor cost and size on the other.

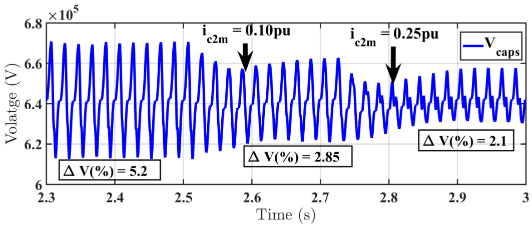

Fig. 8: Capacitor voltages showcasing ripple with and without (i_{c2m})

IV. ARM BALANCING STRATEGY UNDER UNBALANCED CONDITIONS

In the previous section, a strategy for the minimization of the capacitor ripple successfully improved the performance of the system. However, as shown in Fig.4c, the the upper and lower arms of the converter are not completely balanced inducing a DC component. This imbalance becomes severe when unavoidable mismatches are considered between the elements of the arms due to capacitor and inductor tolerances. Fig.9 shows the mean value of the capacitor voltages of a leg, when an unbalance of 20% is introduced between the arm inductors.

Fig.9 indicates the need of implementing an energy balance controller, aiming to keep the difference of the average of the energies between the arms zero as proposed in [4]. This controller injects first order harmonic in the circulating current in order to keep the capacitor voltages equal between the arms.

In this paper a tunning procedure to determine the controller parameters in presented. Furthermore, in order to validate the presented technique, simulation results are depicted for different unbalanced cases between arms. Finally, the limitations of the controller as presented in [4] is discussed.

A. *Tuning of the Arm Energy Balancing controller*

Fig.10 shows the block diagram of the closed loop system of the implemented controller. Unlike presented in [4], the

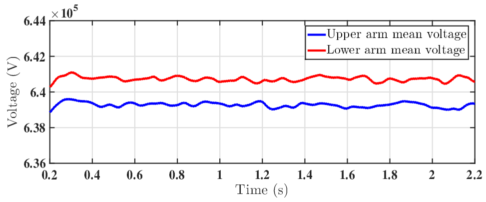

Fig. 9: Mean capacitor voltages without energy controller under 20% arm inductor unbalance.

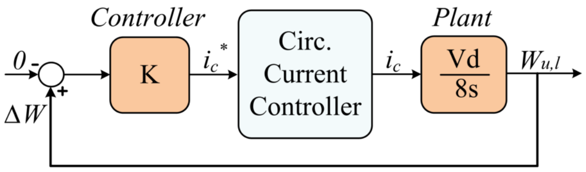

Fig. 10: Control Diagram of the closed loop arm balancing controller.

proposed controller is only composed of a P gain as the plant of the system contains an integrator. In case of energy unbalance within a leg considering the aforementioned fundamental harmonic injection in the circulating current and neglecting the oscillating terms (11) results in:

$$\frac{dW_{\triangle}}{dt} = i_{c0m}V_{c\triangle} - \hat{V}_s\hat{I}_{c1m} \tag{28}$$

where, $V_{c\triangle}$ refers to $v_{cu,l}$ difference constant term.

The first term in (28) shows the unbalance inferred in the power due to the voltage difference between the upper and lower cell capacitors. However, the last term of the same equation can compensate the mentioned unbalance due to the injection of the $50Hz$ component in the circulating current.

In order to determine the transfer function of the system the power in each leg is calculated considering the circulating current containing the fundamental component and neglecting the alternating terms with zero mean value:

$$P_u = P_{inputDC} - P_{outputAC} - P_{circulatingAC} \tag{29}$$

$$P_l = P_{inputDC} - P_{outputAC} + P_{circulatingAC} \tag{30}$$

Therefore, subtraction of (29) and (30) results in (28) and the last term in the previous equations allows determining the transfer function of the system. Assuming $\hat{V}_s = \frac{V_d}{2}$ as inferred in (7) and expressing the power component in terms of energy in Laplace domain leads to:

$$\frac{W_{\triangle_{i_{c1m}}}}{i_{c1m}} = \frac{V_d}{8s} \tag{31}$$

In order to properly tune the controller Fig. 10 is taken as a base. In this paper, the circulating current controller is considered to be tuned accordingly with the system requirements and working as desired. Considering it as the inner-loop in the whole system its closed-loop transfer function if considering it implemented with a Second Order Generalized Integrator yields [5]:

$$G_{cl_{cc}(s)} = \frac{K_p[s^2 + (hw_1)^2] + K_h s}{(sL + K_p)[s^2 + (hw_1)^2] + K_h s} \tag{32}$$

Therefore the open-loop transfer function of the system becomes:

$$G_{ol(s)} = \frac{KVd(K_p[s^2 + (hw_1)^2] + K_h s)}{4s((sL + K_p)[s^2 + (hw_1)^2] + K_h s)} \tag{33}$$

Referring independently the numerator and denominator of the open-loop transfer function results in:

$$N_{ol(s)} = V_d K K_p[s^2 + (hw_1)^2] + V_d K K_p s \tag{34}$$

$$D_{ol(s)} = 4s((sL + K_p)[s^2 + (hw_1)^2] + K_h s) \tag{35}$$

Thus the closed-loop transfer function can be written as:

$$C_{cl(s)} = \frac{N_{ol(s)}}{N_{ol(s)} + D_{ol(s)}} \tag{36}$$

Considering the controller to be designed to track a constant reference and substituting $s = 0$ in (36), $C_{cl(0)}$ yields 0 which ensures the output of the controller to be equal to the input as desired.

In this paper the tuning of the gain K is based on the bode stability criterion where the outer-loop is designed to be slower than the inner-loop which is the circulating current controller. The step response of the system for a gain of $K = 0.0008$ corresponds to a time constant of approximately of $t_r = 37ms$ as depicted in Fig. 11.

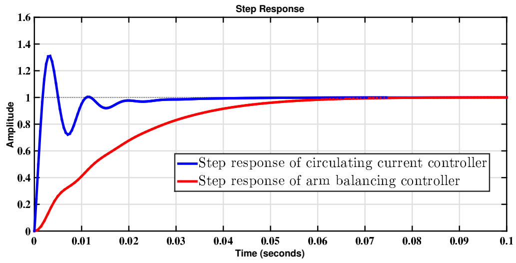

Fig. 11: Step response of the circulating current controller and energy balancing controller.

In order to prove stability the bode plot of the system for the same gain as shown before is presented in Fig. 12 where the phase margin is high and equals 82.4° thus ensuring the stability of the system.

B. Performance evaluation of the controller through simulations

Based on simulation results obtained with the parameters described in Table III, controller's functionality is proved in this section. Three cases of unbalance in the system are discussed in this subsection. Firstly, a difference of 20% between

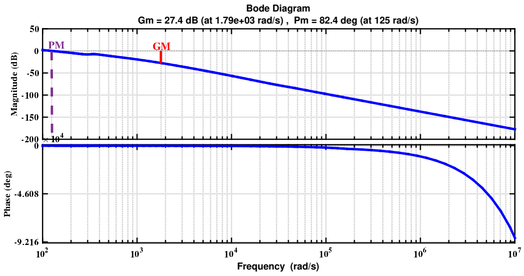

Fig. 12: Bode diagram of the open-loop system of the energy balancing controller.

the arm inductors within each phase is introduced. Secondly, a step in the energy reference of the controller is applied. The last scenario proposes different unbalance conditions in each leg which will highlight the controller limitations due to coupling between phases.

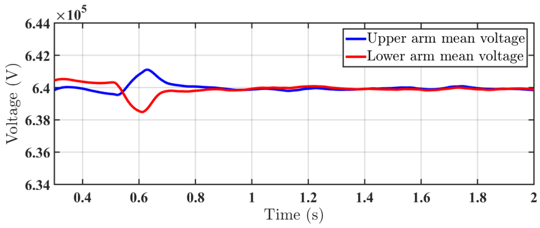

Fig. 13: Mean capacitor voltages with energy controller under 20% arm inductor unbalance.

As proposed in the beginning of this section, a 20% arm inductor unbalance has been introduced in the upper arm of each leg of the converter. Fig.13 shows the mean capacitor voltages when the arm balancing energy controller is introduced at $0.5s$. In this case, the controller manages to keep the voltages completely balanced. Secondly, a step in the energy reference is given depicting the correspondence between the theoretically calculated time response of the system and the one based on simulations as depicted in Fig. 14.

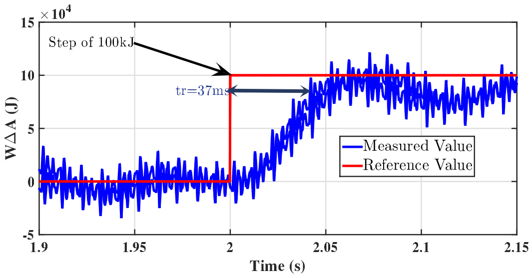

Fig. 14: Response of the system when a step in energy is introduced.

Finally, a step in the energy is introduced only in phase-a of the converter. Fig.15 shows that the injected fundamental circulating current affects the energy difference balance in all phases, proving that with this method an arm's energy cannot be controlled without affecting the other phases. Similar problem was indicated and a solution was proposed in [7].

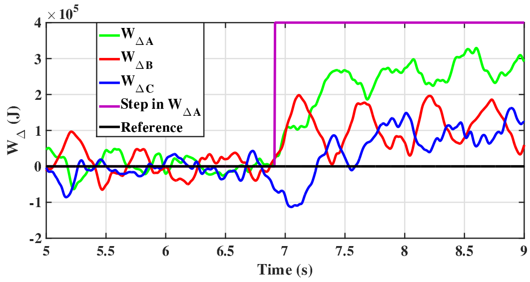

Fig. 15: Energy difference in each leg when energy balancing controller is implemented

V. CONCLUSIONS

In this paper, a systematic approach has been introduced for the effective reduction of the sum capacitor voltage ripple in an MMC application. The injection of a second order harmonic component in the circulating current was proven to be capable of reducing the total capacitor ripple down to 33% of its initial value and could be used to reduce the size of the capacitors in MMC-HVDC. On the other hand, an increase of 7% of the total rms arm currents is also introduced. The effectiveness of the method in terms of cost and size depends on the application and dimensioning of the power components. As a future scope, an optimization method and an in-depth analysis can be carried out to find an optimum point between reducing the capacitor voltage ripple along with the cost and size of the capacitor to overall operational cost.

Finally, the tuning procedure and effectiveness of an energy balancing controller was shown. With high phase margin as mentioned above, the system stability was ensured and the step response had no overshoot with a rise time of 37ms. The energy balancing controller was tuned with the aforementioned gain just to ensure that the bandwidth is lower than the inner loop which is the circulating current controller. The system was simulated under various internal unbalanced conditions and the limitations of the aforementioned controller were highlighted.

REFERENCES

[1] A. Lesnicar and R. Marquardt An innovative modular multilevel converter topology suitable for a wide power range, 2003.
[2] L. Harnefors and A. Antonopoulos and S. Norrga and L. Angquist and H. P. Nee Dynamic Analysis of Modular Multilevel Converters, 2013.
[3] M. Winkelnkemper and A. Korn and P. Steimer A modular direct converter for transformerless rail interties, 2010.
[4] T. Soong and P. W. Lehn Internal Power Flow of a Modular Multilevel Converter With Distributed Energy Resources,2014.
[5] Teodorescu, R. and Liserre, M. and Rodriguez, P. Grid Converters for Photovoltaic and Wind Power Systems,2011.
[6] K. Ilves and A. Antonopoulos and L. Harnefors and S. Norrga and L. ngquist and H. P. Nee Capacitor voltage ripple shaping in modular multilevel converters allowing for operating region extension,2011.
[7] P. Mnch and D. Grges and M. Izk and S. Liu Integrated current control, energy control and energy balancing of Modular Multilevel Converters,2010
[8] Q. Tu and Z. Xu and J. Zhang Circulating current suppressing controller in modular multilevel converter,2010

Bibliography

[1] Global Industry Analysts. *Flexible AC Transmission Systems - A Global Strategic Business Report.* August 2014.

[2] B. A. Shenoi. *Introduction to Digital Signal Processing and Filter Design.* Willey, 2005.

[3] K. Fujii, U. Schwarzer, and R. W. De Doncker. Comparison of hard-switched multi-level inverter topologies for statcom by loss-implemented simulation and cost estimation. In *2005 IEEE 36th Power Electronics Specialists Conference*, pages 340–346, June 2005. doi: 10.1109/PESC.2005.1581646.

[4] H. K. Tyll and F. Schettler. Power system problems solved by facts devices. In *Power Systems Conference and Exposition, 2009. PSCE '09. IEEE/PES*, pages 1–5, March 2009. doi: 10.1109/PSCE.2009.4840205.

[5] ABB FACTS. *A matter of FACTS: Deliver more, high quality power.* December 2015.

[6] H. K. Tyll and F. Schettle. Historical overview on dynamic reactive power compensation solutions from the begin of ac power transmission towards present applications. In *Power Systems Conference and Exposition, 2009. PSCE '09. IEEE/PES*, pages 1–7, March 2009. doi: 10.1109/PSCE.2009.4840208.

[7] M. Pereira, D. Retzmann, J. Lottes, M. Wiesinger, and G. Wong. Svc plus: An mmc statcom for network and grid access applications. In *PowerTech, 2011 IEEE Trondheim*, pages 1–5, June 2011. doi: 10.1109/PTC.2011.6019245.

[8] J. Rabkowski, D. Peftitsis, and H. P. Nee. Silicon carbide power transistors: A new era in power electronics is initiated. *IEEE Industrial Electronics Magazine*, 6(2):17–26, June 2012. ISSN 1932-4529. doi: 10.1109/MIE.2012.2193291.

[9] V. Chitta, Soonwook Hong, and D. A. Torrey. Series connection of igbts with active voltage balancing. In *Industry Applications Conference, 1997. Thirty-Second IAS Annual Meeting,*

IAS '97., Conference Record of the 1997 IEEE, volume 2, pages 961–967 vol.2, Oct 1997. doi: 10.1109/IAS.1997.628977.

[10] S. A. Kamran and J. Muñoz. Study of a state-of-the art m-statcom. In *Industrial Technology (ICIT), 2015 IEEE International Conference on*, pages 2733–2738, March 2015. doi: 10.1109/ICIT.2015.7125501.

[11] B. Singh, R. Saha, A. Chandra, and K. Al-Haddad. Static synchronous compensators (statcom): a review. *IET Power Electronics*, 2(4):297–324, July 2009. ISSN 1755-4535. doi: 10.1049/iet-pel.2008.0034.

[12] C. Hochgraf, R. Lasseter, D. Divan, and T. A. Lipo. Comparison of multilevel inverters for static var compensation. In *Industry Applications Society Annual Meeting, 1994., Conference Record of the 1994 IEEE*, pages 921–928 vol.2, Oct 1994. doi: 10.1109/IAS.1994.377528.

[13] H. Akagi. Classification, terminology, and application of the modular multilevel cascade converter (mmcc). *IEEE Transactions on Power Electronics*, 26(11):3119–3130, Nov 2011. ISSN 0885-8993. doi: 10.1109/TPEL.2011.2143431.

[14] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H. P. Nee. Dynamic analysis of modular multilevel converters. *IEEE Transactions on Industrial Electronics*, 60(7):2526–2537, July 2013. ISSN 0278-0046. doi: 10.1109/TIE.2012.2194974.

[15] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee. Steady-state analysis of interaction between harmonic components of arm and line quantities of modular multilevel converters. *IEEE Transactions on Power Electronics*, 27(1):57–68, Jan 2012. ISSN 0885-8993. doi: 10.1109/TPEL.2011.2159809.

[16] A. Antonopoulos, L. Angquist, and H. P. Nee. On dynamics and voltage control of the modular multilevel converter. In *Power Electronics and Applications, 2009. EPE '09. 13th European Conference on*, pages 1–10, Sept 2009.

[17] M. Hagiwara, R. Maeda, and H. Akagi. Negative-sequence reactive-power control by a pwm statcom based on a modular multilevel cascade converter (mmcc-sdbc). In *2011 IEEE Energy Conversion Congress and Exposition*, pages 3728–3735, Sept 2011. doi: 10.1109/ECCE.2011.6064275.

[18] *IGBT Modules*. Infineon, 10 2013. Rev. 3.

[19] N. Ahmed, L. Ängquist, A. Antonopoulos, L. Harnefors, S. Norrga, and H. P. Nee. Performance of the modular multilevel converter with redundant submodules. In *Industrial Electronics*

Society, IECON 2015 - 41st Annual Conference of the IEEE, pages 003922–003927, Nov 2015. doi: 10.1109/IECON.2015.7392712.

[20] K. Ilves, S. Norrga, and H. P. Nee. On energy variations in modular multilevel converters with full-bridge submodules for ac-dc and ac-ac applications. In *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pages 1–10, Sept 2013. doi: 10.1109/EPE.2013.6634324.

[21] A. Hillers and J. Biela. Optimal design of the modular multilevel converter for an energy storage system based on split batteries. In *Power Electronics and Applications (EPE), 2013 15th European Conference on*, pages 1–11, Sept 2013. doi: 10.1109/EPE.2013.6634660.

[22] M. Hagiwara, R. Maeda, and H. Akagi. Theoretical analysis and control of the modular multilevel cascade converter based on double-star chopper-cells (mmcc-dscc). In *Power Electronics Conference (IPEC), 2010 International*, pages 2029–2036, June 2010. doi: 10.1109/IPEC.2010.5543517.

[23] M. S. Lima, L. A. d. S. Ribeiro, and J. G. de Matos. Comparison analysis of resonant controllers in discrete domain taking into account the computational delay. In *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, pages 1–6, Nov 2015. doi: 10.1109/COBEP.2015.7420135.

[24] T. Nussbaumer, M. L. Heldwein, G. Gong, S. D. Round, and J. W. Kolar. Comparison of prediction techniques to compensate time delays caused by digital control of a three-phase buck-type pwm rectifier system. *IEEE Transactions on Industrial Electronics*, 55(2):791–799, Feb 2008. ISSN 0278-0046. doi: 10.1109/TIE.2007.909061.

[25] Charles Phillips and Royce D. Harbor. *Feedback Control Systems*. Prentice Hall, New Jersey, 2000.

[26] R. Mishra and A. Shukla. A proportional resonator-based control scheme to suppress ac components in circulating current of modulator multilevel converter. In *Industrial Electronics Society, IECON 2013 - 39th Annual Conference of the IEEE*, pages 6170–6175, Nov 2013. doi: 10.1109/IECON.2013.6700150.

[27] T. Soong and P. W. Lehn. Internal power flow of a modular multilevel converter with distributed energy resources. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2(4):1127–1138, Dec 2014. ISSN 2168-6777. doi: 10.1109/JESTPE.2014.2342656.

[28] P. Münch, D. Görges, M. Izák, and S. Liu. Integrated current control, energy control and energy balancing of modular multilevel converters. In *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, pages 150–155, Nov 2010. doi: 10.1109/IECON.2010.5675185.

[29] L. Ängquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H. P. Nee. Inner control of modular multilevel converters - an approach using open-loop estimation of stored energy. In *Power Electronics Conference (IPEC), 2010 International*, pages 1579–1585, June 2010. doi: 10.1109/IPEC.2010.5544607.

[30] R. Teodorescu, M. Liserre, and P. Rodriguez. *Grid Converters for Photovoltaic and Wind Power Systems*. 2011. doi: 10.1109/TIA.1984.4504460.

[31] P. Rodriguez, G. Medeiros, A. Luna, M. C. Cavalcanti, and R. Teodorescu. Safe current injection strategies for a statcom under asymmetrical grid faults. In *2010 IEEE Energy Conversion Congress and Exposition*, pages 3929–3935, Sept 2010. doi: 10.1109/ECCE.2010.5617794.

[32] M. Ciobotaru, R. Teodorescu, and F. Blaabjerg. A new single-phase pll structure based on second order generalized integrator. In *Power Electronics Specialists Conference, 2006. PESC '06. 37th IEEE*, pages 1–6, June 2006. doi: 10.1109/PESC.2006.1711988.

[33] P. Rodriguez, A. Luna, I. Candela, R. Mujal, R. Teodorescu, and F. Blaabjerg. Multiresonant frequency-locked loop for grid synchronization of power converters under distorted grid conditions. *IEEE Transactions on Industrial Electronics*, 58(1):127–138, Jan 2011. ISSN 0278-0046. doi: 10.1109/TIE.2010.2042420.

[34] F. Wang, M. C. Benhabib, J. L. Duarte, and M. A. M. Hendrix. Sequence-decoupled resonant controller for three-phase grid-connected inverters. In *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE*, pages 121–127, Feb 2009. doi: 10.1109/APEC.2009.4802643.

[35] E. Behrouzian, M. Bongiorno, and H. Z. De La Parra. Investigation of negative sequence injection capability in h-bridge multilevel statcom. In *Power Electronics and Applications (EPE'14-ECCE Europe), 2014 16th European Conference on*, pages 1–10, Aug 2014. doi: 10.1109/EPE.2014.6910883.

[36] H. Akagi, Y. Kanazawa, and A. Nabae. Instantaneous reactive power compensators comprising switching devices without energy storage components. *IEEE Transactions on Industry Applications*, IA-20(3):625–630, May 1984. ISSN 0093-9994. doi: 10.1109/TIA.1984.4504460.

[37] M. Vasiladiotis, N. Cherix, and A. Rufer. Impact of grid asymmetries on the operation and capacitive energy storage design of modular multilevel converters. *IEEE Transactions on Industrial Electronics*, 62(11):6697–6707, Nov 2015. ISSN 0278-0046. doi: 10.1109/TIE.2015.2437329.

[38] A. Uphues, K. Nötzold, R. Griessel, R. Wegener, and S. Soter. Overview of lvrt-capability pre-evaluation with an inverter based test bench. In *2015 IEEE 24th International Symposium on Industrial Electronics (ISIE)*, pages 748–753, June 2015. doi: 10.1109/ISIE.2015.7281562.

[39] A. Camacho, M. Castilla, J. Miret, R. Guzman, and A. Borrell. Reactive power control for distributed generation power plants to comply with voltage limits during grid faults. *IEEE Transactions on Power Electronics*, 29(11):6224–6234, Nov 2014. ISSN 0885-8993. doi: 10.1109/TPEL.2014.2301463.

[40] M. Castilla, J. Miret, A. Camacho, J. Matas, and L. García de Vicuña. Voltage support control strategies for static synchronous compensators under unbalanced voltage sags. *IEEE Transactions on Industrial Electronics*, 61(2):808–820, Feb 2014. ISSN 0278-0046. doi: 10.1109/TIE.2013.2257141.

[41] S. M. Halpin. Comparison of ieee and iec harmonic standards. In *IEEE Power Engineering Society General Meeting, 2005*, pages 2214–2216 Vol. 3, June 2005. doi: 10.1109/PES.2005.1489688.

[42] R. E. Betz, T. J. Summers, and G. Mirzaeva. Active filtering and var control of a cascaded h-bridge multi-level statcom. In *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, pages 816–821, Nov 2009. doi: 10.1109/PEDS.2009.5385878.

[43] J. A. Muñoz, J. R. Espinoza, C. R. Baier, L. A. Morán, J. I. Guzmán, and V. M. Cárdenas. Decoupled and modular harmonic compensation for multilevel statcoms. *IEEE Transactions on Industrial Electronics*, 61(6):2743–2753, June 2014. ISSN 0278-0046. doi: 10.1109/TIE.2013.2276058.

[44] W. K. A. Goncalves, J. C. De Oliveria, and V. L. S. Franco. Advanced static var compensator performance under nonideal electric power supply conditions. In *Harmonics and Quality of Power, 2000. Proceedings. Ninth International Conference on*, volume 2, pages 554–559 vol.2, 2000. doi: 10.1109/ICHQP.2000.897739.

[45] P. Lauttamus and H. Tuusa. Three-level vsi based low switching frequency 10 mva statcom in reactive power and harmonics compensation. In *2007 7th Internatonal Conference on Power Electronics*, pages 536–541, Oct 2007. doi: 10.1109/ICPE.2007.4692446.

[46] A. Lesnicar and R. Marquardt. An innovative modular multilevel converter topology suitable for a wide power range. In *Power Tech Conference Proceedings, 2003 IEEE Bologna*, volume 3, pages 6 pp. Vol.3–, June 2003. doi: 10.1109/PTC.2003.1304403.

[47] M. Sakui and H. Fujita. An analytical method for calculating harmonic currents of a three-phase diode-bridge rectifier with dc filter. *IEEE Transactions on Power Electronics*, 9(6):631–637, Nov 1994. ISSN 0885-8993. doi: 10.1109/63.334779.

[48] Betz R and Summers T. *Introduction to Symmetrical Components and their use in STATCOM Applications*. School of Electrical Engineering and Computer Science University of Newcastle, Australia, 2009.