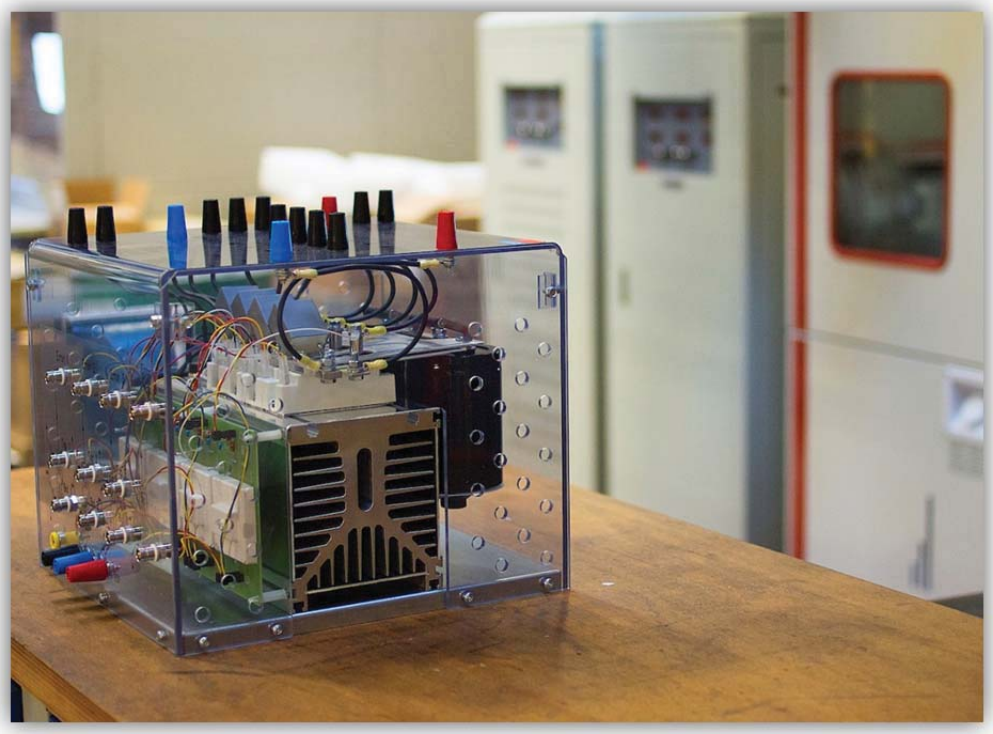
Smart Derating of Switching Devices for Designing More Reliable PV Inverters



Master Thesis

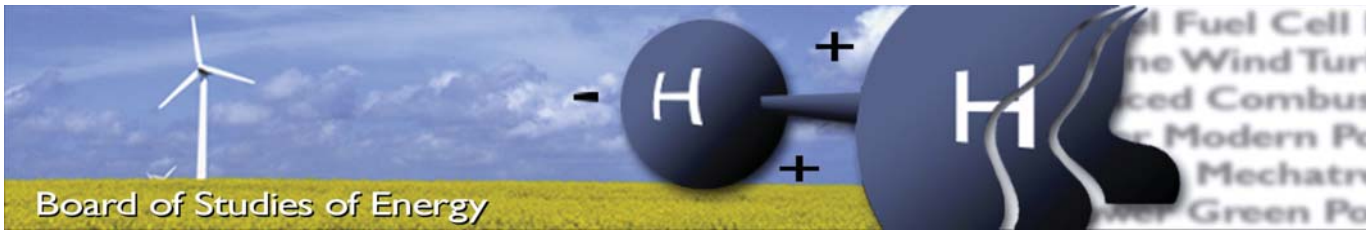
Power Electronics and Drives

PED4-1041, Spring 2014

Department of Energy Technology

Aalborg University, Denmark

AALBORG UNIVERSITY
STUDENT REPORT



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SYNOPSIS:

The increasing reliability performance of next generation Photovoltaic inverters has been sparked across the entire world, which tends to guarantee up to 20 years lifetime. Switching devices have become a key topic in terms of reliability and cost, which lifetime is not easy predictable and measurable to date. This project investigates the reliability analysis of IGBTs by taking into account the long-term mission profiles (solar irradiance and ambient temperature) and the relevant parameter variations. The outcome is a design procedure that can be applied to estimate the reliability of different IGBT solutions for Photovoltaic inverters with a certain confidence level. Thus, Photovoltaic inverter designers can select the most cost-effective IGBTs based on the cost information and the reliability specifications, avoiding either lack of robustness or over-design with unnecessary cost increase.

Paula Diaz Reigosa

Copies:	Three
Pages, total:	74
Appendix:	3
Supplements:	3 Compact Discs

By signing this document, each member of the group confirms that all group members have participated in the project work, and thereby all members are collectively liable for the contents of the report. Furthermore, all group members confirm that the report does not include plagiarism.

PREFACE

The *Smart Derating of Switching Devices for Designing More Reliable PV Inverters* Master thesis was conducted in Aalborg University, Institute of Energy Technology, as part of the 10th semester Master program entitled "Power Electronics and Drives". This project corresponds to 30 ECTS.

The report is written in LaTeX, calculations and data analysis are performed in MATLAB® 2013, simulations are performed in Simulink® and PLECS Blockset®.

All the units used in this report are SI base units, derived units and prefixes as described by The International System of Units. All units are written between brackets, as [unit].

Finally, a CD including all references, simulation files, datasheets, software codes/scripts are annexed in the report.

INSTRUCTIONS FOR READING

The references can be found at the end of the report in the chapter *Bibliography*, they are made according to the Institute of Electrical and Electronics Engineers (IEEE) citation style. In the main context references are shown in square brackets as "[X]". Figures and tables are enumerated continuously in each chapter, e.g. Fig. X.Y refers to X chapter's Y graph. Equations, follow the figures notation, but in round brackets as (X.Y). Oppositely to chapters which are enumerated with integers, appendices are assigned capital letters and are alphabetically sorted.

ACKNOWLEDGEMENTS

The author would firstly like to thank the Master thesis supervisor Huai Wang, assistant professor at Aalborg University, for all his patience, kindness, guidance and enlightening discussions. Further, thanks to the Master thesis co-supervisor Frede Blaabjerg, professor at Aalborg University for the valuable meetings and interest. Last but not least, many thanks to Nicolae-Christian Sintamarean, PhD fellow at Aalborg University for the valuable help and Yongheng Yang, PhD student at Aalborg University for graciously supplying all the necessary equipment and guidance in the laboratory.

Additionally the author would like to express her most sincere gratitude to her family and Enrique Rodriguez Diaz for their support which encourage me along all this large period.

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ABBREVIATIONS

Abbreviation	Description
2L-VSI	Two-level Voltage Source Inverter
3L	Three Level
AC	Alternative Current
BSNPC	Bipolar Switch Neutral-Point Clamped
DC	Direct Current
DNPC	Diode Neutral-Point Clamped
FLL	Frequency-Locked Loop
GM	Gain Margin
IGBT	Insulated Gate Bipolar Transistor
I/O	Input/Output board
MC	Monte Carlo
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PC	Power Cycling
PI	Proportional Integrator
PLL	Phase-Locked Loop
PM	Phase Margin
PR	Proportional Resonant
PV	Photovoltaic
PWM	Pulse Width Modulation
RMS	Root Mean Square
SRF-PLL	Synchronous Reference Frame Phase-Locked Loop
THD	Total Harmonic Distortion

Part I

Introduction to Reliability Analysis of IGBTs in PV Inverters

CHAPTER 1

INTRODUCTION

This chapter serves as an introduction to the entire report. A first presentation of the design for reliability of transformerless photovoltaic inverters and its state-of-the-art is given and then the project motivation, constraints as well as objectives are defined. Finally, a project outline is given for a better understanding of the report structure.

1.1 INTRODUCTION

The development of three-phase transformerless photovoltaic (PV) inverters, which can achieve higher efficiency than traditional transformer-based PV inverters, has been sparked across the entire world. Nowadays, special attention has been dedicated to the reliability and maintenance cost of grid-connected transformerless inverters in order to satisfy the ambitious product requirements for the Photovoltaic market - long operating hours under harsh environments.

Inverters are employed in most of modern life photovoltaic systems, nevertheless they are considered as one of the weakest links in terms of reliability. According to [5], field results pointed out that photovoltaic inverters may fail due to manufacturing and quality control problems, inadequate design, and electrical component failure.

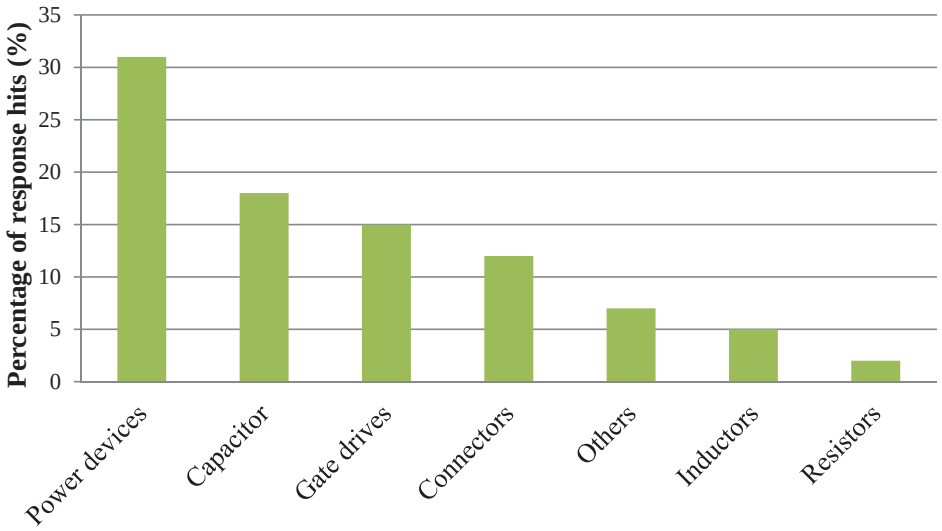

Figure 1.1: Failure distribution in power converters (Data source from [1]).

In order to understand the factors which limit the reliability of PV inverters, each failure mechanism under critical stress conditions must be investigated. A survey based on field experiences from semicon-

ductor manufacturers, integrators and users in the aerospace, automation, motor drive, utility power and other industry sectors [1], reveals that power semiconductor devices are the most critical components in power converters. Figure 1.1 illustrates the distribution of critical components according with the survey published in [1]. It can be observed that 31% of the responders have chosen power semiconductors as the main contributor to failure, therefore the Insulated Gate Bipolar Transistor (IGBT) is the principal focus in this Master Thesis.

As can be observed in Figure 1.2, the most critical stressor in power semiconductors is the thermal stress [2]. There is a strong tendency for continuously reducing the magnitude of the cycling temperature (ΔT) as well as the average junction temperature (T_j) due to the fact that is closely related with reliability and maintenance cost.

Load			**IGBT**		
Type of stress	**Product design**	**Stressor**	**Die**	**Solder joints**	**Wire-bond**
Temperature cycling and steady state	1) Thermal control 2) Operating point. 3) On/Off 4) Operating power.	Temperture swing *ΔT*	***	***	***
		Average temperature *Tm*	**	**	**
		dT/dt	*	*	*
Vibration/chock	1) Mechanical	Vibration /shock	*		
Humidity/Moisture	1) Thermal control 2) On/Off 3) Breating effect 4) Operating power	Relative humidity	*	*	*
Contaminants and dust	1) Enclosure design	Pollution			

Figure 1.2: Critical stressors for IGBTs: high level of importance (***), medium level of importance (**) and low level of importance (*) [2].

1.1.1 IMPORTANCE OF THERMAL STRESS IN PV INVERTER RELIABILITY

As already discussed, cycling and steady-state temperature has the most significant impact on failure modes and failure mechanisms of power semiconductors. For this reason, an effort on exploring highly efficient power semiconductors, low-cost heat sinks and control algorithms capable of lowering the temperature are the aims of the scientific community.

Previous studies [6], [7], [8] revealed the failure mechanism of IGBTs - thermo-mechanical stresses in adjacent layers. As illustrated in Figure 1.3, several layers inside the IGBT are assembled together with different thermal expansion coefficients. Therefore, during normal operation, the uneven expansion and contraction due to thermal cycling generates shear strains and shear stresses until cracks or discon-

nections are triggered. Hence, reduction of these stresses has become crucial to enlarge the reliability of the assembly.

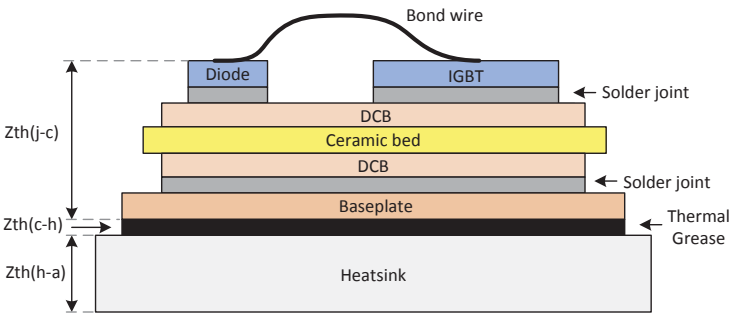

Figure 1.3: Schematic cross section of an IGBT module.

According to [2], there are three main wear-out failure mechanisms of the IGBT modules due to cyclic thermal stress: the bond wire lift-off, solder joints cracking under the chip (diode and IGBT) and solder joints cracking under the DCB.

In order to determine the lifetime models for such failure mechanisms, accelerated temperature cycling tests are normally conducted. To ensure that the test will trigger both failure modes (wire bond and solder degradation), a ByCycle test has been proposed in [9], which is closer to real applications than individual tests. When the IGBTs undergo temperature variations, they are typically exposed to two types of cycling conditions - Power Cycling (PC) and Thermal Cycling (TC). Power Cycling is conducted to determine the robustness of the wire bonds, it raises and lowers the chip junction temperature at short intervals of time (sub-seconds to seconds regime) [9]. Thermal Cycling is conducted to determine the robustness of the solder joints beneath the DCB and the chips, it raises and lowers the case temperature at long intervals (tens of seconds to several minutes) [9].

Once the ByCycle test has been applied, the number of cycles to failure (N_f) can be obtained via a mathematical approach. For extracting lifetime parameters, several analytical models have been proposed in [3], [10] and [11].

- **Coffin-Manson Model:**

$$N = A \cdot (\Delta T_j)^{-n} \tag{1.1}$$

  This is the simplest lifetime analytical model, the fluctuation of junction temperature ΔT_j is the only parameter considered. *A* and *n* are the curve fitting parameters.

- **Coffin-Manson-Arrhenius Model:**

$$N = A \cdot (\Delta T_j)^{-n} \cdot \exp\left(\frac{E_a}{k_b \cdot T_{jm}}\right) \tag{1.2}$$

It takes into consideration one more parameter, the mean junction temperature T_{jm}. E_a is the activation energy and k_b is the Boltzmann constant.

- **Bayerer Model:**

$$N = A \cdot (\Delta T_j)^{-\beta_1} \cdot \exp\left(\frac{\beta 2}{T_{j,max} + 273}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{1.3}$$

This model contains more detailed information to precisely calculate the number of cycles to failure. $T_{j,max}$ is the maximum junction temperature, t_{on} is the duration of the heating time during one power cycle, I is the current per bond foot, V is the blocking voltage and D is the bond wire diameter.

1.1.2 IMPORTANCE OF THERMAL STRESS IN PV INVERTER COST

Even though PV inverters represent a small percentage of the initial system cost (10- 20%), as aforementioned they are one of the weakest points, therefore they may need to be replaced 3-5 times over the life of a PV system [12]. This fact introduces an extra cost to the overall PV system and thus limits Photovoltaic inverters attractiveness.

In order to satisfy both stringent reliability requirements and constrained cost target, the goal is to establish a reliability-cost model which can interrelate first the relationship between the varied-lifetime and the cost as shown in Figure 1.4 (a) and then the relationship between the lifetime variation and the level of reliability as presented in Figure 1.4 (b).

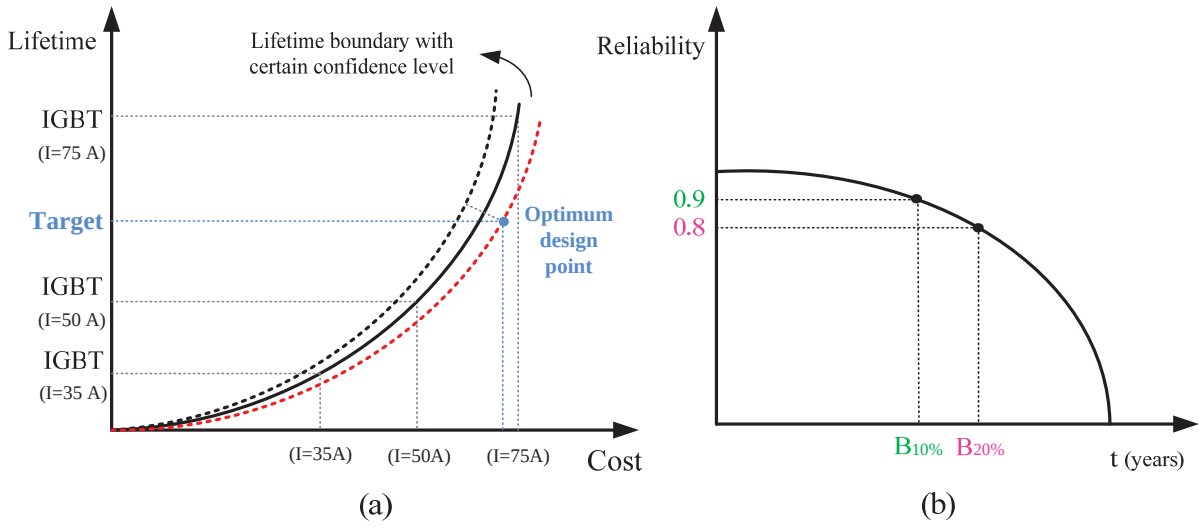

Figure 1.4: Reliability-cost model: a) Relationship between lifetime and cost and b) Relationship between reliability level and lifetime.

The power losses (switching losses and conduction losses) as well as thermal impedance models of power semiconductors determine the device junction temperature mean value T_{jm} and its temperature cycling ΔT_j [13]. The thermal stresses of such devices (IGBTs) have a great impact on the lifetime performance, as a result, a varied-lifetime is expected when using different IGBT solutions. Figure 1.4 (a)

illustrates that power modules with higher nominal current ensure longer operating hours at expense of increased cost. By quantifying the possible lifetime boundary, manufacturers could design PV inverters to fulfil the reliability target with minimized cost by avoiding either lack of robustness or over-design of the IGBTs as pointed out in Figure 1.4 .

1.2 PROBLEM DESCRIPTION

With the advancement of the chip, packaging and manufacturing technologies, IGBT suppliers are continuously improving their component reliability performance. Therefore, in most of the applications, power electronics designers can easily find available IGBTs that can achieve the required lifetime specifications. The practical problem for them is how to select the proper IGBTs to fulfill the reliability target while minimizing the cost. This is especially true in the PV industry having a very stringent cost constraint to reduce the cost of electric power generation. However, due to the following challenges, the reliability analyses of the IGBTs designed in PV inverters are usually not well treated, resulting in either lack of robustness or over-design with unnecessary cost increase [14].

Further on, this research intends to cover two principal aspects when predicting the lifetime of switching devices. 1) The variation of operational and environmental stresses of IGBTs during the whole life cycle (e.g., solar irrandiance and ambient temperature) of PV inverters. 2) Lifetime of IGBTs with the same part number in a large population of PV inverters may be different due to the variations of manufacturing process, uncertainties in the applied lifetime models and in the experienced stresses.

To tackle the above problem, this project investigates the reliability analysis of IGBTs by taking into account the long-term operations and the relevant parameter variations. The outcome is a design procedure that can be applied to estimate the reliability of different IGBT candidates for PV inverters with a certain confidence level. Therefore, by following the presented procedure in Figure 1.5, the PV inverter designers can choose the most cost-effective IGBTs based on the cost information and the reliability specification they have.

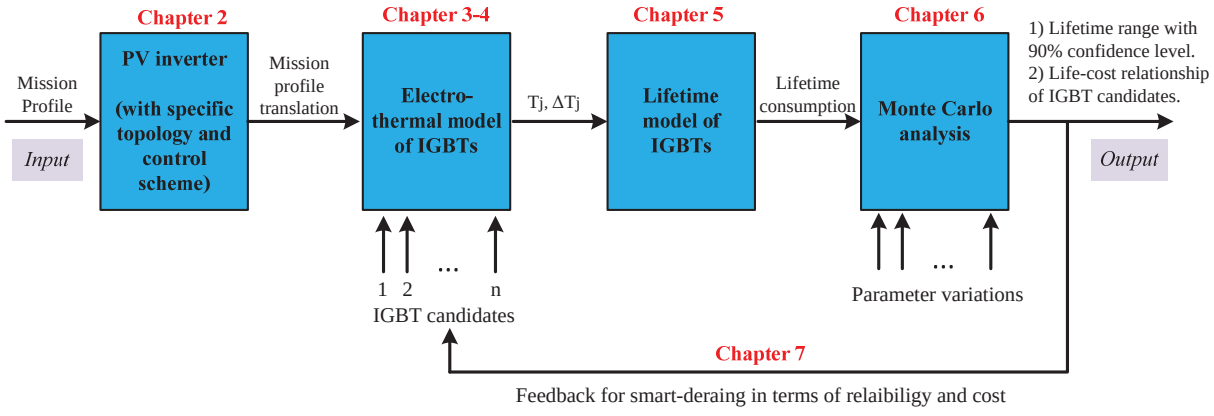

Figure 1.5: Proposed design guideline for smart-derating of switching devices.

According with Figure 1.5, the proposed design guideline takes the mission profile data (measured

solar irradiance and ambient temperature) as an input for a specific inverter topology and control scheme, thus the mission profile can be correctly transformed into the realistic loading of the converter, this is treated in Chapter 2. Afterwards, the electro-thermal model presented in Chapters 3 and 4 calculates the junction temperature T_j and its fluctuation ΔT_j for different IGBT candidates. In Chapter 5 a lifetime model of IGBTs is described, as a result the lifetime consumption can be estimated. Additionally, in Chapter 6 by means of Monte Carlo simulations the lifetime range with a reliability of 90% and the life-cost relationship can be established. Finally, the PV inverter designers can select the most cost-effective IGBT based on the information obtained through the Monte Carlo analysis, this last step is addressed in Chapter 7.

1.2.1 SMART DERATING OF SWITCHING DEVICES

The core of this approach is to render an analysis of the varied-lifetime experienced among different switching devices technologies (i.e. IGBT3, IGBT4) at different current ratings valid for a given inverter topology.

Once the inverter topology is chosen and the electrical parameters have been set, the selection of the most suitable and reliable switching device is crucial. Thus, the suggested evaluation method analyses the trade-off between high-reliable and low-cost switching devices. When selecting a switching device with higher nominal current, usually the total power losses generated are smaller than a switching device rated at lower nominal current when operated at the same conditions. Consequently, the junction temperature of the device which is rated at higher current will be lower. Since the losses and the heat produced by each are different, this could further lead to varied lifetimes.

Moreover, one year mission profile data (the measured solar irradiance and ambient temperature) from the real field is available. Thus the expected hours of life can be obtained for a realistic loading of the switching device. Indeed, a realistic benchmarking of different switching devices could be done in order to efficiently apply smart derating of switching devices.

Finally, it is intended to develop a design guideline that could answer the following questions:

- Which nominal current of the device may be selected?
- How does efficiency evolve with it?
- Depending on the rated current, which is the effect on the switching device lifetime (T_j, ΔT_j)?
- Which is the optimal point that either avoids lack of robustness or over-design of the IGBTs ?

1.2.2 VARIATION ANALYSIS OF IGBT LIFETIME USING MONTE CARLO.

The correlation between the number of cycles to failure and the temperature cycling has been analytically calculated and modelled using different mathematical approaches (i.e. Coffin-Manson, Coffin-Manson-Arrhenius model...). In the late 1990s, tests with modules from various manufacturers were published in the LESIT study [15], with the aid of parameter adjustment, the Coffin-Manson-Arrhenius fitting

parameters were obtained (*A*, *n* and activation energy E_a). So far, packaging has improved and the tests presented in the LESIT study are nowadays obsoleted.

By considering this issue, manufactures have published updated parameters, i.e Semikron [3] and Infineon [9], so that the lifetime could be obtained for the present-day power semiconductor modules.

In order to study the impact of parameter variations on the lifetime of the device, it has been considered the uncertainties in IGBT parameter variations (e.g. $V_{ce,on}$ = f(T_j, ΔT_j)) and the statistical properties of the applied lifetime model (e.g. *A*, β_1, β_2)

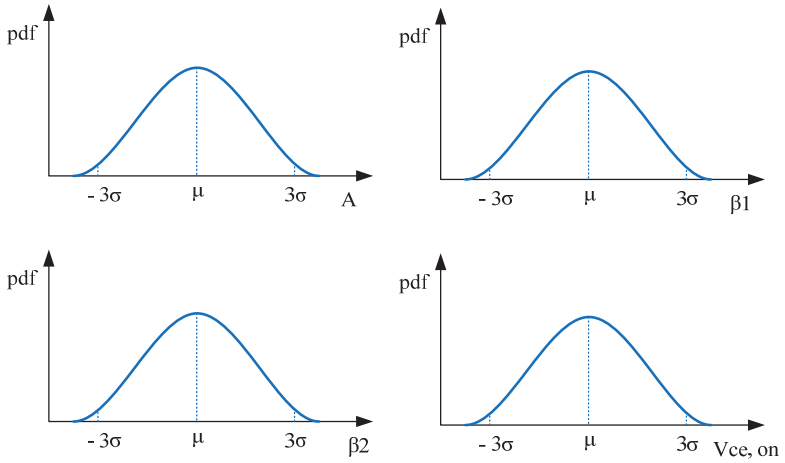

Figure 1.6: Probability density function of parameters A, β_1, β_2 and $V_{ce,on}$.

The aim of this evaluation method is to present a statistical approach for analysis of power semiconductors lifetime performance subjected to parameter variations. A step-by-step procedure is summarised bellow:

1. Define the variance values following the 6σ approach and represent the probability distribution functions of each parameter (A, β_1, β_2 and $V_{ce,on}$ = f(T_j, ΔT_j) as presented in Figure 1.6.

2. Study the sensitivity of each parameter variation on the lifetime of the device and identify which parameter has a greater impact on the PV inverter lifetime.

3. Analyze the effect of these variations by means of Monte Carlo (MC) simulations in order to obtain the lifetime probability distribution function when all the parameters are subjected to changes.

1.3 CONSTRAINTS

The main focus of this research study is the reliability of IGBTs in three-phase PV inverters, however this project does not cover every failure mechanism, indeed only the bond wire failure mode is considered. The major research activities and contributions are the smart derating of switching devices and the variation analysis of IGBT lifetime using Monte Carlo simulations, both are based taking into account

a mission profile (the measured ambient temperature and solar irradiance) recorded at Aalborg University, Denmark. Even though this research is focused on one particular switching device and one mission profile, the main idea could be adapted to specific product and specific load condition.

During the progress of the project, several limitations were encountered, the most important are highlighted as follows:

1. The simulation model built in Simulink/PLECS covers each operating point of the PV inverter, nevertheless the ambient temperature variation has not been considered, it has been fixed to $25°C$ for all the simulations.
2. The simulation model of the PV inverter could not be tested at rated conditions due to switching frequency and current limitations of the experimental setup.
3. The presented analysis considers different IGBT candidates with the same cooling solution (e.g., same heat sink). Since the thermal management could also be a design variable, the scope of study can be extended to the combination of IGBT and cooling solutions.
4. The experimental work is limited to the measurement of heatsink temperature only, since there is still a lack of suitable method that can be applied to measure the on-line junction temperature of IGBT modules.

Finally, the lifetime analysis carried out is based on the experienced environmental and operational stresses taking into account a long-term mission profile. Abnormal conditions such as overloads and system transients which could also contribute to the degradation of the device are not studied.

1.4 OBJECTIVES

The major research contributions of this Master thesis are covered by the following two aspects:

- Study of the design guideline for smart-derating of the switching devices (trade-off between reliability and design margins) in PV inverters.
- Lifetime variations of the switching devices due to parameter variations among different switching devices (either because of manufacture process control or degradation of those devices).

Nonetheless, other aspects were also relevant to the prior-art work, the activities that should be coped during this Master thesis are defined as:

- Analyse, design and simulate a three-phase two-level voltage source inverter (2L-VSI).
- Model and implement an electro-thermal model of switching devices for three-phase photovoltaic inverters.

- Understand and analyse lifetime prediction analytical models of switching devices for further comparison among them.
- Validate the inverter simulations in Simulink/PLECS via direct comparison with experimental results.

1.5 PROJECT OUTLINE

Part I: Introduction to Reliability Analysis of IGBTs in PV Inverters. It consists of a single chapter, namely, "Introduction" and the aim is to introduce the concept of the importance of thermal stress in PV inverter reliability and cost.

Part II: Modelling and Control Design of the Analysed PV Inverter. It consists of two chapters, entitled, "Three-phase two-level voltage source inverter" and "Electro-thermal modelling of IGBT power modules". This part handles the design of the three-phase two-level voltage source inverter and further on an electro-thermal model is implemented in such inverter topology.

Part III: Design Guideline for Smart Derating of Switching Devices. It comprises four chapters entitled, "Thermal stress and number of cycles analysis" which describes the influence of thermal stresses on the IGBT lifetime, the chapter "Mission profile based lifetime prediction" quantifies the accumulated damager over one year for different switching devices, the chapter "Variation Analysis of IGBT lifetime using Monte Carlo" describes the effect of parameter variation in PV inverter reliability and finally "Smart derating of switching devices" shows the rated current dependency with the lifetime of the device and the relationship with the cost of the device.

Part IV: Experimental Results. It comprises a single chapter, named "Laboratory Implementation", which describes the experimental work performed with the inverter teaching system and further comparison with the simulation results.

Part V: Conclusions After all the objectives have been fulfilled, conclusions are gathered in a single chapter, entitled "Conclusions and future work", which proposes challenging future activities that can be done.

Part VI: Appendices. In this last part, two appendices are enclosed mainly associated with the algorithms and simulations carried out during the Master thesis. They are entitled as, "Three-phase 2L VSI Simulation Model" and "Contents of the CD". The author wants to emphasize that due to the limitation of the number of pages of the project, the code algorithms are enclosed in the CD instead of being part of the Appendices.

Part II

Modelling and Control Design of the Analysed PV Inverter

CHAPTER 2

THREE-PHASE TWO-LEVEL VOLTAGE SOURCE INVERTER (2L-VSI)

This chapter introduces the overall modelling and control design of the selected three-phase transformerless photovoltaic inverter. Many different approaches could be used for the implementation of the control loop, but for the needs of this project a simple and versatile solution has been selected in order to achieve the desired functionalities. The simulation model can be observed in Appendix A.

2.1 SYSTEM DESCRIPTION

There are many converter configurations for photovoltaic (PV) systems . Even though, the most efficient three-phase PV inverter topologies are 3L-DNPC and 3L-BSNPC [16], the PV system which is the focus of this study is the well-known three-phase two-level voltage source inverter (2L-VSI). The reason of working with such topology was due to the availability of an experimental platform in the laboratory of the Energy Technology Department from Aalborg University.

The topology of the inverter is illustrated in Figure 2.1, which consists of two IGBTs per phase (upper-arm and lower-arm) that cannot be simultaneously conducting. Such inverter is connected to the three-phase grid via a passive LCL-filter.

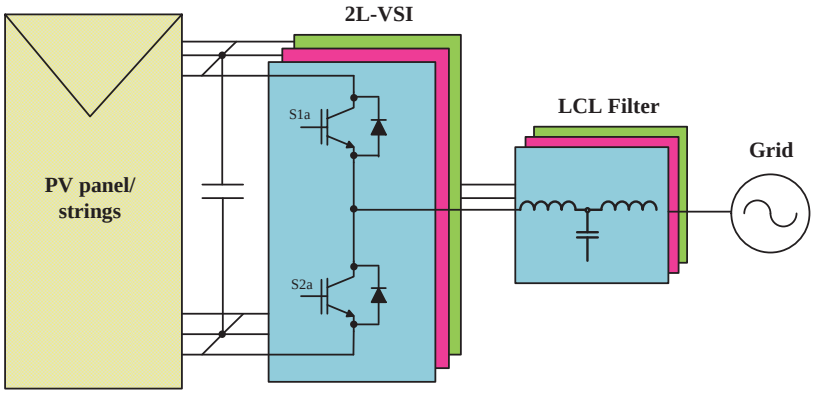

Figure 2.1: Three-phase 2L-VSC topology schematic.

The main features when using such topology are:

- The obtained output phase-to-neutral voltage fluctuates between +Vdc/2 and -Vdc/2, which entails

higher dv/dt in comparison with 3L converters.

- Each IGBT must withstand the full DC-link voltage which means that the IGBTs undergo higher voltage stress.
- Simple structure than other converter topologies (i.e. 3L-DNPC or 3L-BSNPC) due to the reduced number of components.
- High total harmonic distortion (THD), therefore a larger filter must be designed.

Moreover, Table 2.1 summarizes the three-phase two-level voltage source inverter design ratings.

Rated Power	S = 15 kVA
Converter output phase voltage	V_N = 230 V_{RMS} (325 V_{peak})
Max. output current	I = 21 A_{RMS} (30 A_{peak})
Max. DC-link voltage	$V_{DC-link}$ = 1000 V
Switching freqency	F_{sw} = 24 kHz

Table 2.1: 2L-VSI Power Ratings.

2.2 CONTROL STRATEGY OF THE INVERTER

The Voltage Oriented Control (VOC) has been adopted as the control strategy and its basic structure can be seen in Figure 2.2. The DC-link voltage is regulated in accordance to the necessary output power. The VOC control consists of two cascaded loops, the current loop as the inner loop and the voltage loop as the outer loop. As the inner loop, the current loop is designed to achieve short settling time and the voltage loop, on the other hand is designed to ensure the stability.

By applying the Park transformation (*abc-dq*) leads to the possibility of *dq*-control for a three-phase system [17] and therefore PI controllers are easier to implement.

2.2.1 GRID SYNCHRONIZATION

The synchronization of the injected currents with the grid voltage play an important role when dealing with grid connected inverters. Different techniques to extract the phase angle have been proposed in order to have an accurate and fast grid voltage synchronization under distorted and unbalanced conditions. They are classified in the ones based on phase variation (Phase-Locked Loop) and the ones based on frequency variation (Frequency-Locked Loop). Since the grid frequency is a more stable parameter than the grid phase-angle, FLL presents a better performance under unbalanced grid voltages. In spite of FLL good response, PLL has been decided to use as the synchronization technique, due to the system will be tested under ideal voltage conditions.

The block diagram of the PLL based on the synchronous reference frame (SRF-PLL) is shown in Figure 2.3. Park transformation is used to convert the *abc* natural reference frame to the *dq* rotating reference frame, consequently the three-phase voltage can be expressed as:

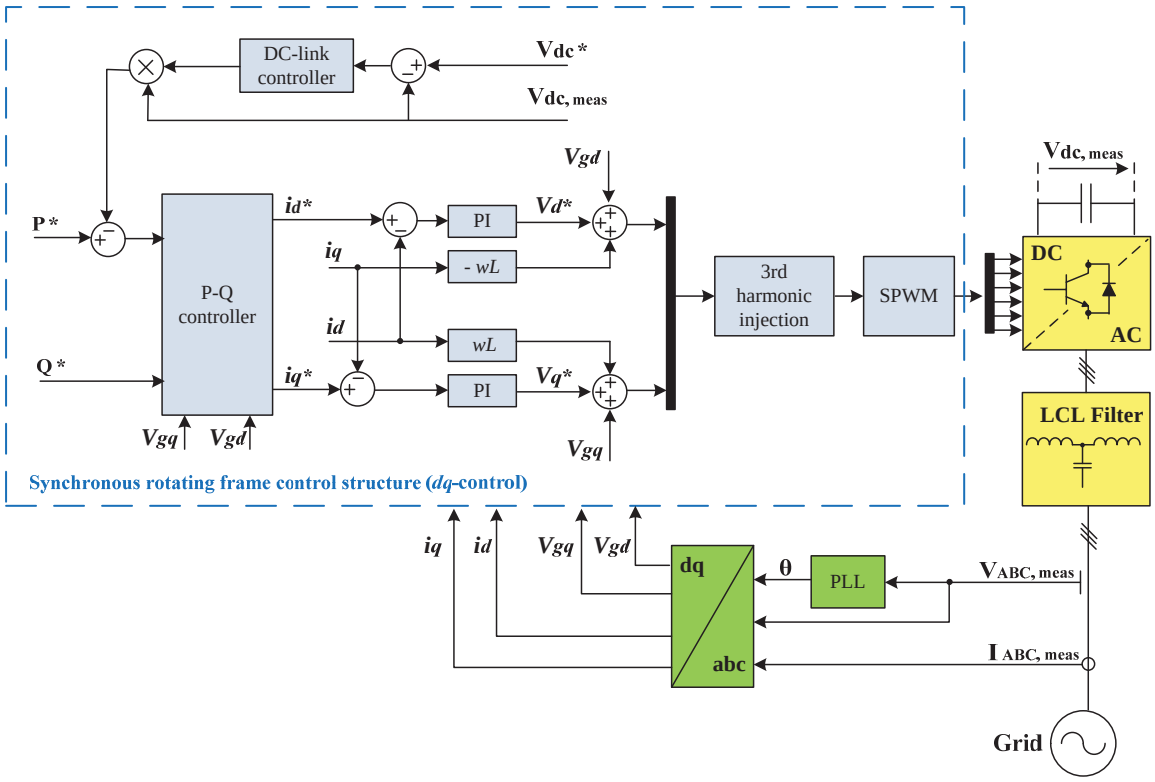

Figure 2.2: Basic control structure of a three-phase grid-connected PV system.

$$V_d = V_m \times cos(\theta - \omega \times t) \tag{2.1}$$

$$V_q = V_m \times sin(\theta - \omega \times t) \tag{2.2}$$

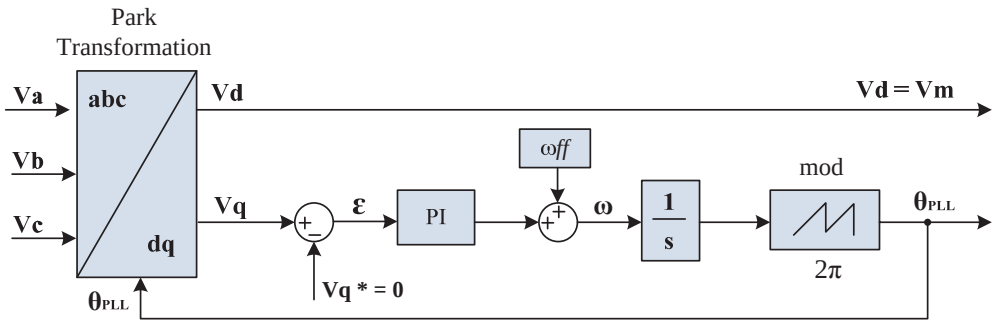

Figure 2.3: Basic block diagram of the SRF-PLL.

Therefore when $\theta \simeq \omega$t, *Vd* = *Vm* and *Vq*=0. Thus, the grid phase angle is obtained by a feedback

loop that drives the *q* component to 0, which is necessary for the Park transformation as well. In order to accelerate the synchronization of the PLL an additional term is included ($\omega ff = 2 \cdot 2 \cdot \Pi \cdot fg$).

The tunning parameters of the PI controller of the PLL can be set according with reference [18] as follows:

$$K_p = 2 \times \xi \times \omega_n = \frac{9.2}{t_s} \Rightarrow t_s = 0.05sec \tag{2.3}$$

$$T_i = \frac{2 \times \xi}{\omega_n} = \frac{t_s \times \xi^2}{2.3} \Rightarrow \xi = 0.7 \tag{2.4}$$

2.2.2 CURRENT CONTROL

The current control is also based on the synchronous reference frame and its block diagram is illustrated in Figure 2.5. Since the reference frame is rotating synchronously with the grid voltage vector, the control signals are transformed from AC to DC control variables, therefore when the system is synchronized, the *d*-axis current provides active power and the *q*-axis current generates reactive power. Generally, PI controllers are used for this control topology, as it gives zero steady state error when controlling DC magnitudes.

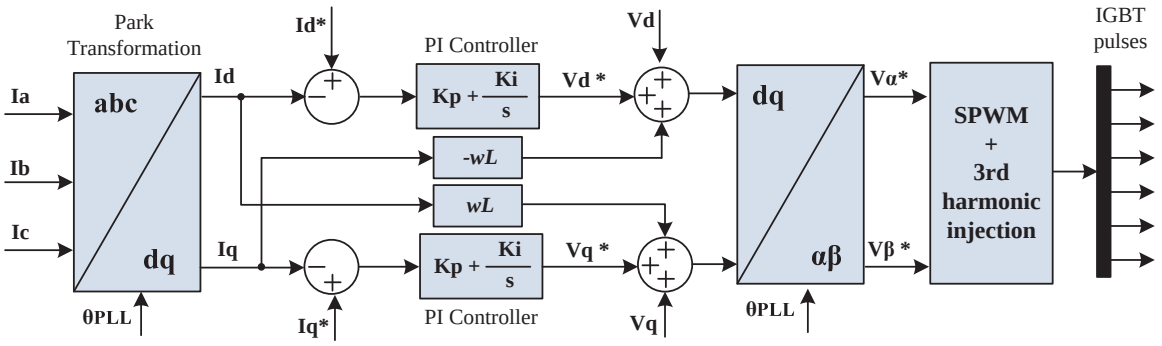

Figure 2.4: Synchronous PI *dq* current control for three-phase two-level voltage source inverter.

Since the *d*-axis and *q*-axis equations are coupled and such an inherent nature of the model will worsen the control performance due to PI regulation is based on decoupled systems, decoupling techniques are required. As shown in Figure 2.5 the *d* and *q* components of the grid voltage are used as feed-forward signals for decoupling, as well as the other two terms *wLiq* and *wLid*.

To sum up, the main advantage of this current control strategy is the easiness of controlling DC signals by using PI controllers, nevertheless this solution presents two well-known drawbacks: the poor disturbance rejection capability even when cross-coupling terms and voltage-feed-forward control is implemented and the impossibility to follow sinusoidal references without steady-state errors [17].

PI TUNNING OF D-AXIS AND Q-AXIS CURRENT CONTROLLERS

The *d*-axis and *q*-axis current loops are responsible to inject the desired active and reactive power to the grid. Both loops must be designed for the same dynamical response, therefore the parameters of the two PI controllers will be identical.

As thoroughly explained in [17], the block diagram of the current loop in the synchronous reference frame *dq* is illustrated in Figure 2.5 . It consists of three transfer functions - PI controller transfer function (*GPI*), delay transfer function (*Gd*) and LCL filter transfer function (*Gf*).

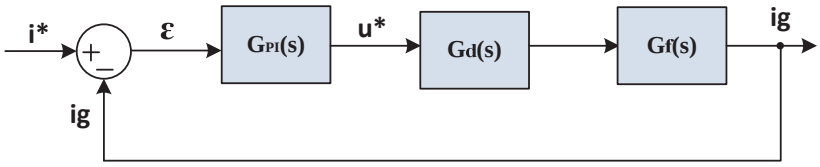

Figure 2.5: Current loop of the PI-based control: *GPI(s)* is the PI controller, *Gd(s)* is the delay due to the microcontroller calculation and PWM and *Gf(s)* is the filter transfer function.

- G_{PI}(s) is the broadly used PI controller transfer function, which in the Laplace domain is defined as:

$$G_{PI}(s) = k_P + \frac{k_I}{s} \tag{2.5}$$

- G_d(s) represents two delay terms. According to [17] the microcontroller will introduce a delay of one sampling time *Ts* due to computational time, additionally, the PWM technique will introduce a delay of half a sampling time due to the time calculation of the IGBTs duty cycle for each period. Hence, the Laplace transfer function is given by:

$$G_d(s) = \frac{1}{1 + 1.5T_s s} \tag{2.6}$$

- G_f(s) is the transfer function of the LCL filter..

$$G_f(s) = \frac{i(s)}{v(s)} = \frac{1}{L_s} \frac{\left(s^2 + \frac{R_d}{L_g}s + z_{LC}^2\right)}{\left(s^2 + \frac{(Lg + Lc)}{Lc}\frac{Rd}{Lg}s + \omega_{res}^2\right)} \tag{2.7}$$

In order to guarantee a good design of the current controller, the integrator time constant T_i is chosen to cancel out the lower corner frequency to increase the bandwidth of the current loops. In this case, T_i is selected to be 0.02 seconds, as a trade-off between a good dynamic response of the system and still good noise rejection.

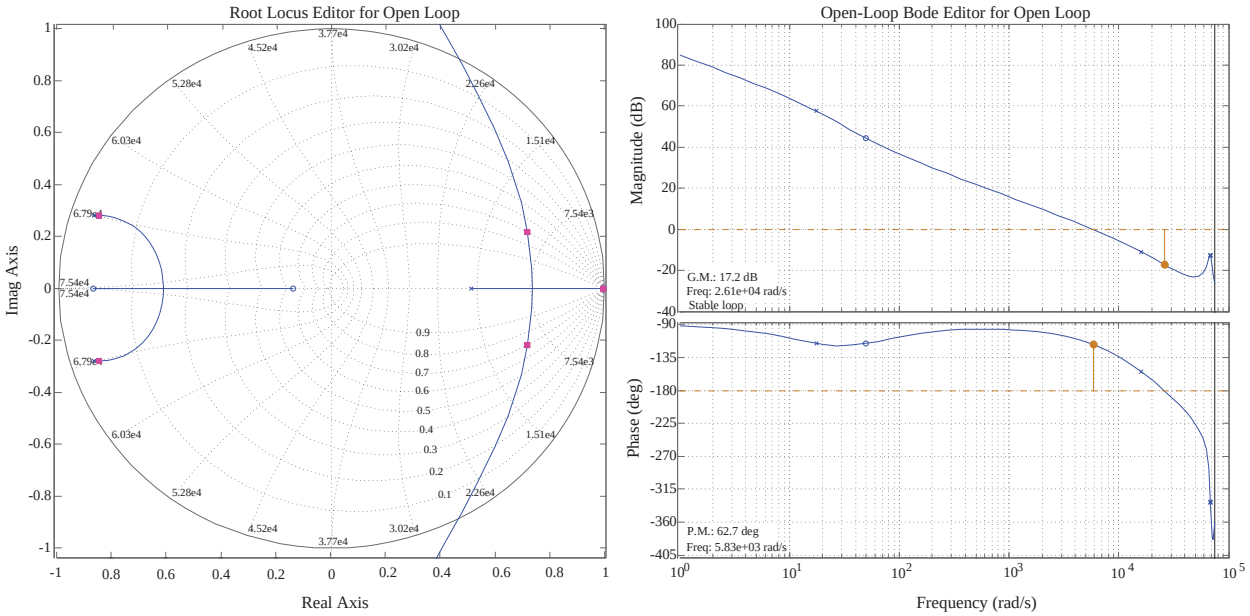

Figure 2.6: Root-locus and open-loop bode response for the PI-based current controller.

Moreover, the current loop presented in Figure 2.6, is introduced in MATLAB/Sisotool toolbox in order to determine the proportional gain k_P of the PI. Then the tunning of the proportional gain establishes the stability phase margin and the bandwidth [19].

As can be noticed in the closed-loop bode plot in Figure 2.7, a gain equal to k_p =2.7 leads to a bandwidth of 1432 Hz (9000 rad/s), which is considered a satisfactory design according to the current control requirement presented in [20], which states that the minimum bandwidth of the current loop is given by:

$$F_{BW} = \frac{1}{T_s \times 20} \Rightarrow 1200Hz \tag{2.8}$$

The open-loop bode plot illustrated in Figure 2.6, demonstrates the high stability of the system since the phase margin (PM) is 62.7° and the gain margin (GM) is 17.2 dB, indicating a stable loop for k_p =2.7.

Further on, in Figure 2.7 the open-loop root locus represented in the discrete domain shows that the LCL dominant poles are well damped as they have a damping factor equal to 0.7 to achieve the *technical optimum* (i.e 5% overshoot) [21]. Furthermore, the high-frequency poles from the LCL-filter are stable as well, since they still are inside the unit-circle.

2.2.3 P-Q OPEN LOOP CONTROL

In order to obtain the reference currents in *dq* synchronous frame, the most straightforward implementation can be done using active and reactive power feed-forward control. According to the instantaneous power theories [22], the three-phase voltages and currents can be represented as space vectors. Equation

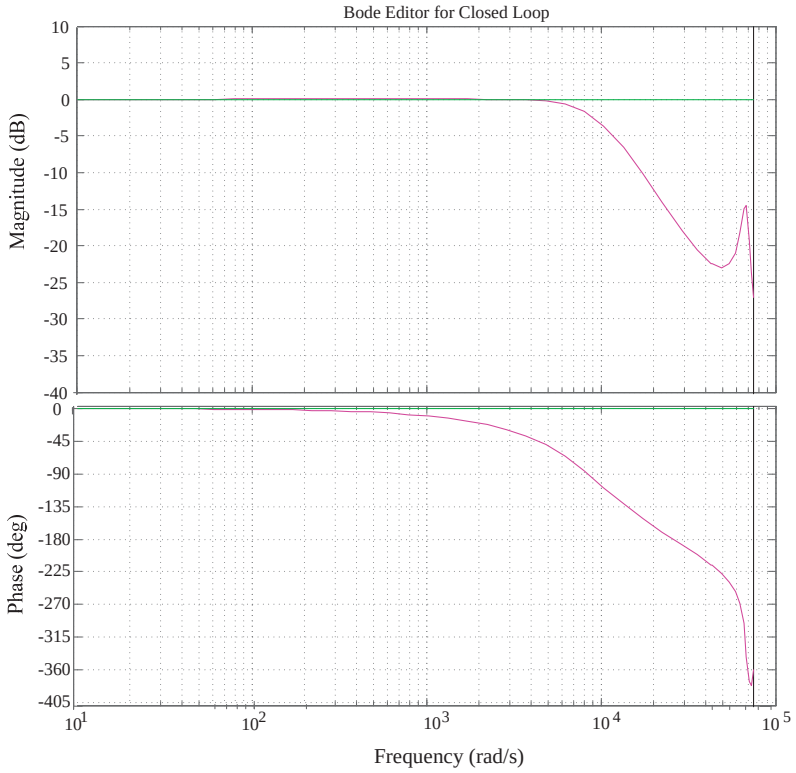

Figure 2.7: Closed-loop bode response for the PI-based current controller.

2.9 defines the conventional power expressed in natural *abc* frame, Equation 2.10 represents the active power in rotating *dq* frame and Equation 2.11 gives the reactive power.

Moreover, the reference current in the d-axis is responsible to inject the active power into the grid while the reference current in the q-axis controls the reactive power control. Indeed, i_q is driven to be 0 to align the grid current vector with the grid voltage vector and therefore obtain unity power factor.

$$P = v_a i_a + v_b i_b + v_c i_c \tag{2.9}$$

$$P = \frac{3}{2}(e_d i_d + e_q i_q) \tag{2.10}$$

$$Q = \frac{3}{2}(e_q i_d - e_d i_q) \tag{2.11}$$

When the d-axis current is aligned with the grid voltage (e_q = 0), the active and reactive power are given by:

$$P = \frac{3}{2} e_d i_d \tag{2.12}$$

$$Q = \frac{3}{2} e_q i_d \tag{2.13}$$

Afterwards, following the basis of the active-reactive control strategy, the reference currents in rotating *dq* frame can be obtained as follows:

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \frac{1}{v_{gd}^2 + v_{gq}^2} \begin{bmatrix} v_{gd} & -v_{gq} \\ v_{gq} & v_{gd} \end{bmatrix} \begin{bmatrix} P^* \\ Q^* \end{bmatrix}$$

where, i_d^* is the d-axis reference active current, i_q^* is the q-axis reference reactive current, v_{gd} is the d-axis grid voltage and v_{gq} is the q-axis grid voltage.

2.2.4 SINUSOIDAL PULSE-WIDTH MODULATION (SPWM) AND 3^{rd} HARMONIC INJECTION

The Pulse-Width-Modulated technique and the addition of the third harmonic to the reference voltage is adopted to generate the gate drive signals of the IGBTs [17]. This technique ensures that the linear modulation range is increased, indeed when setting the amplitude of the injected 3^{rd} harmonics signals as 1/6 of the amplitude of the fundamental reference voltage, the linear modulation range can be increased by 15 % [17].

2.3 LCL FILTER DESCRIPTION MODEL

The three-phase two-level voltage source inverter is connected to the grid via a passive LCL filter to reduce the current ripple in the output of the inverter as well as to comply with the harmonic current injection standards that limit the harmonic content sent to the grid.

The per-phase equivalent diagram of the LCL filter is represented in Figure 2.8.

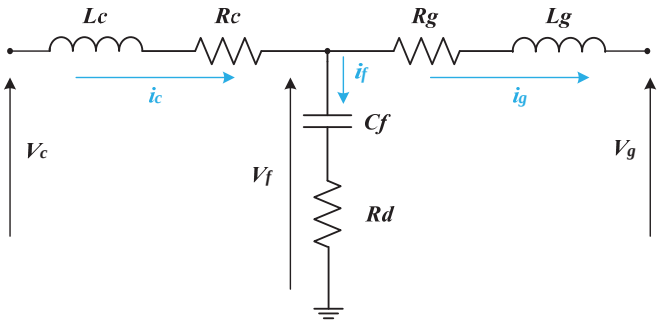

Figure 2.8: Single-phase LCL filter schematic.

Where the converter side inductance and its internal series resistance are respectively L_c and R_c. The grid-side inductance and its internal series resistance are L_g and R_g. C_f represents the capacitor bank which includes a damping series resistance named R_d. The converter, capacitor bank and grid voltages are named V_c, V_f and V_g. In the same manner, the converter, capacitor and grid currents are named i_c, i_f and i_g. The transfer function of the LCL filter can be calculated applying Kirchoff's laws as the relation

between the converter voltage as the input and the grid current as the output. Thus, the transfer function is defined as:

$$F_{LCL} = \frac{i_g(s)}{V_c(s)} = \frac{1 + C_f R_d s}{s^3 A + s^2 B + sC + R_d + R_g} \tag{2.14}$$

where,

$$A = C_f R_g L_c \tag{2.15}$$
$$B = C_f(L_c(R_d + R_g) + L_g(R_d + R_c)) \tag{2.16}$$
$$C = (C_f\left[(R_c R_g) + (R_c R_d) + (R_g R_d)\right] + L_c + L_g) \tag{2.17}$$

The design of the LCL filter parameters has been attained via the step-by-step procedure presented in [23]. The parameters are summarized in Table 2.2. Taking into consideration the LCL filter parameters, the bode plot of the LCL filter is illustrated in Figure 2.9.

Converter-side inductance, L_c	0.319 mH
Grid-side inductance, L_g	0.136 mH
Filter capacitor, C_f	2.27 μF
Damping resistor, R_d	400 mΩ
Converter-side internal resistance, R_c	5 mΩ
Grid-side internal resistance, R_g	3 mΩ

Table 2.2: LCL filter parameters

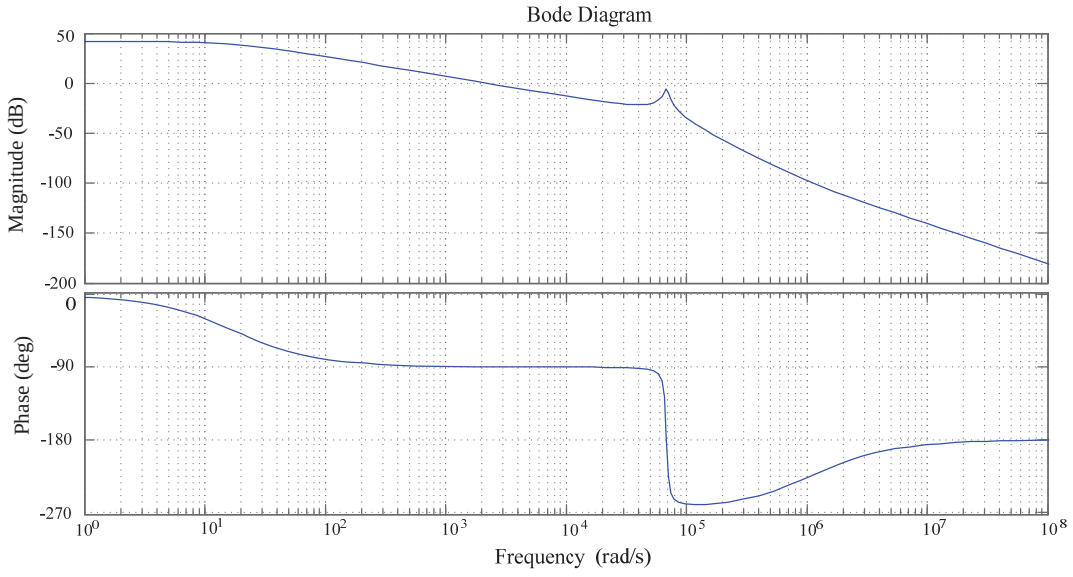

Figure 2.9: Bode diagram of the LCL filter.

CHAPTER 3

ELECTRO-THERMAL MODELLING OF IGBT POWER MODULES

In this chapter the electro-thermal model presented in Chapter 1 is used as a design tool in order to estimate the junction temperature of the power module. The modelling of the device is realized as a function of two aspects - power loss modelling and thermal modelling. The design process is explained side-by-side and the limitations encountered have been highlighted.

3.1 POWER LOSS MODELLING

In order to calculate the total power losses of a power module, the switching and conduction losses of the IGBTs and diodes must be estimated. The modelling can be done via the different approaches, but for the sake of simplicity and the needs of this project, the power loss modelling is attained by means of look-up tables that manufacturers provide in the datasheets.

3.1.1 SWITCHING LOSSES

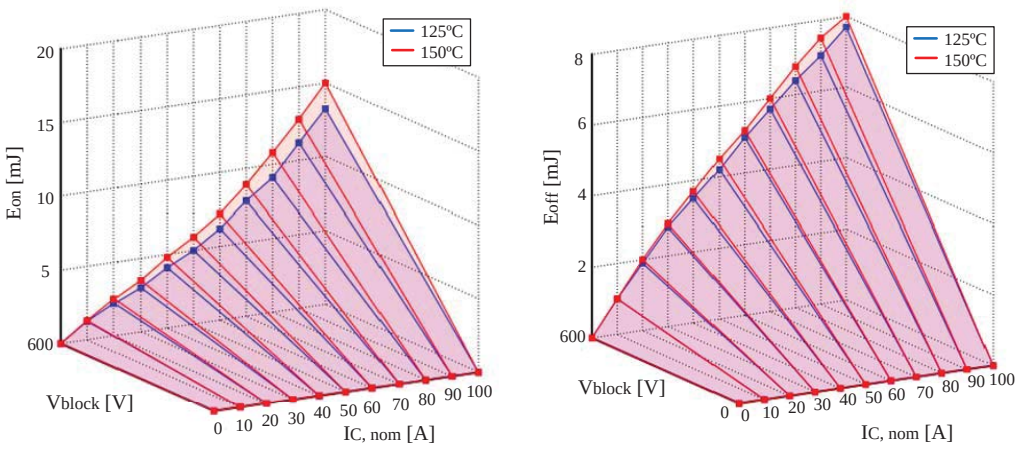

Figure 3.1: Energy loss of FS50R12KT4-B15 IGBT a) Turn-on energy loss and b) Turn-off energy loss.

The energy loss during the turn-on and turn-off switching behaviour has been modelled by means of look-up tables that can be set in PLECS. The model is a four-dimensional matrix, where the input data

is the blocking voltage, forward current and junction temperature, the output data is the energy loss. Figure 3.1 (a) illustrates the look-up table of the turn-on switching losses and Figure 3.1 (b) illustrates the look-up table of the turn-off switching losses of the IGBTs consisting the FS50R12KT4-B15 power module provided by INFINEON.

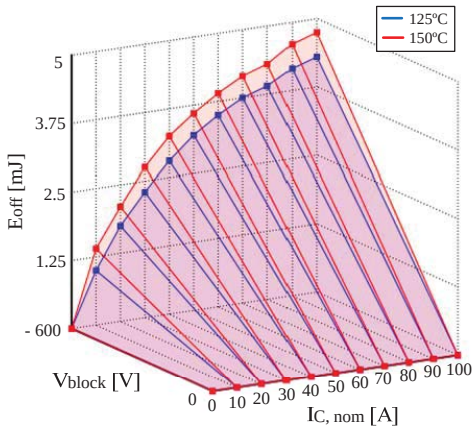

Figure 3.2: Turn-off energy loss of FS50R12KT4-B15 diode.

Moreover, the diodes of the module also contribute to the total power losses, therefore they are also modelled. Since the turn-on losses are very small with respect to the reverse recovery, the datasheets only provide information for the reverse recovery energy loss. Figure 3.2 represents the look-up table of the reverse recovery losses of the diodes consisting the FS50R12KT4-B15 power module.

3.1.2 CONDUCTION LOSSES

Similarly, the same procedure is followed in order to model the conduction losses of power modules. The conduction losses of the IGBT is a two-dimensional matrix, where the input data is the forward current and juction temperature, the output data is the forward voltage drop. Figure 3.3 (a) depicts the look-up table generated in PLECS of the IGBTs consisting the FS50R12KT4-B15 power module and Figure 3.3 (b) illustrates the look-up table of the diodes consisting the FS50R12KT4-B15 power module.

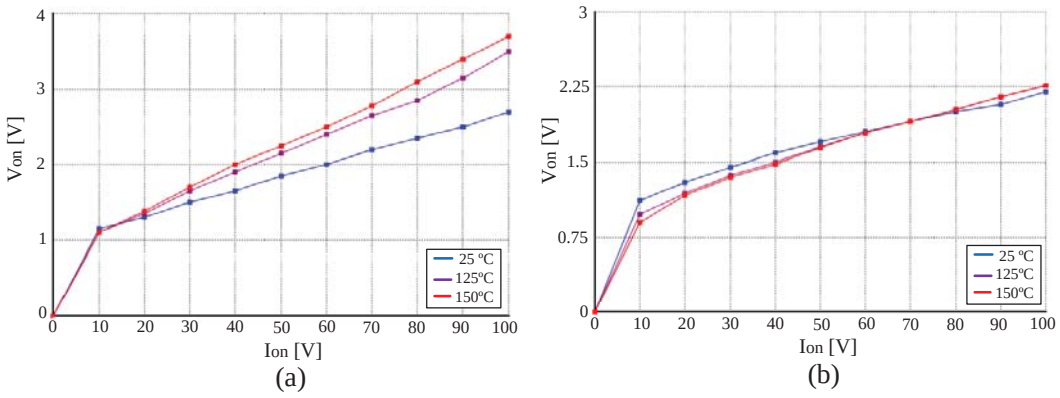

Figure 3.3: Conduction loss of FS50R12KT4-B15 power module a) IGBT and b) diode .

3.2 THERMAL MODELLING

Once the power losses are determined, they have to be optimally conducted through multiple layers consisting the power module to the heat-sink. Since there are two types of commercialized power modules, the ones which include a base plate and the ones that are constructed without base plate, it is meaningful to explain briefly their differences due to the fact that they present different heat dissipation and thermal resistances [3].

As illustrated in Figure 3.4, the power modules containing a base plate, Figure 3.4 (a), the substrate is soldered to a base plate which is mounted on the heat-sink via a thermal grease. This type of power modules present higher thermal resistance chip/heatsink, higher robustness and reduced thermal cycling capability due to the extra solder joint between substrate and base plate [3]. On the other hand, the alternative design is a power module without base plate, Figure 3.4 (b), as can be noticed the substrate is directly mounted to the heat sink. This design presents lower thermal resistance, improved thermal cycling capability, smaller chips and larger ceramic substrates [3].

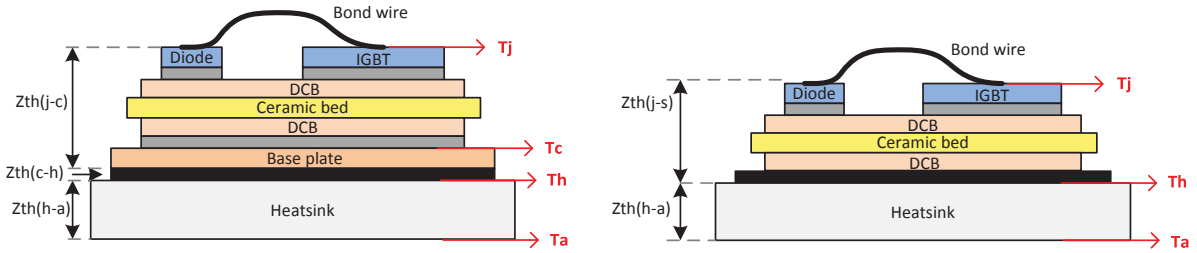

Figure 3.4: Structure of power modules a) with baseplate and b) without baseplate.

3.2.1 HEAT SPREADING

The transient thermal impedance Z_{th} is responsible for the temperature rise through several layers consisting the IGBT with the total dissipated power. Since the number of layers of power modules with and without base plate is different, the total thermal impedance of a power module with and without base plate from junction to ambient can be modelled as depicted in Figure 3.5 [3].

For those modules which are built with a base plate, $Z_{th(j-c)}$ represents the heat dissipated between the junction of the IGBT chips and the module case. On the other hand, those modules which are built without a base plate, the thermal impedance $Z_{th(j-c)}$ cannot be determined, the $Z_{th(j-s)}$ between the junction of the IGBT chip and the heatsink is given instead. Due to this reason, modules with base plate are case rated devices and modules without base plate are heatsink rated devices [3].

The steady-state case temperature for a module with base plate is calculated for constant total power dissipation as follows:

$$T_c = T_a + (R_{th(h-a)} + R_{th(c-h)}) \cdot P_{loss,tot} \tag{3.1}$$

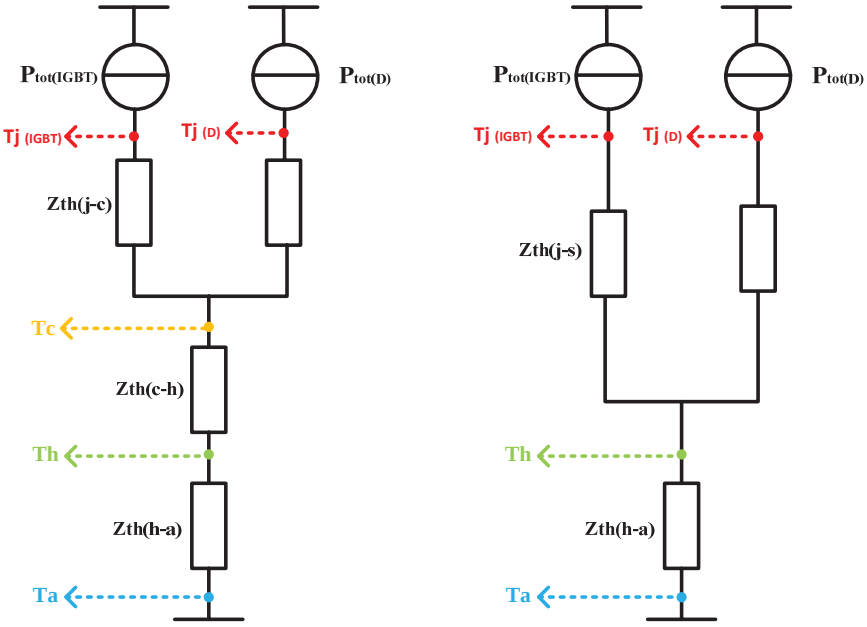

Figure 3.5: Dynamic thermal models for power modules a) with baseplate and b) without base plate.

Similarly, the steady-state heatsink temperature for a module without base plate is given by:

$$T_h = T_a + (R_{th(h-a)} \cdot P_{loss,tot} \tag{3.2}$$

Moreover, the steady-state IGBT junction temperature for a module with base plate is obtained taking into consideration the power losses of the IGBT as follows:

$$T_{j(IGBT)} = T_c + (R_{th(j-c)} \cdot P_{loss,IGBT} \tag{3.3}$$

Following a similar approach, the steady-state junction temperature for a module without base plate is given by:

$$T_{j(IGBT)} = T_h + (R_{th(j-s)} \cdot P_{loss,IGBT} \tag{3.4}$$

3.2.2 THERMAL EQUIVALENT NETWORK

Usually, the dynamic thermal impedance is represented by the thermal resistance R_{th} and the thermal capacitance C_{th} as cascaded RC networks, which model the thermal behaviour of a material [24]. Such RC networks can be modelled via two different approaches:

- **Foster model:** normally parameters are provided by the manufacturers on the datasheets. However, the model is a mathematical fitting of Z_{th} and do not show any physical meaning. The analytical formula which relates the thermal impedance with the thermal resistance is described as [24]:

$$Z_{th(j-c)}(t) = \sum_{i}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \qquad ; \qquad \tau_i = R_i \cdot C_i \tag{3.5}$$

  Thus the junction-to-case thermal model of the power module is modelled as shown in Figure 3.6, where the number of RC terms is not a fixed value. Notice that this model needs to be connected with the heatsink and interface material thermal model.

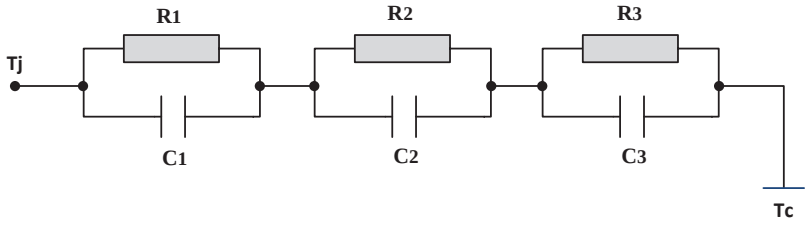

Figure 3.6: Foster thermal model.

- **Cauer model:** it is based on the geometrical and material properties of the layers, therefore it has physical meaning for each RC lump. Cauer model can be obtained by Finite Element Method (FEM) based on the geometry and materials of the module. The number of RC terms is defined by the number of layers inside the IGBT as can be observed in Figure 3.7 [24]. Even though Cauer model has a high accuracy, it will not be selected due to the limited time to render the present master thesis.

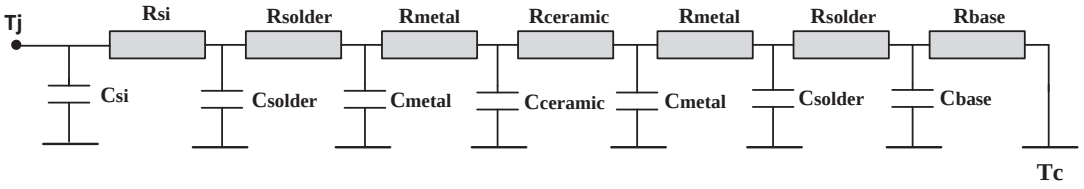

Figure 3.7: Cauer thermal model.

3.2.3 THERMAL MODELLING OF THE HEATSINK

Normally, the thermal resistance from junction-to-case and the thermal resistance from case-to-heatsink are given by the manufacturers on the datasheet. However, the thermal resistance from heatsink-to-ambient must be selected depending on the temperature needed to be dissipated and the type of cooling system employed.

Moreover, the thermal capacitance from heatsink-to-ambient is much larger than the one inside the power module from junction-to-case. As can be appreciated in Equation 3.6, the dynamic thermal impedance mainly depends on two terms τ and R_{th}.

$$Z_{th}(t) = \sum_{i}^{n} R_i \left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{3.6}$$

Therefore, the larger thermal capacitance the larger time constant, which determines the time to reach the steady-state junction temperature. As can be observed from Equation 3.6, when steady-state is achieved (t = 5 $\cdot\tau$) the dynamic thermal impedance only depends on the thermal resistance and thus, the thermal capacitance does not have any longer effect (Z_{th} = R_{th}). Therefore, it is smart to neglect the larger thermal capacitances in $Z_{th(c-h)}$ and $Z_{th(h-a)}$ to execute faster thermal simulations. Consequently, the steady-state case temperature will be set as the reference temperature for each simulation.

In order to analytically calculate the steady-state case temperature, two assumptions are made:

- The heatsink-to-ambient temperature fluctuation must be: $\Delta T_{(h-a)} \leq 30°C$.
- The case temperature, T_c, should never exceed 80°C.

Once the total power losses are obtained, the heatsink-to-ambient thermal resistance can be calculated considering the above assumptions and the worst case scenario(the IGBT that produces the higher power loss), as follows:

$$R_{th(h-a)} = \frac{\Delta T_h}{P_{tot}} \leq \frac{30°C}{P_{tot}} \tag{3.7}$$

Further on, the case temperature can be derived from Equation 3.1 since the case-to-heatsink thermal resistance is a known parameter.

3.3 CONCLUSIONS

The thermo-electrical modelling of power semiconductor modules has been thoroughly explained. The power loss modelling is based on look-up tables provided by the manufacturers in the datasheet that can be implemented in PLECS Blockset in Simulink environment so that the instantaneous switching and conduction losses can be calculated. On the other hand, the thermal modelling is based on a thermal equivalent network named *Foster model*, which parameters are provided also in the datasheets. The only parameter that is not provided in the datasheet is the thermal impedance of the heatsink, this parameter should be selected in accordance with the desired dissipated heat, so that the higher heat removal the higher cost. For this study, the same heatsink will be considered for each IGBT solution, it should be noted that an extended approach is to introduce also the design variable of heatsink parameter so the total cost of IGBT modules and cooling system can be considered. However due to the constrained time frame, it is not included.

Part III

Design Guideline for Smart Derating of Switching Devices

CHAPTER 4

THERMAL STRESS AND NUMBER-OF-CYCLE ANALYSIS

In this chapter six different IGBT solutions are evaluated and simulated at different power levels when the same heatsink is considered. The importance of thermal stress is emphasized by relating it with the design margins, the lifetime, the efficiency and cost performances. An equation for each IGBT solution describing the relation between the number of cycles to failure and the power of the PV inverter is obtained.

4.1 INTRODUCTION

In order to efficiently select the switching device most suitable for a given inverter topology, the design specifications, the design margin limits and the switching device lifetime must be well-defined. Therefore, it is intended to establish a general guideline for smart derating of switching devices that everyone could use.

Power cycles cause temperature changes of the switching devices depending on the loading of PV inverters, which yields to a mechanical stress that can result in a failure and as a consequence reduced lifetime. There are three different kinds of stress factors:

- *Power cycling due to the switching frequency of the devices* (t_{cycle} = T_{sw}). This factor which depends on the converter design is usually neglected when calculating the lifetime of switching devices. As shown in Figure 4.1, the power cycling fluctuations are very small and they do not highly contribute on the lifetime of the switching device.

- *Power cycling due to the line frequency* (t_{cycle} = T_{grid} = 1/50Hz = 0.02s). This factor highly influences the lifetime of the switching devices, the junction temperature fluctuates with the same frequency as the line frequency, consequently the mean junction temperature and its fluctuation are not longer neglectable, it has a great impact on the IGBT degradation.

- *Power cycling due ambient temperature and solar irradiance*. The thermal stress corresponding to environmental disturbances will change hugely but with slow time cycling. Mission profile data is given as a function of the measured solar irradiance and ambient temperature for the real field where the PV inverter operates. Figure 4.2 represents the junction temperature fluctuation due to different solar irradiance and ambient temperature for one day mission profile.

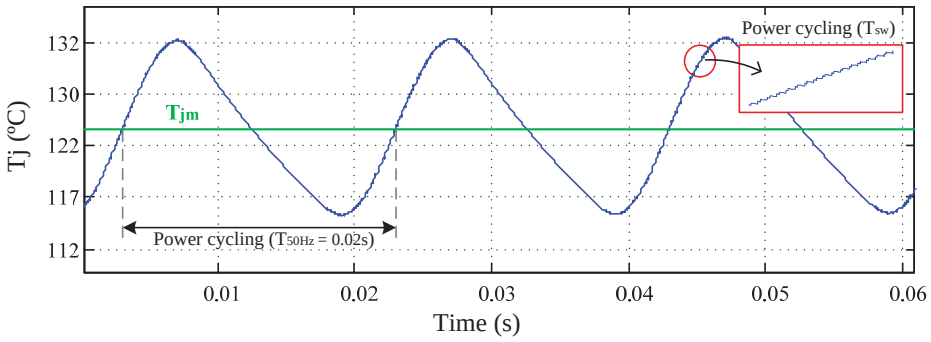

Figure 4.1: Power cycling due to the switching frequency of the devices (t_{cycle} = T_{sw}) and due to the line frequency (t_{cycle} = 0.02 s).

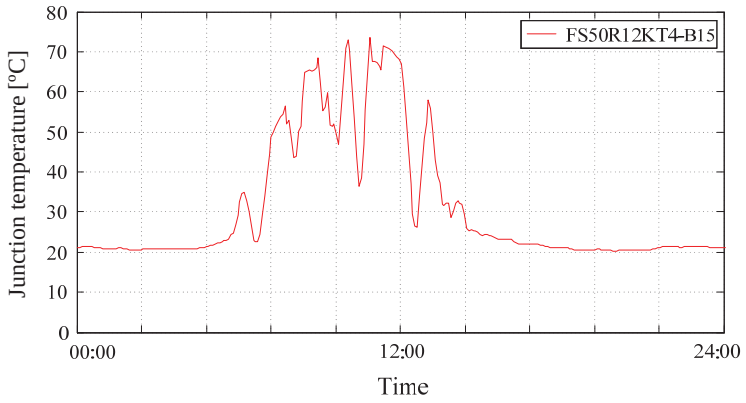

Figure 4.2: Power cycling due to the solar irradiance and ambient temperature for one day mission profile.

4.2 THERMAL PERFORMANCE

The three-phase PV inverter under analysis is rated at 21 A_{rms}, thus the selected switching device current ratings are 35 A, 50 A and 75 A. Two IGBTs have been chosen for each current level to conduct an appropriate thermal performance evaluation. Table 4.1 summarizes the devices studied.

According to the previous loss and thermal models, the junction temperature for each device can be simulated via PLECS Blockset in Simulink environment. As previously discussed, the thermal impedance from junction-to-case, $Z_{th(j-c)}$, is modelled as a multi-layer Foster RC network. The thermal parameters are presented in Table 4.1, where the thermal resistance R_{th} determines the steady state mean value of the junction temperature and the thermal capacitance defined by the manufacturer datasheet as a time constant τ dictates the dynamic change or fluctuation of the junction temperature [25].

The simulations presented and evaluated in this section show only one of the three possible types of power cycling - power cycling due to the line frequency (t_{cycle}= 0.02s). Figure 4.3 illustrates the

IGBT-Module	Collector current	Collector-emitter voltage	$R_{th(j-c)}$ per IGBT	$R_{th(c-h)}$ per module	$R_{th(h-a)}$ per module
FS35R12KT3	35 A	1200 V	0.60 K/W	0.02 K/W	0.005 K/W
FS35R12KE3G	35 A	1200 V	0.60 K/W	0.02 K/W	0.005 K/W
FS50R12KT3	50 A	1200 V	0.45 K/W	0.02 K/W	0.005 K/W
FS50R12KT4$_{B15}$	50 A	1200 V	0.54 K/W	0.02 K/W	0.005 K/W
FS75R12KT3	75 A	1200 V	0.35 K/W	0.02 K/W	0.005 K/W
FS75R12KT4$_{B15}$	75 A	1200 V	0.39 K/W	0.02 K/W	0.005 K/W

Table 4.1: Power modules studied for the smart derating of switching devices.

junction temperature simulation results under rated and steady-state conditions (P = 15 kW) for each nominal current and one IGBT solution. It can be appreciated that each device solution presents thermal performances that vary depending on the rated current level (35 A, 50 A and 75 A). Also, it is observed the unequal thermal distribution among IGBTs and free-wheeling diodes due to different power loss and thermal impedance distribution.

The mean junction temperature value T_{jm}, the temperature fluctuation ΔT_{jm} and the peak junction temperature T_{j-peak} for different IGBT solutions are illustrated in Figure 4.4 (a), 4.4 (b) and 4.5 respectively. The IGBTs whith higher rated current (75A) have lower T_{jm} and ΔT_{jm} during nearly the whole operation range, this fact is because the IGBTs rated at 75A generate lower losses than the IGBTs rated at 35A when operated at the same conditions. Accordingly, it makes sense to select the IGBT with higher nominal current in order to guarantee smaller junction temperature. Furthermore, it is interesting to observe that the improvement on the IGBT packaging leads to unequal junction temperature distribution.

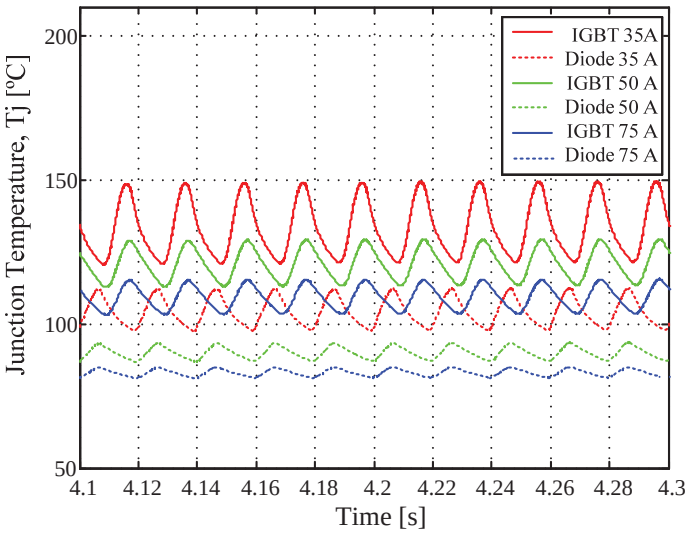

Figure 4.3: Simulated junction temperature of the 2L-VSI under rated conditions (15 kW) for three sets of power modules.

Figure 4.4 (a) shows that the mean junction temperature of each IGBT solution presents slightly deviations for the same rated current. As an example, it becomes apparent that the IGBT FS50R12KT4-B15, which is the latest technology rated at 50 A, tends to have smaller junction temperature due to smaller power losses dissipated. On the other hand, the IGBT FS50R12KT3, which is the former technology rated at 50 A, tends to have higher junction temperatures. Therefore, when selecting IGBTs rated at the same nominal current, two parameters have a great impact on the junction temperature - total power losses and thermal resistances.

The junction temperature fluctuation is obtained according to Equation 4.1, where *tp* is the end of the loss pulse, t_T is the entire length of the period and $R_{th\nu}$ is the thermal resistance of a multi-layer Foster/Cauer RC network [3]. Figure 4.4 (b) shows that the former technology at 75 A nominal current (IGBT3), experiences analogous ΔT_{jm} as the latest technology (IGBT4) at 50 A nominal current. According to Equation 4.1 and since the former technology of IGBT devices have higher power losses per IGBT than the latest technology, it is expected that both present similar ΔT_{jm} as the simulation results demonstrate.

$$\Delta T_j(t_p) = P \times \sum_{\nu=1}^{n} R_{th\nu} \times \left(\frac{1 - e^{\frac{-tp}{\tau_{th\nu}}}}{1 - e^{\frac{-t_T}{\tau_{th\nu}}}} \right) \tag{4.1}$$

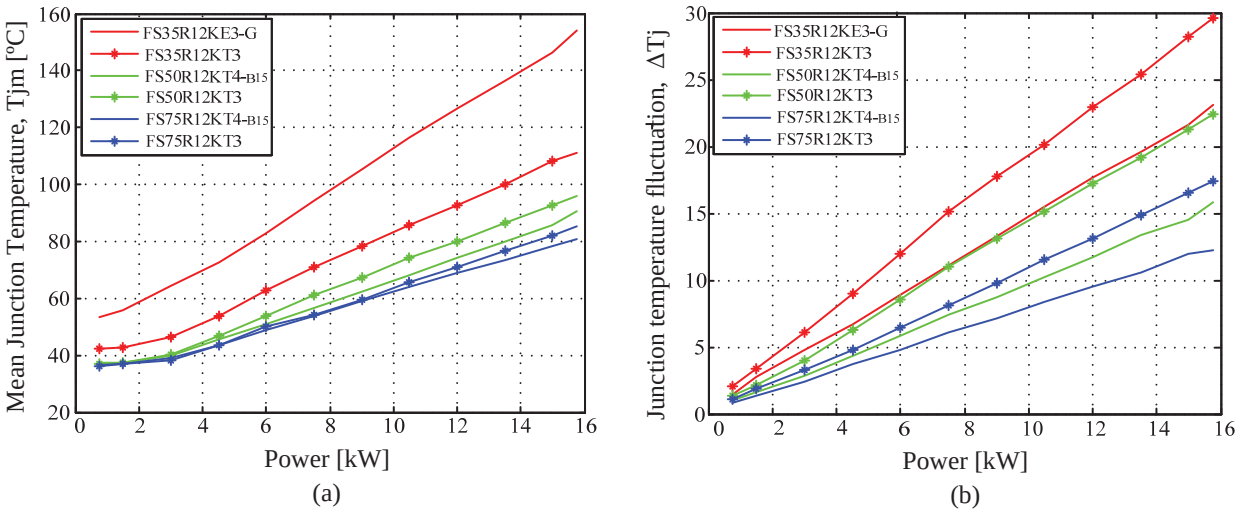

Figure 4.4: Simulated junction temperature for different IGBT solutions, a) mean value and b) fluctuation.

Finally, it is worth to mention that the switching devices must be operated under the maximum allowable junction temperature, which usually is 150°C. However, as a general rule, engineers define a lower junction temperature design limit, in order to guarantee enough margin between the operating junction temperature and its maximum limit, as well as to assure longer lifetime. Figure 4.5 (b) illustrates the maximum junction temperature and its typical design limit, it is interesting to observe that the IGBTs rated at 35 A nominal power exceed the design specifications even though they can handle the current and voltage of the 2L-VSI, while the performance of the other IGBT solutions fairly comply with the design limit. In case the power module exceeds a few degrees the design limit, the improvement of the heatsink/cooling system could lead to smaller junction temperatures and therefore fulfil the design target.

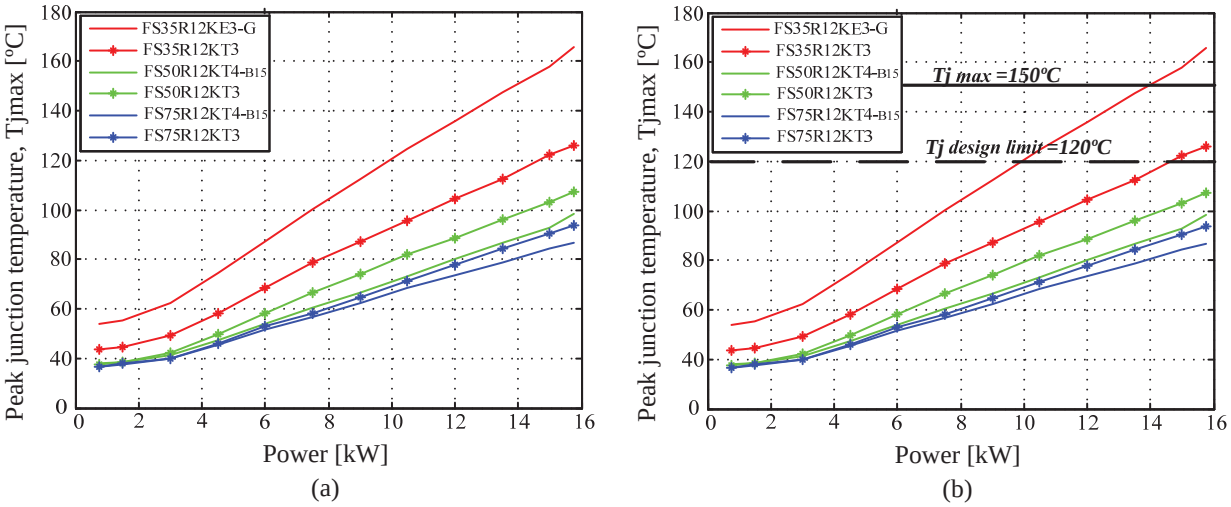

Figure 4.5: Simulated junction temperature for different IGBT solutions a) maximum junction temperature and b) thermal design margin.

4.3 NUMBER OF CYCLES ESTIMATION

In this Section, only the fast power cycling due to line frequency (t_{cycle}=0.02s) is considered, slow cycling due to the solar irradiance and ambient temperature will be treated in Section 5.3

Once the junction temperature fluctuation ΔT_{jm} and the mean value T_{jm} is extracted, the number of cycles to failure N_f of the IGBTs can be estimated based on the Bayerer model as shown in Equation 4.2. The coefficients A, β_1, β_2, β_3, β_4, β_5 and β_6 have to be determined via accelerated thermal tests, however it requires a lot of time and effort. Indeed, these coefficients have been published in [3] by Semikron. Parameters, upper and lower limits and coefficients are summarized in Table 4.2.

$$N = A \cdot (\Delta T_j)^{-\beta_1} \cdot \exp\left(\frac{\beta 2}{T_{j,min} + 273}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{4.2}$$

Parameters	Symbol	Unit	Limits	Coefficient	Value
Technology factor	A	-	-	-	$9.34 \cdot 10^{14}$
Temperature fluctuation	ΔT	K	45...150	β_1	-4.416
Min. junction temperature	$T_{j,min}$	$°C$	20...120	β_2	1285
Pulse duration	t_{on}	s	1...15	β_3	-0.463
Current per bond foot	I_B	A	3...23	β_4	-0.716
Blocking voltage/100	V_c	V	6...33	β_5	-0.761
Bond wire diameter	D	μm	75...500	β_6	-0.5

Table 4.2: Parameters and limits for the calculation of number of power cycles based on the Bayerer model [3].

Since the parameter t_{on} is defined for a range between 1 to 15 seconds and the time period t_{on} for the power cycling due to the line frequency is 0.01 seconds, the model can give an incorrect lifetime esti-

mation. Consequently, the influence on the cycling capability due to t_{on} will be considered according to the two application notes from Infineon [26] 1) *Power Cycling capability for modules rated ant* $T_{vj,op}$= *150°C*, which shows the number of cycles versus the junction temperature fluctuation at different maximum junction temperatures, and 2) *Power Cycling capability: typical dependence on* t_{on}, which shows the dependence of N_{cyc} = f(t_{on}) (Equation 4.3), when the t_{on} range is between 0.1s to 60s. Even though the lower limit is still 10 times higher than the heating time for the real application, it is the best approach that can be found in the present state-of-the-art [26].

$$\frac{N_{cyc}(t_{on})}{N_{cyc}(1.5s)} = \left(\frac{t_{on}}{1.5s}\right)^{-0.3} \quad ; \quad 0.1s < t_{on} < 60s \tag{4.3}$$

Figure 4.6 presents the estimated number of cycles to failure at different power levels for the aforementioned IGBTs. As can be observed, the lifetime decreases while increasing the power level as expected. The outcome of this analysis indicates which IGBT solutions are prone to longer operating hours. It can be further appreciated that the improvement of the packaging technology has a remarkable influence on the lifetime of the device, for example, IGBT FS75R12KT4-B15 (IGBT4 technology) shows higher number of cycles than the IGBT FS75R12KT3 (IGBT3 technology) for the entire operating range.

As it can straightforwardly be appreciated in Figure 4.6, the IGBT FS75R12KT3 (former technology at 75 A) and the IGBT FS50R12KT4-B15 (latest technology at 50 A) show similar number of cycles. In other words, since both imply similar lifetime, the cost of the device should dictate which is the IGBT that must be selected.

Once the relationship between the number of cycles to failure and power level is graphically represented, it can now be inferred a mathematical formula by means of curve fitting, the software OriginLab is used to obtain the best fitting curve. The general fitting function is given as follows:

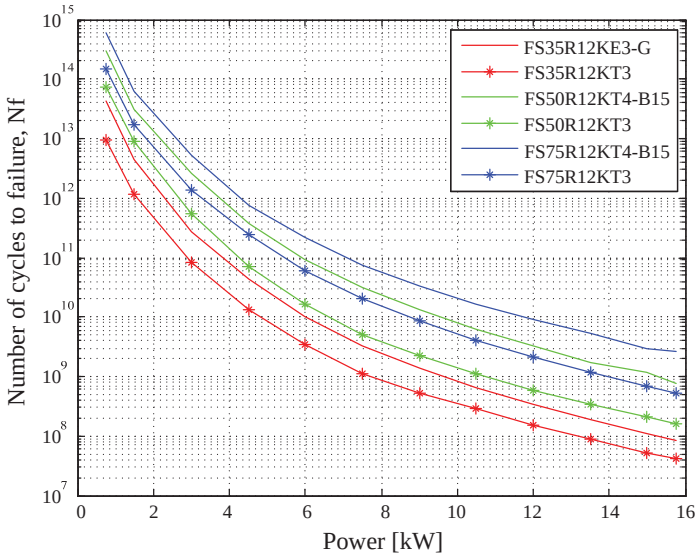

Figure 4.6: Number of cycles to failure for different IGBT solutions (t_{cycle} = 0.02 s) considering a constant ambient temperature (25°C).

$$N_f = a \cdot P^b \tag{4.4}$$

where N_f is the number of power cycles and *P* is the active power of the 2L-VSI; *a* and *b* are the fitting parameters obtained using OriginLab. The values for each IGBT solution are summarized in Table 4.3 .

IGBT-Module	a	b	IGBT-Module	a	b
FS35R12KT3	$2 \cdot 10^{25}$	-4.17	FS35R12KE3G	$4 \cdot 10^{26}$	-4.426
FS50R12KT3	$9 \cdot 10^{26}$	-4.448	FS50R12KT4$_{B15}$	$8 \cdot 10^{26}$	-4.243
FS75R12KT3	$4 \cdot 10^{26}$	-4.226	FS75R12KT4$_{B15}$	$1 \cdot 10^{27}$	-4.17

Table 4.3: Parameters of the Equation 4.4 ($t_{cycle} = 0.02s$) .

4.4 EFFICIENCY

The efficiency of the given 2L-VSI under different active power outputs has been acquired via PLECS Blockset in Simulink environment and plotted in Figure 4.7. Obviously, the loss distribution of power devices vary while the active power changes, which yields to varied efficiency performances that could lead to reduced reliability of the power converter.

Among different IGBT solutions, the larger switching losses of the power module leads to the lower efficiency performances as can be seen in Figure 4.7. It must be highlighted that in contrast with the former IGBT technologies (IGBT3), the latest IGBT technology released to the market (IGBT4) present a remarkable higher efficiency as illustrated in Figure 4.7.

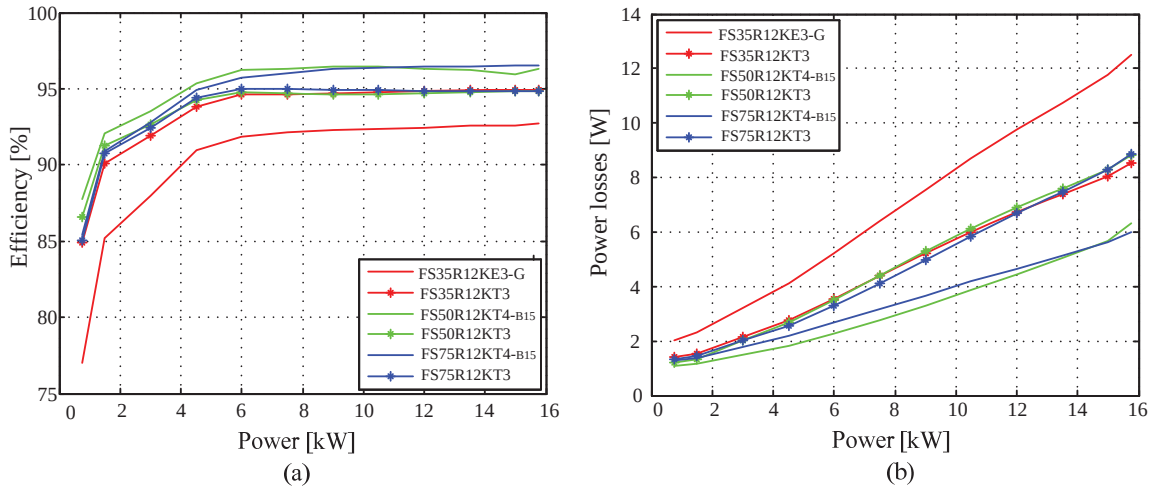

Figure 4.7: Simulated results for different IGBT solutions, a) Efficiency and b) Total power losses.

4.5 CONCLUSION

In this chapter it has been proven that switching devices rated at different nominal currents have shown unequal thermal performances leading to varied-lifetime performances. Also, the continuous improvement of the packaging technology shows a remarkable lifetime increase, which mainly depends on the lower power losses that IGBT4 technology presents. The relationship between the number of cycles to failure and active power has been graphically represented and a equation has been obtained for each IGBT solution.

CHAPTER 5

MISSION PROFILE BASED LIFETIME PREDICTION

In this chapter a real field mission profile (the measured ambient temperature and solar irradiance) is considered to quantify the accumulated damage over one year and further estimate the expected total lifetime of power semiconductor modules. The bond wire failure mechanism is the main focus of this study, therefore two type of stresses are analysed - power cycling due to line frequency and power cycling due to ambient temperature and solar irradiance.

5.1 INTRODUCTION

In a real operating environment power semiconductor modules consisting PV inverters are exposed to electrical and thermal stresses that are influenced by non-uniform ambient temperatures and solar irradiances. Thus, this section considers the mission profile (measured ambient temperature and solar irradiance) of the real field where the converter will perform. Figure 5.1 (a) and (b) represents the available mission profile recorded over one year, a zoomed view can be observed for one day mission profile in Figure 5.1 (c) and (d). The ambient temperature and the solar irradiance have been measured at three different sampling rates - 5 minutes per data, 5 seconds per data and 1 second per data - at Aalborg University (Denmark) from October 2011 to September 2012.

By considering the mission profile, a realistic loading of the inverter can be obtained, thus the analytical lifetime model considered in the present master thesis (Bayerer model) can be applied for a long-term stress analysis. This offers the possibility to predict the used life of a given inverter for the two type of stresses under analysis - power cycling due to line frequency and power cycling due to ambient temperature and solar irradiance.

5.2 LIFETIME CONSUMPTION DUE TO LINE FREQUENCY POWER CYCLING

The long-term mission profile data must be correctly transformed into the corresponding thermal stress of power devices, however, the large amount of loading data can be difficult to handle. Basically, the accumulated damage for one year mission profile has been calculated by three steps that are thoroughly explained in the following.

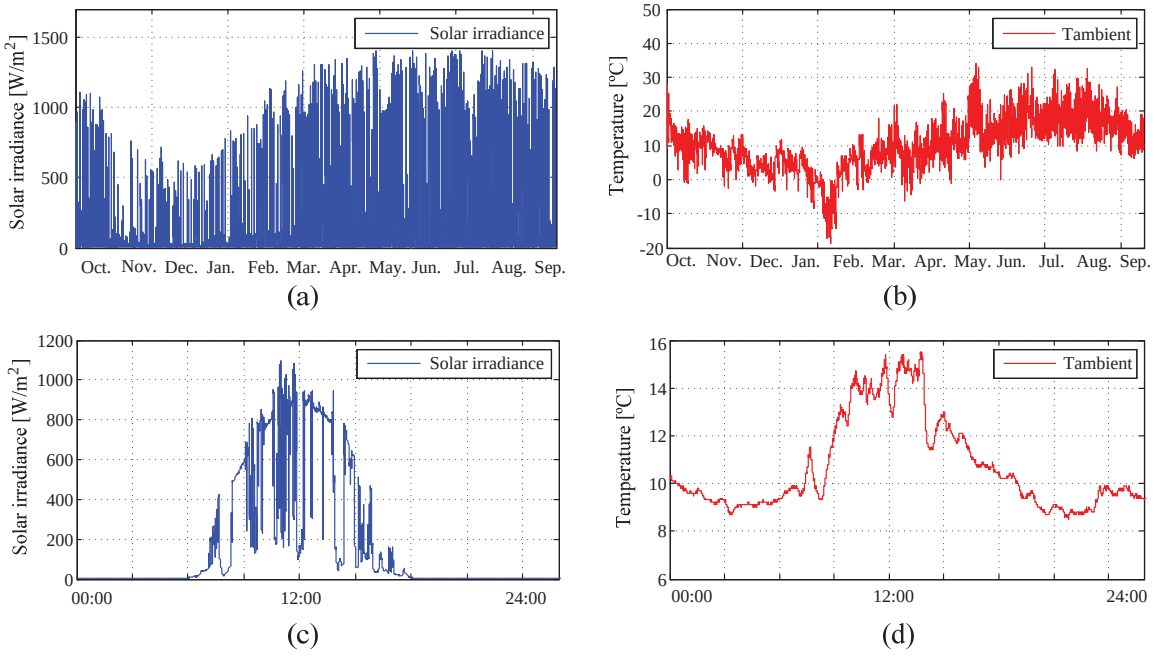

Figure 5.1: Mission profile recorded with a sampling rate of 1 second per data at Aalborg University a) one year solar irradiance, b) one year ambient temperature c) one day solar irradiance and d) one day ambient temperature.

5.2.1 TOTAL POWER OF THE INVERTER BASED ON MISSION PROFILE DATA

The first step is to calculate the maximum power fed into the converter for different solar irradiances and ambient temperatures. Thus, an example of a PV string model based on a BP365 65W module implemented in PLECS Blockset has been used.

The non-linear IV characteristic is obtained based on a non-linear current source that uses the Shockley diode PV model presented in [27]. Moreover, the PV string parameters can be adjusted for the desired nominal power. Since the nominal power of the 2L-VSI is 15 kW, the number of PV modules in string has been set to 45 and the number of PV modules in parallel has been set to 6, when the solar irradiance is 1000 W/m^2 and the ambient temperature is 25 °C.

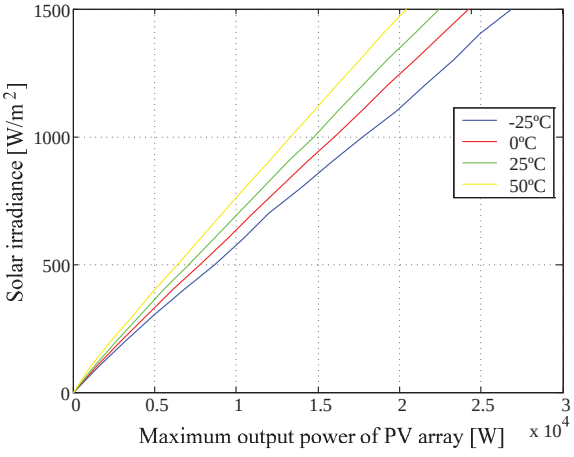

Figure 5.2: Maximum output power of the PV array under different ambient temperatures and solar irradiances.

The PV string model is used to calculate the corresponding current and voltage values based on a 15 kW PV panel installation for four different ambient temperatures (-25°C, 0°C , 25°C and 50°C) and

for 16 different solar irradiances (changes from 0 W/m^2 to 15000 W/m^2). The maximum output power of the PV array under different ambient temperatures and solar irradiances is summarized in Figure 5.2.

In order to acquire the output power based on the mission profile data an interpolation has been done. The output power of the PV array has been obtained according to:

1. It is selected one of the four different temperatures (-25°C, 0°C , 25°C and 50°C) as a function of the ambient temperature from the mission profile data. The closest ambient temperature is chosen.
2. The maximum output power of the PV array is obtained through an interpolation, as a function of the solar irradiance, for the ambient temperature previously selected in the first step.

The obtained results are plotted in Figure 5.3 for a yearly and daily mission profile.

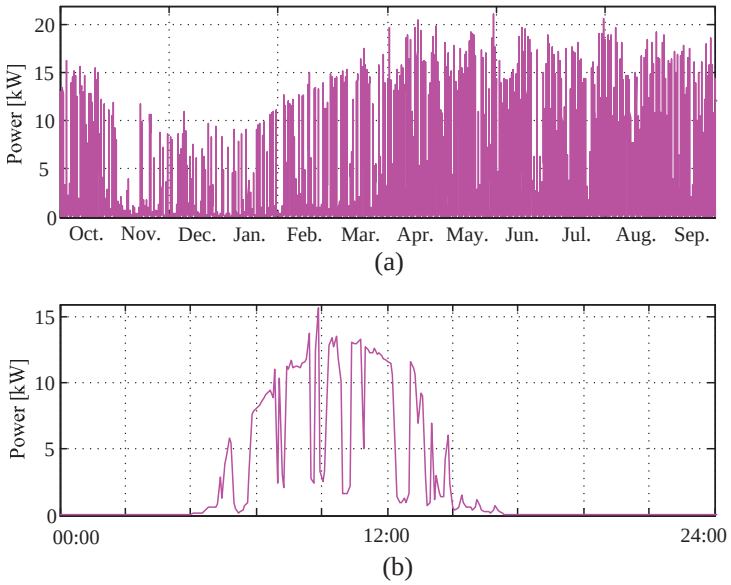

Figure 5.3: Total power of the inverter (5 minutes per sampling data) at Aalborg University a) a yearly mission profile and b) a daily mission profile.

5.2.2 IGBT JUNCTION TEMPERATURE BASED ON MISSION PROFILE DATA

In order to obtain the realistic thermal stress experienced by the IGBTs, the junction temperature must be calculated as a function of the PV inverter power.

As previously exposed in Section 4.3, the relationship between the junction temperature and the power of the converter has been acquired by simulations in Simulink/PLECS blockset. However, since the ambient temperature for all the simulations have been set to 25°C, it is not precise to base the analysis on the junction temperature as a function of the total power. Thus, the solution is to calculate the fluctuation of the junction-to-ambient temperature as a function of the total power and further add the real ambient temperature from the mission profile data. Moreover, six IGBTs solutions have been studied, nonetheless only the latest IGBT solutions (IGBT4 technology) at 50 A and 75 A nominal current are presented.

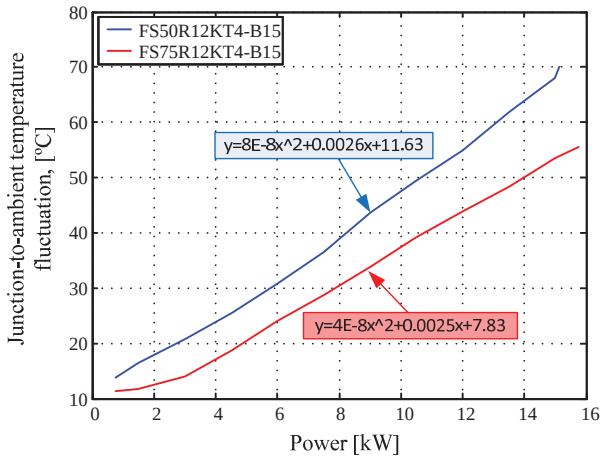

Figure 5.4: Simulated junction-to-ambient temperature at different power levels for two IGBT solutions (FS50R12KT4-B15 and FS75R12KT4-B15).

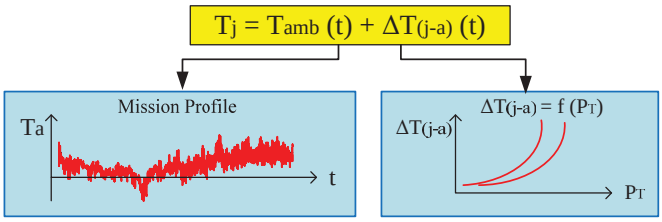

Figure 5.5: Block diagram of the junction temperature calculation considering the mission profile data.

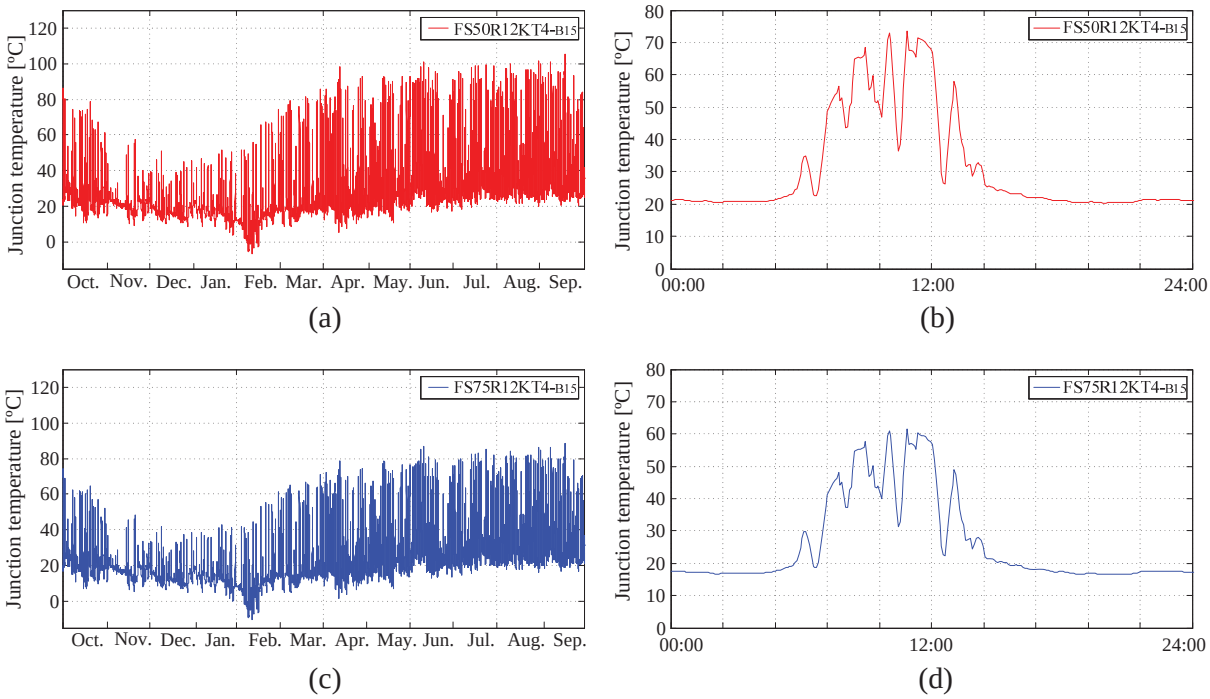

Figure 5.6: Estimated IGBT junction temperature (5 minutes per data) a) one year mission profile with IGBT FS50R12KT4-B15, b) one day mission profile with IGBT FS50R12KT4-B15 c) one year mission profile with IGBT FS75R12KT4-B15 and d) one day mission profile with IGBT FS75R12KT4-B15.

Figure 5.4 illustrates the relationship between the junction-to-ambient temperature as a function of the power of the converter and the fitting curve for each IGBT solution. Further on, the junction temperature is calculated as illustrated in Figure 5.5 and the outcome result is plotted in Figure 5.6.

5.2.3 LIFETIME PREDICTION MODEL

Among the three dominant failure mechanisms of IGBT modules, this analysis is focused on the failure mechanism caused by power cycling - wire bond lift-off. Power cycling raises and lowers the chip temperature at short intervals of time and since the line frequency power cycling has a periodicity of 0.02 seconds, this type of stress highly contributes to the bond wire degradation.

In the real field, the solar irradiance and ambient temperature fluctuation causes non-uniform thermal stresses over the year depending on different seasons, weather conditions and locations. The knowledge of the mission profile for a particular site offers the possibility to evaluate the cumulative damage used for one year time frame. Thus, the Palmgren-Miner linear cumulative damage model [4], shown in Equation 5.1, can be applied in order to calculate the expected life of power semiconductor devices.

$$\sum_i \frac{n_i}{N_i} = 1 \tag{5.1}$$

where n_i is the number of temperature cycles due to the line frequency cycling, the line frequency is 50 Hz and the mission profile data has been recorded with a sampling rate of 5 minutes per data, therefore n_i = 50· 5 · 60 = 15000 cycles each 5 minutes. Moreover, N_i is the number of cycles to failure for the same cycle type and same stress as n_i. Previously, the number of cycles to failure as a function of the total power of the inverter has been determined (see Table 4.3), therefore, the damage corresponding to this type of cycle can be easily obtained and the result is presented in Table 5.1 for two IGBT solutions. Note that failure occurs when the right side of Equation 5.1 reaches 1.

IGBT-Module	Load	t_{on}	Accumulated damage per year	Lifetime consumption per year
FS50R12KT4-B15	Line frequency	0.01 s	0.0477	4.77 %
FS75R12KT4-B15	Line frequency	0.01 s	0.0191	1.91%

Table 5.1: Lifetime consumption due to the line frequency power cycling based on the Palmgren-Miner model [4] for one year mission profile .

5.3 LIFETIME CONSUMPTION DUE TO AMBIENT TEMPERATURE AND SOLAR IRRADIANCE POWER CYCLING

The second type of cycling exposed by the IGBTs is due to the solar irradiance and ambient temperature fluctuations. This type of power cycling is named as slow cycling because is applicable in the seconds

regime. Indeed, since the lifetime model provided by Infineon only considers a heating time change from 0.1 to 60 seconds [26],heating times higher than 60 seconds are discarded and not taken into account to estimate the lifetime consumption due to this type of stress load.

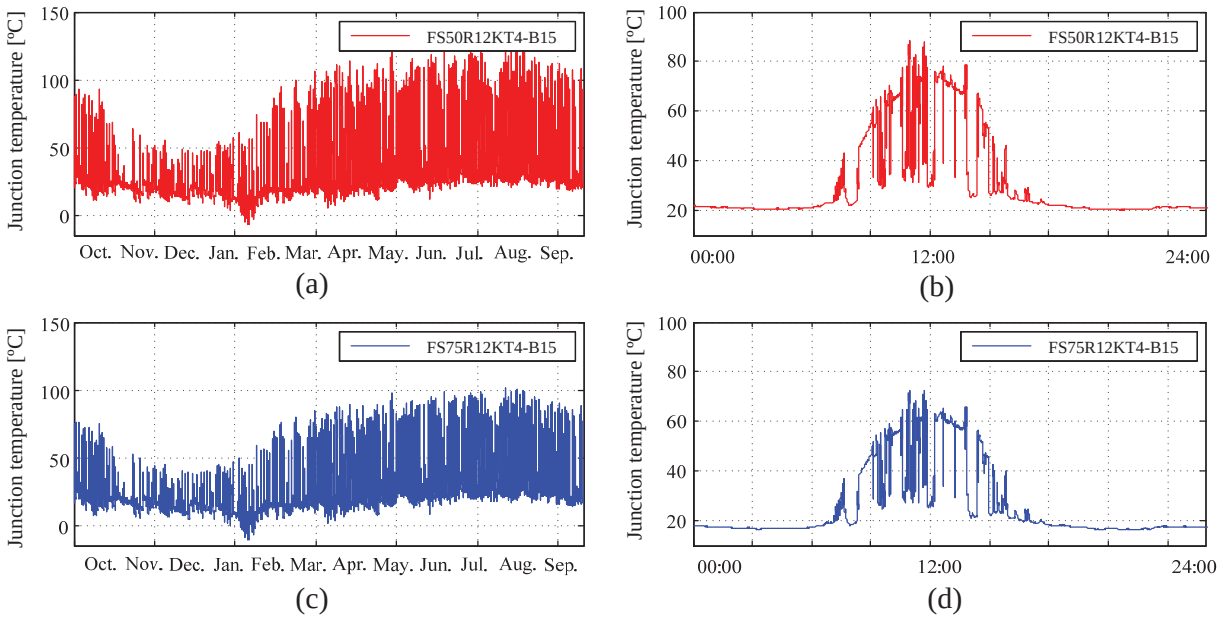

Figure 5.7: Estimated IGBT junction temperature (1 second per data) a) one year mission profile with IGBT FS50R12KT4-B15, b) one day mission profile with IGBT FS50R12KT4-B15, c) one year mission profile with IGBT FS75R12KT4-B15 and d) one day mission profile with FS75R12KT4-B15.

It is thus apparent that in order to determine the accumulated damage per year, the junction temperature must be obtained at least with a sampling rate of 1 second per data. Thus, the mission profile recorded with a sampling rate of 1 second per data is transformed into the corresponding junction temperatures, following the same procedure as before. Figure 5.7 shows the estimated junction temperature and it is straightforward observed that IGBT modules with a higher current rating have lower junction temperatures which means higher number of cycles to failure.

5.3.1 LIFETIME PREDICTION BASED ON RAINFLOW COUNTING ALGORITHM

The obtained one year thermal loading distribution for the two IGBT solutions under analysis has been used as an input to calculate the accumulated damage per year. The Rainflow counting algorithm is applied to extract the mean junction temperature ($T_{j,mean}$), the junction temperature fluctuation (ΔT_j), the heating time (t_{on}) and the number of cycles (n) of switching devices for one year operation.

Figure 5.8 illustrates the distribution of junction temperature cycling obtained with the Rainflow counting algorithm. It is appreciated that most of the temperature cycling has a very low amplitude (ΔT_j), which means that the contribution of this type of cycling to the accumulated damage per year is insignificant.

Once again the Palmgren-Miner linear cumulative damage model [4] is applied to obtain the expected

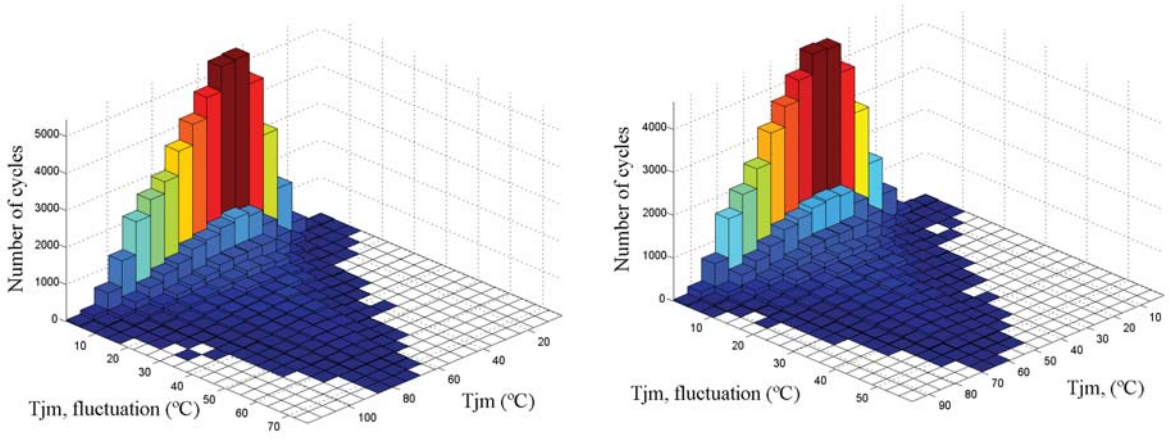

Figure 5.8: Rainflow counting of the junction temperature for the IGBT FS50R12KT4-B15 (left) and IGBT FS75R12KT4-B15 (right).

life of the two IGBT solutions based on the obtained results from the Rainflow counting algorithm. Note that the obtained results considered are the ones which present a heating time lower than 60 seconds, it is assumed that heating times larger than 60 seconds will contribute to solder joint failures instead of wire bonds failures. The damage corresponding to solar irradiance and ambient temperature fluctuations is presented in Table 5.2 for the two IGBT solutions. It is now obvious that this type of cycling has a relatively insignificant impact on the lifetime of the bond wire, nevertheless, remark that the Rainflow algorithm reduces the input data in a sequence of peaks and valleys neglecting some of the cycles in between. Consequently, another method to count the number of cycles is proposed in the following subsection.

IGBT-Module	Load	t_{on}	Accumulated damage per year	Lifetime consumption per year
FS50R12KT4-B15	T_{amb} & S_i	[1-60] s	0.0037	0.37 %
FS75R12KT4-B15	T_{amb} & S_i	[1-60] s	0.0011	0.11%

Table 5.2: Lifetime consumption due ambient temperature and solar irradiance fluctuations based on the Palmgren-Miner model [4] for one year mission profile (t_{on} < 60s).

Further on, in case that long heating times are also counted to estimate the consumed lifetime of the IGBTs, it has been appreciated that the accumulated damage will remarkable increase as shown in Table 5.3. However, as mentioned before, it is belief that heating times of days will not contribute to bond wires lift-off, but solder joints fatigue [9], [26].

5.3.2 LIFETIME PREDICTION BASED ON PROPOSED COUNTING ALGORITHM

Instead of applying Rainflow counting algorithm, the cycles are counted based on slope changes, so each time the slope changes its sign (positive slope to negative slope and vice versa), the junction temperature and the time is stored. Obviously, only the heating times are needed so the cooling times are discarded,

IGBT-Module	Load	t_{on}	Accumulated damage per year	Lifetime consumption per year
FS50R12KT4-B15	T_{amb} & S_i	sec - days	0.0413	4.13 %
FS75R12KT4-B15	T_{amb} & S_i	sec - days	0.015	1.5%

Table 5.3: Lifetime consumption due ambient temperature and solar irradiance fluctuations based on the Palmgren-Miner model [4] for one year mission profile .

the algorithm is enclosed in the annexed CD.

In this case, the proposed algorithm does not neglect any cycle and the long cycles are not taken into account, finally it was noticed that the accumulated damage per year when this algorithm is applied is exactly the same as the results obtained with the Rainflow algorithm when the heating time is lower than 60 seconds.

5.4 CONCLUSION

A yearly mission profile data has been correctly transformed into the corresponding IGBT junction temperature for two different IGBT solutions. The accumulated damage for one year mission profile has been calculated for two type of stresses - power cycling due to the line frequency and power cycling due to ambient temperature and solar irradiance. Finally, by adding the damage corresponding with the two type of stresses, the expected lifetime consumption can be calculated for the two IGBT modules as given by:

$$Damage_{50A} = 0.0477 + 0.0037 = 0.0514 \tag{5.2}$$

$$Damage_{75A} = 0.0191 + 0.0011 = 0.0202 \tag{5.3}$$

$$Lifetime\,Consumption_{50A} = 5.14\% \tag{5.4}$$

$$Lifetime\,Consumption_{75A} = 2.02\% \tag{5.5}$$

CHAPTER 6

VARIATION ANALYSIS OF IGBT LIFETIME USING MONTE CARLO

In this chapter a statistical approach for analysis of power semiconductors lifetime performance subjected to parameter variations is described. The effect of these variations is analysed by means of Monte Carlo simulations. The reliability analysis is rendered based on real field mission profile data to inquire which is the impact in PV inverter reliability due to parameter variations for one particular switching device.

6.1 MOTIVATION

The lifetime prediction carried out in Chapter 5 gives a fixed value of the IGBT lifetime, but it should also consider the uncertainties in IGBT parameter variations (i.e. $V_{ce,on}$) and the statistical properties of the applied lifetime model, for this study case the Bayerer model parameters (i.e. *âĂć*, β_1 and β_2). Accordingly, this study intends to obtain a realistic lifetime, based on mission profile data, within a range with a specified confidence level rather than only a fixed value. Hence the lifetime probability distribution function and the robustness of the IGBTs could be estimated.

6.2 RELIABILITY ANALYSIS BASED ON LINE FREQUENCY POWER CYCLING

In this section, the Monte Carlo algorithm is used for evaluating the variability of different parameters when the stress applied is only due to the line frequency power cycling. The study is based on the IGBT FS50R12KT4-B15 and the parameters studied are *A*, β_1, β_2 (parameters from the applied lifetime model) and $V_{ce,on}$ = f (T_j and ΔT_j) (IGBT parameter variations). All of these variables are part the applied lifetime model which equation is given by:

$$N = A \cdot (\Delta T_j)^{-\beta_1} \cdot \exp\left(\frac{\beta 2}{T_{j,min} + 273}\right) \cdot t_{on}^{\beta_3} \cdot I^{\beta_4} \cdot V^{\beta_5} \cdot D^{\beta_6} \tag{6.1}$$

6.2.1 PROBABILITY DISTRIBUTION FUNCTION

For the system under study, all the parameters are modelled by means of normal probability distribution functions. The uncertain variation of some parameters such as A, β_1 and β_2 leads to the following assumptions: A is assumed to experience 10% variation, β_1 and β_2 a 2% variation within a confidence interval of 99%.

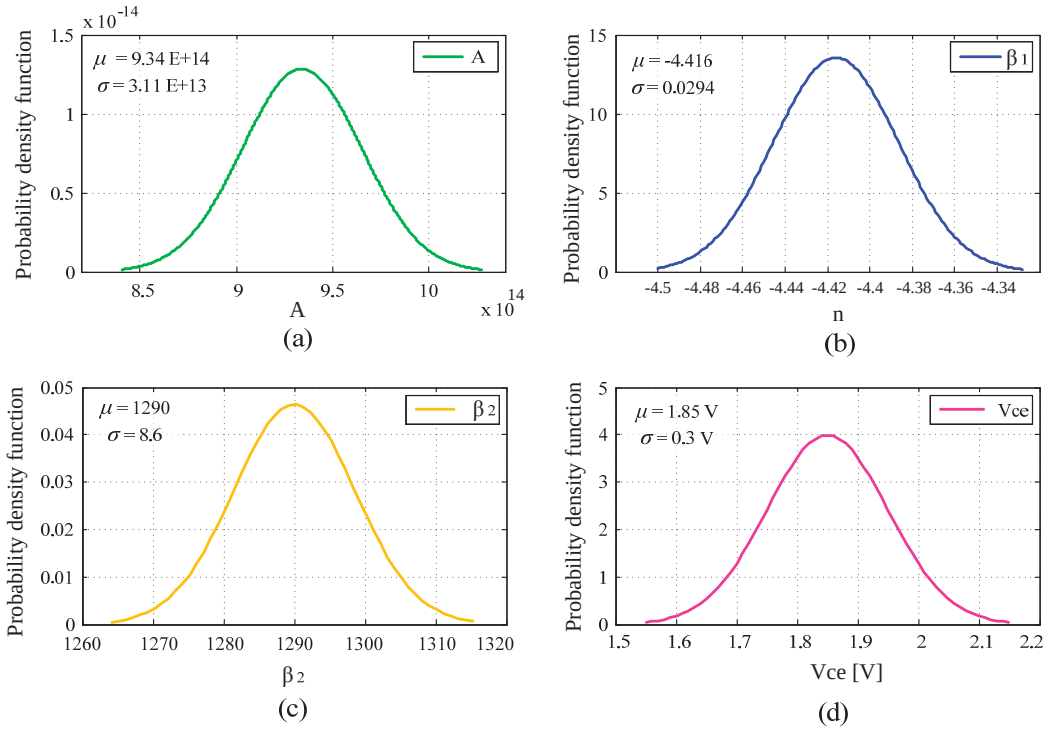

Figure 6.1: Probability density function based on IGBT FS50R12KT4-B15 a)parameter A, b) parameter β_1, c) parameter β_2 and d) collector-emitter saturation voltage at P = 15 kW .

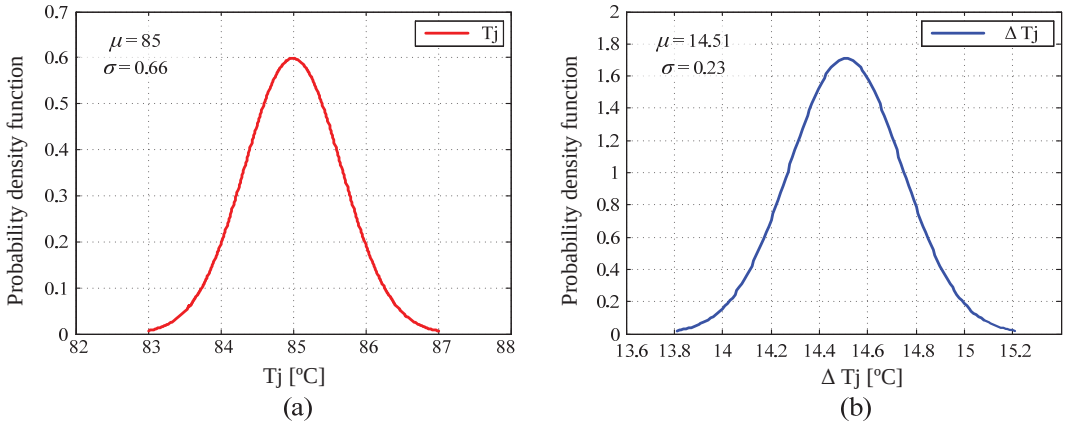

Figure 6.2: Probability density function based on IGBT FS50R12KT4-B15 at P = 15 kW a) mean junction temperature and b) junction temperature fluctuation .

On the other hand, the parameter $V_{ce,on}$ is defined in the datasheet with a typical, maximum and

minimum value as a function of the junction temperature and the collector current. When $V_{ce,on}$ changes, the conduction losses will also vary and thus the junction temperature and its fluctuation may also vary due to the power losses variation. Consequently, the junction temperature, T_j, and its fluctuation, ΔT_j, can be modelled by means of probability distribution fuctions as a function of $V_{ce,on}$. Figure 6.1 shows the probability distribution function of all the parameters considered under this study with both mean value (μ) and variance (σ) and Figure 6.2 shows the junction temperature and junction temperature fluctuation probability density function subject to $V_{ce,on}$ variation at nominal power (P=15 kW).

6.2.2 SENSITIVITY STUDY OF INDIVIDUAL PARAMETER VARIATION

Once the probability distribution function for each parameter is defined, it is possible to deduce the number of cycles to failure probability distribution function in case of individual parameter variation, while maintaining the rest of the parameters to the mean of their distributions. These results are plotted in Figure 6.3, as can be seen the parameters A, β_1 and β_2 have a relatively low standard deviations, which means that the number of cycles range is relatively small, in comparison with the IGBT parameter variation $V_{ce,on}$ that has a larger standard deviation yielding a number of cycles wider range.

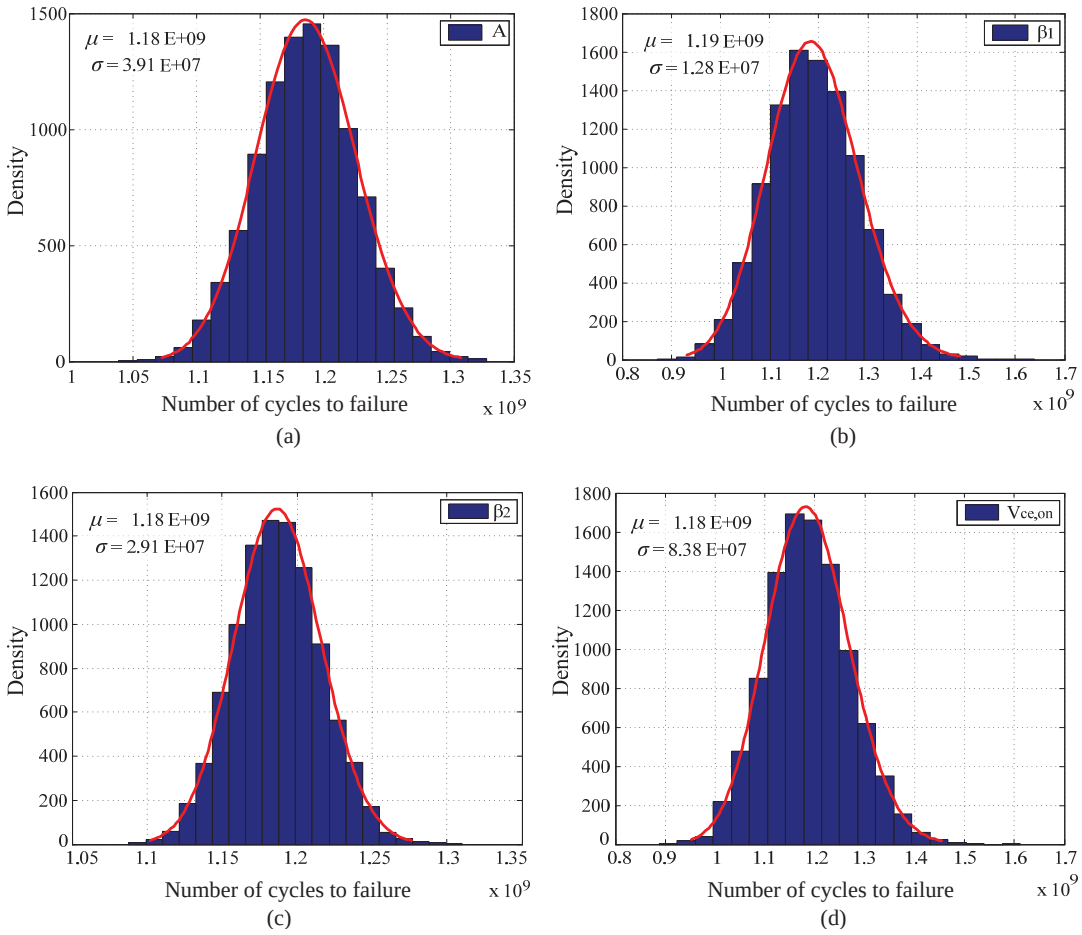

Figure 6.3: Effect of individual parameter variations on the number of cycles to failure of the IGBT FS50R12KT4-B15 at rated power, P=15 kW a) A b) β_1 c) β_2 and d) collector-emitter saturation voltage.

6.2.3 VARIATION OF ALL PARAMETERS BASED ON MONTE CARLO METHOD

ONE OPERATING POINT

The Monte Carlo method is based on a computational algorithm that generates random data within any kind of probability distribution and could be repeated as many times as desired. For this study case, the number of repeated random values is 10000. Figure 6.4 shows the number of cycles to failure probability density function and the cumulative distribution function when all the parameters under analysis can suffer variations within the pre-defined ranges. It is observed that the mean value of the IGBT lifetime is μ = 1.18 E+9 cycles and its variance σ = 1.35 E+8 cycles for one operating point, P=15 kW, in other words, the number of cycles to failure of the IGBT varies 35% of its mean value when operated at the nominal power.

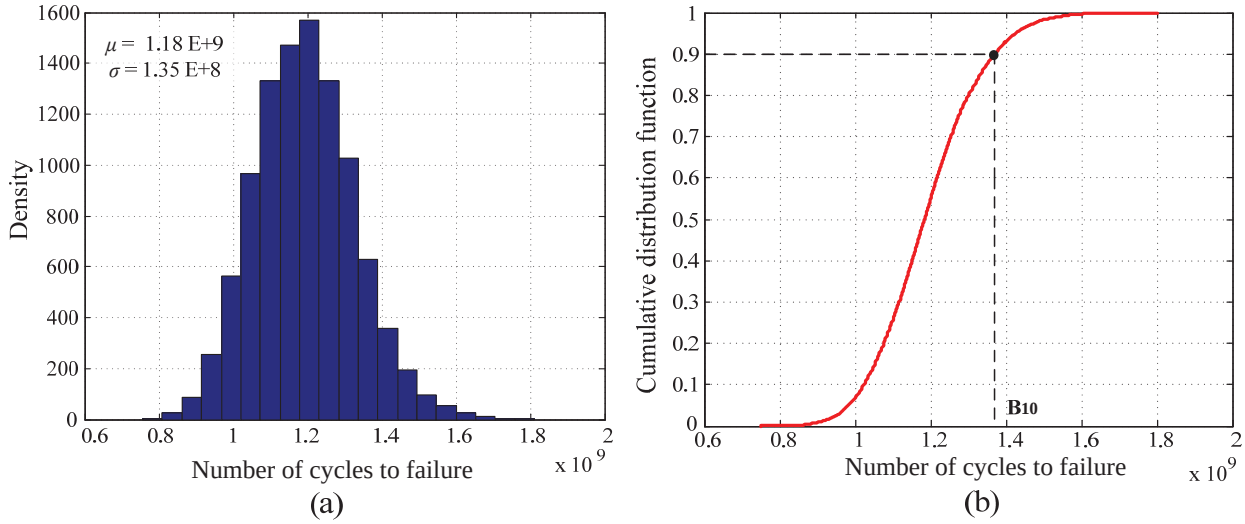

Figure 6.4: Effect of all parameters subjected to variations on the lifetime of the IGBT FS50R12KT4-B15 at rated power (P= 15kW) , a) probability distribution function and b) cumulative distribution function.

DIFFERENT OPERATING POINTS

The final goal is to obtain the lifetime of the IGBT when operated in the field at different power levels. Hence, the following procedure is followed and the overall idea is represented in Figure 6.5

1. Carry out Monte Carlo simulations at different power levels, so the mean and the standard deviation of the number of cycles to failure can be defined for different operating points. The parameters under variation are defined as normal probability distribution functions with a confidence interval of 99%.

2. As previously rendered, an equation describing the relationship between the number of cycles to failure and the power level can be obtained by means of curve fitting for the mean, the maximum and minimum lifetime curve. Equation 6.2 represent the fitted curves.

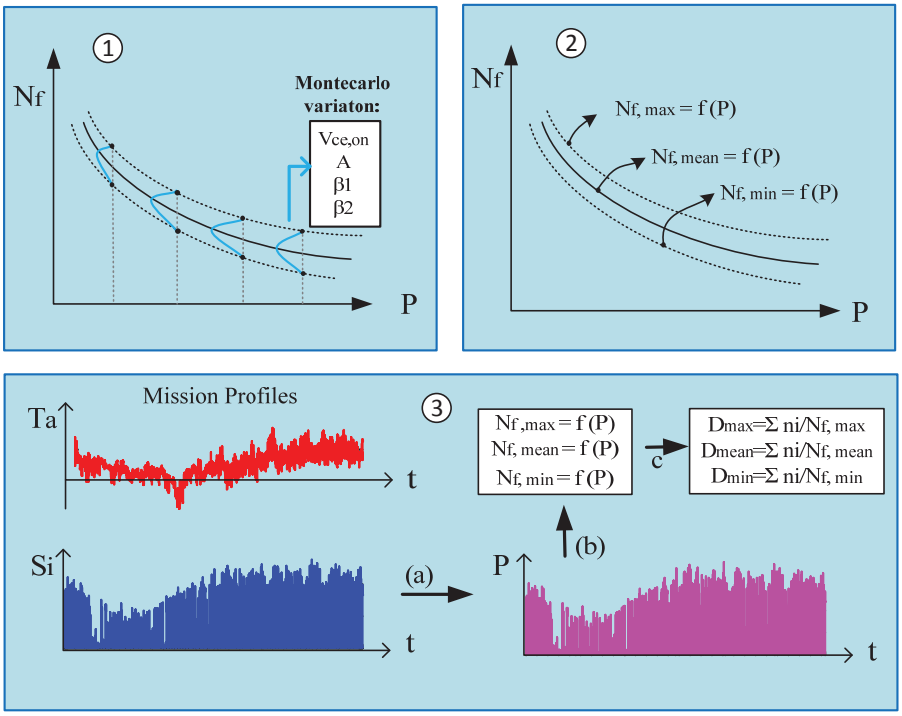

Figure 6.5: Block diagram to estimate the lifetime variation based on Montecarlo simulations for a yearly mission profile: S_i - solar irradiance, T_a - ambient temperature, P - total power of the inverter, N_f - number of cycles to failure, D - damage.

$$\begin{aligned} N_{f,min} &= 9 \cdot 10^{26} \cdot P^{-4.282} \\ N_{f,mean} &= 6 \cdot 10^{26} \cdot P^{-4.203} \\ N_{f,max} &= 3 \cdot 10^{26} \cdot P^{-4.115} \end{aligned} \tag{6.2}$$

3. The damage over one year with the mission profile data can be obtained following the same procedure as presented in Section 4.3, results are summarized in Table 6.1.

Unfortunately, this method is not feasible to determine which is the probability associated with the lifetime obtained. But, it is possible to determine that the lifetime consumption range is within the interval [3.78 % - 6.13 %] with unknown confidence level.

CONVERSION OF DYNAMICAL MISSION PROFILE STRESSES INTO EQUIVALENT STATIC VALUES.

One of the constraints when obtaining the reliability of the power semiconductor devices with the proposed procedure presented in the previous subsection, is the lack of information regarding the probability within the obtained lifetime range.

Range	Load	t_{on}	Accumulated damage per year	Lifetime consumption per year
Minimum value	Line frequency	0.01 s	0.0613	6.13 % (16.31 years)
Mean value	Line frequency	0.01 s	0.0435	4.35 % (23 years)
Maximum value	Line frequency	0.01 s	0.0378	3.78 % (26.45 years)

Table 6.1: Lifetime consumption due to the line frequency power cycling for one year mission profile (IGBT FS50R12KT4-B15).

Therefore, an effort to derive the IGBTs lifetime probability within its variation range is made to completely understand the effect of parameter variation of the IGBT lifetime. The fundamental principle is to determine an effective amount of IGBT degradation by means of converting the dynamical mission profile stresses into equivalent static values which produce the same amount of degradation as the dynamical stresses.

The dynamical mission profile stresses are converted as follows: average minimum junction temperature, $T_{j,min}$ = 20.26°C, accumulated damage per year, D = 0.0477 (IGBT4, 50A) and number of cycles per year, n = $7.8 \cdot 10^8$ (50 Hz, 12 hours/day and 365 days operation).

The number of cycles to failure can be obtained as given by:

$$Damage = \sum_i \frac{n_i}{N_{f,i}} \Rightarrow N_{f,1year} = \frac{7.8 \cdot 10^8}{0.0477} = 1.63 \cdot 10^{10} \tag{6.3}$$

By applying the lifetime model given from Semikron, the equivalent junction temperature fluctuation due to line frequency power cycling is given by:

$$1.63 \cdot 10^{10} = 9.34 \cdot 10^{14} \cdot \Delta T_{j,equivalent}^{-4.416} \cdot \exp\left(\frac{1290}{20.26 + 273}\right) \cdot 9.6 \cdot 10^{-4} \cdot \left(\frac{0.01}{1.5}\right)^{-0.3} \tag{6.4}$$

$$\Delta T_{j,equivalent} = 9.43°C \tag{6.5}$$

Once again the Monte Carlo method is applied, all the parameters are modelled by means of normal probability distribution functions within a confidence interval of 99%, where A is assumed to experience a 10% variation, β_1 and β_2 2% variation and $\Delta T_{j,equivalent}$ 5% variation. The junction temperature and the heating time are considered as fixed values.

Figure 6.6 shows the number of cycles to failure probability density function and cumulative distribution function when all the parameters under analysis suffer variations. Figure 6.7 shows the accumulated damage probability density function and cumulative distribution function. Notice that the mean value of the IGBT accumulated damage is μ = 0.0448, which is slightly different to the mean accumulated damage obtained in subsection 6.2.3. On the other hand its variance σ = 0.0048, results in a variation range from 0.037 to 0.053 (90% confidience level), which is similar to the lifetime variation range obtained

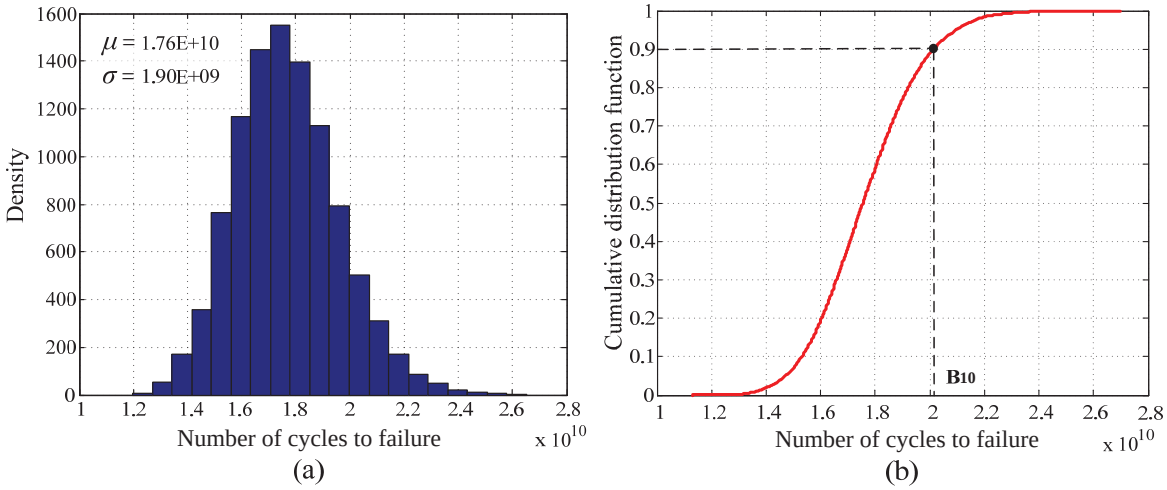

Figure 6.6: Number of cycles to failure based on one year mission profile data (FS50R12KT4-B15) a) probability density function and b) cumulative distribution function.

in subsection 6.2.3. Nonetheless when defining equivalent static values it is possible to determine the number of cycles during which 10% of the modules fail, named as B_{10}.

Finally it is straightforwardly concluded that 10% of the total number of modules fail when they reach 0.0512 accumulated damage due to line frequency power cycling, which corresponds with $2 \cdot 10^{10}$ cycles

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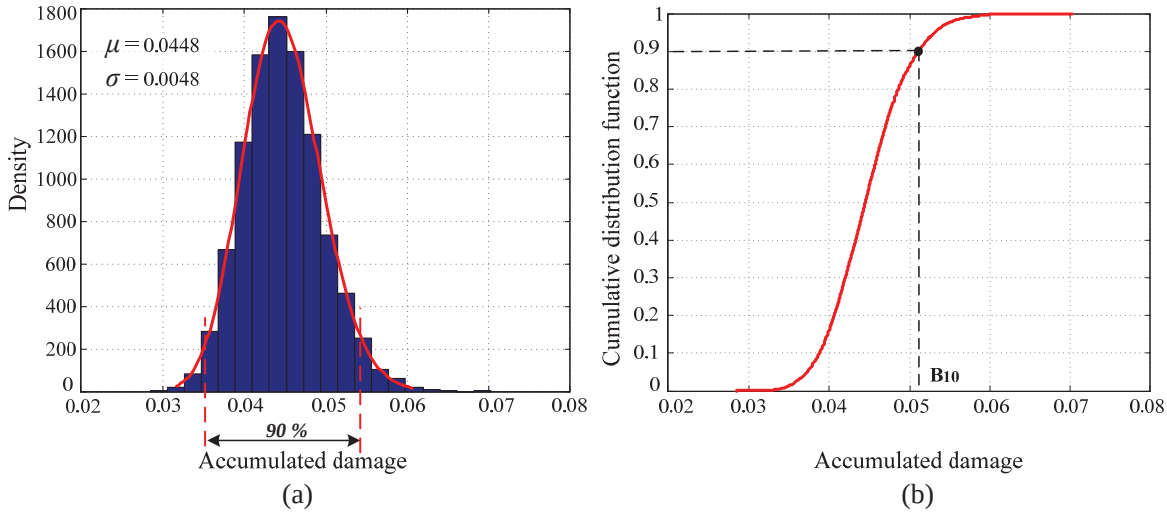

Figure 6.7: Accumulated damage based on one year mission profile data (FS50R12KT4-B15) when power cycling due to line frequency is considered a) probability density function and b) cumulative distribution function.

6.3 RELIABILITY ANALYSIS BASED ON SOLAR IRRANDANCE AND AMBIENT TEMPERATURE FLUCTUATION

For this type of cycling the same procedure can be followed. The effect of parameter variation on the IGBT lifetime is rendered by converting the dynamical mission profile stress into equivalent static values that produce the same amount of degradation as the dynamical stress.

The dynamical mission profile stresses are converted as follows: average minimum junction temperature, $T_{j,min}$ = 20.26°C, accumulated damage per year, D = 0.0037 (IGBT4, 50A), number of cycles per year, n = 71750 cycles (based on Rainflow-counting method) and mean heating time, t_{on} = 23.43 seconds (based on Rainflow-counting method).

The number of cycles to failure can be obtained as given by:

$$Damage = \sum_i \frac{n_i}{N_{f,i}} \Rightarrow N_{f,1year} = \frac{71750}{0.0037} = 1.94 \cdot 10^7 \tag{6.6}$$

By applying the lifetime model given from Semikron, the equivalent junction temperature fluctuation due to ambient temperature and solar irradiance power cycling is given by:

$$1.94 \cdot 10^7 = 9.34 \cdot 10^{14} \cdot \Delta T_{j,equivalent}^{-4.416} \cdot \exp\left(\frac{1290}{20.26 + 273}\right) \cdot 9.6 \cdot 10^{-4} \cdot \left(\frac{23.43}{1.5}\right)^{-0.3} \tag{6.7}$$

$$\Delta T_{j,equivalent} = 25.6°C \tag{6.8}$$

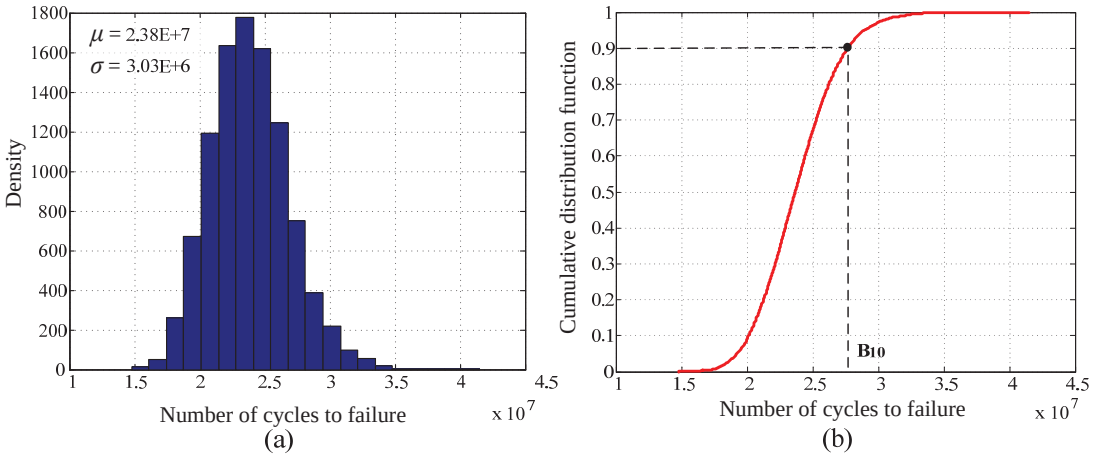

Figure 6.8: Number of cycles to failure based on one year mission profile data (FS50R12KT4-B15) a) probability density function and b) cumulative distribution function.

Once again the Monte Carlo method is applied, all the parameters are modelled by means of normal probability distribution functions within a confidence interval of 99%, where*A* is assumed to experience

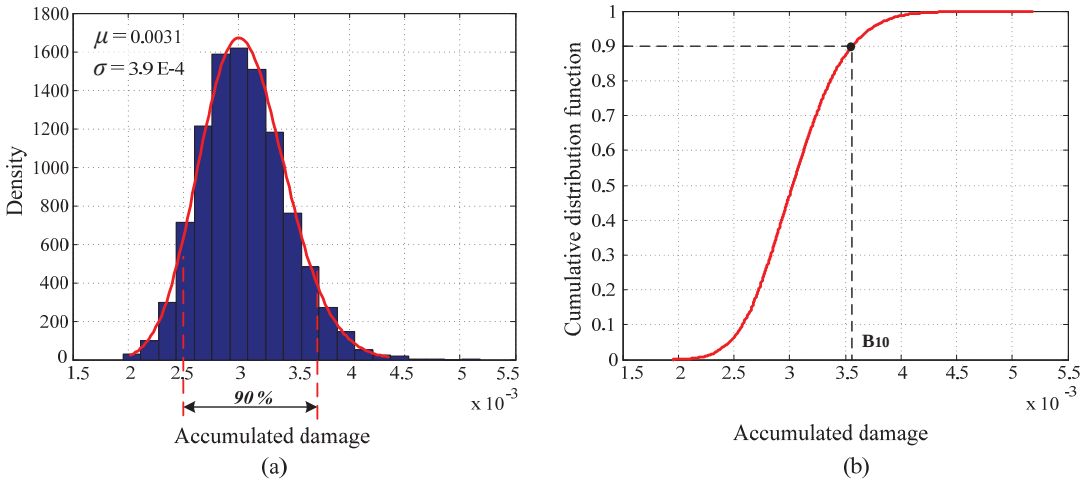

Figure 6.9: Accumulated damage based on one year mission profile data (FS50R12KT4-B15) when power cycling due to ambient temperature and solar irradiance in considered a) probability density function and b) cumulative distribution function.

a 10% variation, β_1 and β_2 2% variation and $\Delta T_{j,equivalent}$ 5% variation. The junction temperature and the heating time are considered as fixed values.

As it can be observed in Figures 6.8 and 6.9 is possible to conclude that 10% of the total number of modules fail when they reach 0.0035 accumulated damage when power cycling due to solar irradiance and ambient temperature effect is taken into account, which corresponds to 2.8 $\cdot 10^7$ cycles.

6.4 CONCLUSION

An effort to provide a better understanding of the PV inverter reliability performance under parameter variations has been rendered. The effect of this variations on the PV inverter reliability is shown when two type of stresses are considered. The performance of the PV inverter and the impact of these variations due to manufacturing process are analyzed by means of Monte Carlo simulations at diverse levels (one operating point and one year mission profile), giving a realistic lifetime variation.

In order to obtain the probability distribution function that describes the variation range of IGBT lifetime, an equivalent thermal stress has been defined so that an equivalent number of cycles to failure for one year mission profile can be acquired.

Finally, by adding the damage corresponding with the two type of stresses, the expected total of years and the reliability of the power semiconductor module under analysis can be obtained, this is further discussed in Chapter 7.

CHAPTER 7

SMART DERATING OF SWITCHING DEVICES

The motivation of this chapter is to provide an overall overview of the expected lifetime of switching devices based on long-term realistic thermal stress. Further on, the total lifetime-cost profile allows to select the best IGBT solution as a function of the nominal current of the device and the cost constraint.

7.1 MOTIVATION

The final goal of this Master Thesis is to evaluate the trade-off between high-reliable and low-cost power semiconductor devices. It has been shown before that switching devices that are used to convert the same amount of power with larger current ratings yields to larger operating hours with the drawback of increased cost. Therefore an effort to find which is the optimum design point that satisfies both long operating hours with a cost-effective solution is crucial to select the best IGBT solution.

7.2 TOTAL LIFETIME BASED ON MISSION PROFILE

By considering the mission profile, a realistic loading of the inverter has been obtained in Chapter 5. Thus the lifetime consumption for the two type of stresses under analysis - power cycling due to line frequency and power cycling due to ambient temperature and solar irradiance- has been acquired.

The next step is to add the damage corresponding with the two type of stresses so that the total expected lifetime of each IGBT solution can be calculated. Table 7.1 illustrates the total lifetime for the six IGBT solutions presented under this study. One extra power module (F0122PA075SC01) that ensures long lifetime has been also included in this analysis.

IGBT-Module	Accumulated damage (Line frequency)	Accumulated damage (T_{amb} & S_i)	Total Lifetime (years)
FS35R12KT3	0.9549	0.0072	1.04
FS35R12KE3G	0.5407	0.0461	1.70
FS50R12KT3	0.2961	0.0037	3.33
FS50R12KT4 $_{B15}$	0.0477	0.0037	19.45
FS75R12KT3	0.0812	0.0017	12.06
FS75R12KT4$_{B15}$	0.0191	0.0011	49.50
F0122PA075SC01	0.0218	0.0007	44.44

Table 7.1: Expected total lifetime for different IGBT solutions based on one year mission profile.

7.3 VARIATION ANALYSIS OF IGBT TOTAL LIFETIME USING MONTE CARLO

In Chapter 6 a variation analysis of IGBT lifetime using Monte Carlo simulations has been carried out for the two type of stresses under analysis - power cycling due to line frequency and power cycling due to ambient temperature and solar irradiance. Based on this reliability analysis, it is possible to determine the total lifetime probability density function, so the expected total of years for a 90 % confidence interval can be shown.

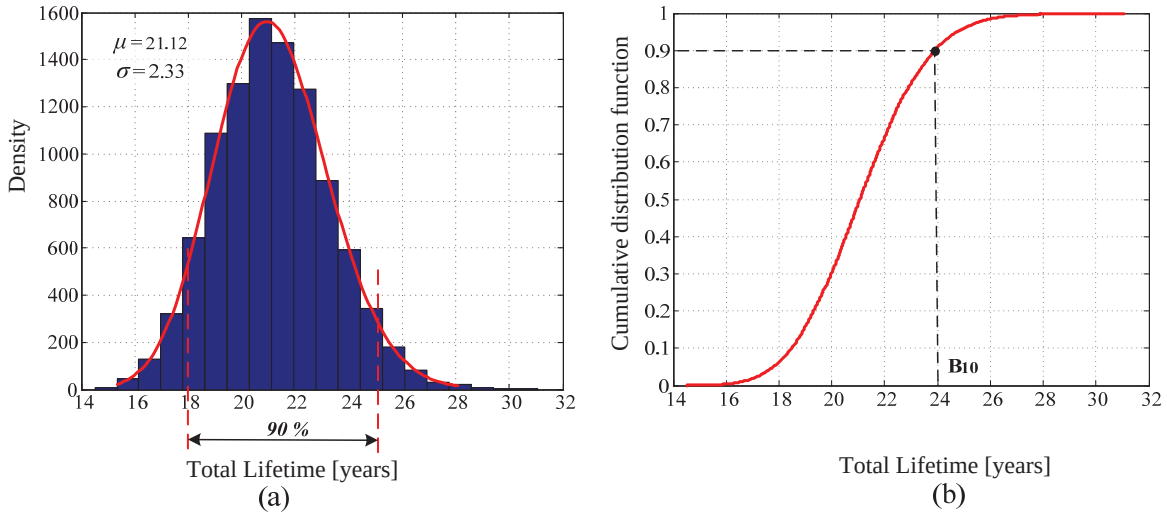

Figure 7.1: Total lifetime based on one year mission profile data (FS50R12KT4-B15) a) probability density function and b) cumulative distribution function.

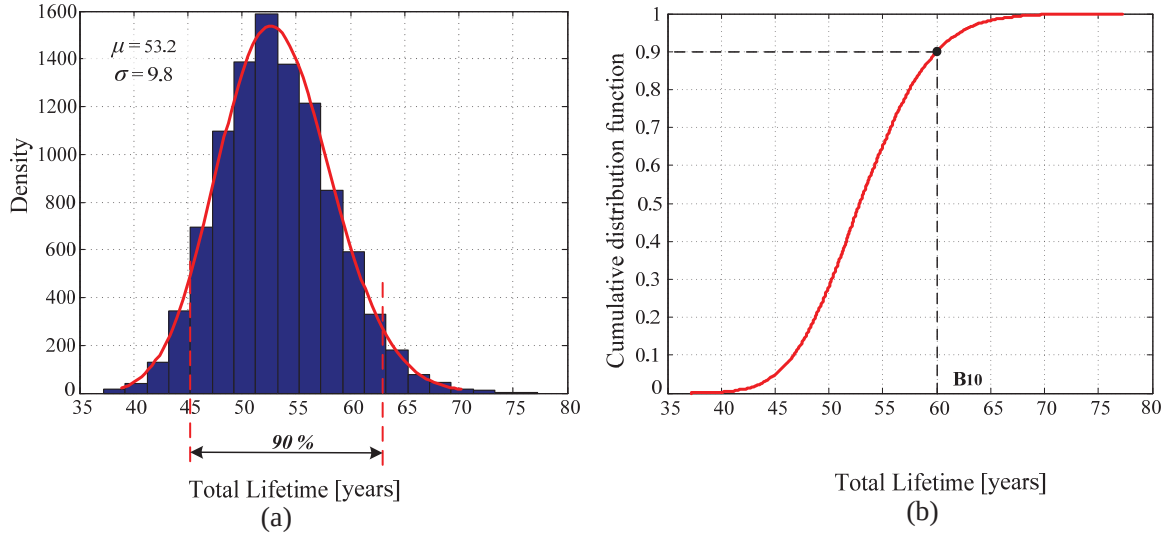

Figure 7.2: Total lifetime based on one year mission profile data (FS75R12KT4-B15) a) probability density function and b) cumulative distribution function.

Since the best power semiconductor solutions seems to be the IGBT4 packaging technology for 50

A and 75 A rated current, Figure 7.1 and 7.2 shows the variation of IGBT lifetime based on one year mission profile using Monte Carlo simulations.

It is thus straightforward concluded the power module rated at 50 A nominal current shows that 50 % of the total number of power modules fail when they reach 21.12 years operation. Additionally, Figure 7.1 (b) illustrates the cumulative distribution function, thus it is possible to tell that 10% of the total number of power modules fail at 24 years operation (B_{10}).

On the other hand, as it can be inferred from Figure 7.2, when IGBT4 at 75 A is selected, 50% of the power modules fail when they reach 53.2 years and B_{10} is 60 years operation.

Finally, Table 7.2 sums up the total lifetime for a reliability of 90% when different IGBT candidates are studied.

IGBT-Module	B_{10} (years)
FS35R12KT3	1.43
FS35R12KE3G	2.2
FS50R12KT3	4.34
FS50R12KT4 $_{B15}$	24
FS75R12KT3	15
FS75R12KT4$_{B15}$	60
F0122PA075SC01	53

Table 7.2: Number of years during wich 10% of the modules fail for different IGBT solutions.

7.4 LIFETIME-COST ANALYSIS

The thermal stress of power semiconductor devices is influenced by many design factors, for this study case, the heatsink has been considered constant for all the power semiconductor modules under analysis due to the constrained time frame, the junction temperature design limit has been set to 120°C and the inverter under analysis is 2L-VSI.

The total lifetime for each IGBT solution has been obtained for a reliability of 90%, based on the available mission profile and the variation analysis of IGBT lifetime using Monte Carlo simulations. Therefore a realistic benchmarking of different switching device solutions can be analysed. Nevertheless, the trade-off among lifetime performance and cost is hard to be quantified. The uncertain trends of price and packaging technology are constantly changing so it is hard to conclude with a general evaluation method. Hence the cost of the power semiconductor module is presented as a normalized cost that can be extrapolated.

Figure 7.3 represents the relationship between cost and expected total lifetime during which 10% of the modules fail, named as $B_{10\%}$. The cost of the IGBT modules has been normalized (1 is equal to 115 Euros). It should be noted that the cost information shown is for illustration purpose only, which depends on the source of distributors, purchase volumes and market changes.

Now it is observed that power modules with higher nominal current ensure longer operating years at the expense of increased cost, however it is also noticed that the latest packaging technology (IGBT4) rated at lower nominal current can reach similar, even higher, lifetimes than the former packaging technology rated at higher nominal currents. On the other hand, even though power modules rated at 35 A can handle the current and voltage of the 2L-VSI, they are not feasible in order to ensure a long lifetime. One possible solution would be to improve the cooling system, but the variation of the heatsink parameter has not been treated and further investigation must be done.

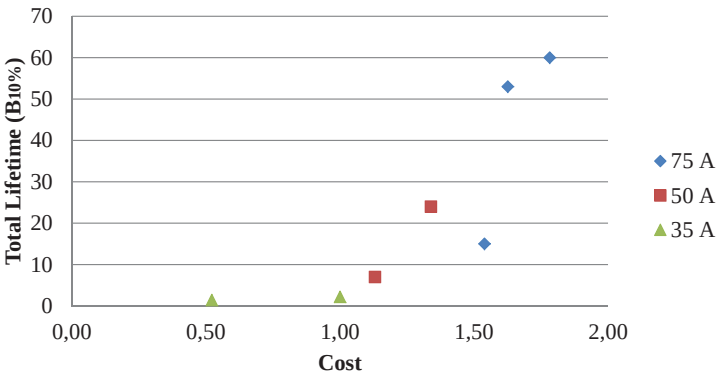

Figure 7.3: Total lifetime-cost profile for different IGBT solutions for a reliability of 90%.

The author would like to highlight the importance of the design procedure to obtain the Figure 7.3 in this Master thesis. The procedure can be followed by PV inverter designers to estimate the lifetime range of different IGBT candidates under specific mission profiles with a specified confidence level of their products. According to the associated cost information they have, the most cost-effective IGBTs can be chosen to fulfil the reliability requirement.

7.5 CONCLUSION

An insight of the expected lifetime of switching devices and the lifetime variations due to parameter variations among different switching devices have been given. The smart derating of switching devices is treated by taking into account the trade-off between reliability performance and cost. Thus, for the present-day, while the IGBT solutions rated at 35 A have been shown not feasible for the PV inverter under analysis, the IGBT4 technology can achieve 20 years operation when using 50 A rated devices and 60 years when using 75 A rated devices.

Additionally, the proposed guideline allows to estimate the reliability of different IGBT solutions for PV inverters with a certain confidence level. Therefore, by following the presented procedure, the PV inverter designers can choose the most cost-effective IGBTs based on the cost information and the reliability specification they have.

Part IV

Experimental Results

CHAPTER 8

LABORATORY IMPLEMENTATION

This chapter presents the laboratory implementation of the three-phase two-level voltage source inverter. It is worth to mention that the simulation of the inverter presented in previous chapters is not identical to the system conditions and controller parameters that have been considered in the laboratory setup. The main reasons have been highlighted in this chapter. Finally, the obtained laboratory results have been compared with a simulation that is identical to the system conditions in the laboratory.

8.1 SETUP DESCRIPTION

Figure 8.1 illustrates the schematic of the setup, which has been simplified to show only the fundamental components. It consists of a flexible system that can be configured into two-level single-phase and three-phase PV inverters, it is connected to the grid through a LCL filter and a three-phase transformer. The system controllability is achieved by implementing the designed control algorithm using dSPACE software in the controller board DS1103. The drivers must be powered with 0/15V, therefore a voltage level amplifier is needed between the output of the DS1103 controller board (0/5V) and each inverter leg driver. Moreover, a LEM box measures the grid currents and grid voltages which are also monitored through an oscilloscope. The heatsink temperature is measured with the LM225Z temperature sensor integrated in the system and with a DMM multimeter BK PRECISION 390 A .

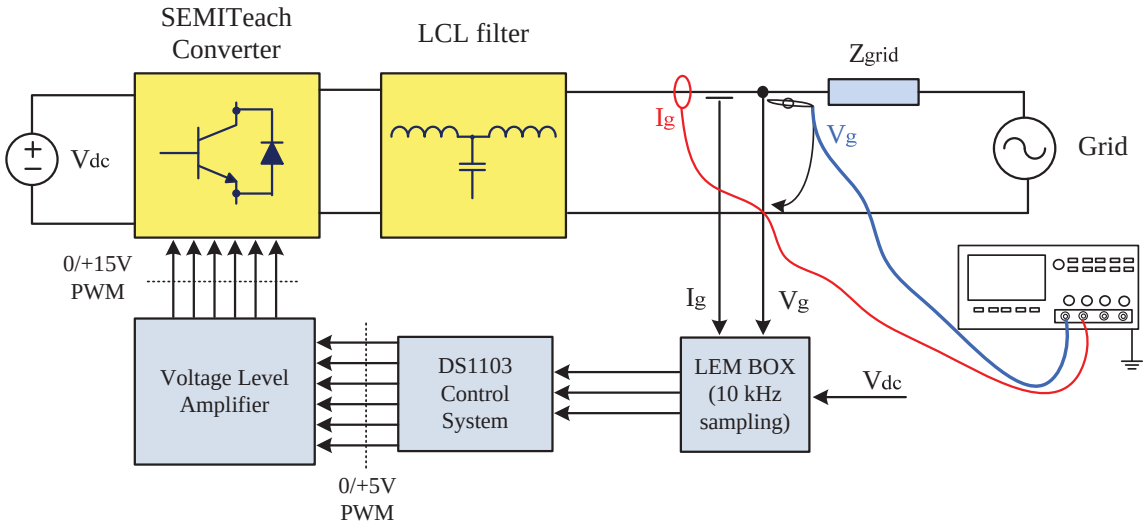

Figure 8.1: A simplified schematic of the 2L VSI inverter test setup.

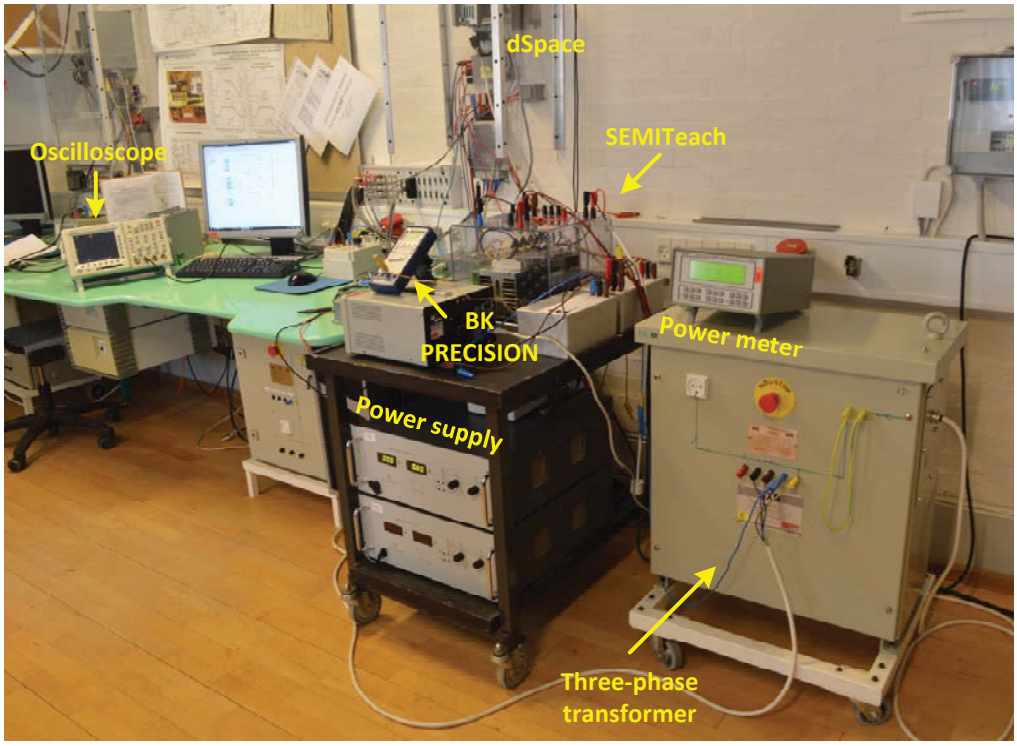

Figure 8.2: Experimental setup of the proposed system.

The experimental setup used in the laboratory of the Institute of Energy Technology at Aalborg University, Denmark can be observed in Figure 8.2 and a zoomed view of the inverter flexible system in Figure 8.3. The grid voltage is 230 V_{rms} and 50 Hz. The nominal power of the PV inverter has been set to 4.5 kW. A programmable power supply charges up the DC-link up to 650 V (V_{dc} = 650V). The switching frequency of the PV inverter has been set to three different frequencies: 6 kHz, 7 kHz and 8 kHz. The current controller is a Proportional Resonant (PR) with Harmonic Compensators (HC) for low-order harmonics (5th, 7th, 11th and 13th harmonics are compensated) that can be implemented in parallel with the PR controller [28].

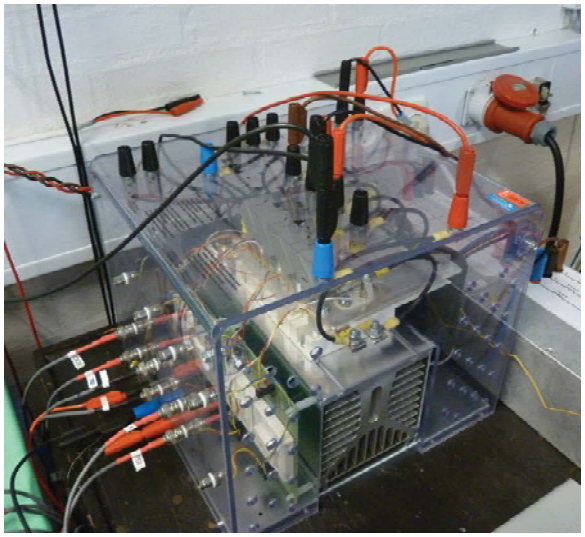

Figure 8.3: A zoomed view of the SEMITeach converter.

8.1.1 CONTROL IMPLEMENTATION: DSPACE

The proposed control of the three-phase two level voltage source inverter has been built in Matlab/Simulink and implemented in the laboratory by using a dSPACE system. The interaction between the physical system and the control unit is done by using I/O boards. The measured signals from the LEM box (grid

current, grid voltage and DC-link voltage) are sent to the I/O boards that are responsible for acquiring the measured signals and sending the IGBT control signals to the gate drivers of the inverter.

The system behaviour can be controlled and monitored in real time by using the Control Desk Interface presented in Figure 8.4. The user can easily interact with the control parameters of the system by using the control interface shown in Figure 8.4, so the settling time, the damping, the PR control gains (k_p and T_i), the HC control gains (k_{i5}, k_{i7}, k_{i11} and k_{i13}) and the active and reactive power reference can be established. On the other hand, the user can observe the online monitoring of the control signals such as grid current, grid voltage, DC-link voltage, grid frequency, AC power, DC power, phase of the SOGI-PLL and Total Harmonic Distortion (THD).

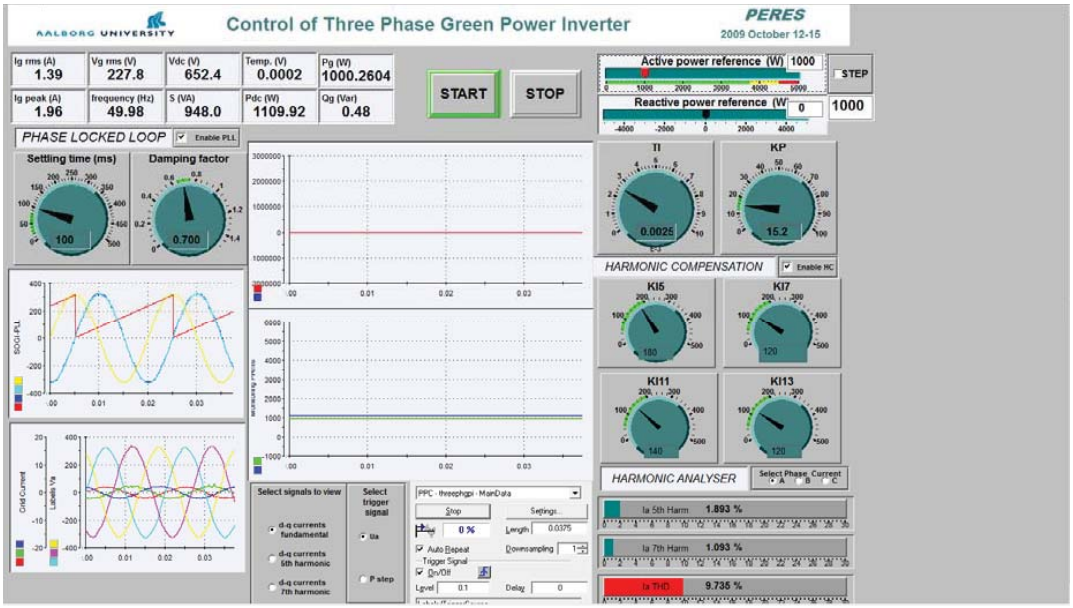

Figure 8.4: dSPACE Control Desk interface.

8.1.2 SEMITEACH INVERTER

The flexible system has been configured as a three-phase inverter with one IGBT module for each phase. Each IGBT module is made of 2 IGBTs connected in series and each IGBT has an anti-parallel diode. During the ongoing of the experiments in the laboratory two limitations were encountered.

1. **Current limitation.** The nominal power of the flexible system is 15 kW (the maximum allowed current is 30 A), however the nominal power of the PV inverter has been set at 4.5 kW because the the applicable sensing current of the LEM box is only up to 10 A, bigger current rating LEM box was not available in the laboratory at Aalborg University.

2. **Switching frequency limitation.** Prior to the experiments carried out during this Master thesis, the control dead time selected in order to avoid bridge shoot through was 3.25 μs for a switching frequency of 6 kHz. Nevertheless, when increasing the switching frequency the dead time becomes unnecessary large when operated at switching frequencies around 24 kHz, so the current will

become distorted and the system may become unstable. A redesign of the dead time should be done to avoid bridge shoot through and ensure a dead time as small as possible to guarantee the proper operation of the inverter. Due to the limited time frame was not feasible to design a new control board satisfying both requirements.

8.1.3 LCL-FILTER

The parameters of the three-phase LCL filter implemented in order to fulfil the total harmonic distortion requirements are summarized in Table 8.1. The grid inductance is part of the inductance of the three-phase transformer.

Converter-side inductance, L_c	3.6 mH
Grid-side inductance, L_g	2 mH
Filter capacitor, C_f	4.7 μF
Converter-side internal resistance, R_c	40 mΩ
Grid-side internal resistance, R_g	20 mΩ

Table 8.1: LCL filter parameters

8.2 EXPERIMENTAL RESULTS

The experimental setup has been tested under three different switching frequencies (6 kHz, 7 kHz and 8 kHz) at four different power levels (1 kW, 2 kW, 3 kW and 4.5 kW) to show the impact on the temperature distribution which is proportional to the power losses generated.

During the test, the heatsink temperature has been measured with two instruments - LM225Z temperature sensor integrated in the system and DMM multimeter BK PRECISION 390A. The multimeter provides more accurate measurements, therefore the experimental verification will rely on the heatsink temperature measured with the BK PRECISION 390A. The measured temperature is the steady-state temperature after 60 minutes of operation at each power level.

One-phase grid current and one-phase grid voltage has been monitored with a Tektronix oscilloscope and results can be seen in Figure 8.5 when the switching frequency is 6 kHz at 4.5 kW (left) and when the switching frequency is 8 kHz at 4.5 kW (right). The pink waveform is the grid voltage and the blue waveform is the grid current, it can be appreciated that the grid current at 8 kHz presents higher total harmonic distortion than the grid current at 6 kHz due to control limitations (dead-time contribution).

The estimation of the power losses can be done as the Application Note from Semikron suggests [29], based on the formula P_{loss} = ΔT / $R_{th(h-a)}$, where ΔT is the temperature difference between the heatsink and the ambient and $R_{th(h-a)}$ is the thermal resistance of the teaching system heatsink, P3/250 (extruded type P3 and 250 mm long). It is worth to mention that in this Master thesis natural cooling of the heatsink has been considered, therefore during the test the fan of the heatsink was not turned on. In order to obtain the thermal resistance of the heatsink for natural cooling, the datasheet of the P3/250

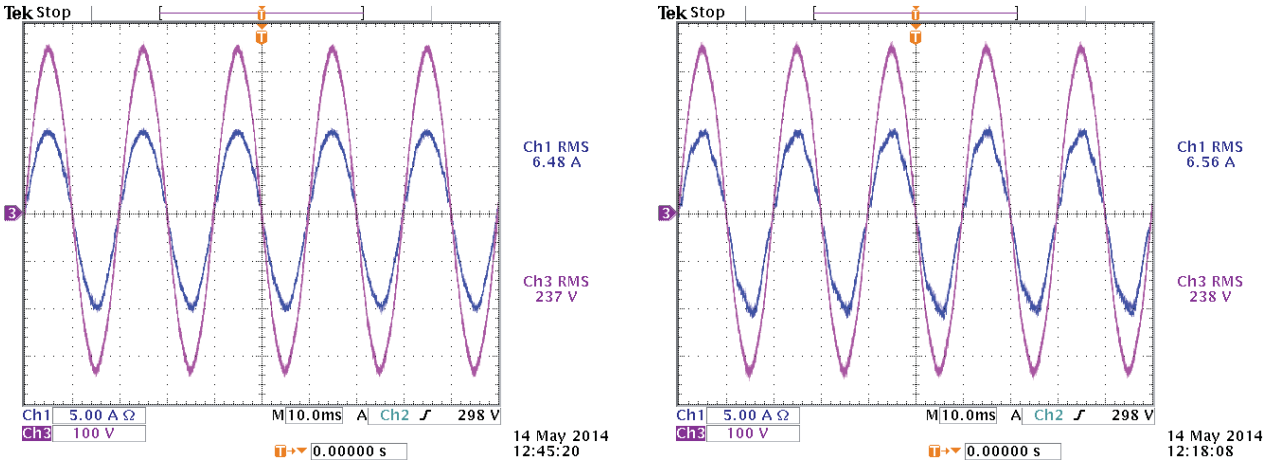

Figure 8.5: Grid voltage and current at 4.5 kW, f_{sw} = 6 kHz (left) and f_{sw} = 8 kHz (right).

provides $R_{th(h-a)}$ as a function of the total dissipated power, the length of the heatsink and the number of power modules attached to the heatsink. Finally, $R_{th(h-a)}$ results to be 0.32 K/W.

Additionally, the IGBT modules SK50GB12T4T provided from Semikron present a thermal resistance junction-to-substrate, $R_{th(j-s)}$ = 0.9 K/W, therefore the junction temperature of the IGBTs can be estimated.

To sum up, Table 8.2 provides the results obtained in the laboratory and the estimated power losses and junction temperature.

Fsw = 6 kHz					
Power [W]	Theatsink [ºC]	Ploss (measured) [W]	Tj [ºC]	Efficiency [%]	Ploss (simulated) [W]
1000	32	37.5	37.6	96.25	26.39
2000	41	68.7	51.3	96.56	45.34
3000	48	87.5	61.1	97.08	62.03
4500	56	112.5	72.8	97.5	81.5
Fsw = 7 kHz					
Power [W]	Theatsink [ºC]	Ploss (measured) [W]	Tj [ºC]	Efficiency [%]	Ploss (simulated) [W]
1000	32	37.5	37.6	96.25	28.11
2000	42	68.7	52.3	96.56	50.48
3000	52	100	67	96.66	70.77
4500	64	137.5	84.6	96.94	93.05
Fsw = 8 kHz					
Power [W]	Theatsink [ºC]	Ploss (measured) [W]	Tj [ºC]	Efficiency [%]	Ploss (simulated) [W]
1000	33	40.6	39.1	95.94	29.74
2000	44	75	55.2	96.1	57.34
3000	54	106.2	70	96.46	79.54
4500	67	146.9	89	96.73	103.4

Table 8.2: Experimental results obtained in the laboratory compared with simulated results.

8.3 SIMULATION VERIFICATION PROCESS

Before starting with the presentation of the simulation results, it needs to be highlighted that the datasheet of the IGBTs in the testing system (SK50GB12T4T) does not provide the energy loss distribution for currents lower than 25 A. Therefore, the energy losses must be estimated by following the procedure presented in [30]. Indeed, the switching losses calculation relies on the typical transfer characteristic curves that normally can be found in the datasheet, unfortunately, SK50GB12T4T datasheet provides a bare information of the transfer characteristic curves which makes it even harder to correctly estimate the energy losses.

By taking into consideration several manufacturer's datasheets, it has been noticed that the energy losses distribution is normally linear with the collector current when the collector current is relatively small in comparison with the nominal current of the device. Thus the energy loss has been obtained considering the possible linearity between energy loss and collector current, in accoradance with the procedure presented in [30].

The measured heatsink temperature has been set in the simulation model as a reference to obtain the simulated power losses of the inverter. The simulated total power losses are compared side-by-side with the experimental results in Table 8.2. It is appreciated a remarkable difference between the simulation and experimental results, this could be further improved if the datasheet provides more detailed information about the behaviour of the IGBT. Note that the simulation is included in the annexed CD.

8.4 CONCLUSIONS

The experimental tests conducted have shown the steady-state heatsink temperature distribution under three switching frequencies and at four different power levels. It can be appreciated the temperature increase when the user increases either the power level or the switching frequency of the inverter. Simulations have been carried out and compared side-by-side with the experimental results, however further investigation should be made in order to obtain detailed information about the transfer characteristic curves of the IGBT.

Part V

Conclusions

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

In this chapter both the Master thesis's conclusions and future work are presented.

9.1 CONCLUSIONS

The conclusions will take place separately on each project's objectives:

Objective 1. Study of the design guideline for smart-derating of switching devices in PV inverters.

This objective rendered to be the most intriguing and challenging of all. Indeed, the procedure followed to estimate the lifetime consumption of switching devices by taking into account a realistic mission profile is the most important contribution to this report. The work reflected in Chapters 4, 5, 6 and 7 verifies that this objective was satisfactory fulfilled as the lifetime of the IGBTs has been analysed for different IGBT candidates based on a long-term mission profile and furthermore the IGBT lifetime variation with a known confidence level has been obtained by means of Monte Carlo simulations.

Challenging parts have been well heightened , as for example the fixed heatsink parameter considered among several IGBT solutions. Finally, the proposed guideline allows PV inverter designers to select the most cost-effective IGBTs based on the cost information and the reliability specification they have.

Objective 2. Lifetime variations of the switching devices due to parameter variations among different switching devices.

Certainly this study has been presented in Chapter 6. Special efforts to analyse the uncertainties in IGBT parameter variations and statistical properties of the applied lifetime model has been conducted by means of Monte Carlo simulations. As a result, the lifetime probability distribution function with 90% confidence level and the life-cost relationship of several IGBT candidates can be established.

Objective 3. Analyze, design and simulate a three-phase two-level voltage source inverter (2L-VSI).

In Chapter 2 this objective has been addressed. A step-by-step modelling and control design procedure has been comprehensively described. Based on the design process followed a simulation has been built in PLECS/Simulink.

Objective 4. Model and implement an electro-thermal model of switching devices.

Undoubtedly, this objective has been presented in Chapter 3. The modelling of switching devices is

realized as a function of two aspects - power loss modelling and thermal modelling. The design has been sufficiently explained as well as the limitations encountered are adequately highlighted.

Objective 5. Validate the inverter simulations in Simulink/PLECS via direct comparison with experimental results.

Regarding this objective, the simulation model used in previous chapters has been modified according with the setup limitations encountered. Therefore, it was possible to experimentally verify the correlation between the simulation model and the experimental results. All efforts are described in Chapter 8, which correspond with the analysis, running and testing processes of the inverter system.

Finally, the inverter was tested under different operating points to show the temperature rise impact which is proportional to the power losses generated.

9.2 FUTURE WORK

The tasks carried out during this Master thesis have enlightened different paths for future investigation. Future activities that can be done are detailed as follows:

- Design variable of heatsink impedance could be considered in order to obtain the total cost of IGBT modules and cooling system.
- The robustness of solder joints could also be investigated by taking into account Thermal Cycling.
- Include the impact of device degradation (e.g. R_{th} variations) and environmental conditions (e.g. $T_{ambient}$ variations) in the the variation lifetime analysis carried out by means of Monte Carlo simulations.
- The experimental setup, SEMITeach system, could be further designed to be tested at rated conditions (P = 15 kW).
- The experimental work could be extended to the measurement of junction temperature of IGBTs if proper methods are available in the future.

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