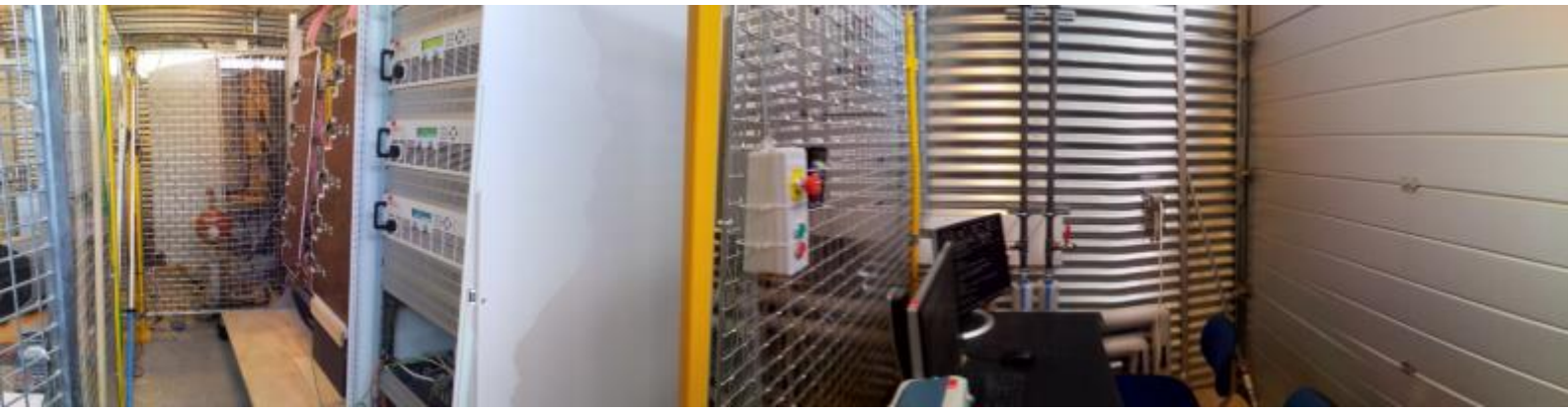
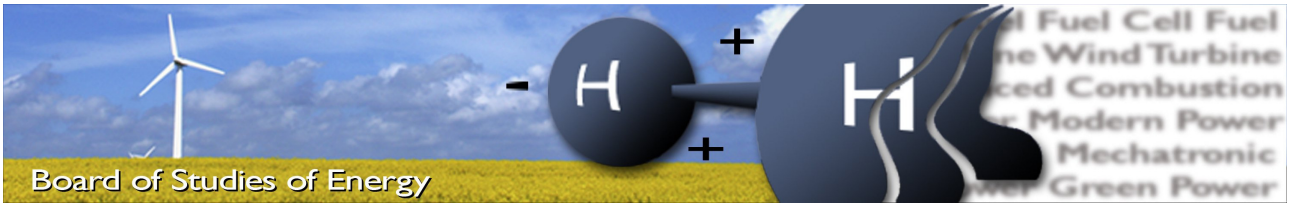
Power Cycling Test Setup for Accelerated Wear-out of High Power IGBT Modules



Master Thesis Report
Group PED4-1047, Spring 2014
Department of Energy Technology
Aalborg University, Denmark

AALBORG UNIVERSITY
STUDENT REPORT



Title:	Power Cycling Test Setup for Accelerated Wear-out of High Power IGBT Modules
Semester:	9. and 10. semester
Semester theme:	Master thesis
Period:	1 Sep 2013 - 27 May 2014
ECTS:	50
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Number of reports: 6
Number of pages: 102
Appendices: 5
CD: 6

SYNOPSIS:

IGBT modules are one of the main components subjected to failures in high power converters for wind turbine applications. This Master thesis deals with the analysis, design, implementation and validation of a power cycling test setup for accelerated wear-out and lifetime investigation of high power IGBT modules. The setup is able to test 10 PrimePACK™3 IGBT modules with DC current up to 2000A, providing a wide flexibility on its operating conditions. The gate signals control, data acquisition and monitoring systems have been developed in NI LabVIEW. In addition, two methods for junction temperature estimation based on datasheet parameters have been implemented. Currently, the PrimePACK™3 IGBT module from Infineon (FF1000R17IE4) is being tested and the obtained results are depicted in this report.

By signing this document, each member of the group confirms that all participated in the project work and thereby that all members are collectively liable for the content of the report. Furthermore, all group members confirm that the report does not include plagiarism.

Preface

This document presents the Master thesis report written by the 10^{th} semester students of the PED4-1047 group from the Department of Energy Technology at Aalborg University. The thesis is submitted in partial fulfillment of the requirements for a Master of Science's degree in 'Power Electronics and Drives' and 'Wind Power Systems', respective Master programs of each of the authors named in the title page. The report summarizes the 50-ECTS long Master thesis project "Power cycling test setup for accelerated wear-out of high power IGBT modules" which has been realized within the IEPE framework. The depicted test setup, as well as all the experiments presented in this work have been carried out at the Reliability Laboratory located in the Department of Energy Technology.

This report is written in LaTeX.

The softwares used for the fulfillment of this work are MATLAB®, PLECS Standalone®, LTspice, Altium Designer® and NI LabVIEW®. All licenses have been provided by the Department of Energy Technology.

A CD which contains all the relevant material used in this project is attached to the report.

Reading instructions

- The references made to some parts of the text are specified with numbers in square brackets. The details of these references can be found in the Bibliography, in page 99.
- All the units used in this report are SI base units, derived units and prefixes as described by the International System of Units. All units of each equation are written between brackets, as [unit].
- The figures, tables and equations are enumerated per chapter. For example, Figure 3.2 is the second figure of the third chapter of the report.
- The Appendices are organized in alphabetical order and are located at the end of the report.

Acknowledgments

The authors would like to thank their Master thesis' supervisors Stig Munk-Nielsen, Professor at Aalborg University, and Ángel Ruiz de Vega, Research assistant at the Department of Energy Technology, for all their guidance, support and knowledge dissemination during the entire thesis period. Also, thanks to the IEPE project which financially supported this project with all the necessary equipment.

Moreover, the authors would like to express their gratitude to the laboratory staff at the Department of Energy Technology, specially to Walter Neumayr, Jan Christiansen, Frank Rosenbeck and Mads Lund, for their technical advices and help during the setup implementation period. Furthermore, special thanks to Bjørn Rannestad from kk-electronic A/S for his valuable and enlightening discussions and ideas.

Finally, the authors would like to express their deepest gratitude to their families and girlfriends for their patience, as well as, support and encouragement during these last 2 years of Master program.

Contents

List of Nomenclature

Symbol	Description	Unit
$T_{j,mean}$	Average junction temperature	$°C$
$T_{vj,mean}$	Average virtual junction temperature	$°C$
T_C	Case temperature	$°C$
ΔT_{Case}	Case temperature difference	$°C$
I_C	Collector current	A
V_{CE}	Collector-emitter voltage	V
$V_{CE,sat}$	Collector-emitter saturation voltage	V
$V_{CE,on}$	Collector on-state voltage	V
P_{Cond}	Conduction losses	W
T_{cool}	Coolant temperature	$°C$
A	Cross-Sectional area	m^2
t_{cyc}	Cycle time duration	s
d, D	Duty cycle	%
rho_{el}	Electrical resistivity	$\Omega \cdot m$
C_{eq}	Equivalent capacitance	F
G_{eq}	Equivalent conductance	S
Q	Flow	l/min
V_{GE}	Gate-emitter voltage	V
V_{GES}	Gate-emitter peak voltage	V
Q_{th}	Heat flow	J
ΔQ_{th}	Heat flow difference	J
T_h	Heat sink temperature	$°C$
ΔT_j	Junction temperature difference	$°C$
m	Mass	kg
$T_{C,max}$	Maximum case temperature	$°C$
$V_{GE,max}$	Maximum gate-emitter voltage	V
$T_{j,max}$	Maximum junction temperature	$°C$
Δ_{max}	Maximum temperature difference	$°C$
$T_{vj,max}$	Maximum virtual junction temperature	$°C$
$T_{C,min}$	Minimum case temperature	$°C$
$T_{j,min}$	Minimum junction temperature	$°C$
$T_{vj,min}$	Minimum virtual junction temperature	$°C$
$I_{C,nom}$	Nominal collector current	A
N_f	Number of cycles to failure	$-$
t_{off}	Off pulse Time	s
t_{on}	On pulse Time	s
P_d	Power dissipation	W
P	Pressure	bar
ρ	Relative density	$-$
C	Specific thermal capacity	J/K
f_{sw}	Switching frequency	Hz
T_{sw}	Switching period	s
T	Temperature	$°C$
Δ_T	Temperature difference	$°C$
$I_C(t)$	Time variant collector Current	A
$v_{CE}(t)$	Time variant collector Emitter Voltage	V

Symbol	Description	Unit
C_{th}	Thermal capacitance	J/K
λ	Thermal conductivity	$W/(m \cdot K)$
Z_{th}	Thermal impedance	K/W
$Z_{th,JC}$	Thermal impedance Junction to Case	K/W
R_{th}	Thermal resistance	K/W
$R_{th,JA}$	Thermal resistance Junction to Ambient	K/W
$R_{th,JC}$	Thermal resistance Junction to Case	K/W
$R_{th,JW}$	Thermal resistance Junction to Water	K/W
τ_{th}	Thermal time constant	s
d	Thickness	mm
P_{tot}	Total power	W
$P_{Sw,on}$	Turn on switching losses	W
$P_{Sw,on}$	Turn off switching losses	W
w	width	m

Acronyms and abbreviations

Description	Acronym
Alternating Current	AC
Analog-to-Digital Converter	ADC
Accelerated Life Test	ALT
Bayonet Neill-Concelman	BNC
Coefficient of Thermal Expansion	CTE
Device Under Test	DUT
Direct Bonded Copper	DBC
Direct Current	DC
Finite Element Analysis	FEA
First In First Out	FIFO
Field Programmable Gate Array	FPGA
Ground	GND
Graphical User Interface	GUI
High Temperature Gate Bias Test	HTGB
High Temperature Reverse Bias Test	HTRB
Integrated Circuit	IC
Intelligent and Efficient Power Electronics	IEPE
Insulated Gate Bipolar Transistor	IGBT
Input/Output	I/O
Local Area Network	LAN
Least Significant Bit	LSB
Mean-Time-Between-Failure	MTBF
Mean-Time-to-Failure	MTTF
Negative Temperature Coefficient	NTC
Operating System	OS
Overvoltage Protection	OVP
Poly Butylene Terephthalate	PBT
Polyphenylene Sulphide	PPS
Power Cycling	PC
Physics-of-failure	PoF
Printed Circuit Board	PCB
Pulse-Width Modulation	PWM
Root Mean Square	RMS
Real Time	RT
Real Time Operating System	RTOS
Scanning Electron Microscope	SEM
Temperature Sensitive Electrical Parameter	TSEP
Transistor-Transistor Logic	TTL
Transient Voltage Suppressor	TVS
Vortex Flow Sensor	VFS
Virtual Instrument	VI

Part I

Introduction to lifetime of IGBT modules

1 Introduction

In this chapter, an overview of this thesis topic is presented. First, the relevant background which leads to the initial problem statement is given. In addition, the project objectives and limitations are also depicted. Finally, the project outline is shown.

1.1 Background

Power electronic converters are crucial in the vast majority of electrical energy conversion processes. Their operation is based on power semiconductor devices, which are used as switches blocking or allowing the current flow. Together with a proper control strategy for the commutation of the switches, the power processed by a converter can be fully controlled, i.e. amplitude, frequency and phase shift can be modified, which makes this device suitable for a wide range of applications [1, 2] (Fig. 1.1). Depending on the application, the power ratings of these converters can vary from W, e.g. a laptop charger, to MW, e.g. a wind power converter.

Figure 1.1. Array of applications of power electronics.

In the last decades, great efforts have been made to improve the overall performance of these power electronics systems, leading to higher requirements in terms of efficiency, power density, reliability and lower cost. Especially the energy, industrial, aerospace and automotive sectors are seeking for more reliable and cost effective solutions for the new generation power converters [3].

For instance, reliability issues have emerged in the wind power industry due to the continuous development and latest trends. Without regard to the location, the size of a single wind turbine has been continuously increasing in order to achieve low price per kWh. The wind turbines started from few kilowatts in the 80s up to the current 8MW, which is the largest wind turbine in the world,

installed in Denmark by Vestas [4]. However, it has been demonstrated in [5–8] that the larger size of wind turbines leads to a higher failure rate, as shown in Fig. 1.2.

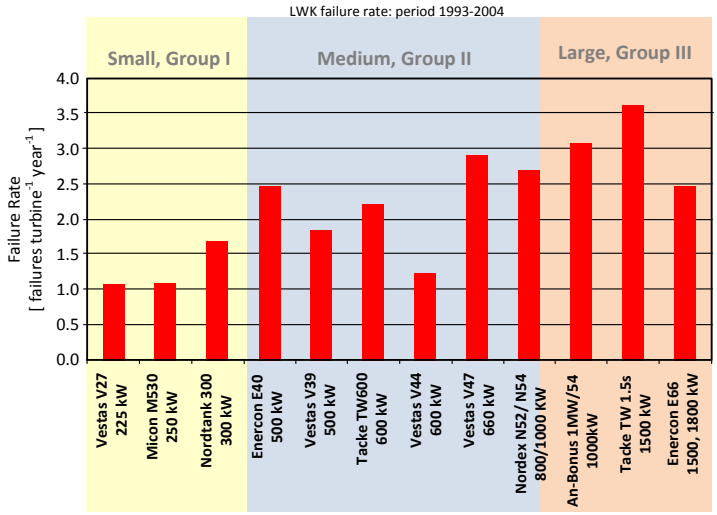


Figure 1.2. Number of failure per turbine and year for several wind turbine models. Results from the survey carried out by the Schleswig Holstein LandWirtschaftsKammer (LWK) from 1993 to 2004 [5].

Moreover, off-shore wind power installations showed a record growth of 34% in 2013 while the on-shore share decreased by 12% compared to 2012 [9]. This tendency of moving from on-shore to off-shore installations, because of richer and more constant wind potential [3], gives again an opportunity for larger wind turbines since it allows higher power ratings and larger mechanical size. Nevertheless, this implies a more expensive and less frequent maintenance which in turn requires equipment which is less prone to failures and capable to withstand harsh environmental conditions (humidity, salt, etc.).

In order to investigate these failures, the wind power industry carried out several surveys regarding reliability in wind turbines, as described in [5–8, 10, 11]. An interesting outcome of these studies, which indicated the starting point of this project, was the distribution of failures among the different components within a wind turbine, depicted in Fig. 1.3. These results show that the component which has the highest failure rate is the power converter and, particularly, the capacitors and semiconductor power devices [12].

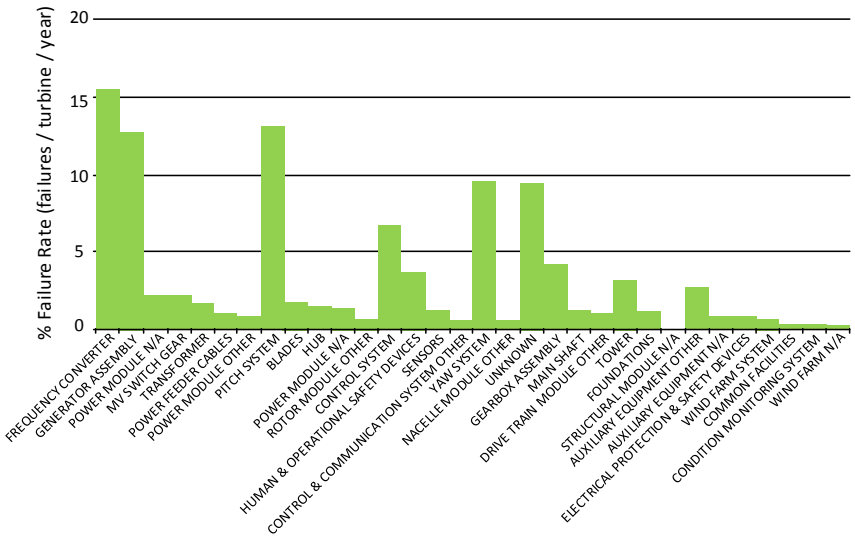


Figure 1.3. Distribution of failure rates per turbine and year of each of the components in a wind turbine. Data obtained from multiple wind turbine manufacturers [10].

Taking into account the preceding paragraphs, the main point of discussion can be summarized as: since power electronics are widely used in many applications, the increase on their reliability is of utmost importance for a diverse array of industrial sectors.

Within this frame, the Intelligent and Efficient Power Electronics (IEPE) research center was started in 2012 [13, 14] with the purpose of developing the new generation of reliable power electronics devices and establishing an infrastructure of testing facilities which can broaden the diversity of applied research. The IEPE center has merged academia (Aalborg University, University of Southern Denmark, Danish Technological Institute) and industrial partners (Danfoss A/S, Grundfoss A/S, KK-electronic A/S and Vestas Wind Systems) together on several on-going research projects, as the present Master thesis, in order to analyse and provide solutions to the necessities of the market.

1.2 Evolution in the research field of reliability

The term reliability defines the ability of an item to perform its required function under stated conditions (mission profile) for a stated period of time (mission time) [15]. Usually, it is expressed by the probability of failure, or the frequency of failure. The necessity of addressing reliability issues in power electronics came up even since the 1950s mostly for transport and military applications. In these primitive stages, the research on predicting the lifetime of a power electronic product was relied on handbook-based models (e.g. military hand-book MIL-HDBK-217F [16]) and statistical metrics (e.g. mean-time-to-failure (MTTF), mean-time-between-failures (MTBF)) without regard to the test methods, operational conditions and different technologies, leading then to uncertainties [3].

During the last 30 years, several international standards have been issued in the effort of building common guidelines over the testing methods and the assessing criteria which are used to quantify the expected lifetime of a product. At the same time, each manufacturer of power electronic modules has followed a specific internal approach on this process inserting a factor of uncertainty when a comparison of results between different testing methods, failure criteria and manufacturers is done [17].

In the 1990s a new era in reliability studies has begun with the introduction of a different approach, the so-called Physics-of-Failure (PoF). This approach intends to investigate the reliability avoiding empirical data and taking into account both deterministic (i.e. physics, material, chemistry) and probabilistic parameters (i.e. statistics). Trying to identify the root of failure mechanisms, PoF implies modelling and analysis of the wearing out factors, such as temperature cycles, voltage, humidity etc., which can lead to a specific failure. In contrast to the initial empirical methods, the acquired knowledge earned by PoF approach can be used later in the design and manufacturing phase and improve the performance of power electronics [3].

Nowadays, a more integrated lifetime prediction tool is used to determine the design requirements of a power electronic module, its expected lifetime and failure rates. This involves inputs such as the manufacturer's datasheets, field data and simulations, which are all manipulated as input data by the test setup. Then on, lifetime prediction models are applied to determine about the reliability.

A kind of tests that are widely used in latest reliability studies are the Accelerated Life Tests (ALT) [18]. In principle, during ALT, the device-under-test (DUT) is stressed at higher levels than the expected normal operation with the purpose of minimizing the time up to the failure. By these tests, the product limits and weaknesses are found in the shortest period of time. In this project a similar ALT test will be performed together with real-time condition monitoring of different parameters of the system (i.e. temperatures, voltage and current values).

1.3 Problem analysis

As it has been pointed, power converters are entitled to be highly efficient and feature high power density. In addition, their performance must be reliable and, thus, the expected operational times should be fulfilled according to the product specifications. Insulated Gate Bipolar Transistor (IGBT) modules are one of the most used semiconductor power devices in high power applications but at the same time they are also the main components subjected to stress within a power converter [17, 19]. In the current work, high power IGBT modules will be used as they are dominating in high power applications [20, 21]. Hence, it is necessary to analyse and understand the main stressors of these devices which lead to their failure.

The research within this field has already demonstrated that the main failure mechanisms are of mechanical nature, as described in [17, 22–24]. The explanation of this lies in the internal structure of the device: the IGBT module consists of various layers of different materials [24]. Each of these materials presents different thermo-mechanical properties, and hence, different Coefficients of Thermal Expansion (CTEs).

As a consequence, the mismatch of the thermal expansion coefficients between the different attached parts causes mechanical fatigue and, consequently, the failure of the module. The main failures of IGBT power modules found in the literature [17, 22–24] have been summarized in Table 1.1:

Table 1.1. Summary of the main failure mechanisms in wire-bonded IGBT power modules [17, 22–24]

Main failure mechanisms in IGBT power modules
Bond wire lift-off
DBC solder joint fatigue
Bond wire heel cracking
Aluminium reconstruction
Cosmic ray induce burnout
Chip-mount-down solder joint
Busbar solder joint

This mechanical fatigue is induced mainly by the thermal stress in the IGBT silicon chips due to load variations and device commutation, or in other words, changes in the current flowing through the devices which causes power dissipation. The thermal stress is described by the temperature variation in the chip junction. Fig. 1.4 serves a representative example of a temperature profile of IGBT switches, as consequence of wind and load variations (mission profile) in a wind turbine converter.

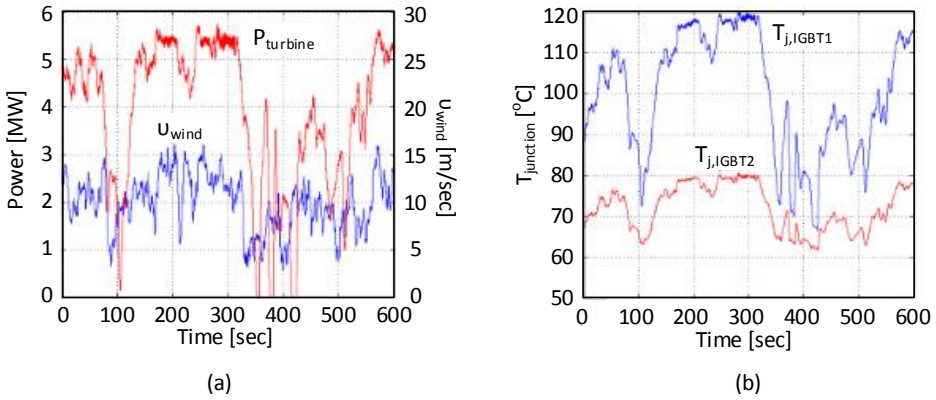


Figure 1.4. (a) Wind and power profiles of 5.6MW wind turbine at $v_{av} = 10m/s$, (b) Junction temperatures of 2 IGBT switches in an NPC converter for the wind profile with $v_{av} = 10m/s$ [25]

Moreover, since the mechanical fatigue, and subsequent failures shown in Table 1.1, are induced by a temperature stress, it can be observed a direct relation between lifetime and junction temperature variation. Hence, the lifetime of semiconductor devices can be predicted using several lifetime models, such as the Coffin-Manson-Arrhenius lifetime model (see Fig. 1.5), which provides the number of cycles to failure in function of ΔT_J and $T_{j,mean}$. This example has been used due to the simplicity of the needed parameters [24].

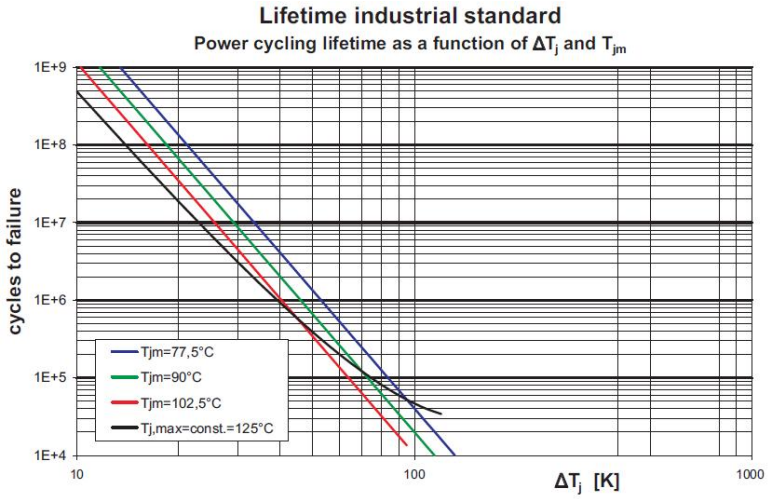


Figure 1.5. Coffin-Manson-Arrhenius curve: number of cycles to failure in function of the junction temperature variation ΔT_J and $T_{j,mean}$.

Therefore, a test bench which is able to stress and wear out the IGBT modules at different temperatures is crucial to trigger the desired failure mechanisms. Afterwards, a lifetime model can be applied in order to estimate and to investigate the life expectancy of the device under test (DUT).

1.4 Problem statement

The analysis presented in the previous sections has highlighted the importance of the reliability of power electronics. Industry is seeking for more robust and durable converter designs, which implies a longer lifetime time of the semiconductor power devices and specifically the IGBT modules. In order to fulfill these requirements, test platforms which can emulate real stress conditions and can accelerate the wear out process of the modules in order to identify their failure mechanisms, should be designed and implemented.

The above-mentioned leads to formulate the following questions:

- Is it possible to design and build a test setup which emulates the thermal stress due to high current variations and triggers the main failure mechanisms in high power IGBT modules?
- Is it possible to develop an accurate and reliable junction temperature measuring system that only relies on electrical measurements?
- And which are the other capabilities of this test setup? Is it possible to determine the thermal impedance?

1.5 Objectives

Based on the problem statement formulated above, the following objectives of this Master thesis are defined:

- Design and implement a power-cycling test setup which is able to wear out IGBT power modules in an accelerated manner and describe its capabilities
- Conduct an acceptance test of the power-cycling test setup
- Develop, implement and validate a junction temperature estimation system for IGBT power module devices
- Perform wearing out tests on the IGBT modules for subsequent lifetime investigation

1.6 Limitations

The limitations of the current work are listed below:

- Because of design constraints such as cooling technology (Danfoss ShowerPower®) and the lay-out of the IGBT module (package), the power cycling wear out test setup has been designed to accommodate only one type of device under test (DUT): PrimePACK™3 IGBT Module.
- Due to the module package, the electrical quantities to characterize the behaviour of IGBT chips will be measured only on the accessible terminals of the module and not directly on the inner circuitry.
- The baseplate temperature of the device is assumed to be equal to the coolant fluid temperature which is measured by means of sensors placed in the inlet and outlet of the ShowerPower®. Moreover, as stated in the Danfoss ShowerPower® documentation [26, 27], the temperature gradient is considered to be equally distributed throughout the entire baseplate.
- Regarding the cooling system, this report does not deal with its design specifications which were performed by external collaboration. Therefore, only a general description of the cooling system layout and the components used for its implementation is provided.

1.7 Project outline

The present master thesis is divided into three main parts. **Part I** is called **"Introduction to lifetime of IGBT modules"** and contains the first two chapters of this report. In *Chapter 1*, the background, problem analysis, objectives and limitations are presented, while in *Chapter 2* all the relevant information regarding packaging, thermal analysis and reliability tests of the IGBT modules is given.

Part II is called **"Accelerated wear-out test setup"** and is constituted by three chapters. Particularly, *Chapter 3* provides the analysis, design and implementation of the test setup which has been built in the Reliability garage during the thesis period. All the acceptance tests regarding the performance of the power cycling test setup are presented in *Chapter 4* by means of experimental results. At the end of this part, *Chapter 5* deals with the junction temperature estimation methods.

First, a literature review of the different methods is made and afterwards, the two selected and implemented methods are presented.

Part III, "Results and conclusions" is divided into two chapters. *Chapter 6* demonstrates the outcomes from the wearing-out process of the IGBT modules, and the main body of the report ends with *Chapter 7* where the conclusions are drawn followed by the perspective work.

Finally, **Part IV, "Appendices"** provides all relevant information regarding the test setup diagram, the most important datasheets, a summary of the PCBs, a description of the data acquisition and monitoring system of the cooling and the contents of the CD attached to this report.

Packaging, reliability and power cycling of high power IGBT modules

2

In this chapter, a theoretical analysis of the main topics relevant to this thesis is given. A detailed description of the IGBT modules, its package technology and the associated failures, is provided. In addition, the main testing procedures on reliability of semiconductor devices are presented.

2.1 Insulated Gate Bipolar Transistor (IGBT) modules

As mentioned in the previous chapter, IGBT modules are the most used power semiconductor devices in medium to high power applications and also the main component subjected to failure in a power converter.

From an electrical point of view, the main components of interest within a module are the semiconductor chips i.e. IGBT and diode chips. The properties of these chips allow blocking voltage potentials and conducting currents. Consequently, this process generates power dissipation in the module and, therefore, heat losses. These switching characteristics will be comprehensively described in Section 2.1.2. In brief, three variables define the main characteristics of a power semiconductor device:

- Blocking voltage, V_{CE}
- Current capability, I_C
- Power dissipation, P_d

Since the ratings for voltage and current are continuously increased by the market needs, the amount of power dissipation is also increased and, hence, the necessity of a package which can properly handle the thermal stress within a certain range (normally ranging from -55°C to 175°C in IGBT applications). This is the main reason why semiconductor technology in high power applications has moved towards the use of advanced power modules, which are designed under the premise that heat from the module package is efficiently evacuated [17].

In order to understand the internal structure of an IGBT module, a picture of the Danfoss PrimePACK3 IGBT module (DP1000B1700T) without plastic frame is shown in Figure 2.1.

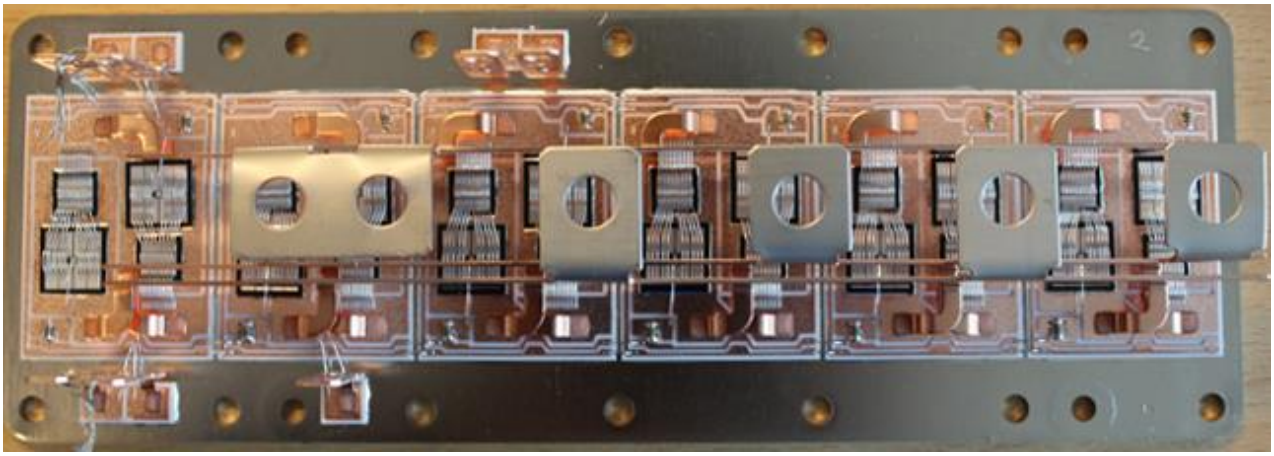


Figure 2.1. Top view of a Danfoss PrimePACK3 IGBT (DP1000B1700T) open module where the different parts of the module assembly can be observed.

The above IGBT module from Danfoss is a half-bridge module rated for a collector-emitter blocking voltage of 1700V and a collector current of 1000A. The nominal current is obtained by paralleling 6 IGBT chips attached to 6 different DBC sections, with their respective high-side and low-side IGBT and diode chips also interconnected. This example is given to demonstrate the complexity of an IGBT module and, at the same time, the importance of a proper dissipation of the heat in a package of 25x8.9 cm when working in such high power levels. A detailed description of the thermal design is given in Section 2.2. The device under test (DUT) of this project is the Infineon PrimePACK™3 module, which has the same ratings and similar configuration as the Danfoss module. Further details about it will be given in Chapter 3 where the DUT is presented.

2.1.1 Structure and construction of IGBT modules

To thoroughly investigate its failure mechanisms, an IGBT module cannot be treated as a single power semiconductor device but as an assembly of different parts and components within a package. In fact, the behaviour of the module relies on the interaction between mechanical, electrical and thermal interfaces [28].

The structure, materials and manufacturing processes chosen for the design of such IGBT module play a crucial role in the final performance of the device. A simplified diagram of the typical structure of an IGBT module is depicted in Fig. 2.2.

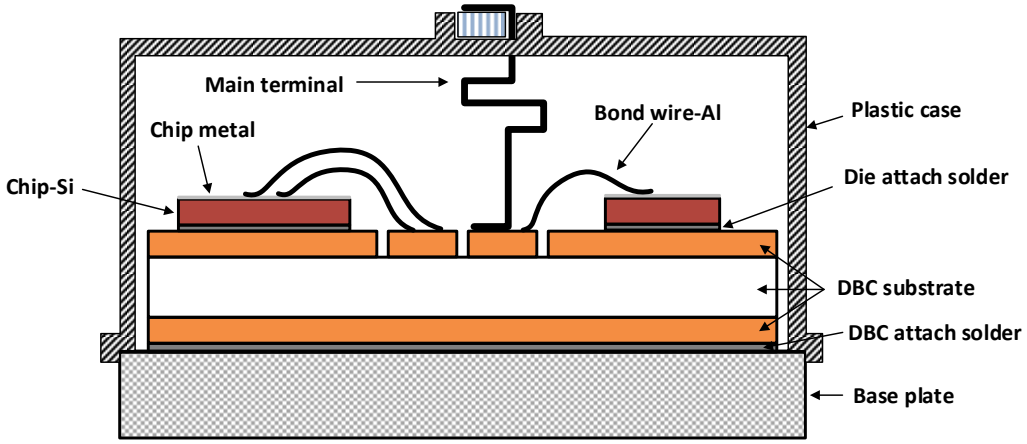


Figure 2.2. Layout of the different parts and components within an IGBT module and their corresponding materials.

As can be observed in Fig. 2.2, an IGBT module is made up of different layers of different materials. These multiple layers can be outlined as: the silicon chip, the die attach-solder, the Aluminium bond wires to interconnect the chips metal, the Direct Bonded Copper (DBC) substrate and its attach-solder, and finally, the baseplate.

Regarding the materials, the latest designs of IGBT module consists of [17, 28]:

- **Plastic frame**
  The requirements that the plastic frame must fulfil can be divided into 4 categories: mechanical stability, high tensile strength under different operating temperatures, electrical insulation and isolation from environmental factors such as moisture and dust. For that purpose, polymer plastics such as polyphenylene sulphide (PPS) and poly butylene terephthalate (PBT) are used. The temperature range covered by this plastic materials ranges from -50°C up to 240°C (for PPS) [28].

- **Direct Bonded Copper (DBC) substrates**
  The DBC consists of a ceramic dielectric insulator where 2 layers of pure copper (top and bottom) are bonded. It has three main functions: providing electrical insulation between the semiconductor device and the cooling, providing a thermal path to the cooling system and allowing the current flow between the different copper tracks and connections [28].

- **Baseplate**
  The baseplate works as a thermal interface between the DBC and the heat sink. It is normally made of copper with a thickness of 3 to 8 mm, plus a nickel coating of 3 to 10 μm. Other alloys such as aluminium silicon carbide (AlSiC) and copper molybdenum (Cu/Mo) can be used [28].

- **Moulding compound**
  The material usually chosen in high power modules is silicone gel. This serves as the last interface between the module components and the plastic frame. Therefore, it offers great electrical insulating properties and, at the same time, it can withstand temperatures ranging from -100°C to 200°C [28].

Another important factor to take into account is the electrical bonding technology of the different components. Since the used technologies can improve or worsen the electrical, thermal and mechanical performance of the module, this factor is critical to analyse its ageing mechanisms. The next paragraphs will focus on the characteristics of the internal bonding technologies applied in latest IGBT module designs, which are [28]:

- **Chip soldering**
  The semiconductor die is attached to the DBC substrate in order to provide electrical and thermal connection. This process is based on vacuum soldering in order to prevent air voids which can lead to an undesired increment of the thermal resistance between chip junction and DBC [28].

- **DBC-to-Baseplate soldering**
  The DBC is attached to the baseplate, which is screwed to the heat sink, forming a thermal path for the heat dissipation. Most of the used solders are lead-free. Similarly to the chip soldering, air voids should be avoided in order to not increase the thermal resistance [28].

- **Ultrasonic wire bonding**
  Most commonly, it consists in an aluminium wire which is welded to a contact pad by means of ultrasound at high frequencies (40 kHz to 100 kHz) providing a firm connection. Depending on the current rating of the module, the number of bond wires, and their diameter and length

will differ [28]. An example of wire bonding between the different chips and the DBC can be observed in Figure 2.3.
The bond wire is one of the critical factors for lifetime assessment. Since the beginning and end sections of the wire are attached to the chip, DBC or frame, the highest temperature of the wire occurs in the middle part of it. Coincidentally, the bond wire middle section is also subjected to a large mechanical fatigue, leading to the destruction of it. Latest designs have introduced the copper wire bonding as a new bonding technology since the mismatching between thermal expansion coefficients is lower and hence the ageing of the module is reduced [28, 29].

- **Soldering connections between DBC sections**
  In high power modules, several semiconductor devices must be connected in parallel to meet the current requirements. Consequently, several DBCs are electrically connected one to each other. The interconnection of these DBC regions can be performed by means of bond wires or metal bands.

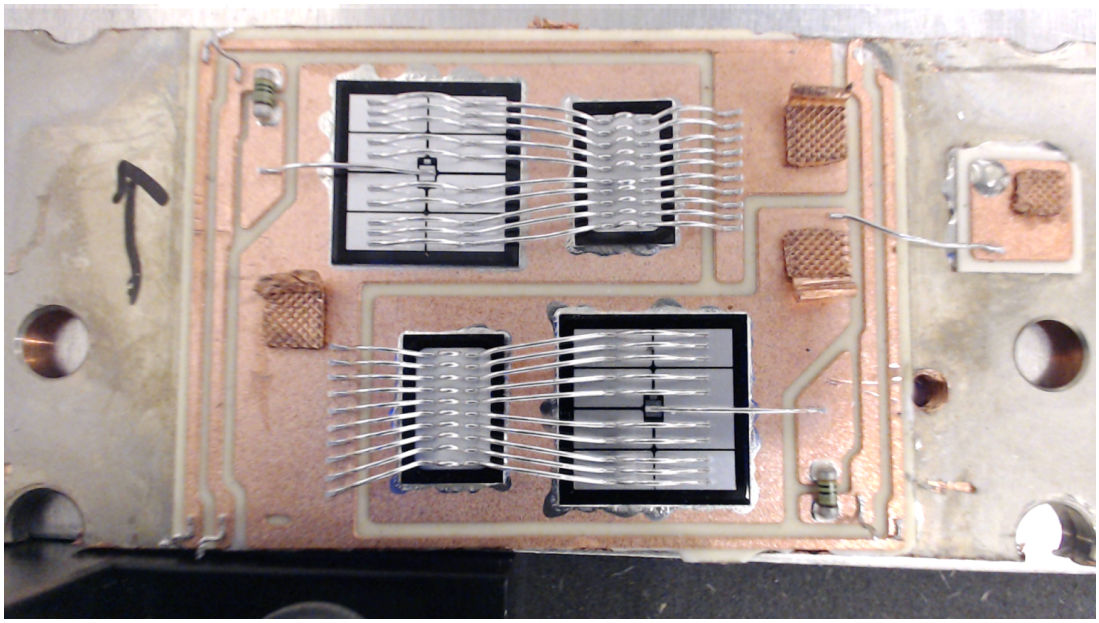


Figure 2.3. DBC section of Danfoss PrimePACK™3 IGBT open module with the bond wires connecting IGBT chips, Diode chips and DBC substrate. Picture of a healthy module, borrowed from the Department of Physics and Nanotechnology (AAU).

2.1.2 Switching characteristics and losses of an IGBT module

Even though great efforts can be done in the design of IGBT power modules, the power dissipation losses of a semiconductor device are an unavoidable consequence of its electrical properties. The forward characteristics and switching behaviour of these devices are the main contributors to these losses.

The forward characteristics of an IGBT provide information on how the device behaves in conduction mode. As an example, the forward characteristics provided in the datasheet of the Fuji Electric PrimePACK™3 IGBT module (2MBI1400VXB-120P-50) are depicted in Figure 2.4. These are given for 3 different junction temperatures (25°C, 125°C and 150°C) and for a test current ranging from 0A to $2{\cdot}I_{C,nom}$. The term junction temperature is defined in Section 2.2.4.

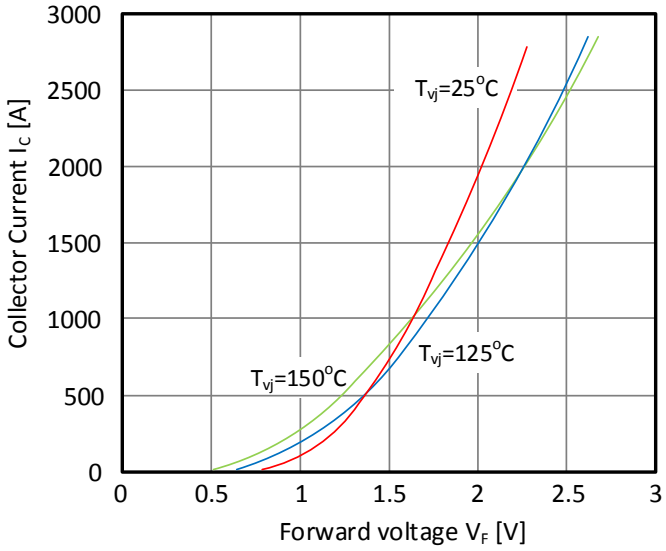


Figure 2.4. Forward characteristics of the 1200V/1400A PrimePACK™3 IGBT module (2MBI1400VXB-120P-50) from Fuji Electric.

As can be observed, when the IGBT conducts, a voltage drop appears across the device. This on-state voltage drop is known as $V_{CE,sat}$ or $V_{CE,on}$ and it occurs because of the on-state resistance of the chip. This resistance can be calculated with the slope of the curves plotted in Figure 2.4. Obviously, as the current level increases, the on-state voltage drop is also higher and, hence, the conduction losses. Figure 2.4 also opens another discussion which is the direct relation between the collector-emitter saturation voltage and the junction temperature. This topic will be addressed in Chapter 5.

By analysing the switching characteristics of a generic IGBT (Fig. 2.5), it can be realized that the IGBT losses are divided into 3 stages: turn-on process, turn off process and conduction mode.

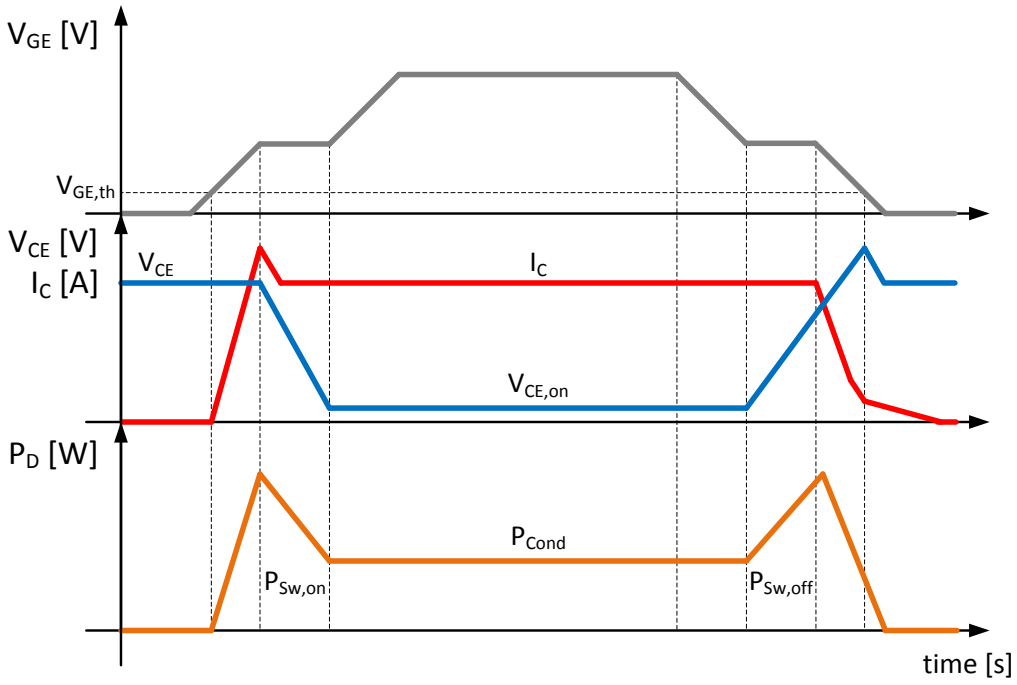


Figure 2.5. Simplified representation of the switching characteristics of an IGBT.

The average total losses of an IGBT module over a switching period T_{sw} can be calculated as the product of collector current I_C and collector-emitter voltage V_{CE}. Similarly, considering one switching period with switching frequency f_{sw} and duty cycle d, these are the sum of the switching losses ($P_{Sw,on}$ and $P_{Sw,off}$) and conduction losses (P_{Cond}), as in Eq. 2.1. The blocking losses can be negligible [17, 28].

$$P_{total} = \frac{1}{T_{sw}} \int_0^{T_{sw}} v_{CE}(t) \cdot i_C(t) dt = P_{Cond} + P_{Sw} \quad [W] \tag{2.1}$$

Separately, the conduction losses (Eq. 2.2) and switching losses (Eq. 2.3) can be calculated as,

$$P_{Cond} = V_{CE} \cdot I_C \cdot d \quad [W] \tag{2.2}$$

$$P_{Sw} = P_{Sw,on} + P_{Sw,off} = (P_{Sw,on} + P_{Sw,off}) \cdot f_{sw} \quad [W] \tag{2.3}$$

However, the switching losses can be considered negligible when applying power-cycling conditions with low switching frequency.

2.2 Thermal modelling of IGBT modules

Reliability of an IGBT module is strongly dependent on the performance of its thermal design. This section presents an analysis of the thermal design in IGBT power modules. It comprises the basic concepts to be used within the thermal domain, the definitions of the relevant temperatures and the thermal networks to be used for modelling of IGBT modules.

2.2.1 Introduction to the thermal domain: thermal resistance and capacitance

As discussed in Section 2.1.2, semiconductor characteristics generate switching and conduction losses which are dissipated in the form of heat. This heat must be evacuated of the device by all means and, therefore, all components within a module assembly must be designed to provide the most optimal and highly conductive thermal path to the cooling medium.

The similarities between the physics describing heat conductivity and electrical conductivity in a medium allow the use of equivalences between the electrical and the thermal domains. In Figure 2.6, a layer of conductive material with thickness d and cross-sectional area A is presented. This material with a specific thermal conductivity λ will allow a specific amount of heat flux P_d to be conducted through it and, at the same time, this heat flow will generate a temperature difference ΔT across it. Same will happen if it is considered the electrical resistivity ρ_{el} of the material, which will determine the amount of current flowing through it.

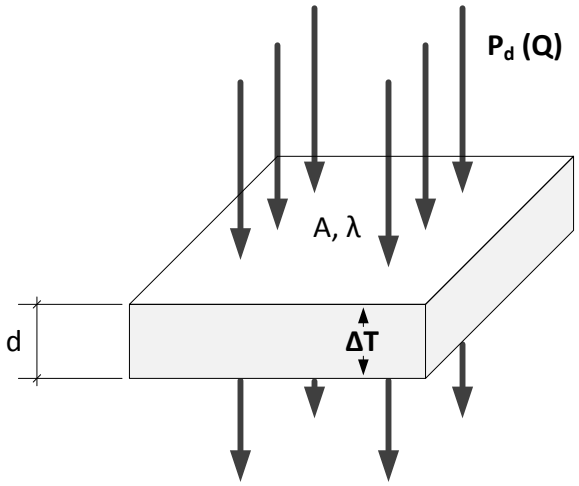


Figure 2.6. Example of heat conductivity through a layer of material with specified dimensions (d and A) and thermal conductivity λ.

Moreover, the above said serves as a great introduction to the concept of thermal resistance R_{th}. The thermal resistance of a material represents its ability to resist heat flow. Therefore, it can be calculated according to its dimensions and its thermal properties, as shown in Eq. 2.4.

$$R_{th} = \frac{1}{\lambda} \cdot \frac{d}{A} \qquad [K/W] \tag{2.4}$$

Similary, if the thermal resistivity of the layer depicted in Figure 2.6 is represented by its thermal resistance, the relation between temperature difference and heat flow can be calculated by the thermal Ohm's law or Fourier's thermal conduction law in Eq. 2.5 [28].

$$P_d = \frac{\lambda \cdot A \cdot \Delta T}{d} \qquad [W] \tag{2.5}$$

which combined with Eq. 2.4 becomes,

$$R_{th} = \frac{\Delta T}{P_d} \qquad [K/W] \tag{2.6}$$

On the other hand, due to its physical properties, a material not only conducts heat but it also has the capacity of storing part of that thermal energy. This storage capacity is represented by means of the thermal capacity C_{th}. It can be calculated according to the relation between heat flow P_d and temperature difference ΔT as in Eq. 2.7.

$$C_{th} = \frac{\Delta Q_{th}}{\Delta T} = \frac{\Delta P_d}{\Delta T} \qquad [J/K] \tag{2.7}$$

Then, if the layer in Figure 2.6 is considered with a temperature difference ΔT, a mass m, a specific thermal capacity c, its heat flow can be described as in Eq 2.8.

$$\Delta P_d = c \cdot m \cdot \Delta T \quad [J] \tag{2.8}$$

By combining Eq 2.7 and 2.8, and considering the material dimensions and relative density ρ [28], the thermal capacity becomes:

$$C_{th} = c \cdot \rho \cdot d \cdot A \quad [J/K] \tag{2.9}$$

As a final comment, the thermal resistance can be used to analyse the steady-state response of a material temperature to a specific power dissipation input. However, it does not represent the dynamic characteristics, which are represented by the thermal capacitance. Further details about this fact are given in Section 2.2.3. In addition, it should be taken into account that the value of the thermal resistance is not fixed as it depends on the temperature.

2.2.2 Thermal equivalent networks: Cauer and Foster

In the thermal analysis of IGBT modules, the pn-junction of the semiconductor device works as the heat source while, as the name indicates, the heat sink operates as the thermal sink of all that heat energy. However, as can be observed in Figure 2.2, an IGBT module is made up of multiple layers. This means that several R_{th}-C_{th} combinations are needed to model its complete thermal interface.

Two different one-dimensional thermal equivalent networks are used to model the different layers in between of the thermal source and thermal sink: Cauer model and Foster model.

2.2.2.1 Cauer model

A Cauer model of an IGBT module is depicted in Fig. 2.7. This thermal equivalent circuit accurately represents the physical properties of each of the layers.

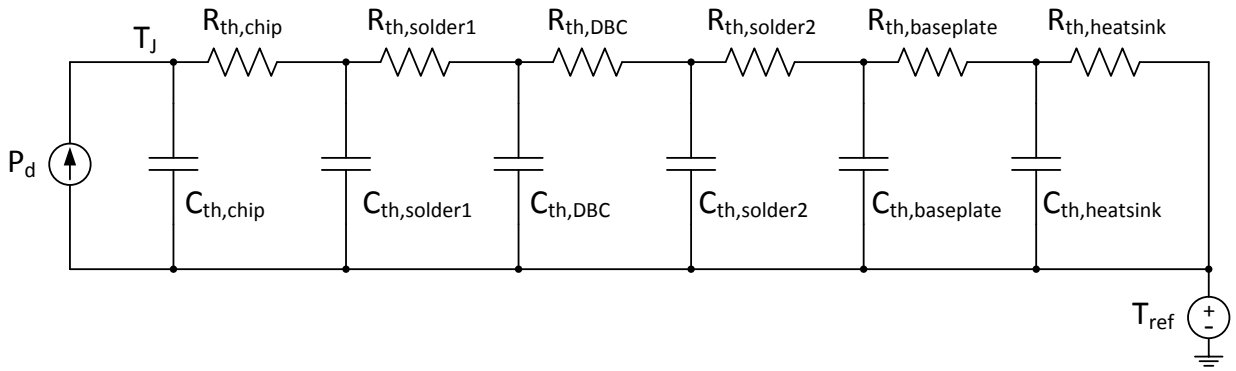


Figure 2.7. Cauer equivalent network for modelling the thermal interface of an IGBT module.

The values of R_{th} and C_{th} can be calculated according to Eq. 2.4 and Eq. 2.9, respectively. Therefore, temperature variations can be calculated in each of the nodes and be easily related to its geometrical locations. However, the calculation of this model is not straightforward since the exact material parameters are not always available.

2.2.2.2 Foster model

The Foster model of an IGBT module is depicted in Fig. 2.8. Contrary to the Cauer model, the Foster model is a combination of R_{th}-C_{th} values which does not have any physical meaning, but it describes the transient behaviour of the overall thermal system in the same manner [17, 28].

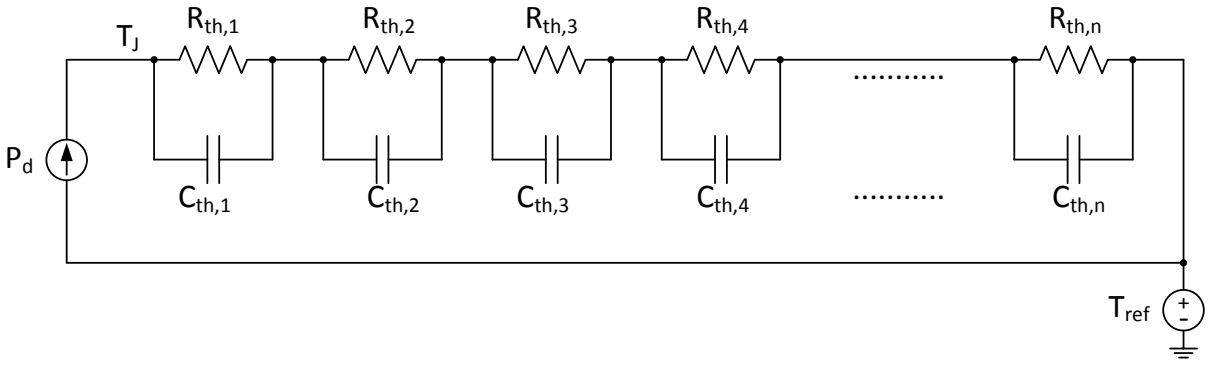


Figure 2.8. Foster equivalent network for modelling the thermal interface of an IGBT module.

This model is widely used in thermal modelling of power semiconductor devices since it is easier to be acquired by means of experimental measurements. Normally, Foster model parameters are provided in the datasheet of the devices as pairs of $R_{th,i}$ and $\tau_{th,i}$ and represented by the thermal impedance curve.

2.2.3 Thermal impedance, Zth

The term thermal impedance Z_{th} or transient thermal resistance is used to describe the time varying behaviour of a thermal system. An example of thermal impedance curve is shown in Fig. 2.9.

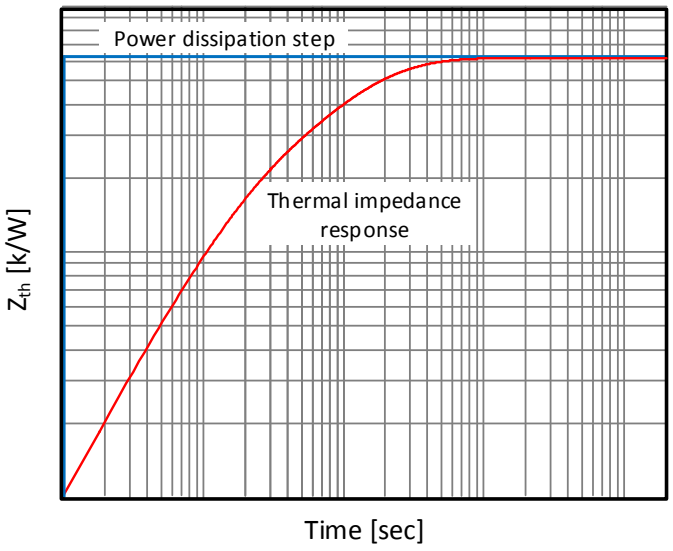


Figure 2.9. Thermal impedance curve of a generic IGBT chip.

As previously explained, the thermal interface of a power module is represented by sets of R_{th}-C_{th}, or likewise, $R_{th,i}$ and $\tau_{th,i}$. The $\tau_{th,i}$ is known as the thermal time constant, and it provides the same information as in the electrical world: the transient response of the system.

The thermal impedance can be expressed by the analytical expression shown in Eq. 2.10 [17].

$$Z_{th} = R_{th}(t) = \sum_{i=1}^{n} R_i \cdot [1 - e^{\frac{-t}{\tau}}] \quad [K/W] \tag{2.10}$$

considering the thermal time constant as,

$$\tau_{th} = R_{th} \cdot C_{th} \quad [s] \tag{2.11}$$

In addition, the temperature difference will also show a time varying behaviour due to the influence of the thermal capacity, as described in Eq. 2.12.

$$\Delta T(t) = \Delta T_{max} \cdot (1 - e^{\frac{-t}{\tau}}) \quad [^{\circ}C] \tag{2.12}$$

Since the thermal impedance and the temperature change in time, Eq. 2.6 can now be rewritten as,

$$Z_{th}(t) = \frac{\Delta T(t)}{P_d} \quad [K/W] \tag{2.13}$$

Therefore, the steady-state and transient response of the temperature variation in a semiconductor device, for a given step input of power losses, can be analysed by means of using Eq. 2.6, Eq. 2.13 and the information provided in the thermal impedance curve of the datasheet (Fig. 2.9).

If the constant power pulses are periodically injected, the maximum temperature variation on stationary conditions can be calculated according the power level, the on-state time and the off-state time [17], as in Eq. 2.14.

$$\Delta T_{max,steady} = P_{on} \cdot \sum_{i=1}^{n} R_i \cdot \frac{1 - e^{\frac{-t_{on}}{\tau_i}}}{1 - e^{\frac{-(t_{on}+t_{off})}{\tau_i}}} \quad [^{\circ}C] \tag{2.14}$$

This formula will be very helpful to define the characteristics of the power cycling test setup.

2.2.4 Definitions of the relevant temperatures

The definitions of the temperatures which will be taken into account in this report are [17, 28]:

- **Virtual junction temperature,** T_{vj}
  It corresponds to the temperature inside the pn-junction of the chip. Due to the difficulties to directly measure this temperature, the term virtual is used since it does not refer to the exact temperature gradient in the silicon device but an average approximation. This estimation/approximation is done by means of indirect measuring methods such as measuring the on-state collector-emitter voltage drop. In other words, T_{vj} is the average chip temperature assuming homogeneous cooling of the semiconductor device [30].
  This term is used to calculate the thermal impedance and resistance ($Z_{th,J-C}$ and $R_{th,J-C}$).

- **Junction temperature swing,** ΔT_{vj}
  It corresponds to the junction temperature swing when the IGBT is heated (current conduction) and cooled (no current conduction). It is calculated as the difference between the maximum and minimum junction temperatures, $T_{vj,max}$ and $T_{vj,min}$. $T_{vj,min}$ is assumed to be equal to the case temperature T_c:

$$\Delta T_{vj} = T_{vj,max} - T_{vj,min} \quad [^{\circ}C] \tag{2.15}$$

- **Maximum junction temperature,** $T_{vj,max}$
  It corresponds to the maximum peak value of a junction temperature swing. It also indicates the maximum allowable temperature to operate the semiconductor within its safe operating area.

- **Mean junction temperature,** $T_{vj,mean}$
  It corresponds to the mean value of a junction temperature swing. This parameter is very relevant for the assessment of the lifetime of the module and can be calculated as,

$$T_{vj,mean} = \frac{T_{vj,max} - T_{vj,min}}{2} \quad [^{\circ}C] \tag{2.16}$$

- **Case temperature,** T_c
  It corresponds to the temperature gradient across the surface of the baseplate. When the module is completely cooled, this temperature should be equal to $T_{vj,min}$ and T_h.

- **Heatsink temperature,** T_h
  It corresponds to the temperature gradient across the surface of the heatsink. This temperature is assumed to be equal to the temperature of the cooling fluid.

- **Coolant temperature,** T_{cool}
  It corresponds to the temperature of the cooling fluid which flows through the heat sink. It is measured by a temperature sensor in the outlet of the heat sink.

Because of the importance of the determination of the junction temperature, Chapter 5 presents different methods for its estimation.

2.3 Reliability tests on IGBT modules

Reliability has already been stated as a critical and demanding characteristic of the power electronics in general and in this case of the IGBT modules. It is a prerequisite and continuous challenge for any critical and cost-sensitive application in automotive, energy and industrial sectors. It becomes even more difficult to meet the qualifications regarding reliability as the demands for higher power densities per IGBT module induce higher operating temperatures. Proof of this fact is the tendency of increasing the maximum operation module temperature from 150°C to 175°C [17].

Therefore, manufacturers and researchers carry out tests to investigate the degradation process, the failure mechanisms and finally to determine the life span of power modules. Obviously, these tests cannot be performed under real field conditions but they have to be accelerated and reduce the expected lifetime of a device up to few weeks. International standards are specified in order to set a common framework for these tests regarding the general test setup, testing procedures as well as the main failure criteria of these tests. The different types of qualification tests and failure criteria will be presented in the following sections. In addition, power cycling will be thoroughly described due to its importance for lifetime estimation of IGBT modules.

2.3.1 Types of reliability test and failure criteria

There are many different types of endurance and reliability tests for IGBTs according to IEC standards [17] which examine the chip itself and the module performance as a whole. The most representative tests are the following:

- **High temperature reverse bias test (HTRB)**
  During this test, reverse voltage is applied on the semiconductor with a preferably value 80% of the nominal blocking voltage and the junction temperature is kept at its maximum limit. By this test, the blocking capability of the semiconductor is assessed expecting leakage current less than the upper specified limits during 1000h of test duration. These test conditions are considered as highly accelerated due to the fact that in the real field the blocking voltage from the DC link is usually 30% less than the rated value of the chip and it is exceeded only for short times during switching overvoltages [IEC60747-9:1998].

- **High temperature gate bias test (HTGB)**
  In this case, the gate-emitter leakage current is evaluated by applying 80% of the specified maximum allowable $V_{GE,max}$ for 1000h and it is required to stay below the given nominal value. Again the operating temperature is set very close to the maximum limits in order to accelerate the process. [IEC60749:1998].

- **High and low temperature storage life test**
  This test is carried out to identify the ability of the materials of the module (plastic, glue, rubber, silicone etc.) to withstand long term extreme temperatures and at the same time to maintain their physical and thermo mechanical properties. Typical test conditions are temperatures of -65°C to 150°C for 1000h [IEC60749:1996].

- **High humidity high temperature reverse biased test**
  The purpose of this test is to qualify the impact of prolonged high temperature and humidity on a non-hermetic module. Humidity has always been a degradation factor against semiconductors because it penetrates the enclosure case and reaches up to the chip surface causing internal corrosion and oxidation. Typical tests conditions are 80%-100% of maximum applied blocking voltage, gate-emitter shorted ($V_{GE} = 0$) , $RH = 85\%$, 85°C and 1000h duration. The leakage current should not self-heat the device more than 2°C [IEC60749:1996].

- **Temperature cycling test**
  Temperature cycling tests can also be found in reliability standards as temperature shock tests. During these tests the module is exposed to extreme high (125°C) and low temperatures (-40°C) alternatively and immediately one after the other. It remains in these temperatures until the thermal equilibrium is reached; this time is longer than 1h. The required number of cycles (as cycle is considered one transition) varies from device to manufacturer, but typical number is 20 cycles for high power modules [IEC60749:1998]. This type of test has also another version where the module faces temperature change of 80°C at the case ($T_{min} = 5$°C) and cycle time between 2min and 6min. The requirement for high power module is set to 2000 cycles [IEC6074-9:1998]. Semiconductor manufacturers (Infineon, Semikron) follow their own variations regarding the specifications and assessing criteria of these tests. The temperature swings affect the module internal structure causing cracks and delamination at the constructive materials due to the different material properties. However, as the temperature variations are caused by an external source and not by the semiconductor itself, therefore, only the materials and their assembly can be evaluated. On the other hand, during power cycling tests the semiconductor is the heat source dissipating the loss power.

2.3.2 Power cycling test and standards

Power cycling (PC) is defined as the test procedure during which alternating power dissipation is induced at the power module by means of the injection of pulsating current. As a consequence, temperature swings are caused exclusively by the semiconductor itself which dissipates the losses (conduction and switching) and heats up actively the whole system.

The power module is heated up by the conduction of a constant load current and a temperature gradient is created to the inner module structure. When maximum junction temperature $T_{j,max}$ is reached, the IGBT is switched off and is let to cool down up to the minimum temperature $T_{j,min}$. The baseplate of the device is placed on a heat sink which is usually cooled by forced air or water [31]. Using the baseplate, an indirect control of the junction temperature is performed. Particularly, when the module is turned on, the baseplate reaches its maximum temperature $T_{c,max}$ and then is turned off, until the baseplate will take its minimum temperature $T_{c,min}$. At this point, one cycle is completed. Fig. 2.10 shows a typical test circuit and the different temperatures variations with respect to the load current.

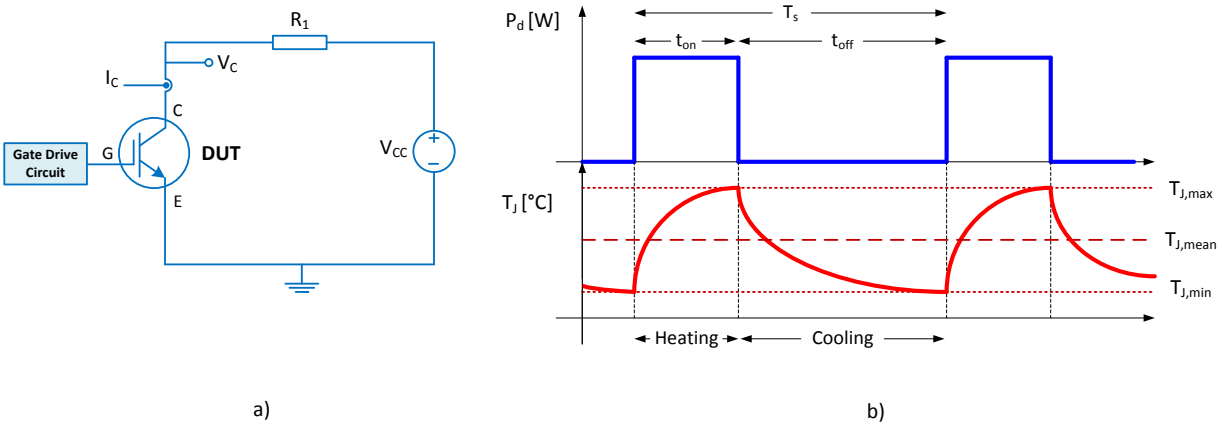


Figure 2.10. (a) Typical test circuit for PC tests recommended by IEC 60747-9, (b) Temperature swing during PC test.

Two very important parameters that are used together to characterize the PC tests are the temperature variation ΔT_j and the average temperature $T_{j,mean}$ as they are given in Eq. 2.15 and Eq. 2.16, respectively.

These parameters are tightly dependent on the duration and amplitude of the current pulse, as well as, the efficiency of the cooling system [17]. The heating process takes longer time, whereas the cooling phase is fast due to small thermal mass of the chip. The duration of cycles usually varies from 1s up to 10s [IEC60747-9:1998, Infineon]. The temperature differences ΔT_j are typically from 60°C to 100°C [17]. The selection of testing parameters should be done with great care. Recent studies [32, 33] have shown that testing factors such as $T_{j,mean}$, ΔT_j, current rating, bond wire diameter and the chip blocking rating, affect the cycles until failure and they need to be considered when tests with different conditions are compared. Four general testing principles have been established [33]:

- Constant on and off pulse times.
- Same ΔT_{case} for all cycles.
- Constant power losses.

- Same ΔT_j for all cycles.

The first two cases are more straightforward as they pass by the module structure and for that reason they are assumed to be more intense and destructive. On the other hand, the other methods need more advanced control. Requiring constant temperature cycles, the power dissipation decreases when the wearing out process increases the thermal resistance. In contrast to this, when the power consumption from the chips is maintained constant by changes in the V_{GE}, the temperature swings can be altered due to degradation of the thermal behaviour.

The selection of DC current pulses during PC tests provides some advantages compared to AC current. The measurement of the electrical and thermal parameters such as $V_{CE,sat}$, current and temperature, becomes less demanding regarding noise, accuracy, switching overvoltages and DC-link voltage. This allows on-line measurements without power cycling interruptions. Also, testing simultaneously several modules using a DC circuit requires a relatively simple test setup [34, 35]. In the contrary, higher current levels than the nominal are needed to create high ΔT_j values which are not appeared in real normal operation of the IGBT power modules. Moreover, the losses on the devices are produced only by their on-state resistance and the switching losses are neglected due to low switching frequency.

2.3.3 Failure criteria and limits

During PC tests, failure indicators are used to notify that the power module does not provide reliable operation anymore and is prior to breakdown. These are defined as:

- $V_{CE,sat}$ increment up to 5% or to 20% of the initial value for the same load conditions. An example is shown in Fig. 2.11. Although the limits are varied between manufacturers depending on the achieved measurement accuracy, the first considerable raise of $V_{CE,sat}$ indicates the upcoming failure of the DUT.

- Increase of R_{th} by 20% [17].

- Loss of any of the functionalities of the DUT such as the blocking voltage capability or the gate-emitter insulation capability (i.e. gate-emitter shorted) [17].

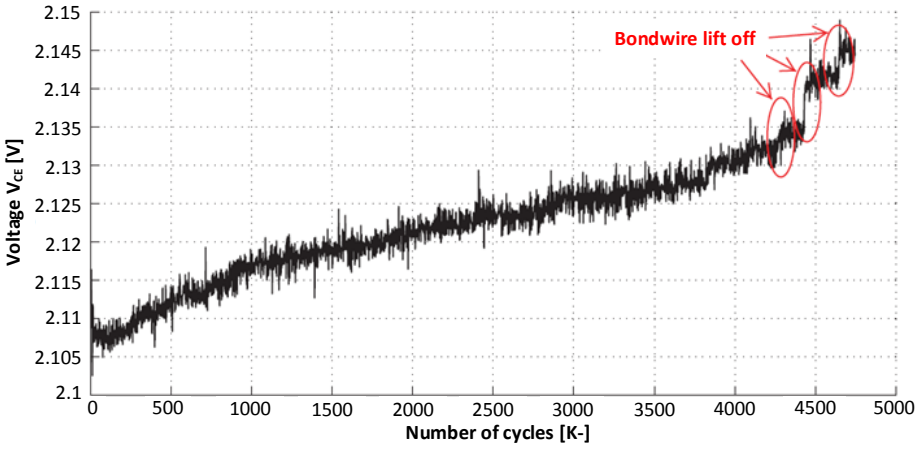


Figure 2.11. V_{CE} increment of 40mV after 4748 kcycles power cycling tests [36].

2.3.4 Main failure mechanisms triggered by power cycling

The purpose of power cycling tests is to stress the power devices in an accelerated way, wear out and degrade their performance by triggering certain failure mechanisms. The multilayer structure of the IGBT devices is affected seriously by the temperature variations. The mismatching in the CTE of the different used materials (plastic, silicon, copper, solder, Al) implies different expansion and contraction behaviour during the alternated temperatures. When the materials are inserted in the plastic deformation region, cracks are appeared between the joint interfaces [12]. In Table 2.1, the different CTEs are shown. It can be noticed, for example, that the CTE of aluminium is 10 times higher than CTE of silicone. The two most dominating failures appeared in IGBT modules are: 1) solder fatigue, 2) bond wires lift off [37].

Table 2.1. Coefficients of Thermal Expansions (CTEs) of the different material layers of an IGBT module

Coefficients of Thermal Expansion (CTEs)	
Si	$2.6 \cdot 10^{-6} K^{-1}$
Cu	$17.5 \cdot 10^{-6} K^{-1}$
Al	$23.5 \cdot 10^{-6} K^{-1}$
AlN	$4.7 \cdot 10^{-6} K^{-1}$
Al_2O_3	$6.8 \cdot 10^{-6} K^{-1}$
Si_3N_4	$2.7 \cdot 10^{-6} K^{-1}$
Mo	$5.1 \cdot 10^{-6} K^{-1}$

2.3.4.1 Solder fatigue

As previously explained, the solder material is necessary to join the chip to the DBC substrate layer. During thermal stress between the interconnecting materials, the solder experiences forces which result in cracks and holes across the surface. In Figure 2.12 the condition of solder between chip and DBC, DBC and baseplate is shown after PC tests. The solder degradation increases the thermal resistance of the IGBT and causes higher losses and, thus, higher operating chip temperatures. The solder between the chip and the substrate is responsible for the collector emitter voltage rise during PC. The higher temperatures accelerate the other main failure mechanism, the bond wire lift off.

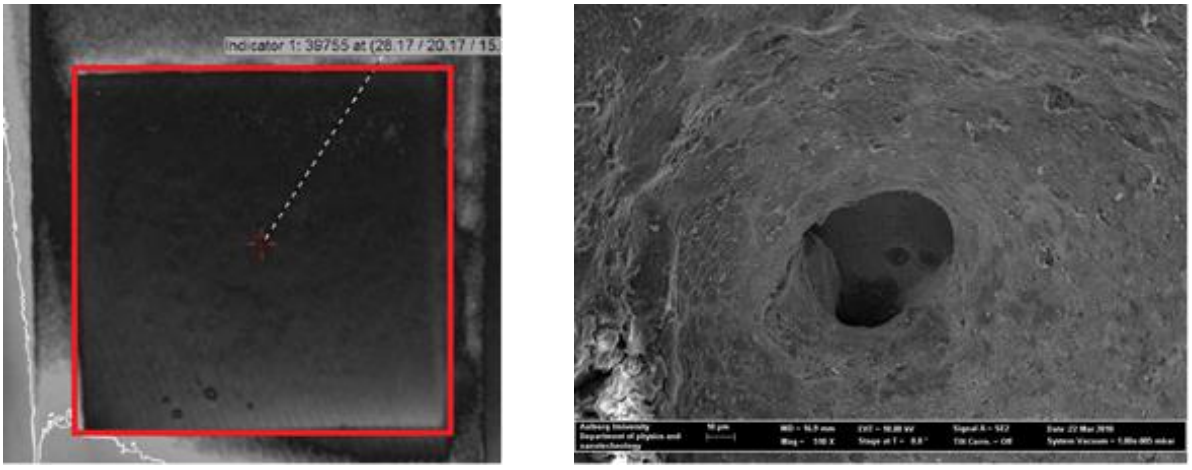


Figure 2.12. Solder joint fatigue produces holes after power cycling tests [36].

2.3.4.2 Bond wire lift-off

The bond wires are used in the IGBT power modules to interconnect the silicon chips. In most of the cases are made by aluminium and they are attached on the metallization layer above the chip surface. Stressing the IGBT module with temperature swings, fatigue and stress results in cracks on the heel or the toe of the bond leading finally to complete disconnection (bond lift off). This has a severe impact on the reliability of the IGBT module. It increases the ohmic resistance and the V_{CE} voltage, and also it changes the current distribution between the different chips inside the module stressing even more the remaining healthy bond wires. This avalanche effect reduces steeply the reliability performance of the device. In Figure 2.13 typical bond wire lifts off are shown.

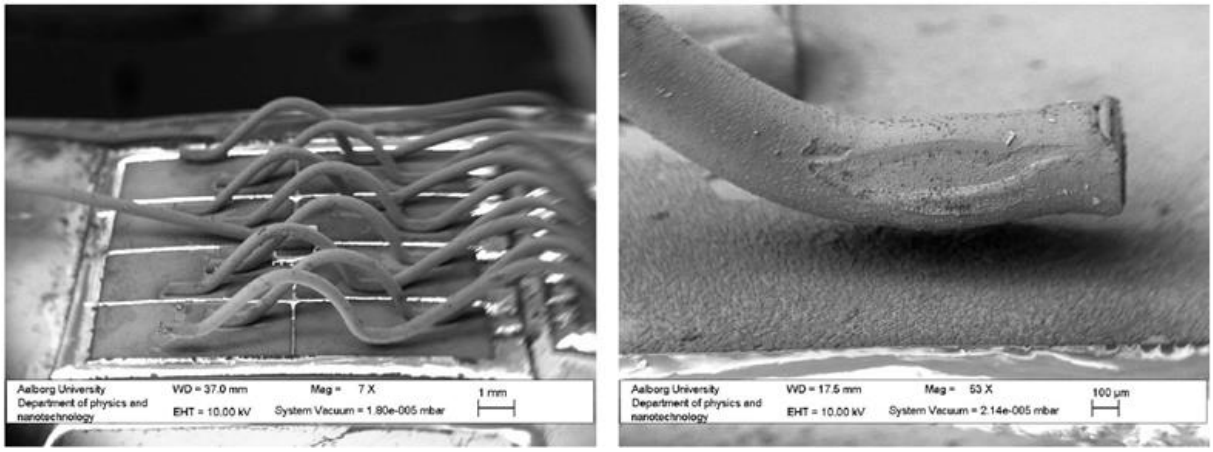


Figure 2.13. IGBTs bondwire lift-off images using Scanning Electron Microscope (SEM) [36].

Part II

Accelerated wear-out test setup

Analysis, design and implementation of the power-cycling test setup

3

In this chapter, the power cycling accelerated wear-out test setup, also known as Sven, is presented. Firstly, the device under test (DUT) is introduced and test specifications and description of power cycles are given. Afterwards, the entire implementation of the setup, both from a hardware and software point of view, is depicted.

3.1 DUT: Infineon PrimePACK3 module and Danfoss ShowerPower

The devices under test (DUT) in the current work are the PrimePACK™3 IGBT high power modules (FF1000R17IE4) manufactured by Infineon. These modules are standard components in many high power applications such as wind turbines, motor drives and high power converters. As shown in Fig. 3.1, each module consists of two IGBT switches with anti-parallel diodes forming a half bridge. The basic electrical and thermal parameters are given in Table 3.1. Also, the I-V characteristic for different junction temperatures and the thermal impedance of the DUT are presented, respectively, in Fig. 3.2(a) and Fig. 3.2(b). More detailed information is provided in Appendix B (DUT datasheet). It also should be noted that only the IGBTs parameters are under concern as the diode is not worn-out. In addition, only the conduction losses are taken into account due to the low switching frequency used in this PC setup, a fact that allows the switching losses to be neglected.

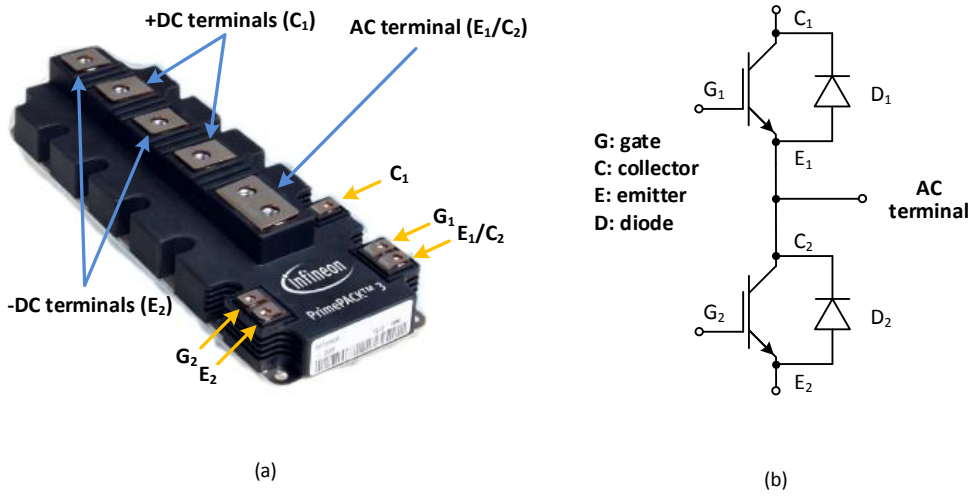


Figure 3.1. Infineon PrimePACK™3 IGBT module: (a) Pinout, (b) Equivalent electrical diagram

Table 3.1. Main electrical and thermal parameters of FF1000R17IE4 IGBT modules

Electrical Parameters			
Parameter	**Test Conditions**	**Symbol**	**Value**
Collector-emitter voltage	-	V_{CES}	1700 V
Continuous DC collector current	$T_C = 100°C$, $T_{vj} = 175°C$	$I_{C,nom}$	1000 A
Gate-emitter voltage (peak)	-	V_{GES}	± 20 V
Power dissipation (max)	$T_C = 25°C$, $T_{vj} = 175°C$	P_{tot}	6.25 kW
Collector-emitter saturation voltage	$I_C = 1000A$, $V_{GE} = 15V$, $T_{vj} = 25°C$		2 V (typ.)
	$I_C = 1000A$, $V_{GE} = 15V$, $T_{vj} = 125°C$		2.35 V (typ.)
	$I_C = 1000A$, $V_{GE} = 15V$, $T_{vj} = 150°C$		2.45 V (typ.)
Thermal Parameters			
Maximum Junction Temperature	-	T_{vj}	$175°C$
Thermal resistance, junction to case	per IGBT	$R_{th,JC}$	24 K/kW

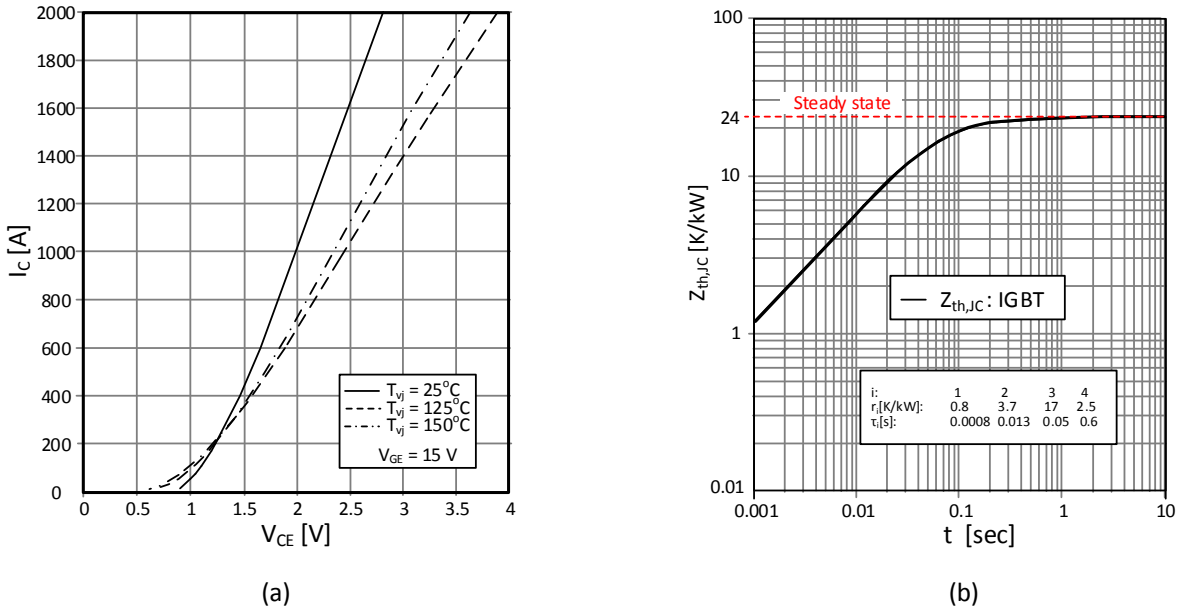


Figure 3.2. Infineon PrimePACK™3 IGBT module: (a) I-V characteristic, (b) Thermal impedance curve

The DUTs are cooled down by the ShowerPower® cooling technology produced by Danfoss A/S. According to [26], this type of cooling device provides a more efficient and lower cost solution compared to the conventional cold plates (closed coolers) which provide a cold surface by means of a metal plate, usually aluminum, which is penetrated by copper tubes. This method implies the use of thermal interface material (often thermal grease) between the cooling surface and the power modules base plate. The thermal grease has low thermal conductivity ($\sim 0.6\ W/(m \cdot K)$) which degrades the cooling efficiency. For this reason, open coolers are implemented where water comes into direct contact with the baseplate. More than this, Danfoss ShowerPower® has managed by only one plastic structure to achieve parallel cooling with meandering channels taking out the heat fast before it is reflected back to the module. This concept is shown in Fig. 3.3 and it eliminates the inhomogeneous cooling and temperature gradients at the baseplate which are major issues in liquid cooling systems.

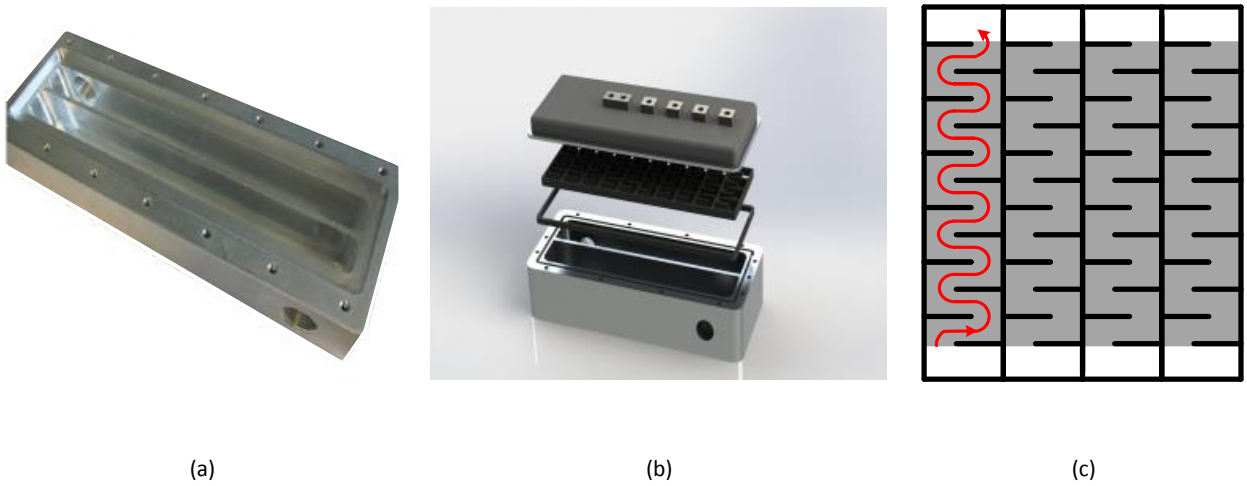


Figure 3.3. Danfoss ShowerPower®: (a) Picture, (b) 3D picture of the assembled parts (c) Water flow in a single cell.

3.2 Power cycling characteristics and test setup specifications

A power cycling (PC) test setup is designed in order to wear-out the IGBT power modules by loading them during a certain number of cycles (N_f) until failure is reached. Based on the guidelines given by the literature and the standards presented in Chapter 2, it can be concluded that the main factors to vary the applied stress are the temperature swing ΔT_j which is adjusted by the on and off times of the loading cycles (t_{on} and t_{off}), current (I_C) and power (P_d). The wear-out process can be accelerated by means of increasing the junction temperature swing amplitude and heating up the device during longer times.

Therefore, the initial design specifications that the PC test setup should fulfill are:

- To provide a loading capability that can generate a junction temperature variation (ΔT_j) on the DUT(s) which ranges from 30°C to 150 °C.
- To provide the ability of adjusting amplitude and mean value of the ΔT_j cycles by means of both the electrical and cooling system. In addition, a maximum junction temperature of 175 °C should be achievable.
- To provide the ability of adjusting the on and off times (t_{on} and t_{off}) according to the requirements of the loading cycle.
- To provide a flexible structure for the DUT(s) so that several DUTs can be simultaneously tested.
- To provide constant monitoring of the DUT(s) during the entire wear-out process so that a more complete assessment of the lifetime and its degradation factors can be performed.

These initial design specifications and their feasibility are analyzed in the following sections.

Their implementation will be presented in Section 3.3.

3.2.1 Loading capacity for generation of junction temperature swings

The accelerated wear-out of IGBT module for lifetime assessment is achieved by increasing the amplitude of the ΔT_j compared to normal operating conditions. The junction temperature swing is determined according to the power dissipation losses and the thermal impedance (rearranging Eq. 2.13, Section 2.2.3):

$$\Delta T_j = P_d \cdot Z_{th} \quad [K/W] \tag{3.1}$$

Besides modifying the cooling water flow rate, the electrical parameter to adjust the junction temperature swing is the power dissipation step applied to the DUT. This means that the test setup should provide enough current to obtain the desired power dissipation and consequent ΔT_j.

To analytically calculate the necessary current level, the power pulse duration is assumed to be long enough to reach steady-state conditions and, therefore, the thermal resistance $R_{th,j-c} = 24\ K/kW$ given in the datasheet of the DUT [38] is used. Further details about the pulse duration are given in Section 3.2.2.

According to the DUT datasheet, its maximum junction temperature is 175°C at a case temperature of 25°C ($T_{vj,max} = 175°C$ @ $T_c = 25°C$), which means a ΔT_j of 150°C as stated in the initial design specifications.

The power dissipation losses needed to obtain that temperature swing can be calculated as,

$$P_d = \frac{\Delta T_j - c}{R_{th,j-c}} = \frac{150}{24} = 6,25kW \quad [kW] \tag{3.2}$$

The DUTs forward characteristics presented in Section 3.1 are given for the 3 different values of T_{vj} (25, 125 and 150°C). Since the V-I curve for 175°C is not given, $V_{CE,sat}$ is assumed to have a value around 3.9 V (maximum value of V_{CE} in the 150°C curve). In these conditions, the collector current yields as,

$$< i_C >= \frac{< P_d >}{< u_{CE,sat} >} = \frac{6250}{3.9} \approx 1600A \quad [A] \tag{3.3}$$

This analytical result can give an initial idea of the current level, however, it is a rough approximation since the value of $U_{CE,sat}$ at 175°C is not known.

Additionally, to validate the above calculation a model of the test setup is built in PLECS Blockset (MATLAB-Simulink environment) and is shown in Fig. 3.4a. This model includes the thermal description of the DUT which consists in the losses model (Fig. 3.4(b)) and the thermal impedance parameters obtained through the DUT's datasheet [38].

The simulated junction temperature swing for a current pulse of 1705A and 2 s of on-time can be observed in Figure 3.5.

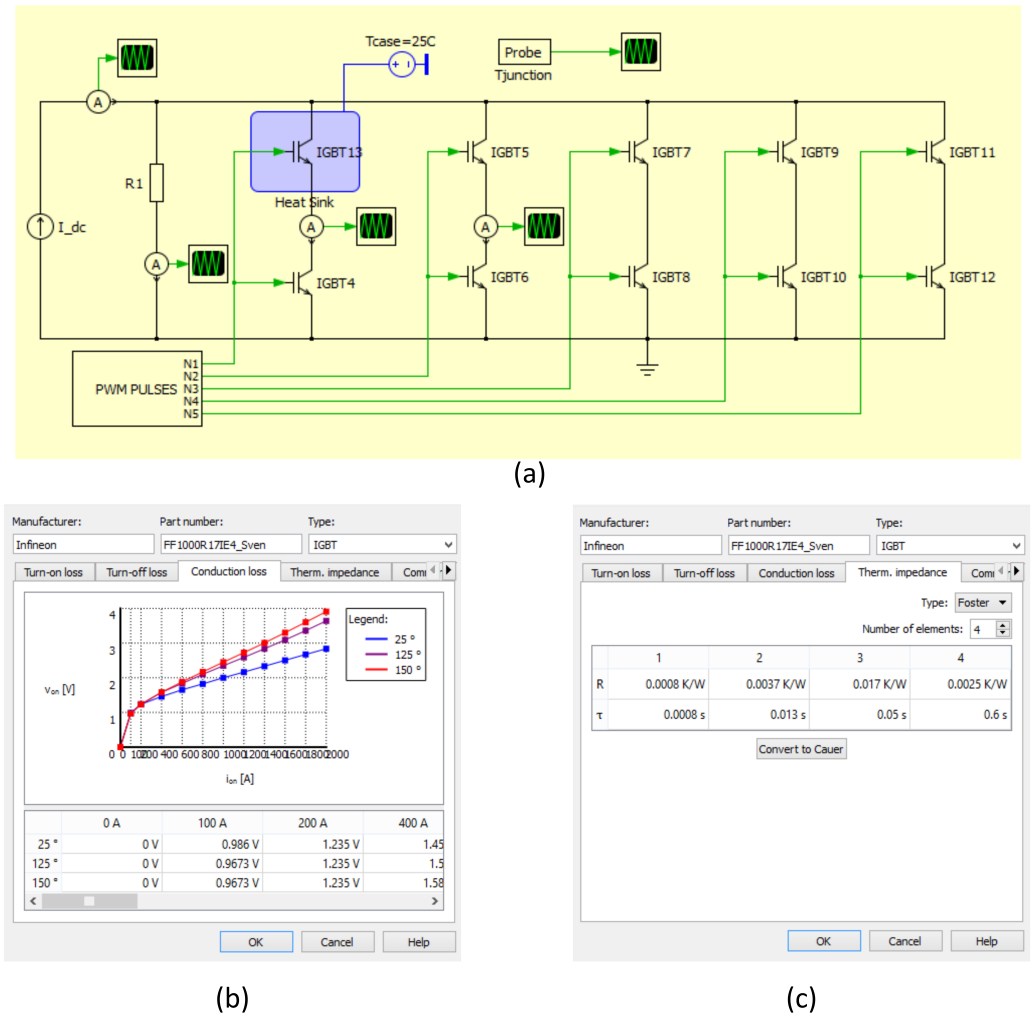


Figure 3.4. Simulation model of the PC test setup in PLECS Blockset®: (a) Circuit diagram, (b) Condution losses model based on datasheet I-V curves and (c) Thermal impedance model based on Foster parameters from datasheet.

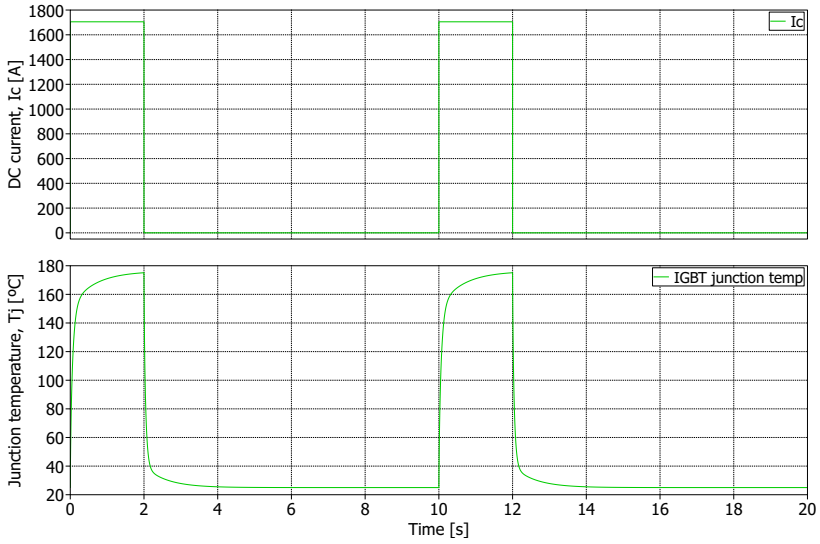


Figure 3.5. Simulated result of the junction temperature variation for the Infineon PrimePACK™3 IGBT module. Simulation model performed in PLECS Blockset®.

The simulated temperature varies between 25°C and 175°C which confirms the previous analysis but using a current of 1705A. Therefore, the necessary current to obtain a ΔT_j of 150°C (first design specification) is at least 1700A. However, it should be noted that the simulated ambient temperature is set to 25°C, whereas the temperature in the cooling water of the real system will be between 25 and 40°C depending on the cooling performance. This means that less current will be needed to obtain the same maximum junction temperature of 175°C (1610A in the simulated results).

In addition, as highlighted in Section 2.3.2, DC current pulses are used due to their advantages for measuring and simultaneous testing. To design a more flexible setup, which can provide similar levels of stress to devices with other characteristics, the power supply should be able to deliver DC current pulses from 0 to 2000 A (Table 3.2).

Table 3.2. Loading capability of the test setup according to the junction temperature swing

Loading capability of the test setup	
Temperature swing, ΔT_j	0 - 150°C
Supply current, I_c	0 - 2000 A

3.2.2 Duration of the on and off times

The duration of the on and off times determines the heating and cooling phases of the junction of the DUT. Longer on-time pulses generate higher temperature swings. These values should be adjusted in order to ensure that the desired maximum and minimum junction temperatures ($T_{vj,max}$ and $T_{vj,min}$) are reached. In addition, the cycle time is used to calculate the expected testing time for a specific lifetime of the DUT.

Generally, in the standards regarding PC test setups, the cycle period time covers a wide range (from a few seconds to minutes). Therefore, in order to design a flexible setup, the on and off times should be adjustable according to the user requirements (duty cycle and ΔT_j characteristics), as stated in the third design specification. In this test setup, the adjustment of the on and off times will be performed by means of controlling the pulses of the gate signals. This flexible control will be implemented in LabVIEW™ . Further details about the gate control are given in Section 3.3.2.

As an initial design criteria, it is desired that the junction temperature reaches steady-state conditions. Based on the information provided in Section 2.2.3 and the thermal impedance curve of the DUT (Fig. 2.9), the steady-state conditions are reached for pulse lengths greater than 1s. Additionally, similar test setups carried out in the industry present a loading cycle with a 20% duty cycle [39].

The initial testing conditions are summarized in Table 3.3.

Table 3.3. On and off times of the input power pulse

Loading cycle test conditions	
Cycle time, t_{cyc}	10 s
duty cycle, d	20%
On time, t_{on}	2 s
Off time, t_{off}	8 s

The test setup should be able to apply different testing conditions regarding duty cycle and on and off times.

3.2.3 Test setup topology

The circuit topology suggested by the standards on power cycling (IEC 60747-9) is depicted in Fig. 3.6.

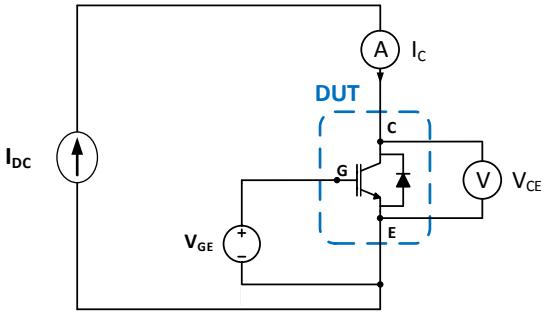


Figure 3.6. Equivalent diagram of the circuit topology suggested by the standards on power cycling [40].

As can be observed, the main objective of this topology is to supply a current which can load the DUT during a certain time and generate power dissipation losses. However, an external switch or an extra string in parallel for an alternative current path would be needed in order to shut down or to reconduct the loading current during the cooling phase of the DUT. Moreover, if it is desired to test a higher number of IGBT modules, as in this setup, this topology does not offer a wide flexibility.

Considering the above-mentioned, a first approach would be to connect in series the different DUTs so that a larger number of devices can be aged. Nonetheless, as previously, this topology will require an external switch or extra leg for the cooling time. Furthermore, the latter will limit the duty cycle to 50%.

Therefore, combining the idea of an extra control leg which works as current free-wheel path, and taking into account the suggested number of DUTs (10 DUTs, Section 3.1) and operating conditions for the pulse duration (2s heating, Section 3.2.2), the circuit topology illustrated in Fig. 3.7 has been designed.

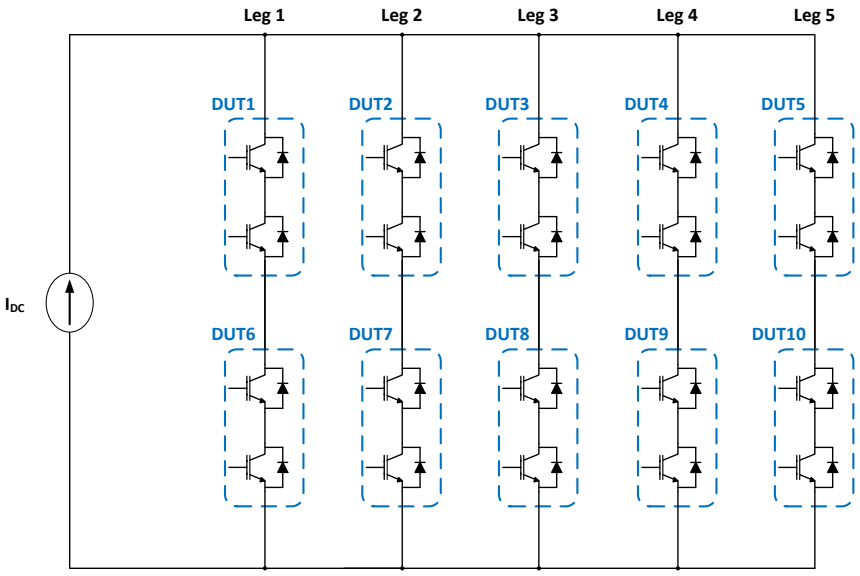
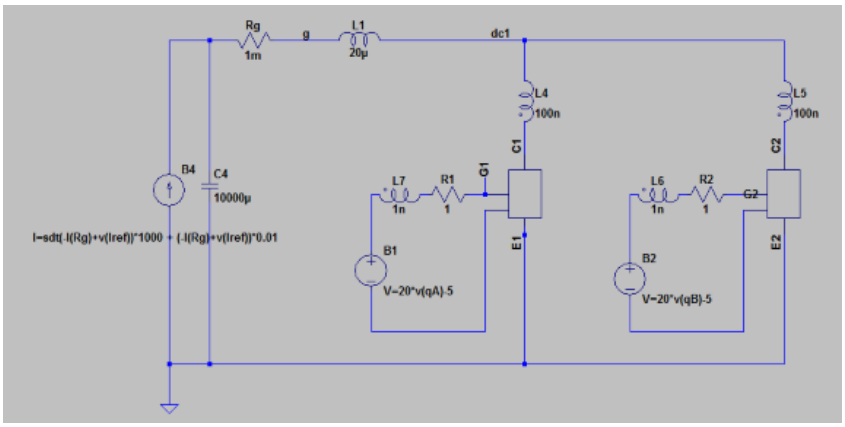


Figure 3.7. Equivalent diagram of the circuit topology applied in Sven.

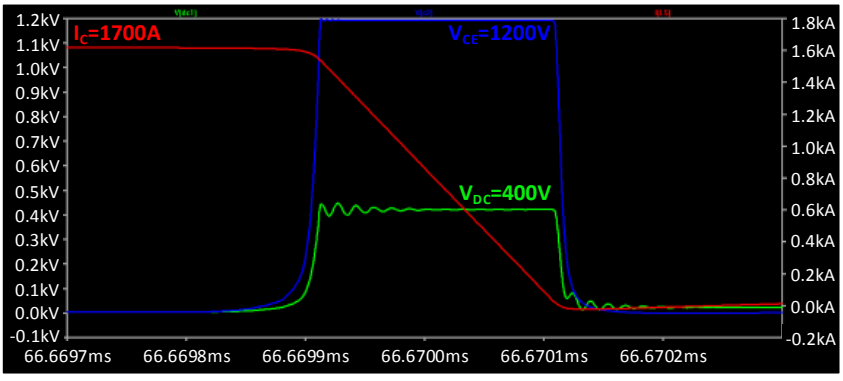
This circuit topology allows 10 IGBT modules to be simultaneously tested (20 IGBTs, 240 IGBT and Diode DIEs). In addition, it can be extended to more DUTs by interleaving a higher number of strings. The operating principle is that the power supply will provide constant current and, all the IGBTs in one leg will be turned on at the same time, short-circuiting its output. It is designed in order to not disconnect the current during the cooling periods, which is done by shifting the circulating current from one leg to the other, so all the DUTs are loaded with identical power cycle. This control is performed by means of the gate signal pulses (Section 3.3.2). Another great benefit of this topology is that it requires low voltage (4x IGBT on-state voltage), which presents advantages for the design of both the power supply and the measurement system.

On the other hand, a potential problem of this test system is the appearance of overvoltages due to parasitic inductances in the DC-side circuitry. Because of the high current level (2000A), the change in current (di/dt) seen by each leg will be very large and, therefore, a small value of stray inductance (range of nH) will represent a large overvoltage. Even though the topology has been designed to have a small DC-link voltage, this overvoltage can be hazardous for the measuring system.

To validate the proper operation of the topology and to quantify the potential overvoltages on the IGBTs, the circuit topology has been simulated in LTspice with an input current of 1700A and a value of stray inductance of 100 nH. The simulated results are shown in Fig. 3.8.



(a)



(b)

Figure 3.8. Simulated results of the overvoltage event at the IGBT turn off obtained through LTspice.

The simulated voltage, measured between collector and emitter terminals of the IGBT module, results in an overvoltage of 1200 V. As a consequence, special attention should be given to the design of the DC-side circuitry, aiming for a low-inductance connection, and to the protection of the measuring system and the IGBT itself.

3.2.4 Overview of the cooling system

The cooling system plays a crucial role for the proper evacuation of the generated heat inside the DUTs ($\approx$ 4kW). Moreover, the cooling system must be designed in order to provide flexibility considering the number of DUTs and different operating conditions. The design of the cooling system has been realized by Henrik Sørensen (AAU Associate Professor collaborating in the IEPE project).

An overview of the cooling system designed for Sven is depicted in Fig. 3.9.

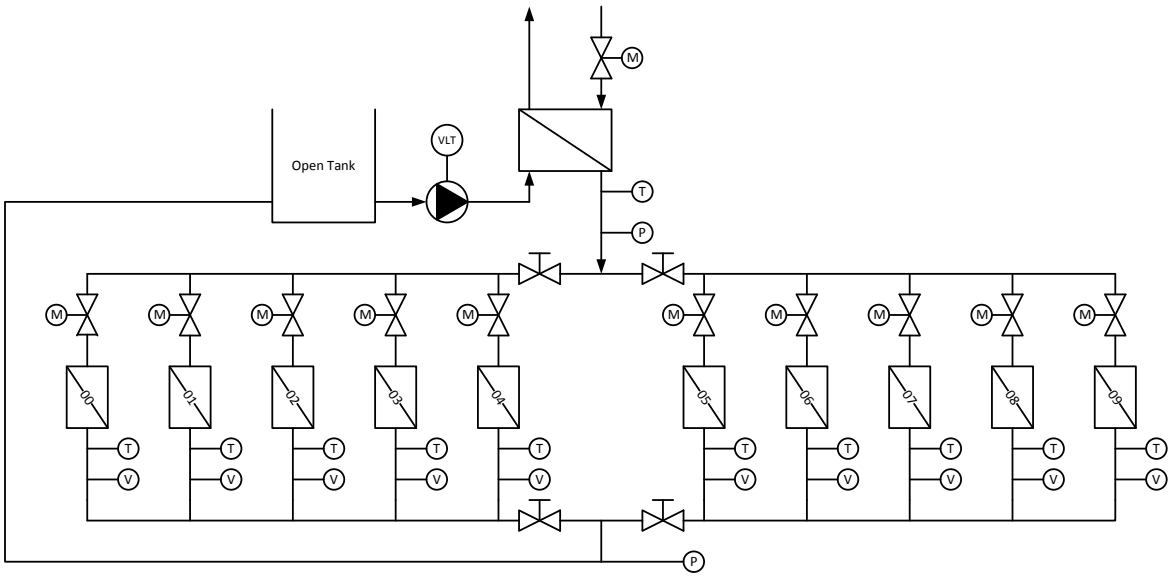


Figure 3.9. Layout of the cooling system designed for Sven

The cooling of this test setup is a non-pressurized system with an open water tank connected to the output manifold and to the heat exchanger. The water tank has a volume of 90 liters of coolant, which is a mix of 33% glycol and 66% pure water, and provides a large capacity to avoid a fast heating of the system. The flow of the system is provided by a Grundfoss pump which is controlled by a 7.6 kVA frequency converter (Danfoss VLT). The heat exchanger is connected to the Central Cooling System (CCS) of the Department of Energy Technology, and it has an actuator which can be adjusted to modify the water flow coming from the CCS.

As can observed in the above figure, the cooling system has been designed in order to provide individual control of the flow in each of the devices. This is performed by means of check valves installed in the inlet manifold, which currently are manually regulated. Therefore, in addition to the electrical power dissipation, it is possible to adjust the junction temperature swing inside the DUTs ΔT_vj by changing each flow rate. Moreover, each section of 5 DUTs (0 to 4, 5 to 9) has its own main valves, fact that allows to operate it independently in case of testing only 1 group of DUTs.

Regarding the necessary measurements for a complete monitoring of the cooling system, these are:

- Temperature and flow in the outlet of each of the DUTs.
- Inlet manifold temperature.
- Inlet and outlet pressures at the two manifolds.

The control of the cooling system, as well as the acquisition and monitoring of the thermal quantities, will be performed in the NI LabVIEW platform.

3.2.5 Monitoring and control of the DUTs

In order to meet the test setup specifications, a reliable, adequate and efficient system for control and monitoring should be designed and implemented. The control system refers to the pulse generation for switching the IGBT modules and the control of the cooling. The monitoring system is needed to provide continuous supervision and storage of all the electrical and thermal quantities which are necessary to assess the condition of the devices. Specifically, the purpose and the characteristics of the measurements and the control parameters, are given in Table 3.4 from both the electrical and cooling point of view.

Table 3.4. Control and monitoring system parameters and their characteristics

Monitoring System		
Parameters	**Purpose**	**Observations**
Collector-emitter voltage (V_{CE})	Evaluate wearing-out Estimate junction temperature	All measurements have 10Hz sampling
Gate-emitter voltage (V_{GE})	Check the switching condition of the devices	frequency and they are differential.
Collector current (I_C)	Determine load Estimate junction temperature	
Pressure (P)	Cooling performance and safety indicator	-
Flow (Q)	Cooling performance and determination the ShowerPower thermal impedance	-
Temperature (T)	Determination of water tempature	-
Control System		
Parameters	**Purpose**	**Observations**
PWM generation	Switch the IGBTs according to user's needs	Allows different string configurations and times
Pump speed	Control flow of the coolant	-

To realize such a control and monitoring system that is able to run reliable, without interruptions in a 24/7 basis, a certain system configuration has been built (see Fig. 3.10) and it consists of:

- Host computer which has Windows operating system (OS) and provides the graphical user interface (GUI). The software design has been made using NI LabVIEW which is a graphical programing platform from National Instruments.
- Real Time (RT) OS dedicated to execute only the tasks related with the measurement, the control of the module and the data logging functionalities. In general, a RTOS is necessary when tasks need to be done in precise timing. A general purpose OS (e.g. Windows) is not accepted in this case because it runs many different tasks at the same time and delay or crash is always possible.
- NI 9144 EtherCAT RIO chassis which supports master-slave expansion configuration with another chassis while keeping the determinism and synchronization between them. In addition, this chassis offers FPGA (Field Programmable Gate Array) option that allows hardware-level logic implementation onboard. FPGA is used in time critical tasks and for this reason the PWM signals have been implemented on this.
- NI I/O modules that contain built-in signal conditioning for a variety of I/O types such as analog or digital input/outputs, thermocouple inputs etc.

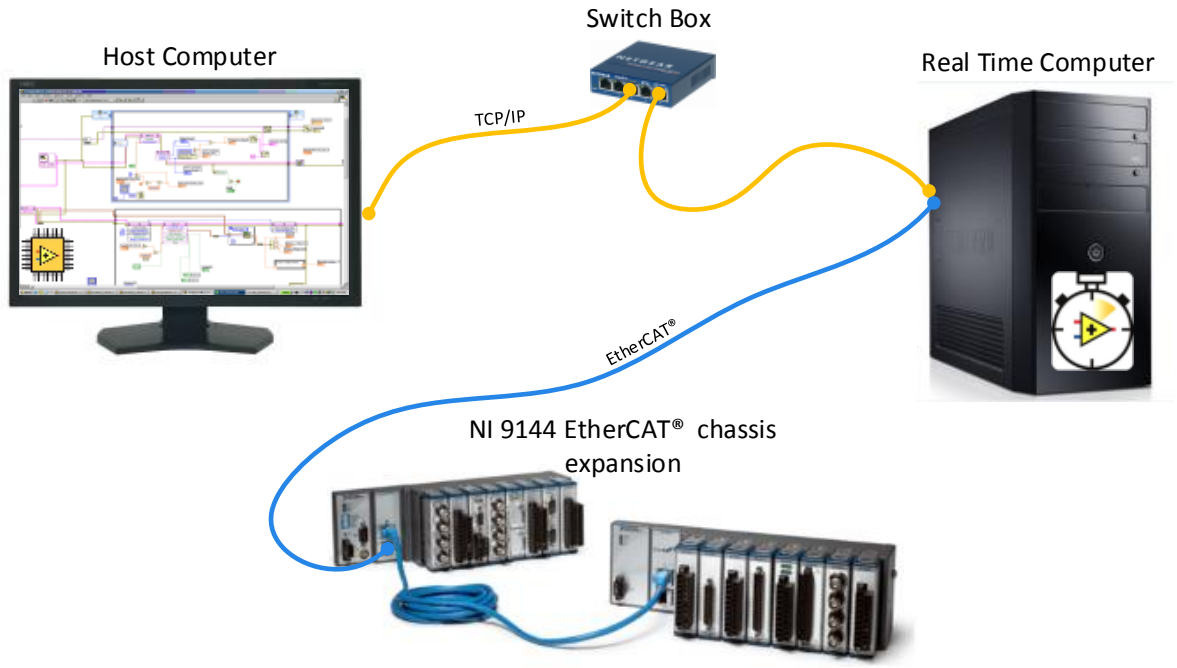


Figure 3.10. Hardware setup architecture using Real time target and two NI 9144 EtherCat expansion chassis

The software architecture of the control and monitor system is shown in Fig. 3.11. It is implemented in hybrid mode that means both Scan Engine and FPGA interface are used at the same time, one for the data acquisition and logging and the other for the pulse generation respectively. Three types of VIs (LabVIEW code) are used: one host VI, RT target VI and FPGA VI. The host VI allows the user to communicate with the RT target by sending commands and also provides the interface for the data to be displayed on the monitor. The RT VI is responsible to receive and send data to the I/O modules and store the measurements. Finally, FPGA VI executes the code to generate the pulses for the IGBTs.

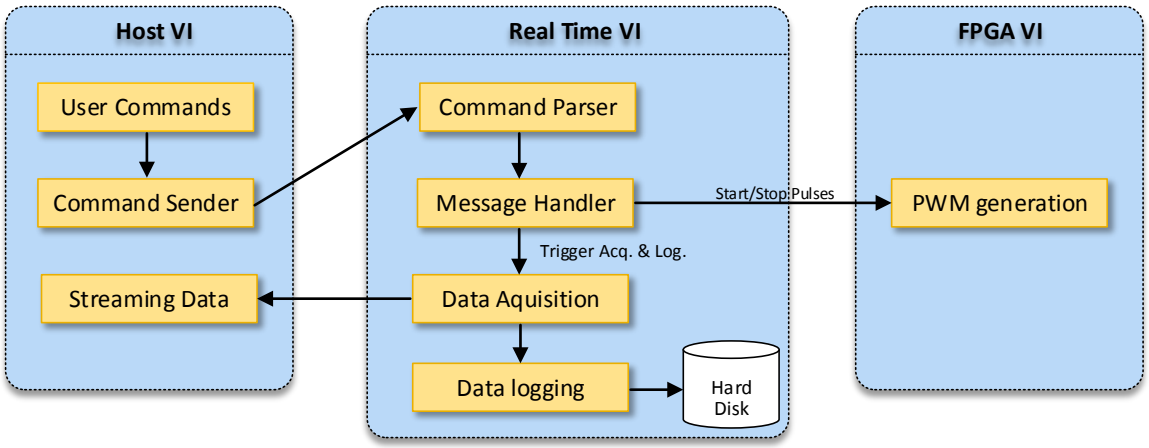


Figure 3.11. Software architecture of control and monitor system, implemented with NI LabVIEW

3.2.6 Expected number of cycles to failure

In order to have an initial idea, a rough calculation of the expected number of cycles to failure can be performed based on [22, 41]:

- In the test setup developed in [22], a $\Delta T_j = 30°C$ was applied ($T_j = 110°C$, $T_c = 80°C$, $T_{j,mean} = 95°C$) and the DUT failed after 2000K cycles (approx. 3 weeks)
- In the LESIT-project [41], several modules were tested at different ΔT_j (30 to 80$°C$) and different $T_{j,mean}$ (60, 80 and 100$°C$). The results can be observed in Fig. 3.12.

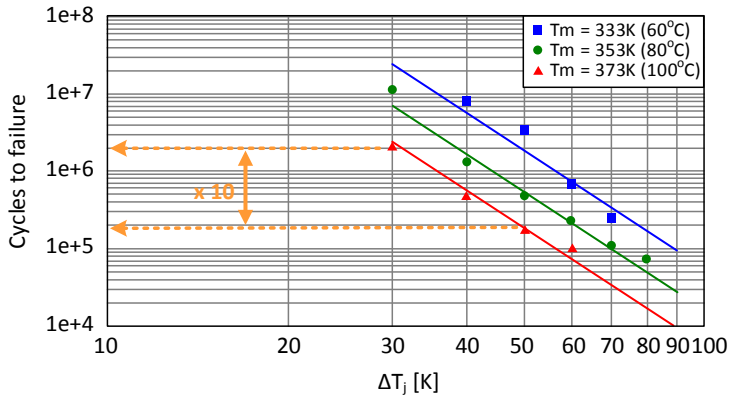


Figure 3.12. Results of the LESIT project regarding the number of cycles to failure for different ΔT_j and different $T_{j,mean}$ [41]

The tendency observed in Fig. 3.12 shows that the number of cycles to failure is dramatically reduced when increasing the values of ΔT_j and $T_{j,mean}$. For instance, the N_f is reduced by a factor of 10 from a ΔT_j of 30$°C$ to a ΔT_j of 50$°C$. This test setup is designed to provide ΔT_j up to 150$°C$. Therefore, if the same DUT under a ΔT_j of 30$°C$ was wore out in 3 weeks [22], and now it is intended to apply a ΔT_j at least 3 times larger (90$°C$), roughly, the number of cycles is expected to be reduced by at least a factor of 3 (1 week).

3.2.7 Summary of test setup design specifications

According to the analysis performed in the previous sections, the accelerated wear-out test setup will have the following specifications in Table 3.5.

Table 3.5. Design specifications of the accelerated wear-out test setup, also known as Sven

Design specifications of Sven		
Type of DUT	(fixed)	PrimePACK™3 module
Max. No. of DUTs	(adjustable)	10
ΔT_j	(adjustable)	0 - 150°C
Water temperature, T_w	(adjustable)	25 - 80°C (constant)
DC current, I_c	(adjustable)	0 - 2000 A
On-time, t_{on}	(adjustable)	2 s (d=0.2)
Off-time, t_{off}	(adjustable)	8s (d=0.2)
Gate voltage, V_{GE}	(fixed)	+15/-10V

3.3 Hardware and software implementation

This section presents the entire hardware and software implementation, describing the details of the different parts that the system consists in. An overview diagram of the PC accelerated wear-out test setup for IGBT modules (SVEN) is depicted in Fig. 3.13. A picture of the test setup implementation has been provided in Appendix A.

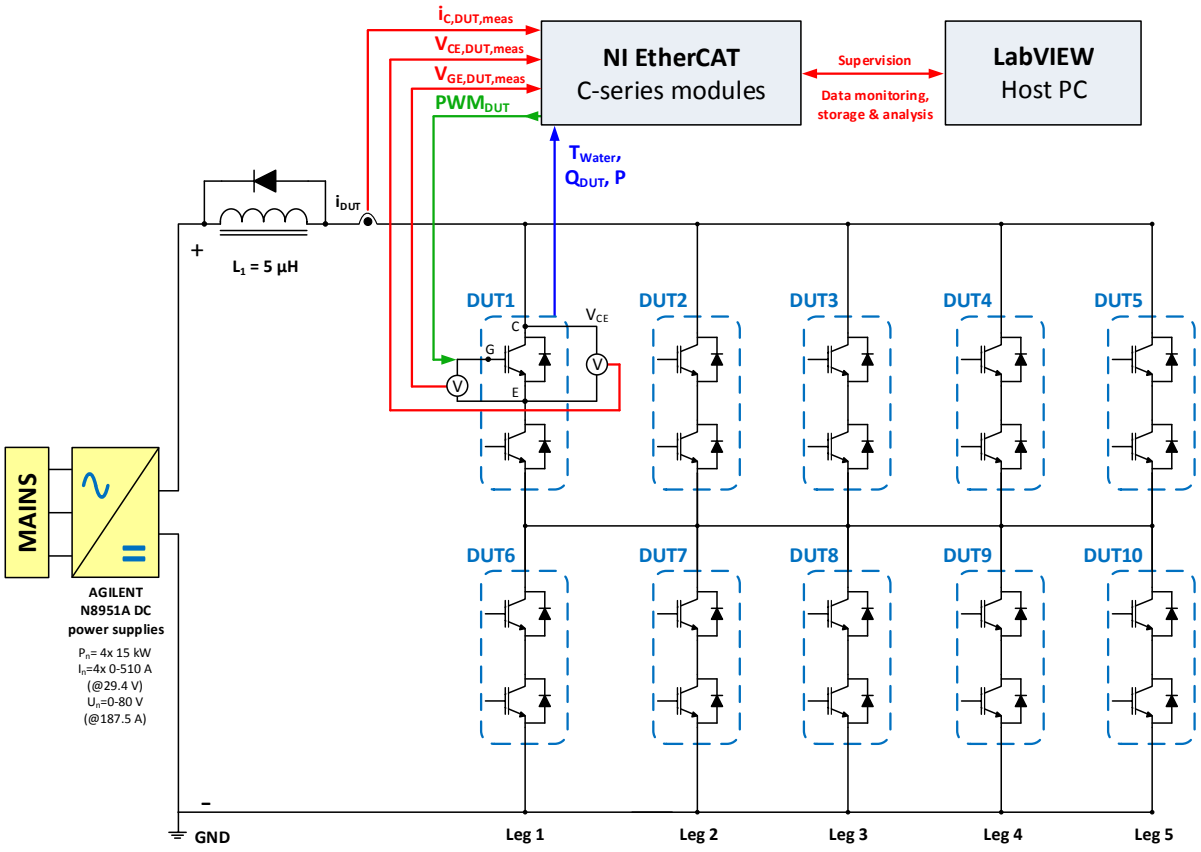


Figure 3.13. Simplified diagram of the PC accelerated wear-out test setup for IGBT modules (Sven).

3.3.1 Power supply circuit

The implementation of the power supply circuit consisting of the DC power supplies, the DC-link inductor and the rest of DC-side circuitry (laminated and flexible busbars) is introduced in the following subsections.

3.3.1.1 DC power supplies

DC current needs are covered by 4 DC power supplies which are connected in parallel. The available Master-Slave configuration allows full control only by one supply and using the LAN connection, control can be achieved by the users PC. A picture of the power supplies placed in the Rittal cabinet can be seen in Fig. 3.14a. All necessary specifications of the power supplies are given in Fig. 3.14b.

(a)

DC power supply	
Model	Agilent N8951A
Power	15 kW
Current range	0-520 A
Voltage range	0-82 V
Over-voltage protection	0-88 V

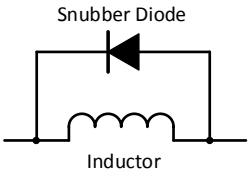
(b)

Figure 3.14. DC power supplies: (a) Picture of the 4 DC supplies in the Rittal cabinet, (b) Specifications of each of the DC power supplies.

3.3.1.2 Decoupling inductor and snubber diode

A 3-phase inductor (Fig. 3.15a, 1000A RMS / 0.01 mH per phase) is used, connecting two phases in parallel which gives an equivalent inductance of $5\mu H$. As shown in Fig. 3.13, the inductor is placed in series at the positive terminal of the DC supplies. With such high inductance is aimed to form a current source that provides constantly the needed current no matter the switching events at the IGBT modules. In this way, the rapid changes in case of high di/dt and dV/dt during IGBTs turn on and off respectively, are prevented to be seen from the supplies. Thus, decoupling the supplies from the rest of the circuit leads to safer operation of such expensive equipment.

(a)



(b)

Figure 3.15. The three phase reactor used as DC decoupling inductor: (a) Picture, (b) Equivalent circuit with snubber diode.

Moreover, in case of an accidental open circuit, for example due to breakdown of a module or for any other reason, the stored energy in the inductor should be dissipated safely. Therefore, a snubber diode is added to provide an alternative current path and force the energy to be dissipated by the forward resistance of the diode and the resistance of the inductor itself.

3.3.1.3 Laminated busbars

Overview

Common issue in high power circuits is the appearance of DC bus overvoltages and voltage spikes across the switching semiconductors. Especially in new generation devices, where fast commutation is applied together with high current levels, the transient voltage spikes are magnified and if these exceed the blocking voltage ratings of the devices, they can lead to damage. The presence of overvoltages when high di/dt occurs, is caused by the stray inductance in the commutation loop of the circuit ($V_L = L_p \cdot \frac{di}{dt}$). Also stray inductance slows down the switching events increasing the losses [42].

One traditional solution to minimize the voltage spikes is to use snubber capacitors which conduct the transient current and protect both DC link and devices. Moreover, active gate control technique is often applied to modify dynamically the switch off behaviour of the semiconductor device and reduce the effects of high di/dt (see Section 3.3.2). Another, approach is to use laminated bus bars which can provide the desired low parasitic inductance and high capacitance. This helps to keep the switching overshoots inside the safe limits. At the same time the capacitance of the bus bars acts in the same way as a snubber capacitor and also enhances the noise attenuation [43].

Laminated bus bars are constructed, in principle, by two parallel metal plates, with a dielectric sheet layer placed between them. Conductor materials are copper or aluminum and common dielectrics materials are Mylar, Kapton, Teonex etc. which provide insulation between the conduction parts. This structure allows to minimize the current loop by placing the $+DC$ and $-DC$ as close as possible to one each other. Thus, the mutual inductance is cancelled when parallel current paths appear at the terminals of the device. Important factors in laminated bus bar assembly are the width (w), length (l) and thickness (t) of the plates as well as the distance (d) between them which is determined by the thickness of the insulation material. Larger width and smaller thickness reduces the stray inductance (L_{eq}) and together with a thin insulator the capacitance (C_{eq}) increases. Also, conductance (G_{eq}) and resistance (R_{eq}) should be eliminated. The basic structure and the equivalent circuit of a laminated bus bar are shown in Fig. 3.16 [44].

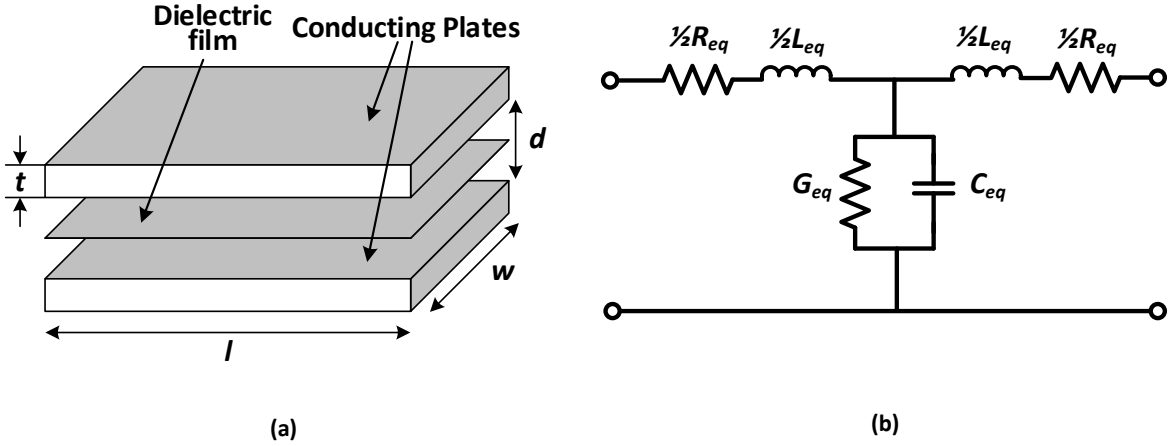


Figure 3.16. (a) Basic laminated bus bar construction (b) Electrical equivalent bus bar circuit with lumped parameters

However, analytical calculations to determine the parameters of the bus bars are not straightforward because these are dependent on the physical layout (e.g. commutation loop length, dimensions, holes, terminals) and the non-uniform current distribution. In this case the parameters can be estimated by experiments or by using Finite Element Analysis (FEA).

Implementation

In this setup, two laminated bus bar assemblies have been constructed. Copper plates have been chosen due to higher conductivity than aluminum. It is considered that copper has current ampacity of 2 A/mm^2 approximately. This depends also on the allowable temperature rise of the equipment. In this case the maximum temperature have set at 105°C. Mylar is the dielectric material between the plates providing insulation. Dimensions and material properties of copper plates and Mylar are given in Table 3.6.

Table 3.6. Dimensions of copper plates and Mylar used for the assembly of the laminated busbars

	Thickness (t)	Width (w)	Length (l)	Price
Copper plates	3 mm	min. 250 mm - max. 650 mm	1200 mm	20000 Kr
	Thickness (d)	Max. Temperature (T)	Dielectric strength	
Mylar	50 μm	150°C	7 kV	

The overall structure is presented in Fig. 3.17. The dimensions of the plates have been determined by targeting DC current handling capability of 2000 A and the shape was resulted from design constrains (cooling, frame size, electrical connections etc.) and easy access to the IGBT modules.

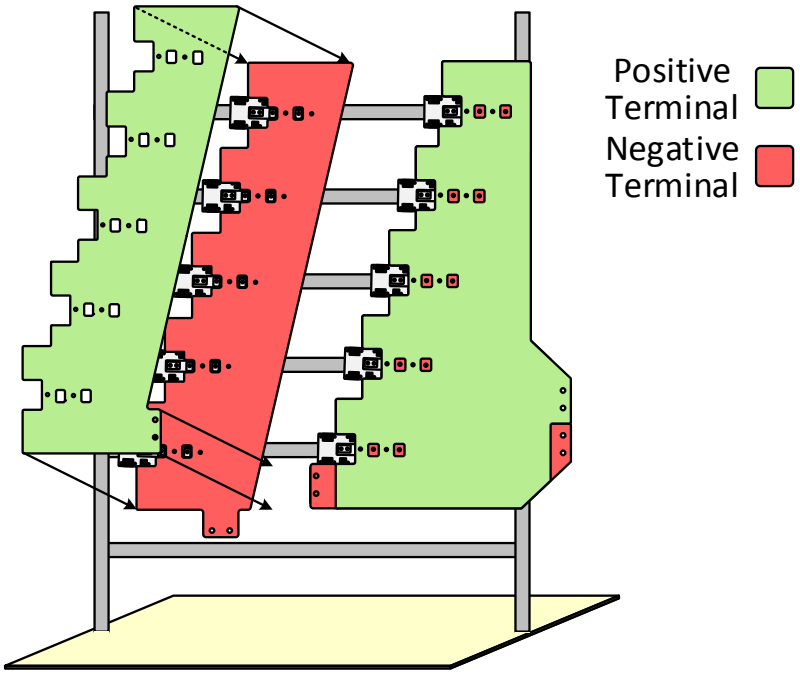


Figure 3.17. Laminated busbars mounted on the frame: (a) Sketch representation, (b) Actual implementation.

However, it has some disadvantages and a more optimized designed need to be done in the future. Despite its high electrical performance, copper is a heavy and expensive material. Thus, a more compact structure is necessary and it will be cheaper and convenient to handle when a power module

needs to be replaced. A new idea is suggested in Fig. 3.18 which is a three layer laminated bus bar with a middle layer working as the connection between two power modules in series.

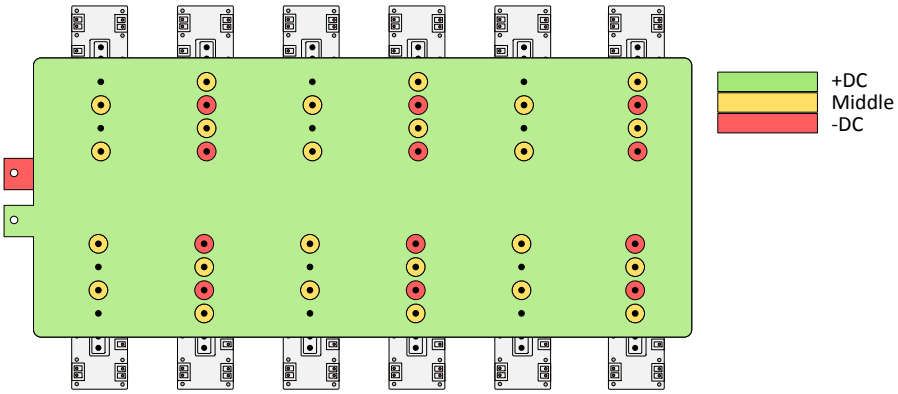


Figure 3.18. Suggestion for a new design of the laminated busbars consisting of 3 layers.

3.3.1.4 Flexible and rigid busbars

The interconnections between the power supplies, the inductor and the laminated bus bars have been made by flat flexible cables or rigid bus bars. Particularly, flat flexible copper cables by CUBIC form the DC circuitry for both positive and negative sides. In order to ensure that these can handle up to 2000 A in continuous operation without exceeding their maximum allowable temperature of $105°C$, 4 of them (FB240) were used in parallel for all the circuit sections considering that a single one can carry 495 A with 65 degrees temperature rise (Fig.3.19a). In order to connect the power supplies in parallel avoiding thick and heavy cables which could lead to mechanical stress at the terminals of the supplies, the solution of rectangular copper bars was preferred. Again, the dimensions were chosen according to the current capacity of the copper resulting in a cross section area of $50mm \times 20mm$ as shown in (Fig.3.19b). The flexible busbars are supported by a horizontal metal backing (Fig.3.19b).

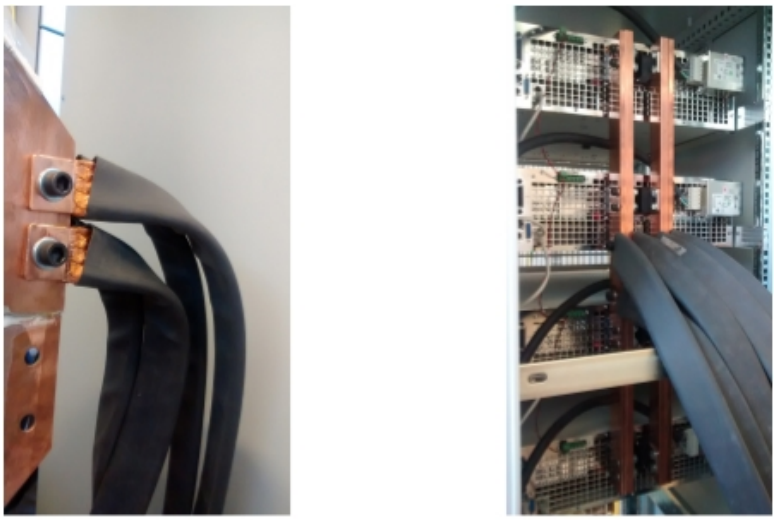


Figure 3.19. (a) Flexible copper cables assembly, (b) Parallel connection of DC supplies with rectangular copper bars.

3.3.2 Gate signals control

Based on the design specifications given in Section 3.2 and the topology of the system presented in Section 3.2.3, the design criteria that the gate signals control must fulfill are summarized as:

- **Adjustable on and off times.**
  One of the main requirements in PC tests is the on and off times (heating and cooling phases of the device), therefore, it is crucial to provide the capability of adjusting these times according to the test requirements. These values will be adjusted by means of software in offline conditions.

- **Overlapping time between pulses.**
  The design of the gate pulses should take into account the implementation of an adjustable overlapping time between them. As explained in Section 3.2.3, the implementation of this overlapping time is due to the overvoltages that can occurr when an IGBT is turned off with a very high di/dt in the presence of parasitic inductance. The overlapping time between pulses aims to reduce the overvoltage by sharing the current between two legs and, therefore, reduce the di/dt.

- **Flexibility regarding the number of paralleled active strings.**
  Since the system should be operated in different modes, having a higher or lower number of paralleled strings, the gate pulses should be adjusted according to the test requirements. This also means that the duty cycle (or similarly, the on and off times) will be constrained by the number of active strings in parallel.

According to the initial design specifications given in Section 3.2, the gate pulses will be designed for a system with 5 interleaved active strings. The pulses will have 2s of heating time and 8s of cooling time (20% duty cycle), and the initial overlapping time will be 20 μs.

The generation of the pulses will be performed in a LabVIEW™ -based embedded system. The pulse-width-modulated (PWM) pulses will be transferred to each of the IGBT's gate drivers through an interface PCB which conditions the signals and also supplies the drivers.

An overview of the IGBT gate driving system applied in Sven is depicted in Fig. 3.20.

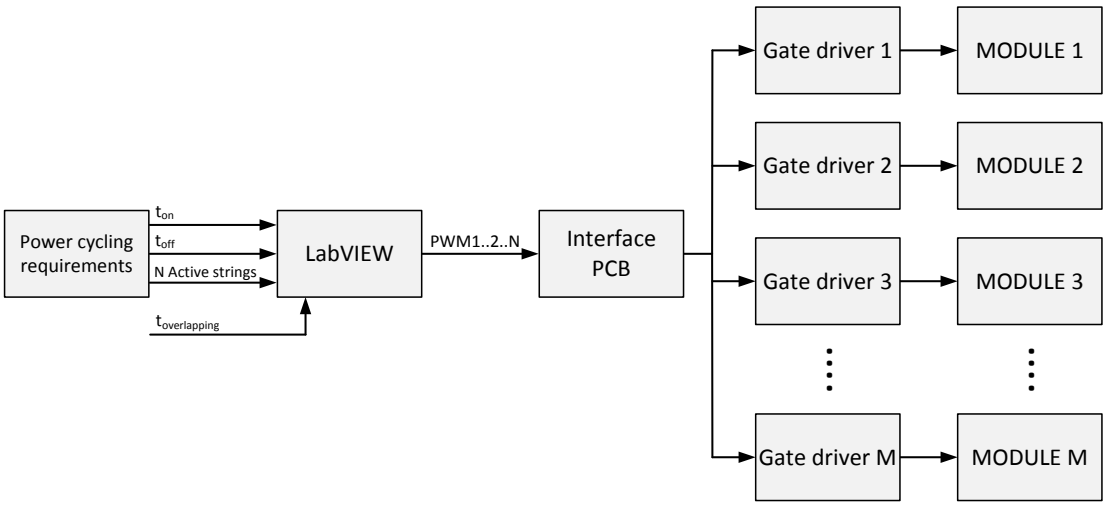


Figure 3.20. Overview of the gate driving system applied in the accelerated wear-out test setup. N refers to the number of paralleled legs, M refers to the total number of IGBT modules.

3.3.2.1 Gate signal characteristics

According to the above specifications, the gate signals must be designed as in the simplified diagram shown in Fig. 3.21.

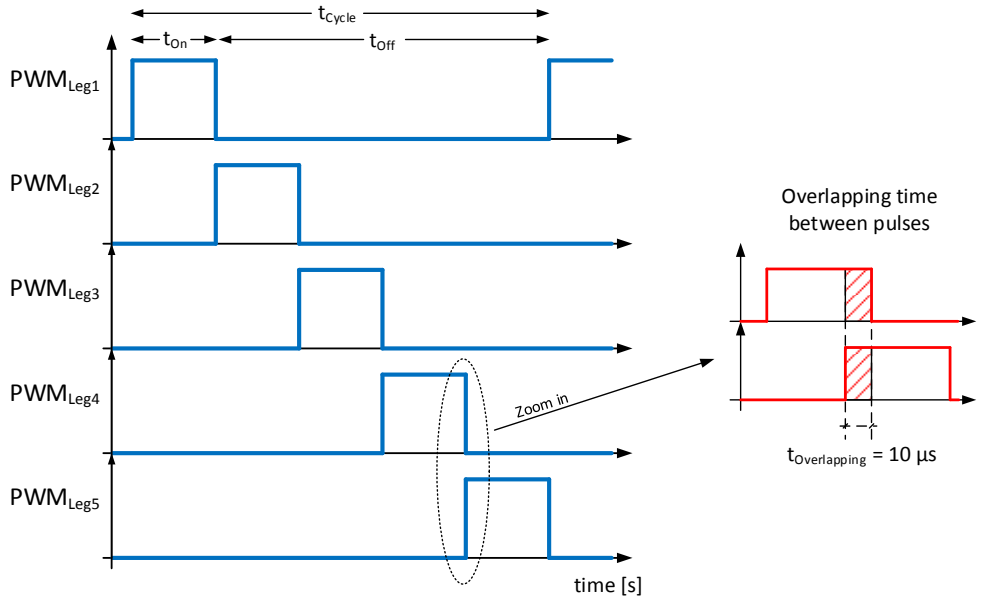


Figure 3.21. Overview of the gate signals for the different legs of the test setup, including the concept of overlapping time between pulses.

The PC accelerated wear-out test setup is operated with 5 interleaved strings as in Fig. 3.13 (2 IGBT modules in series for each string, a total of 10 IGBT modules). In order to avoid overvoltages due to parasitic inductances, the current circulation must not be interrupted. Consequently, the maximum allowable duty cycle will be limited to the inverse of the number of interleaved active strings, as in Eq. 3.4

$$d_{max} = \frac{1}{N_{Active}} = \frac{1}{5} = 20\ \% \qquad [\%] \tag{3.4}$$

Moreover, as explained in Section 3.2.2 (page 34), it is desired to have a pulse on-time of 2s in order to reach steady-state thermal conditions (steady state T_j). Thus, the total cycle time when operating 5 interleaved strings at 20% duty cycle is 10s (Eq. 3.5).

$$d = \frac{t_{on}}{t_{cycle}} \longrightarrow t_{cycle} = \frac{t_{on}}{d} = \frac{2}{0.2} = 10\ s \qquad [s] \tag{3.5}$$

Additionally, the fact of having 5 available legs in parallel allows to use some of the legs as a free-wheel path for the current in case that other operating conditions are desired with a lower number of active paralleled strings.

3.3.2.2 Gate driver circuit: CONCEPT 2SP0320T

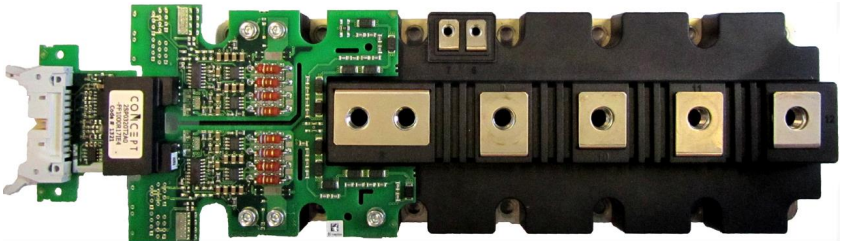
The gate driver circuit chosen to operate the IGBT modules in this setup is the CONCEPT 2SP030T2A0 (Electrical interface). This driver is specially designed for the PrimePACK™3 IGBT module (FF1000R17IE4) and provides the following technical features:

- Input electrical interface with galvanic isolation.
- Advanced active clamping for overvoltage protection at turn off (1200V).
- Fault detection (V_{CE} monitoring for short-circuit protection).
- 2 operating modes (Half-bridge and short-circuit).

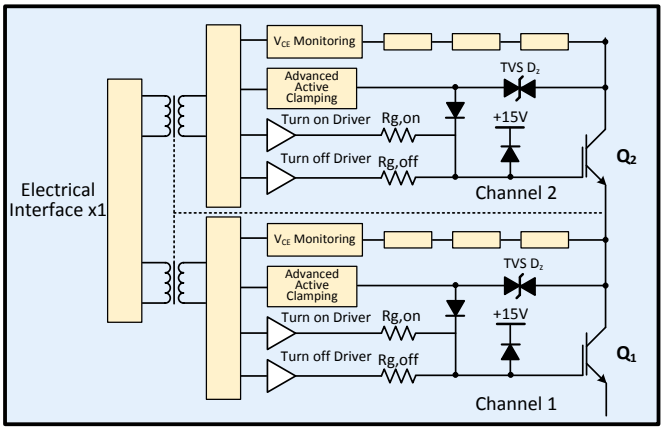
Even though some of the above-mentioned features will not be used in this setup, this driver was chosen in order to accelerate the setup implementation time, since its plug-and-play capabilities allow to operate the IGBT modules in a rapid and safe manner. The characteristics of the gate driver which are more relevant to the goal of this test setup are summarized in Table 3.7. In addition, a picture of the gate driver mounted on an IGBT module (Fig. 3.22a) and its simplified diagram (Fig. 3.22b) are shown below.

Table 3.7. Main electrical characteristics of CONCEPT Gate Driver

CONCEPT Gate Driver 2SP0320T2A0 - FF1000R17IE4				
Parameter	**Min**	**Typ**	**Max**	**Unit**
Power supply voltage, V_{DC}, V_{CC}	14.5	15	15.5	V
Average supply current, I_{DC}	-	-	600	mA
Logic signal voltages	-0.5		V_{CC}+0.5	V
Turn-on threshold	-	2.6	-	V
Turn-off threshold	-	1.3	-	V
Active clamping voltage, V_{clamp}	-	1200	-	V



(a)



(b)

Figure 3.22. CONCEPT driver 2SP0320T2A0-FF1000R17IE4: (a) Picture of the gate driver installed over the IGBT module, (b) Simplified schematic of the gate driver circuit.

3.3.2.3 Gate signal implementation in LabVIEW

The pulse generation to obtain the gate signals shown in Fig. 3.21 has been carried out in LabVIEW. This platform provides an easy-to-customize embedded system (both from hardware and software point of view) which is great in case that some design specification must be changed.

On the hardware side, the chosen NI C Series module (I/O module) is the NI 9401, specially designed for PWM generation (8 channels, 5V/TTL 100 ns High-speed Digital I/O). The main characteristics relevant to this application are summarized in Table 3.8. A picture of the module (Fig. 3.23a) and the chosen pin designation (Fig. 3.23b) are also presented below. The module is installed in one of the slots of NI9144 EtherCAT chassis (which works as Slave of the RT computer).

Table 3.8. Main specifications of the NI 9401 C series module used for the pulse generation

NI 9401 C Series module specifications	
Number of channels	8 Digital I/O
Input/Output type	5V TTL
Speed	100 ns
Digital Output Logic levels	
- High, V_{OH}	5.25V (max), 4.3V (min)
- Low, V_{OL}	0.4V
I/O connector	25-pin D-Sub

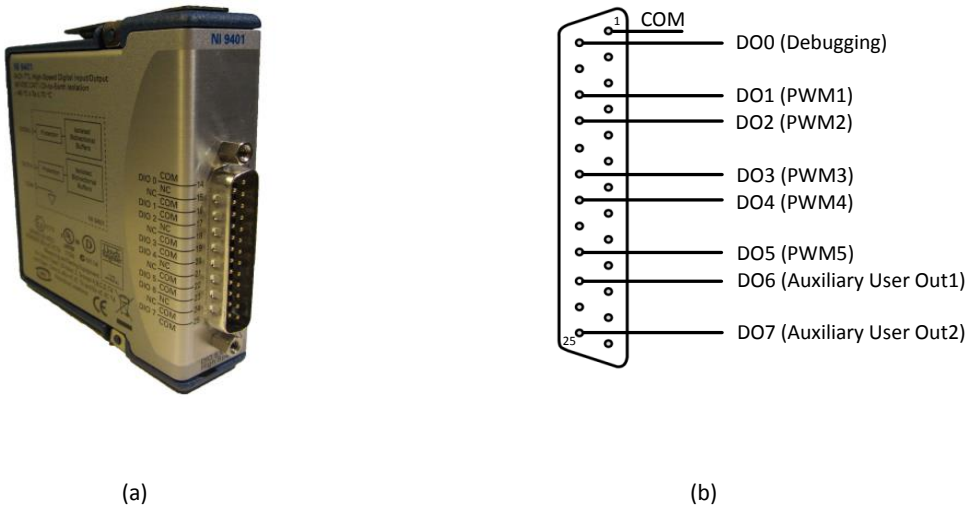


Figure 3.23. NI 9401 C Series DIO module: (a) Picture of the module, (b) Pin designation.

On the software side, the pulses have been programmed in LabVIEW graphical programming environment. Since the pulse generation requires microseconds resolution (overlapping generation), which cannot be obtained through the NI Scan Engine, this task has been carried out in the FPGA of the NI 9144 EtherCAT chassis. The FPGA uses the internal clock of the board, which can be set up to 40 MHz and, therefore, it is suitable for this application. An overview of the software architecture used for the pulse generation, summarizing its main loops and components, can be observed in Fig. 3.24. The initial LabVIEW code was developed by Michael Møller Bech (AAU Associate Professor), however, several modifications have been performed in order to adjust the pulses to the application requirements.

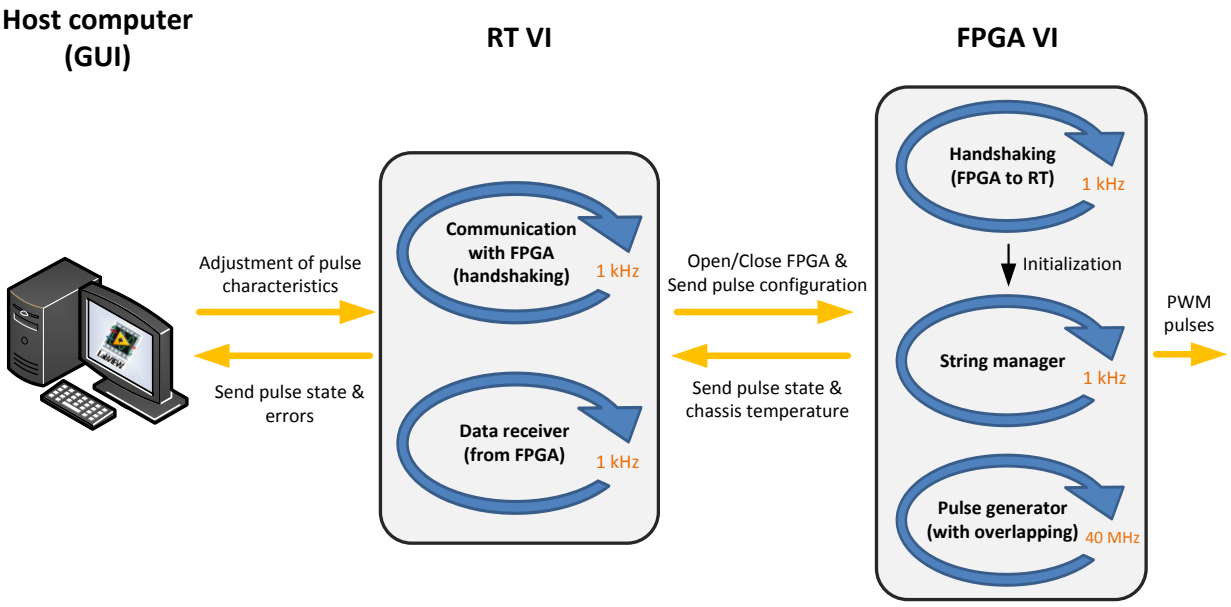


Figure 3.24. Software architecture implemented for the pulse generation.

Additionally, in order to have a more flexible and customizable system, a front panel, which allows the adjustment and monitoring of the main characteristics of the pulses, has been designed. This front panel can be accessed through the host desktop computer located in the garage, as indicated in Fig. 3.24. A screenshot of the front panel is depicted in Fig. 3.25.

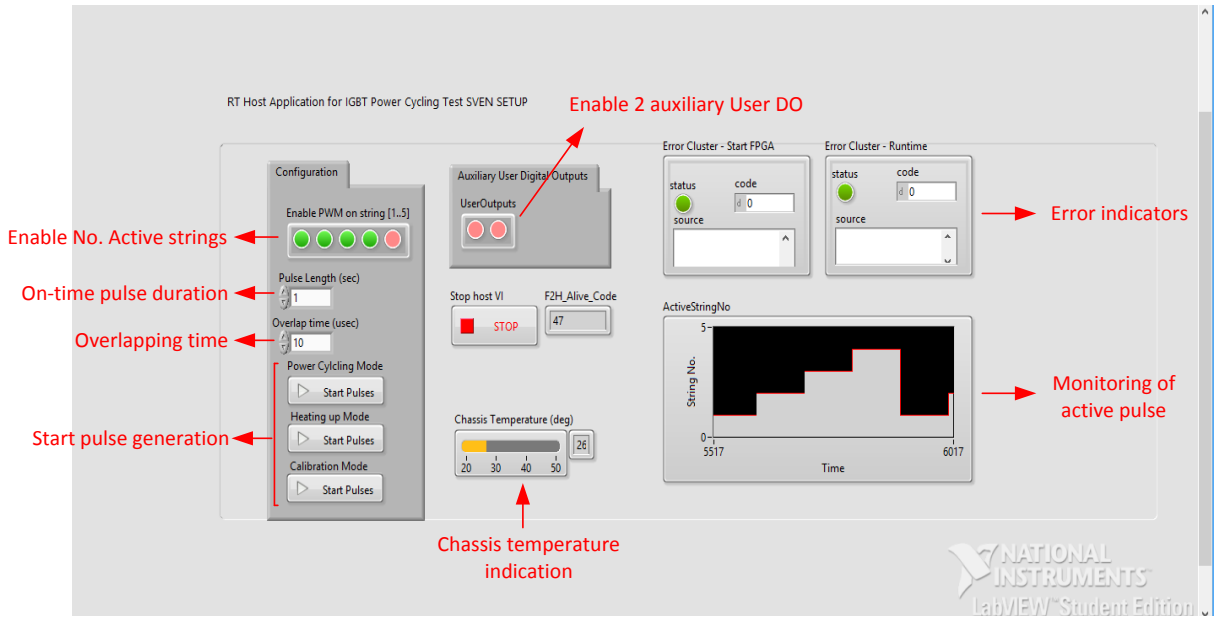


Figure 3.25. Printscreen of the front panel VI build in LabVIEW programming environment for the PWM pulses generation.

The experimental validation of the proper operation of the pulses will be presented in Chapter 6 (Section 4.2).

3.3.2.4 Interface PCB for gate drivers

The CONCEPT gate drivers need an external circuit for power supply and control electronics. For this purpose, a PCB has been designed to operate as interface between the CONCEPT drivers, mounted in each of the IGBTs (10), and the LabVIEW control system. The schematic and PCB layout is attached in Appendix B. The main design objetives of this PCB are:

- To provide a 15V power supply to each of the gate drivers.
- To send the PWM pulses to each of the gates in an adequate manner (signal conditioning).
- To adjust the settings of the gate drivers (Half-bridge/Short-circuit mode and $T_{blocking}$).
- To monitor possible fault conditions in the IGBT.

In order to comply with the above objectives, the circuit shown in Fig. 3.26 has been designed and implemented. This diagram is given only for 1 IGBT to simplify its complexity, however, the interface board has been designed for 10 IGBTs.

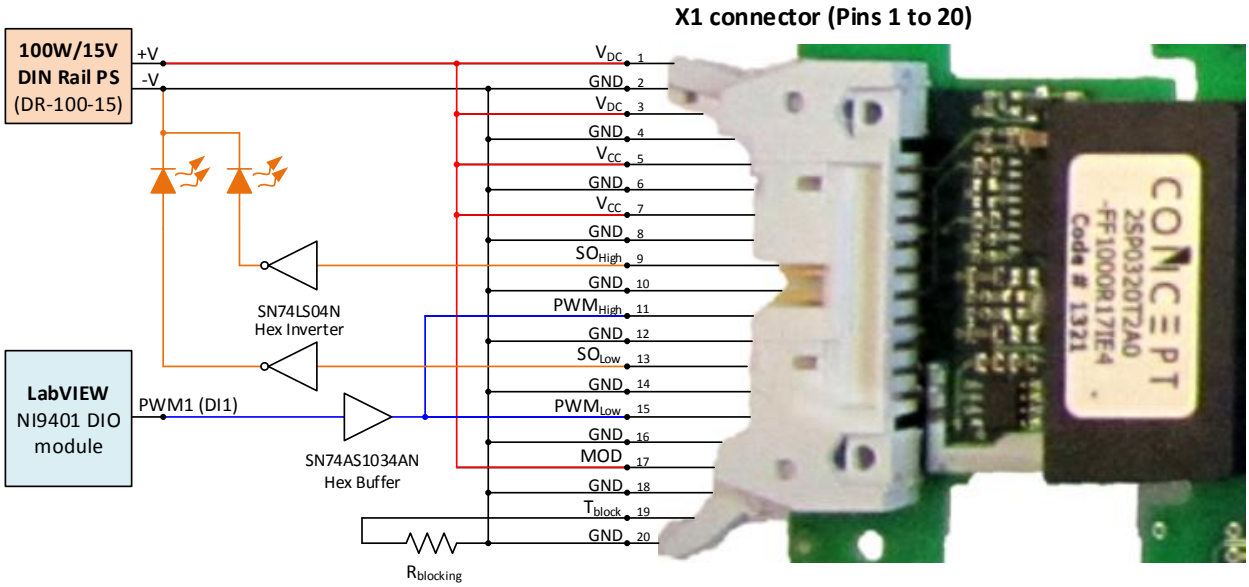


Figure 3.26. Simplified schematic of the gate driver interface board for 1 CONCEPT gate driver (PCB is designed for 10 gate drivers).

Firstly, the 15V power supply is provided by a 100W DIN Rail power supply (DR-100-15, 15V-100W-6.5A) installed inside the cabinet. This has been selected according to the current needs of each of the gate drivers (10x 600 mA max. current). In order to supply the different ICs (V_{CC}= 5V), an off-the-shelf LM7805 voltage regulator has been chosen to reduce the voltage level from 15 to 5V.

Secondly, regarding the PWM pulses, a non-inverting hex buffer (SN74AS1034AN) is used to drive the pulses coming from LabVIEW and send them to each of the X1 connectors. It should be mentioned that the NI9401 outputs 5 PWM signals (for 5 legs), and then, the total amount of IGBTs to be driven with the same pulse is 4 (2 modules per leg, 2 IGBTs per module). This means that the gate signals could become too weak (i.e. slow) because of the current sharing. Moreover, since the connectors are disposed with different distances along the PCB, the impedance of the tracks can worsen even more

this effect, resulting in delays between gate signals of the same string. This fact is taken into account for future versions of this interface board, moreover, after that the performance of the gate signals has been analysed and presented in Chapter 4.

Regarding the monitoring of possible faults, the CONCEPT gate driver provides 2 open-collector status outputs (for each IGBT) which are activated in case of a fault event. Under fault conditions, these status outputs are pulled to low and, therefore, hex inverters (SN74LS04) have been used to process them. Each of the outputs of the hex inverters is connected to an LED indicator so that fault conditions can be easily detected. Additionally, the 20 fault signals could also be sent to the LabVIEW monitoring system, however, this feature has not been implemented in the actual PCB.

Lastly, the parameters that can be adjusted by means of the user are the operation mode (Half-Bridge/Short-circuit, Pin 17) and the blocking time ($T_{blocking}$, Pin 19). In this system, the IGBT modules are operated in short-circuit mode, which means that both IGBTs are driven by the same PWM signal and there is no need of dead time compensation. In order to select this mode, Pin 17 is connected to V_{CC}. Regarding the blocking time, this is adjusted by means of a resistor connected between Pin 19 and GND. The chosen value for the resistor is $2.37k\Omega$, according to the calculation given in the CONCEPT gate driver manual.

The PCB layout has been designed in Altium Designer® and the 2-layer PCB has been built in the laboratories of the Department of Energy Technology. A picture of the resulting PCB is depicted in Fig. 3.27. It should be mentioned that from the experience obtained during the testing period, this PCB can still be further improved both in the PCB layout and in the selection of the electronic components and, therefore, a second version of it is planned to be performed.

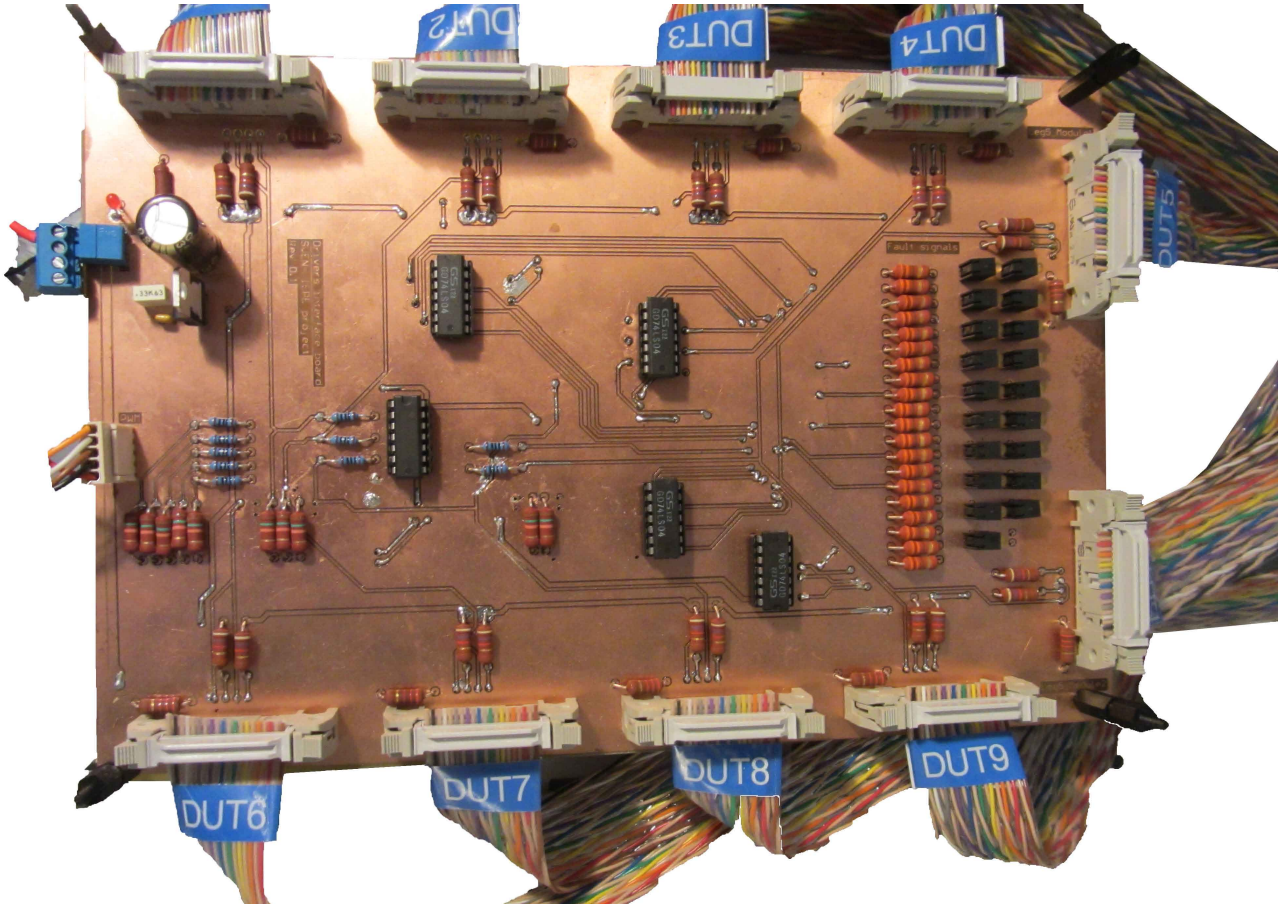


Figure 3.27. Picture of the interface PCB placed in the cabinet of the power supplies.

3.3.3 Electrical measurements

3.3.3.1 Voltage and current measurements on the IGBTs

The electrical measurements that need to be carried out at each IGBT module have already been mentioned at Section 3.2.5. In more detail, the V_{CE} and V_{GE} voltages for both high and low side IGBTs at a single module, are measured through the auxiliary terminals provided by the PrimePACK™3 package and the terminals of the CONCEPT gate diver. A shielded 4 pair twisted cable is used together with ring connectors to ensure that signal quality is kept as high as possible. A clear representation of the voltage measurements is shown in Fig 3.28.

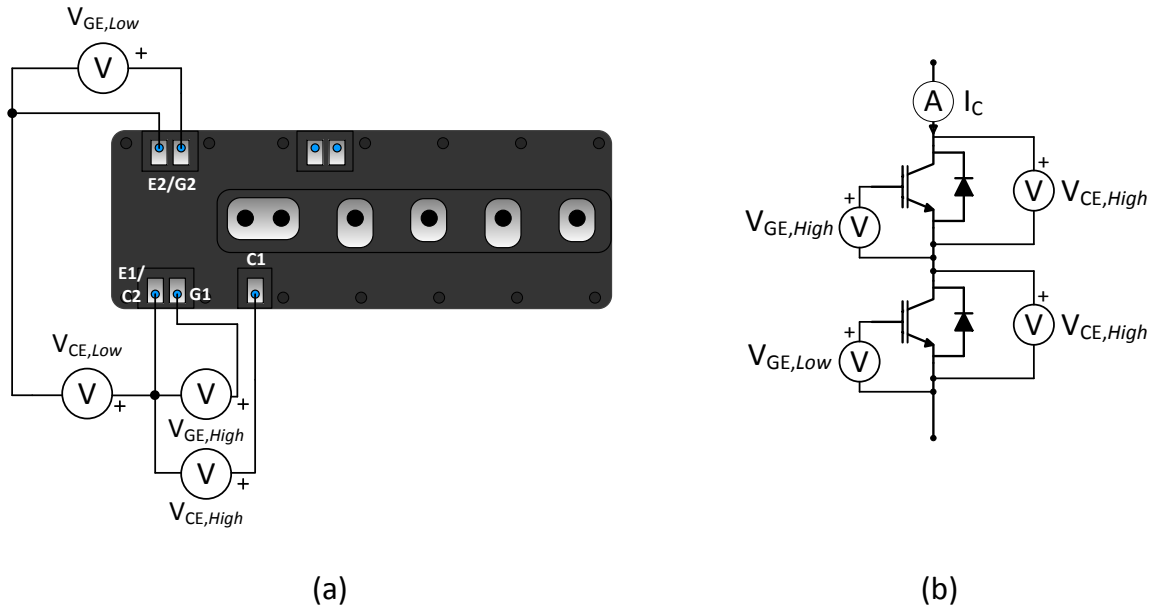


Figure 3.28. Representation of voltage measurement points at: (a) Auxiliary terminals of PrimePACK™3 IGBT module, (b) Schematic symbol of IGBT module.

The aforementioned voltages are measured by the NI 9215 C Series Module which has 4 Simultaneous Differential Input channels of 16 bits each one. This module has been selected as it can provide the prerequisite speed and accuracy for the performed tests. According to the datasheet, this module has 7 LSB (Least Significant Bit) which means an accuracy of $2.13mV$. The most representative characteristics are given in Table 3.9 and in Fig. 3.29 the module with the input channels is shown.

Table 3.9. Main specifications of the NI 9215 C series module used for the voltage measurements

NI 9215 C Series module specifications	
Number of channels	4 Analog Inputs
Signal type	Differential
ADC resolution	16 bits
Input range	±10 V
Input noise peak-peak	7 LSB
Input impedance	1 GΩ
Overvoltage protection	30 V

Figure 3.29. The NI 9215 module.

As it has shown in Table 3.9 the input module has rated input range of $\pm 10V$ and built in overvoltage protection of $\pm 30V$. Even though, the module should be protected from the V_{CE} overvoltages that appeared during the switching of across the IGBT modules. Similarly, the V_{GE} voltages are set from the CONCEPT gate driver from -10 to 15V and in order to be measured from the NI9215 a scaling is necessary. For these reasons, an interface board has been built that is plugged at the input terminals of each measuring module. The schematic of is presented in Fig 3.30 and is presented analytically in the following section.

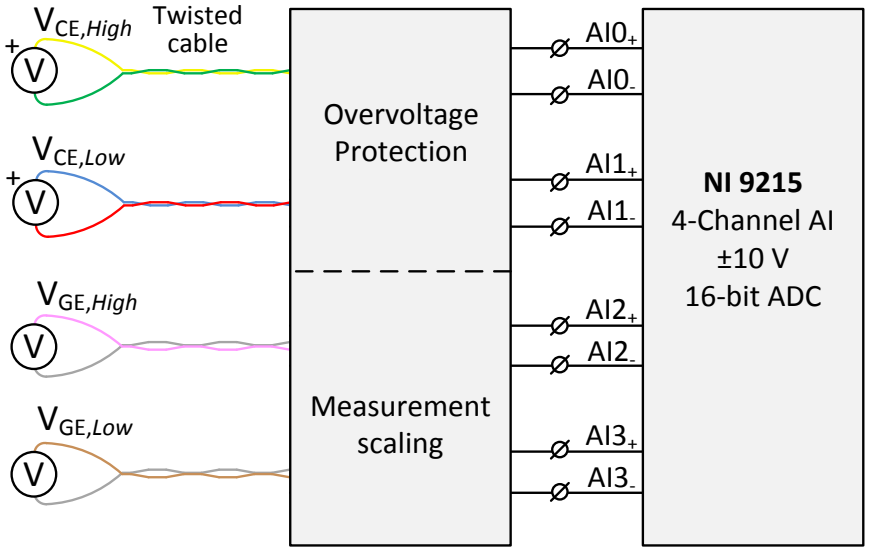


Figure 3.30. Schematic diagram of the measurement system between the IGBT module and the NI9215 module.

Another necessary measurement is the current through the IGBT modules. However, due to the laminated bus bars layout it is not possible to access the path through each string. Hence, the full DC current is measured using a current transducer (LEM®) rated for 4000A shown in Fig.3.31. Moreover, the value can be double checked through the monitor panel of the DC supplies.

Figure 3.31. Picture of the LEM module used in Sven, rated for 4000A.

Table 3.10. Characteristics of the current transducer

LEM®MODULE	
Measuring range	±4000 A
Supply voltage	±15 V
Output voltage	±10
Output load resistance	10 kΩ

3.3.3.2 Overvoltage protection and measurement interface

The purpose of the overvoltage protection (OVP) circuit is to protect the NI 9215 module from voltages that exceed its nominal input range of ±10V. The NI9215 module is measurement equipment designed for differential analog measurements and it consists in an instrumentation amplifier whose output is connected to an ADC. Therefore, to protect these electronic components from hazardous overvoltages which can occur during system operation, a protection circuit has been designed and built, as in classical ADC protection circuits. In addition to the OVP circuit, a voltage divider with a gain of 1/2 has been implemented to adjust the V_{GE} measurement to the input range of the module. The PCB mounted on the NI module and the schematic diagram of the circuit are shown in Fig. 3.32.

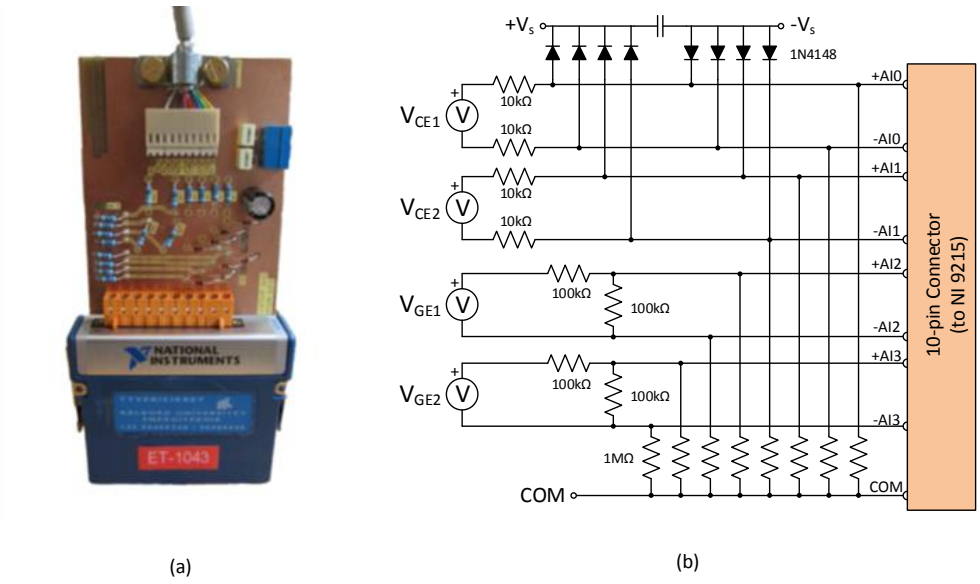


Figure 3.32. Measurement interface PCB for NI9215: (a) Picture of the resulting PCB, (b) Equivalent circuit diagram.

The working principle of the overvoltage protection circuit is that when the input voltage (V_{CE} measurement) exceeds the supplied voltage at the cathode terminal of each diode (V_S), the diode is turned into conduction mode, hence, clamping the voltage at inputs of the protected device. In particular, the clamping voltage level is equal to the supply voltage plus the forward voltage of the diode. Two diodes are used with positive and negative supply voltages to protect from both input voltage polarities. Moreover, in this case where the input signals are differential, one more pair of diodes is added to the other source terminal (AI_-), protecting the NI module from voltages that are double the absolute supply voltage plus the two voltage drops at the diodes. Finally, two resistors are placed in the inputs in order to limit the current when the diodes conduct during overvoltage event.

However, some considerations should be taken into account during the design of this circuit. At first, diodes with fast response and low leakage current are needed to clamp in very short time and also not affect the measurements during normal conditions. For these reasons, a classical high speed Schottky diode 1N4148 has been selected. In addition, the limiting resistor values should be high enough to limit the current under the short circuit level of the diodes but, at the same time, as low as possible to not degrade the measurement accuracy. Thus, $10k\Omega$ resistors have been selected, and together with the high input impedance ($1G\Omega$) of the NI modules, sufficient accuracy is obtained. Finally, 1 $M\Omega$ resistors have been placed between each of the inputs and the COM terminal of the module in order to keep the voltage measurement within the common-mode voltage range (floating inputs).

3.3.3.3 Data acquisition and logging system

The data acquisition and storing process have been done in LabVIEW using the Scan Engine mode of the Real Time computer. A typical program algorithm has been implemented where the input measurements from the NI9215 modules are buffered into a FIFO memory with 100Hz and afterward are stored at the hard disk of the real time target into .tdms format with a frequency of 10Hz. The rates of buffer and logging can be changed according to the users needs but in principle high values ($\geq$500Hz) are not recommended. Fig. 3.33 shows the LabVIEW code which carries out the above tasks.

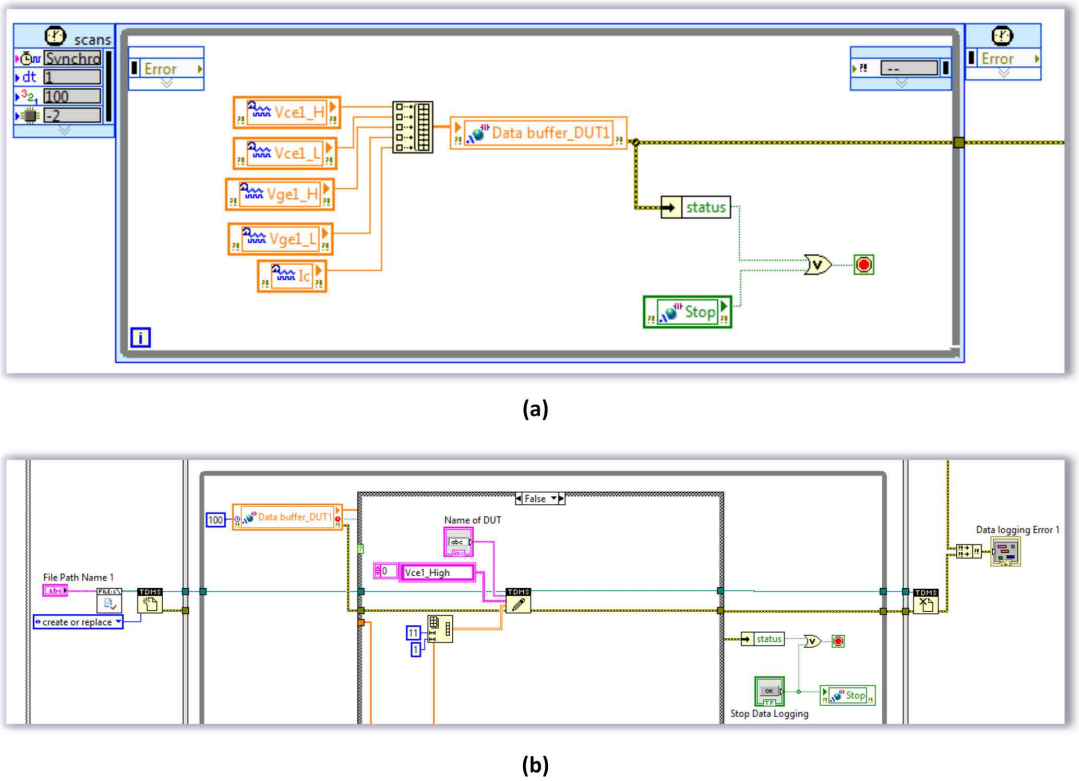


Figure 3.33. (a) Measurements stored into a FIFO buffer, (b) Data logging into a .TDMS file.

3.3.4 Cooling system

This section briefly describes the implementation of the cooling system according to the design presented in Section 3.2.4.

As previously explained, the cooling system is a non-pressurized system based on an open water tank of 90 liters connected to a heat exchanger (Fig. 3.34a). The flow of the system is provided by a Grundfoss CR 16-20 pump (Fig. 3.34b) which is controlled by a 7.6kVA Danfoss Series 5000 VLT (Fig. 3.34c). The VLT is operated at 30 Hz, following recommendations of the designer, which yields an individual flow rate in each of the DUTs of 8.8 l/min (individual check valves completely released, shown in Fig. 3.35).

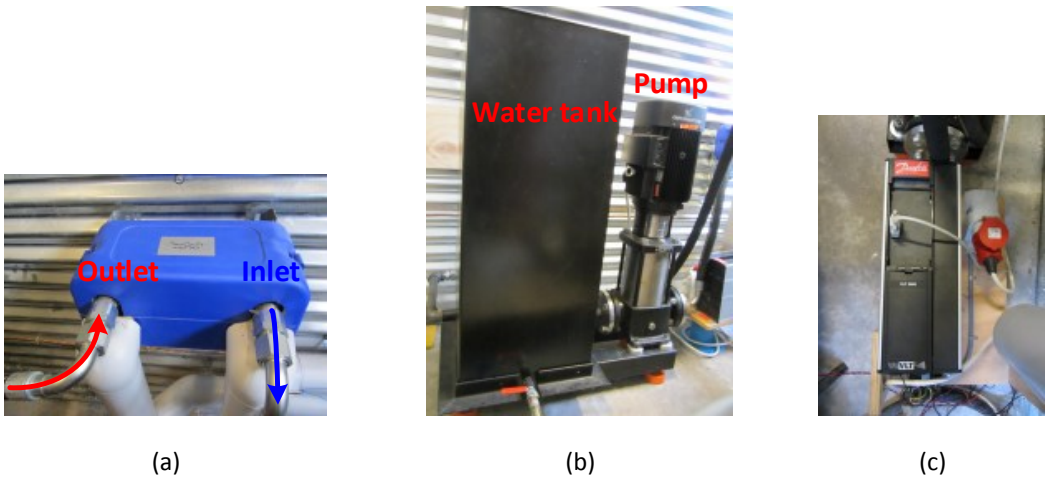


Figure 3.34. (a) Heat exchanger in the input of the cooling circuit, (b) Grundfoss CR 16-20 pump connected to 90-liters open water tank, (c) Danfoss VLT for variable speed operation of the pump.

Regarding the measurements of the cooling system, the implemented sensors are:

- Input and output pressure: GEMS 3300 Series Low Pressure OEM 0-6 bars (Fig. 3.35a)
- Input temperature: AMETEK Thermocouple Type K.
- Temperature and Flow in each DUT: Grundfoss VFS 1-20L G (Fig. 3.35c)

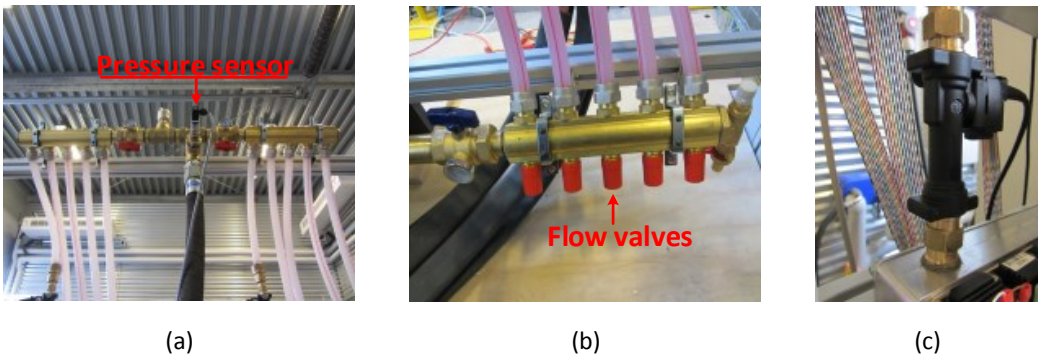


Figure 3.35. (a) Pressure sensor, (b) Manifold check valves, (c) Temperature and Flow sensor.

The data acquisition and monitoring system implemented in LabVIEW is presented in Appendix D.

Acceptance testing of the power-cycling test setup 4

This chapter presents the validation of the different functionalities of the PC test setup described in Chapter 3, focusing on the implemented hardware and software depicted in Section 3.3. Firstly, to ensure the proper driving of the IGBT modules, the verification of the gate driver signals is performed. Afterwards, the overvoltages of the test setup are experimentally analysed and the validity of the implemented protections is shown. Finally, the maximum allowable current level of the test setup is tested.

4.1 Testing conditions

The testing conditions applied during the tests described in the following sections are summarized in Table 4.1.

Table 4.1. Testing conditions applied during the validation tests of the PC setup

Test conditions	
Current level	500 A [(1)] 1000 A [(2)]
Pulses on-time	2 s
Pulses off-time	8 s
duty cycle	20 %
Overlapping time	10 μs
No. Active strings	5 strings (10 modules)
Pump VLT frequency	30 Hz (1720 rpm)

Regarding the current levels (Notes [(1)] and [(2)]): the 500A were applied in the initial tests of the gate signals (Sections 4.2.1 and 4.2.1.1) and in the initial tests to determine the maximum allowable current of the setup (Section 4.5), whereas the 1000A were used in the rest of the tests shown below.

4.2 Gate driver signals

As presented in Section 3.2, sequential pulses are needed to activate each string of IGBT modules according to the PC test setup specifications. In addition, the overlapping characteristic is necessary as thoroughly explained in Section 3.3.2. To validate the precise and proper performance of the generated gate driver signals, several verification tests have been carried out. The followed process was to measure the signals at multiple points across the circuit and to monitor them with an oscilloscope. With this systematic approach, in case of undesired outcomes, possible improvements and solutions

can be investigated and applied. A graphical illustration of the measuring points and the different components within the gate driving system is given in Fig. 4.1.

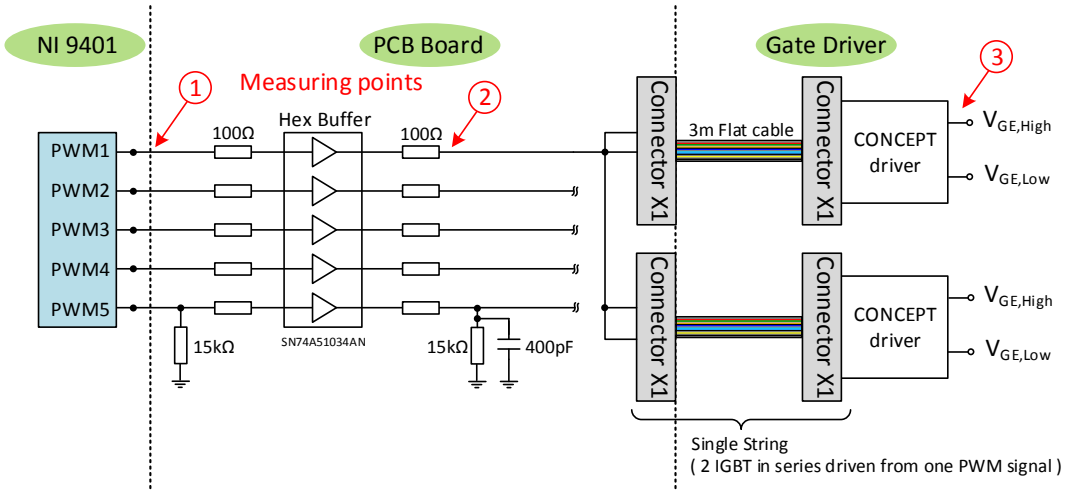


Figure 4.1. Tests points for validation of the gate driving signals.

4.2.1 Initial gate pulses performance

The PWM pulses generated in LabVIEW should fulfill the PC requirements shown in Table 3.3 (Section 3.2.2, page 34). Therefore, these were measured at the output terminals of the NI9401 C-series module (Digital I/O) without connecting them to the interface board for the CONCEPT gate drivers (Measuring point 1). The resulting waveforms are depicted in Fig. 4.2.

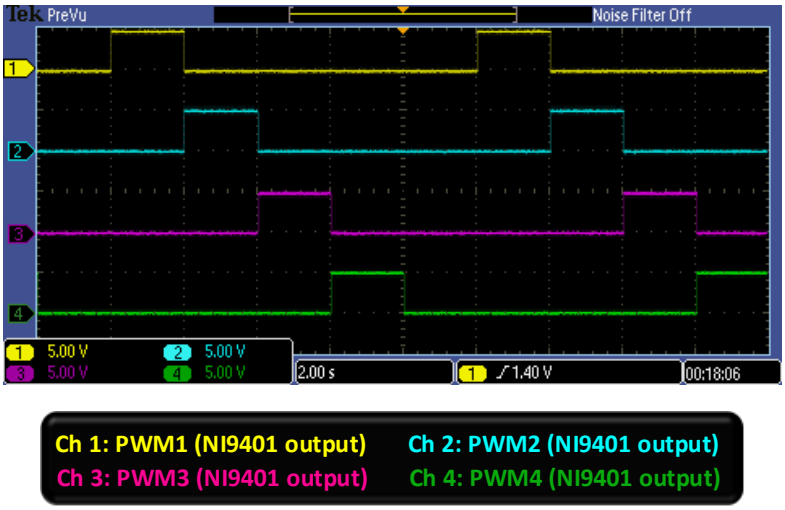


Figure 4.2. Measured PWM signals for power cycling test (2s on-time, 8s off-time) at the output of the NI9401 module (DIO module). The signals are not connected to the Interface PCB.

Regarding the characteristics of the NI9401 (Table 3.8, page 49), the output signal is measured and monitored with nanoseconds resolution to assess the correct performance of the module.

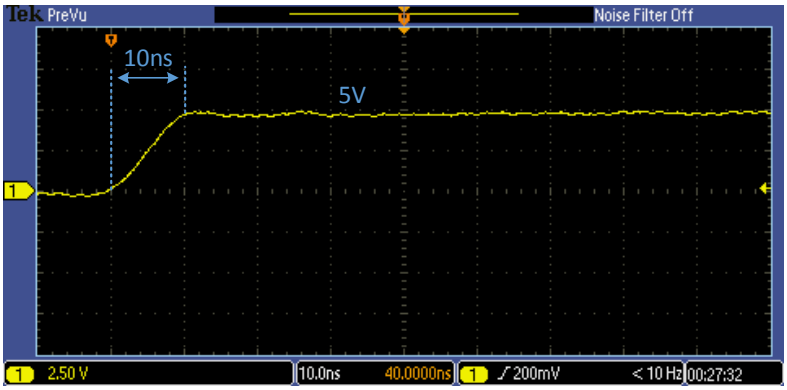


Figure 4.3. Measured PWM output of the NI9401 module (DIO module) at the turn-on instant.

As can be observed, the module fulfills the stated characteristics and it is able to provide 5V output signal with a rise time of 10 ns (whereas the specified time was 100ns). This means that the signals provided by the module shown a healthy condition and, therefore, the signals could be debugged in the next stages of the gate driving system (Interface PCB and CONCEPT driver). Prior to that, the adjusted overlapping time was verified and the results are presented in the next section.

4.2.1.1 Overlapping times

In this section, the capability to overlap between strings of the PWM generation program created in LabVIEW is tested. First, an overlap time is set at $10\mu sec$ and then at $100\mu sec$. The overlap times can be adjusted occasionally to the desired values. The results are shown Fig. 4.4 where the overlap between two gate signals is presented.

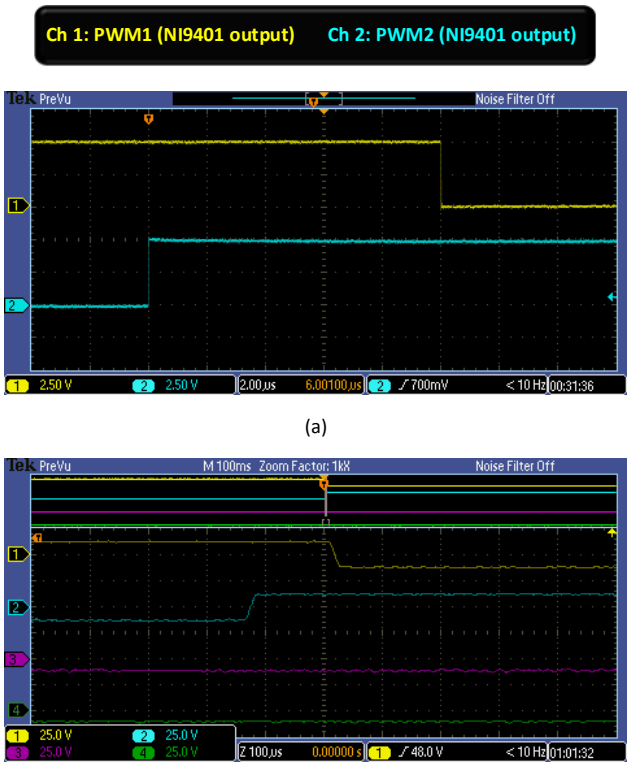


Figure 4.4. Overlapping times between PWM signals of two strings set at (a) $10\mu sec$, (b) 100 μsec.

4.2.1.2 Delays between gate signals

The next step is to verify whether IGBTs that belong to the same string are switched at the same instant as they are controlled from the same PWM signal. For this reason, the V_{GE} signals of DUT1 and DUT6 have been measured with the PWM control set as trigger for the delay calculation. Delays up to $105\mu sec$ and $13\mu sec$ during turn on and turn off, respectively, were found and they are demonstrated in Fig. 4.5a. and Fig. 4.6a. Even for the same module, the V_{GE} signals were different regarding the on and off times. This is shown in Fig. 4.5b. and Fig. 4.6b.

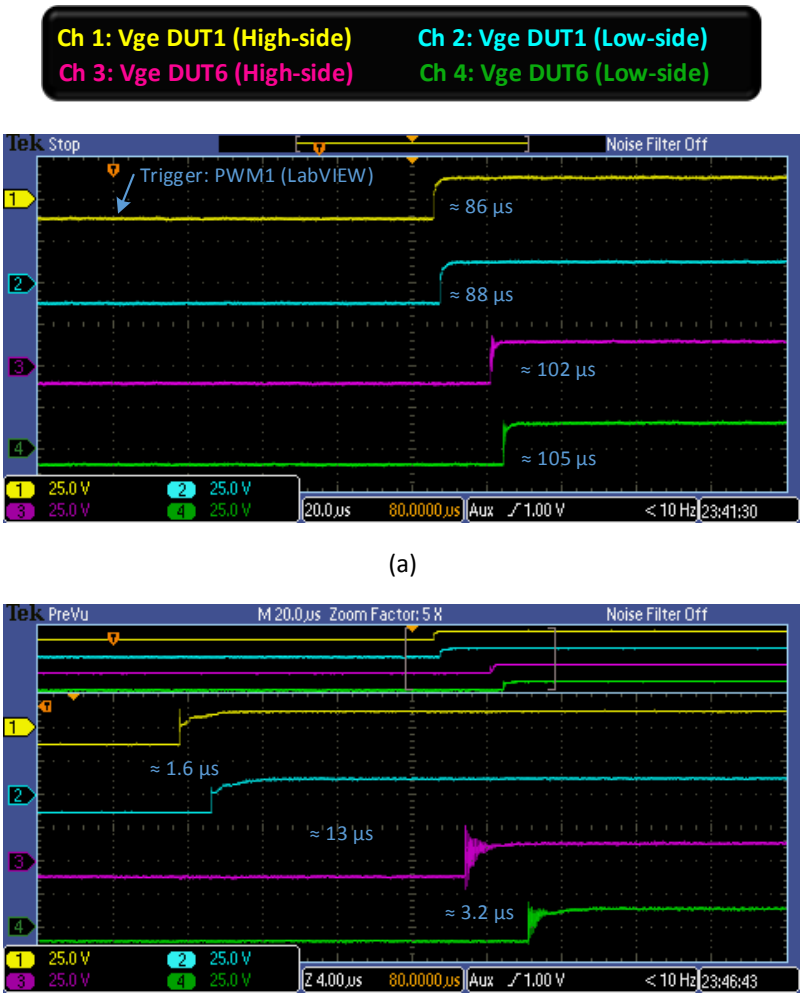


Figure 4.5. Delays between gate signals of the same string during turn on: (a) With respect to the PWM signal from LabVIEW, (b) Between gate signals.

With the overlapping time set at $10\mu sec$ for the initial tests, a fault during operation at $I_C = 500A$ was noticed. As shown in Fig. 4.7, the current falls down to zero at every switching from one string to another. A first solution to this problem was to increase the overlapping time to $120\mu sec$. However, further investigations needed to be carried out in order to identify the cause of the delays at the gate signals as well as the open circuit.

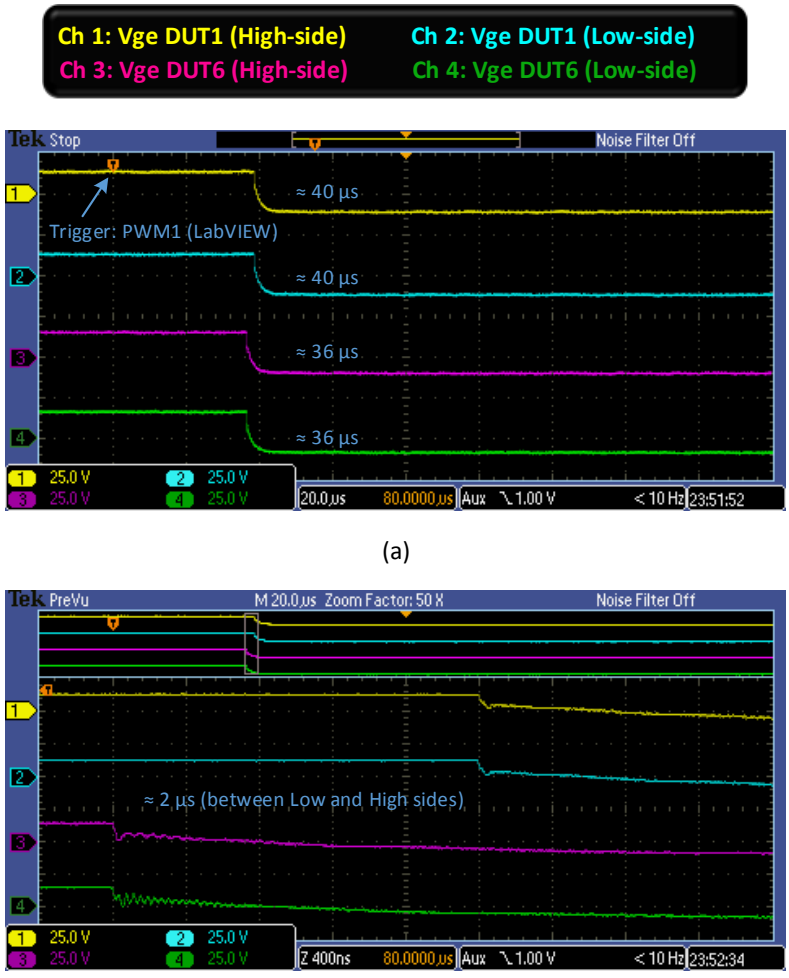


Figure 4.6. Delays between gate signals of the same string during turn off: (a) With respect to the PWM signal from LabVIEW, (b) Between gate signals.

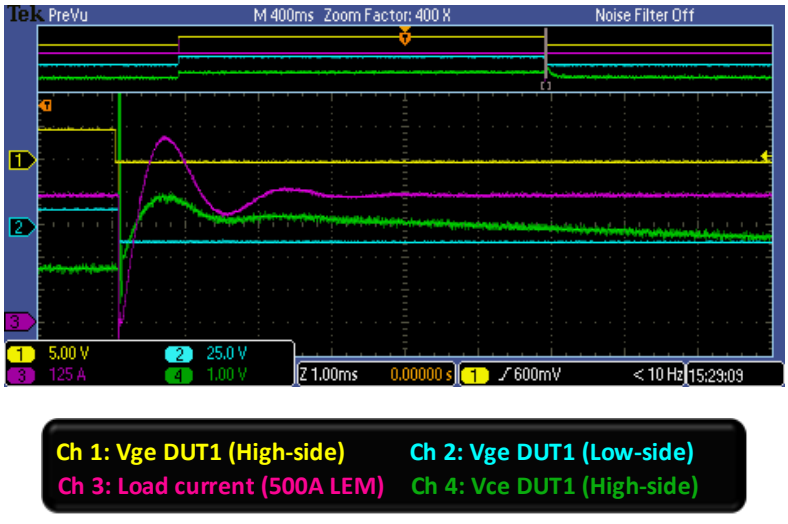


Figure 4.7. Open circuit during shifting between strings with the current fall to zero and ramp up again.

4.2.1.3 Problem identification and solution

The delays between the gate signals and the open circuit at the switching moments from one string to another implied additional measurements on the gate signals. The next step was to check the signal condition at the points located on the interface PCB for the gate drivers. Hence, the PWM signal which is generated from NI9401 digital module was measured after passing through the hex buffer and reaching finally the CONCEPT gate drivers. The results of these measurements are shown in Fig. 4.8 for both turn on and off. Apparently, the PWM signal slows down after the Hex buffer. For this reason the time to reach the turn on and off thresholds of the CONCEPT gate driver is longer than the expected one.

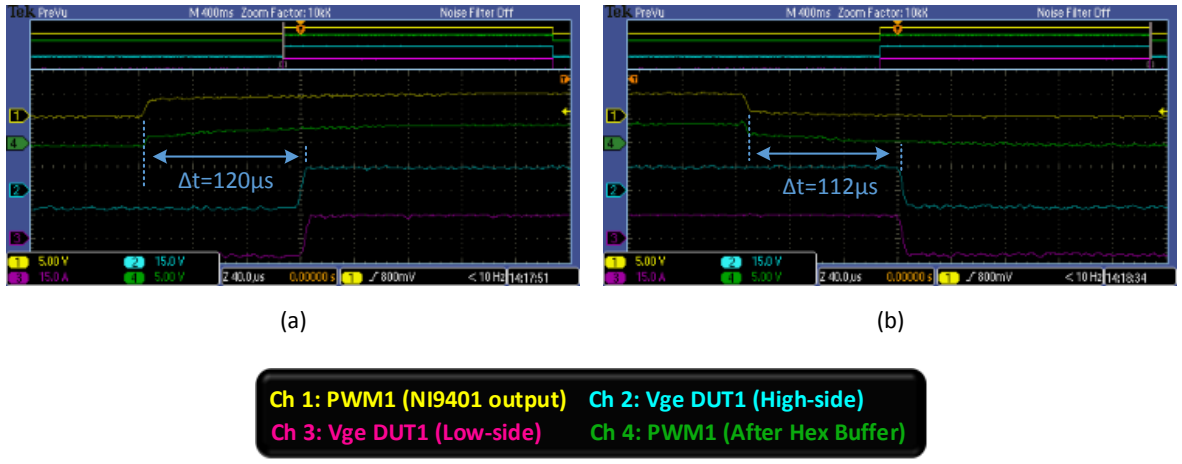


Figure 4.8. Initial PWM signal after the hex buffer IC during: (a) turn on, (b) turn off.

Later, it was realized that the selected value of capacitance at the output of the hex buffers was too high ($400nF$), and instead, $400pF$ capacitance was placed, which means 1000 times lower. Obviously, this was slowing down the gate signal when shifting from high state to low or the opposite. Finally, the mistake was corrected and new measurements showed that the delays were reduced to very low values (Fig. 4.9). After that, the current was not interrupted anymore and the explanation to this is that the initial overlapping of $10\mu sec$ was not enough to overcome the delays introduced from the high value capacitors. The problem was solved only when the overlapping time was increased or the delays were reduced to values lower than this time.

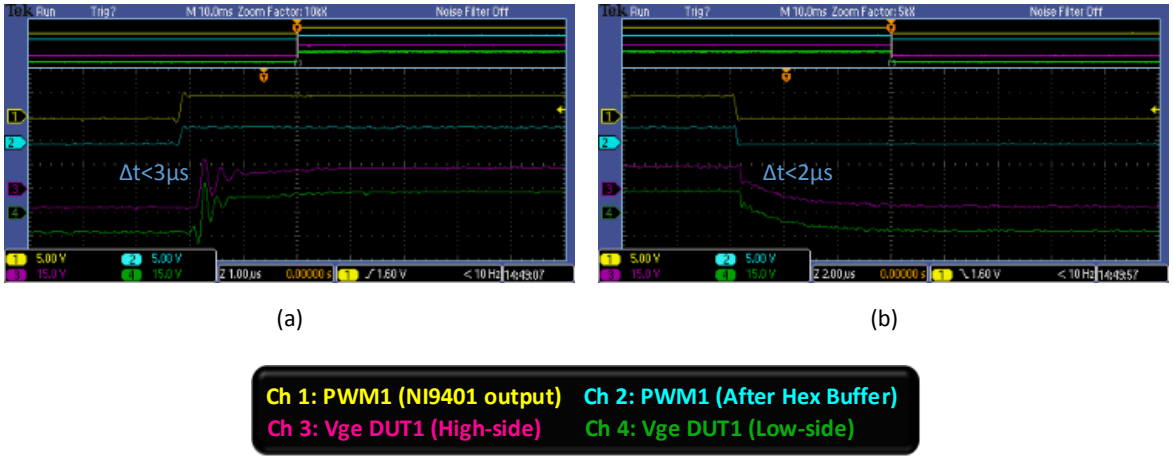


Figure 4.9. Improved PWM signal after the hex buffer IC during: (a) turn on, (b) turn off.

4.3 Overvoltages in the test setup

As described in Chapter 3, the appearance of overvoltages during the turn-off transient of the IGBTs, as a consequence of the circuitry parasitic inductances, is a potential problem of this test setup. Moreover, this fact is aggravated by the high value of supply current, which is translated into an even higher di/dt. These overvoltages can be harmful for both the measuring system (LabVIEW NI9215 modules) and the IGBT itself. In order to reduce the parasitic inductances of the circuit, a laminated busbar was designed and implemented (as described in Section 3.3.1.3).

To quantify the above-mentioned overvoltages, V_{CE} of both High-side and Low-side IGBTs of DUT1 were measured and the results are depicted in Fig. 4.10.

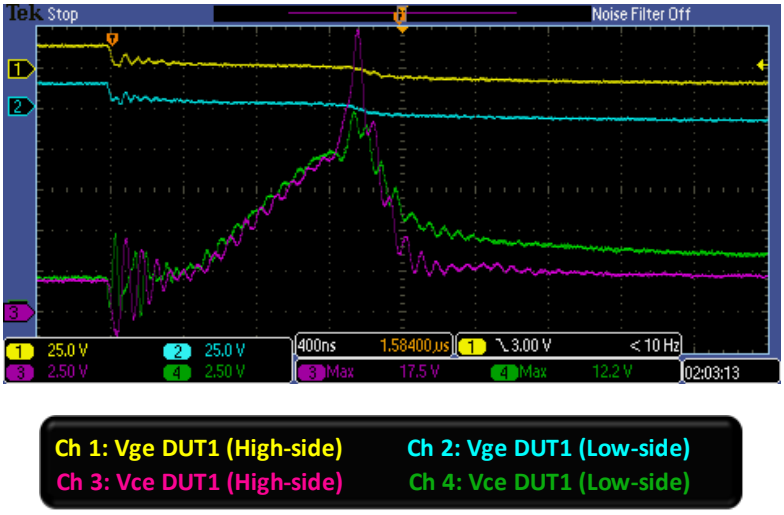


Figure 4.10. Measured overvoltages on High-side and Low-side IGBTs of DUT1 during the turn off transient.

The peak value of the overvoltages for both high-side and low-side IGBTs is 17.5V and 12.2V, respectively. This is considered a positive outcome since they do not represent a potential problem for the measuring system (which is protected up to 30V). However, it is not desired to apply these continuous stresses to the NI C-series modules and, hence, extra protection was still considered.

The validation of the different protection measures that have been applied in the test setup is presented in the following sections.

4.3.1 Customization of Advanced Active Clamping on the CONCEPT driver

Prior to the design and building of the NI9215 external overvoltage protection circuit, another approach was tested to prevent the measuring system from undesired overvoltages. This approach was based on the customization of the Advanced Active Clamping implemented in the CONCEPT gate driver (previously presented in Section 3.3.2.2).

This driver has an Advanced Active Clamping functionality which aims to clamp voltage levels higher than 1200V and use that energy to turn on the device again during a short period. The clamping is done by means of 5 Transient Voltage Suppressors (TVS) in series which are rated for 240V each (obtaining the previously mentioned 1200V). To carry out the customization (Fig. 4.11a), the 5 TVS were bypassed by a wire and 2 Zener diodes of 47V were installed. This process was done for both high-side and low-side driver circuits.

Regarding the test procedure, as the 4x 500A power supplies were not available at that moment of the thesis period, the test circuit shown in Fig. 4.11b was implemented.

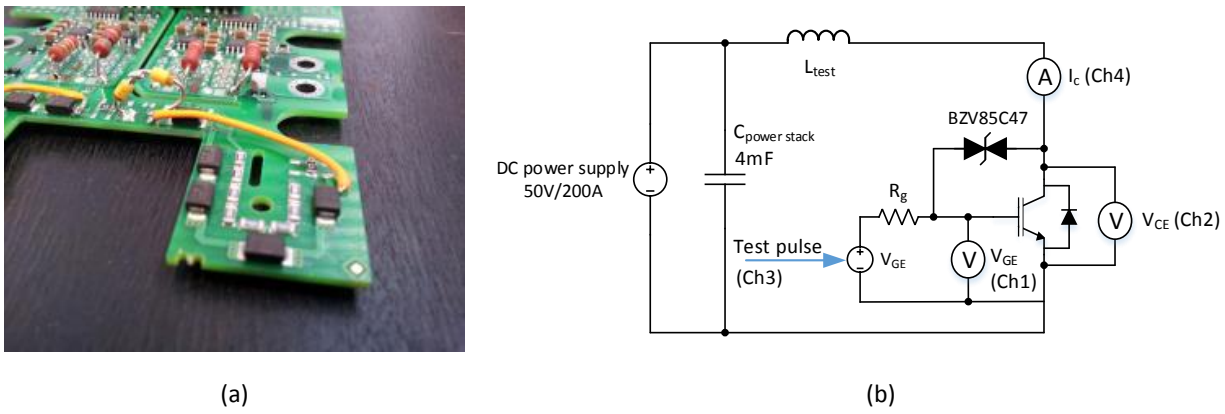


Figure 4.11. Customization of CONCEPT driver: (a) TVS modification, (b) Test circuit.

A 50V/200A power supply was used as input voltage source connected to the DC-link capacitor bank of a power stack ($\approx 4mF$). In series to that huge capacitor bank, a hand-made inductor was placed which was build using an industrial terminal block and making several turns around it. Finally, as DUT, the high-side IGBT of the previously presented IGBT modules (PrimePACK™3) was used. The test procedure was to charge the capacitor bank with 50V and once this was charged, a single pulse of 30 μs was applied to the gate of the IGBT, whose current was ramped up thanks to the inductor. The 30 μs pulse was used because the lack of cooling system. The obtained measurements can be seen in Fig. 4.12.

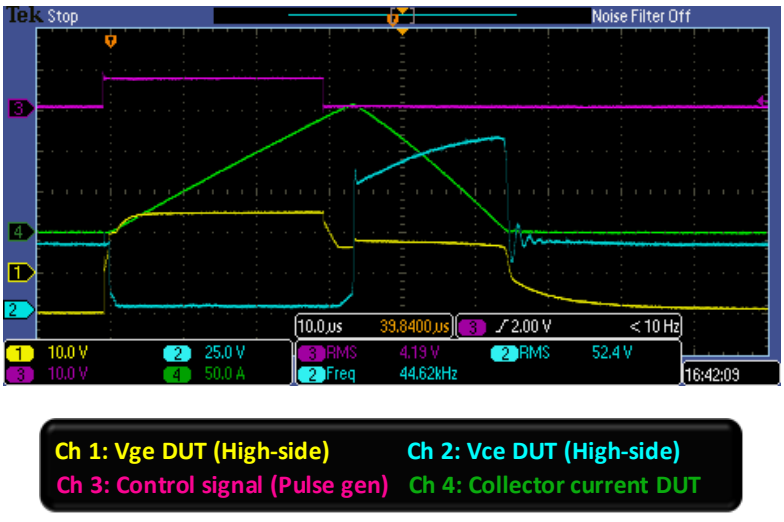


Figure 4.12. Measured waveforms during the test and demonstration of the advanced active clamping functionality after customization.

The results show that the active clamping is activated and, thus, this solution may have been successful. However, considering that the system runs with 10 IGBTs, the customization of these gate drivers could carry mistakes which lead to damage them and decrease other functionalities of the device. Moreover, by building a local protection of the NI9215, the rated active clamping level of 1200V can be maintained in case of unexpected overvoltage levels.

4.3.2 Local overvoltage protection of the NI 9215

The overvoltage protection (OVP) circuit installed in the NI9215 modules must be tested both out of the system and during operation to ensure its correct performance. The equivalent circuit diagram of this interface board was depicted in Fig. 3.32b (Section 3.3.3.2, page 55).

To test if the implemented design is correct, the PCB has been tested outside of PC test setup and testing each of the V_{CE} measurements separately. A picture of the test setup can be seen in Fig. 4.13a. Instead of the V_{CE} measurement, a GW-Instek GFG-8216A function generator was connected to the inputs of the PCB providing pulses of variable length to test the diodes under continuous clamping. This pulse generator could provide 15V output and, therefore, it was suitable for the test since the NI9215 module input range is 10V, and the OVP aims to clamp voltage levels over 9V. The test circuit can be observed in Fig. 4.13b.

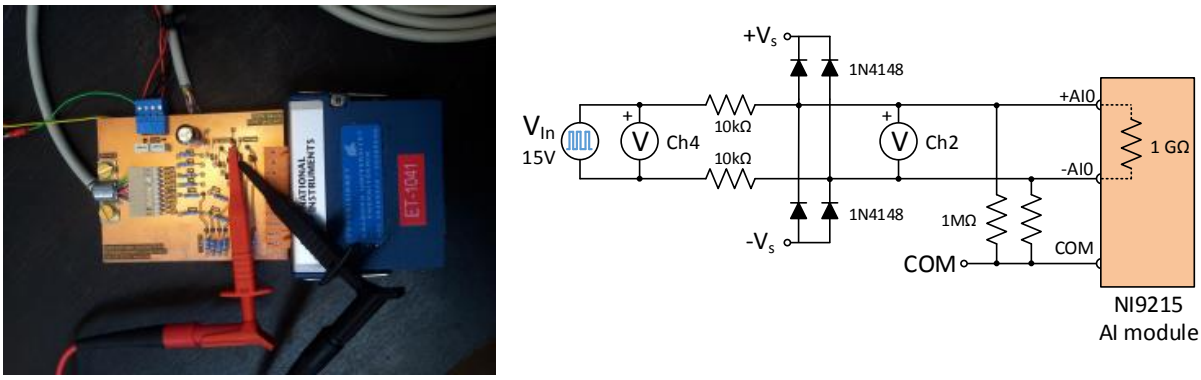


Figure 4.13. Test on OVP circuit (out of PC setup): (a) Test setup picture, (b) Test circuit.

The measured values were, V_{input} (V_{CE} while operation) which corresponds to the output of the signal generator and was monitored directly in the oscilloscope by a BNC cable, and V_{output} ($V_{CE,LabVIEW}$) which is the signal going to the NI9215 Analog Input module. The latter was measured with a Tektronix P5200A Differential Probe. The clamping voltage level was adjusted to 9V. The results are shown in Fig. 4.14

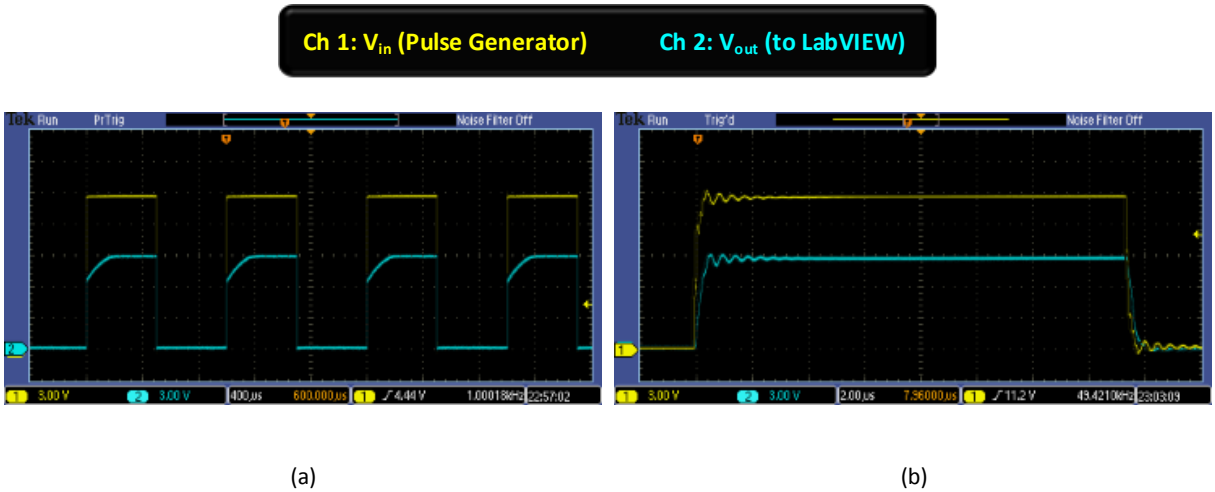


Figure 4.14. Measured waveforms to verify the effectiveness of the clamping voltage: (a) 500 μs pulse, (b) 15 μs pulse.

It can be observed that the overvoltage protection is working properly and that the voltage is clamped at approximately 9V, as expected.

Regarding the effectiveness of the OVP circuit during operation, the measured results can be observed in the next section where the data acquisition and measuring system is validated. In the results shown in Fig. 4.17c, it can be observed that the peak of the overvoltages never surpasses the clamping voltage, whereas the measured overvoltage in Fig. 4.10 (Section 4.3) was at least 12.2V. This means that the OVP circuit works correctly while system operation.

On the other hand, it was commented in Section 3.3.3.2 that 2 series resistors of 10 $k\Omega$ were placed in the inputs of the V_{CE} measurement to limit the current while diode conduction. These resistors may introduce an error on the V_{CE} measurement which is not desired because of the necessary accuracy (50 mV error would be translated in 14°C error). To verify this error, the input V_{CE} coming to the circuit and the output V_{CE} going to LabVIEW were measured and monitored both with an oscilloscope and in the LabVIEW GUI. The input voltage was given by a Laboratory DC power supply and was fixed at 4V (checked with a multimeter). The obtained measurements are shown in Fig. 4.15a (Oscilloscope) and Fig. 4.15b (LabVIEW GUI).

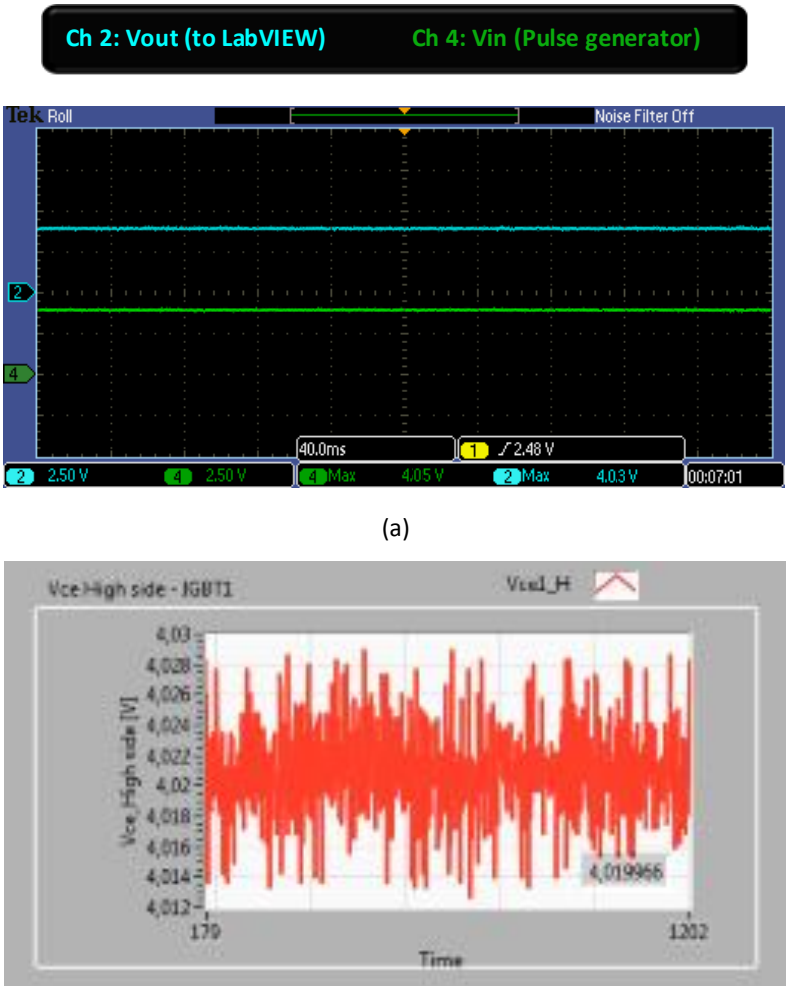


Figure 4.15. Measured V_{CE} at the input and output of the OVP board: (a) Results in the oscilloscope, (b) Results in LabVIEW.

By looking to the measurements added to the oscilloscope (Max. value measurements in Fig. 4.15a), it can be observed that the error between input and output is 10 mV. However, these values were double-checked with a Digital Multimeter and only 5mV of difference were found (with 3 digits of precision). Also the input DC voltage was adjusted to 4.000V before starting the test, which leads to consider possible offsets in the measurements shown in the oscilloscope (4.050V).

Regarding the result obtained in LabVIEW, it has -30 mV error with respect to the input voltage, however, the error introduced by the resistor as well as possible offsets can be corrected by means of software to the V_{CE} value that is monitored and stored.

4.3.3 Effectiveness of decoupling inductor and snubber diode

The last component to protect the test setup against overvoltages is the decoupling inductor placed between the DC power supplies and the laminated busbars. As explained in Section 3.3.1.2 (page 42), a snubber diode has been placed in parallel with the inductor to provide an alternative current path for the energy stored in the inductor which must be released (i.e. in case of open-circuit in the system).

The effectiveness of the snubber diode has been tested by measuring its current during an overvoltage transient, as shown in Fig. 4.16.

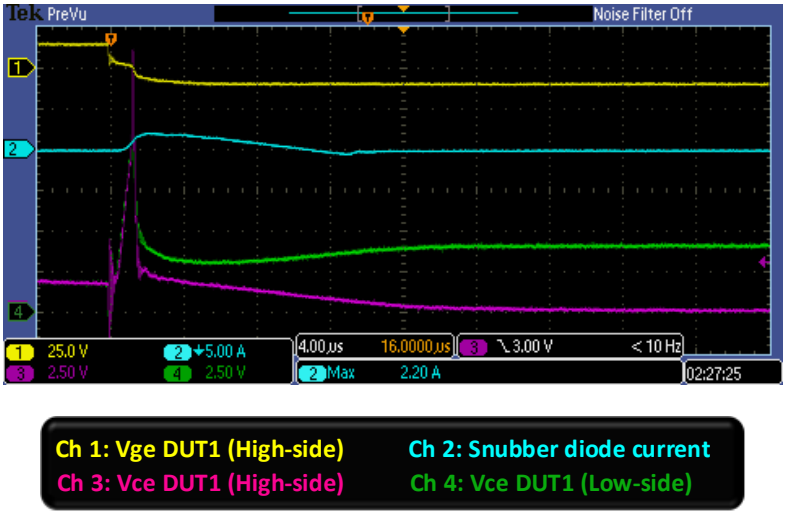


Figure 4.16. Measured waveforms for the demonstration of the effectiveness of the snubber diode.

4.4 Data acquisition and monitoring system

In this section, the data acquisition and monitoring system regarding the electrical parameters and temperatures is verified. First, V_{GE} and V_{CE} measurements have been carried out at DUT7 using differential probes and monitoring them with an oscilloscope. The I_C which is measured with the 4000A LEM module is compared with the current seen from Web interface that is available by the DC supplies. The low offset of 10A is introduced from the LEM and is corrected manually. Finally, all results are validated from the corresponding measurements taken with LabVIEW. In Fig. 4.17, 2 given pulses ($I_C = 1000A$, $t_{on} = 2sec$ and $t_{off} = 4sec$) are shown from the oscilloscope and the GUI in the host PC both for the same instance.

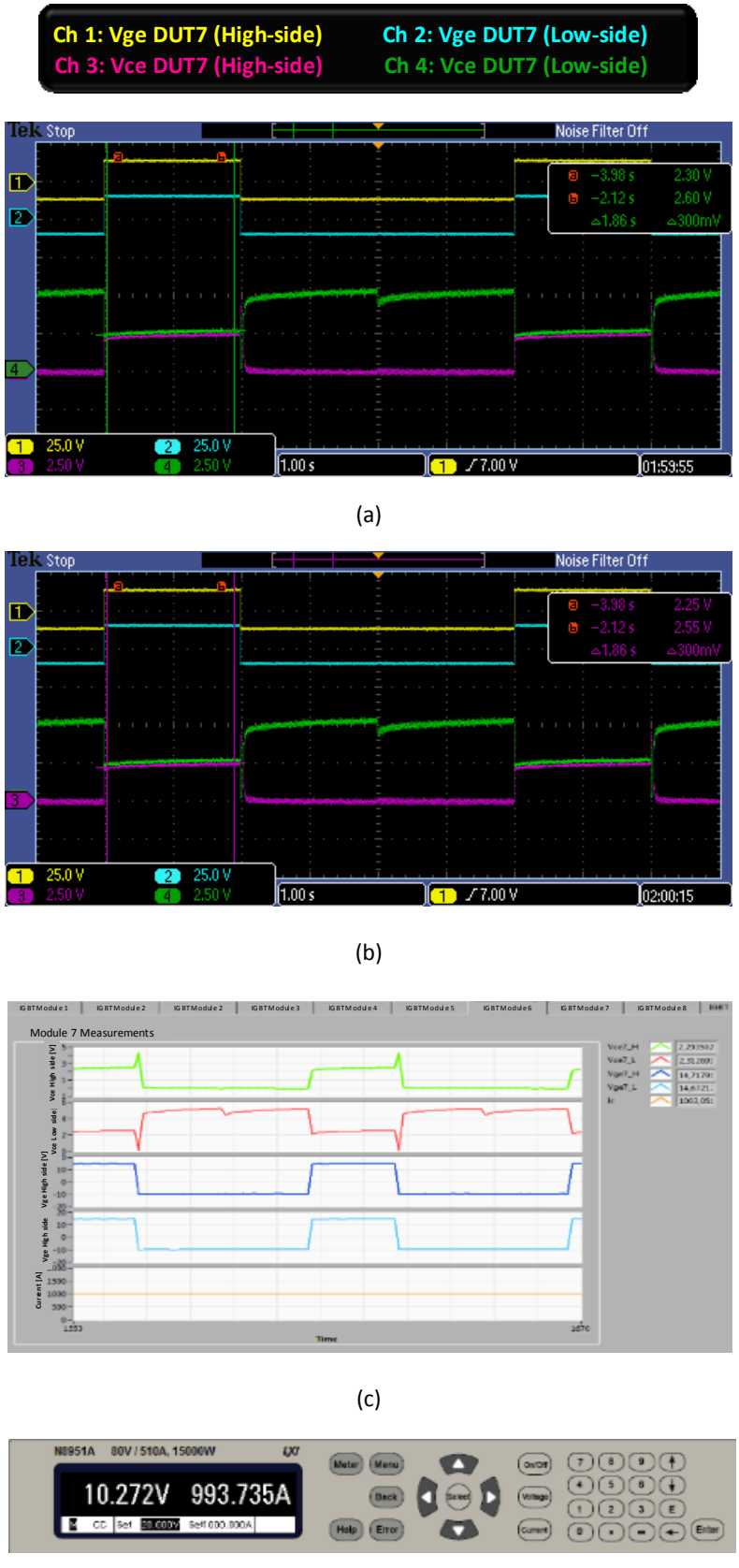


Figure 4.17. Two consecutive pulses of $I_C = 1000A$,$t_{on} = 2sec$ and $t_{off} = 4sec$ shown for DUT7 with: (a) cursors at $V_{CE,high}$, (b) cursors at $V_{CE,high}$ and (c) plots seen from LabVIEW GUI. In (d) Full DC current value as seen from the Web interface of DC supplies.

For a more clear depiction of the measured voltages by the NI LabVIEW modules, the samples are plotted in Fig. 4.18. The sampling frequency is set at 10Hz giving 20 samples during 2 sec pulse. However, higher sampling speed is needed in order to obtain the same values indicated by the cursors of the oscilloscope in Fig. 4.17a and b.

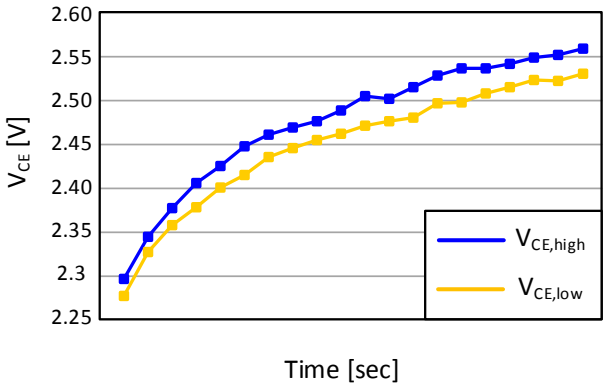


Figure 4.18. V_{CE} measurements during 2sec pulse obtained from Labview for DUT7.

In addition, calculated values for the junction temperature and power dissipation are provided continuously from the LabVIEW GUI as shown in Fig. 4.19. However, the temperatures can only be validated by the accuracy of the estimation method itself as explained in Section 5.2.1. It should be noticed that all measurements concerning V_{CE}, Tvj and P_d have meaning only during the on state of the IGBT switch.

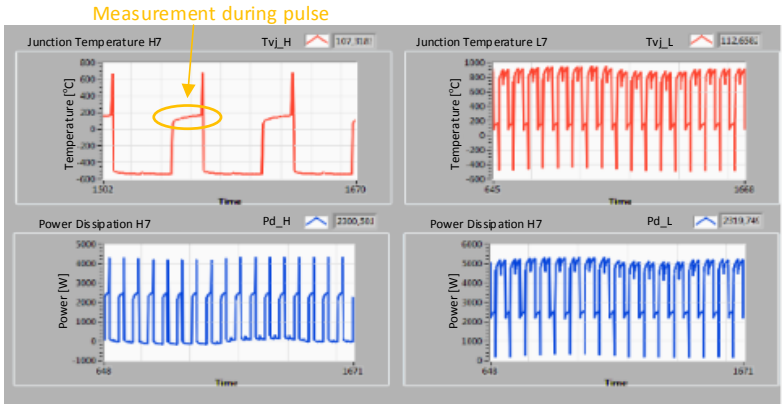


Figure 4.19. Junction temperature and power dissipation monitoring in the LabVIEW GUI.

4.5 Maximum allowable DC current

The PC test setup has been designed to supply a current up to 2000A so that different operating points for accelerated wear-out of IGBT modules can be implemented. Such a high current level implies taking some considerations into account regarding the thermal behaviour of the power circuitry, moreover, when the setup should provide a continuous and reliable operation 24/7. In Section 3.3.1 (Chapter 3, page 41), the designed components for the power supply circuit (rigid, flexible and laminated busbars) were presented. The maximum allowable temperature rise of these components was set to $105°C$. Therefore, this section presents the verification of the temperatures on the most crucial points of the power circuitry.

The maximum allowable current achieved in operation (Power-cycling pulses with $t_{on} = 2s$ and $t_{off} = 8s$) has been 1200A. Several pictures regarding the above-mentioned components, which were taken with the FLIR® thermal camera located in the *Reliability garage*, are presented in Fig. 4.20.

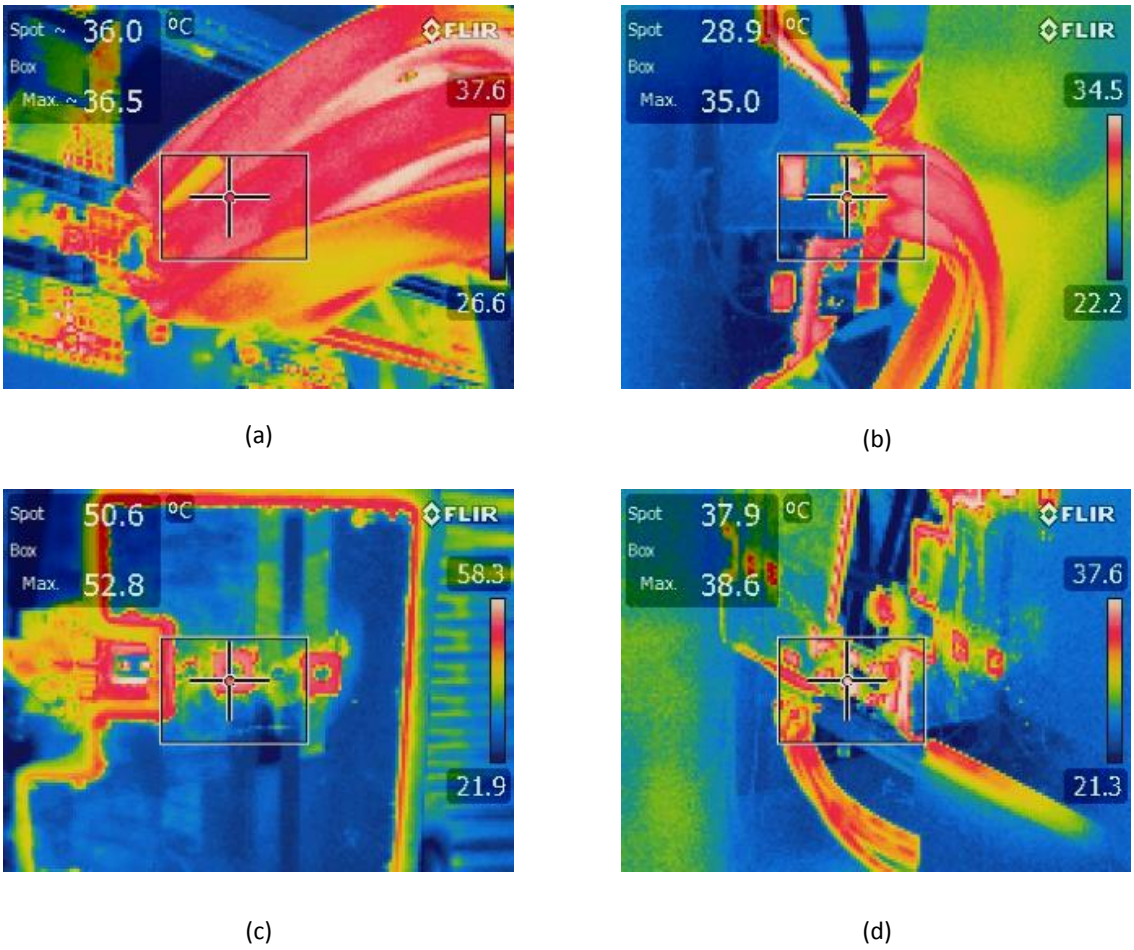


Figure 4.20. Temperature distribution at 1200A: (a) Rigid and flexible busbars on DC supplies output, (b) Input positive terminal of laminated busbars, (c) Screws on laminated busbars connecting to IGBT module, (d) Interconnection between busbars and flexible busbars for current return.

As depicted in the above figures, the temperatures on the analysed spots are well below the maximum limit ($105°C$) at 1200A, which is considered a positive outcome. One of the points to take into account for future current increments is the silicon cover around the laminated busbar (Fig. 4.20c) which has reached a temperature of $\approx 52°C$.

The above results allow to state that current can still be increased until its rated value, without encountering any problem regarding the thermal behaviour of the power circuitry. However, this test at 1200A was conducted during 1 hour and was stopped because of a sudden breakdown of one of the IGBT modules. Further investigations should be carried out before increasing the current. The temperature monitoring system displayed a value of $T_{j,max}$ around $185°C$, which leads to affirm that the root of the problem was an excessive temperature stress within the device. Nonetheless, the temperature estimation is based on the method presented in Section 5.2.1 which is still under test and, therefore, the causes of this failure are still not clear.

Finally, because of the sudden failure while running 1200A, it was decided to maintain the testing current level at 1000A which has demonstrated reliable operation during the 22h of wear-out test.

Junction temperature estimation methods 5

This chapter discusses the methods to estimate the junction temperature in IGBT modules. Firstly, a review of the different methods presented in the literature is given. Then, two methods, one based on datasheet and one based on the thermal impedance, are implemented and the results are depicted. In addition, the process to calibrate the collector-emitter voltage with the temperature is described as a possible method to be performed in the PC test setup. Finally, a suggestion on the procedure to determine the thermal impedance of the device is also provided.

5.1 Literature review and theoretical analysis

The monitoring of the IGBT junction temperature is one of the most crucial functions in a modern power converter operation in terms of thermal management and reliability. The awareness of the thermal behaviour of the IGBT modules allows their operation to be maintained below the specified maximum temperature limits. Moreover, temperature measurements are necessary input data for the lifetime estimation models. For these reasons the accurate determination of the junction temperature becomes imperative.

Many different methods have been proposed in literature to determine the chip temperature and they can be classified as:

- Direct measurements on the chip using thermocouples or IR camera
- Temperature estimation using thermal models and load conditions
- Estimation of the temperature by measure the Temperature Sensitive Electrical Parameters (TSEP)

The direct measurement of the junction temperature using a thermocouple attached straight on the chip is one method that provides continuous monitoring of the temperature and is used for laboratory purposes, usually as reference to validate other methods and thermal models. However, handling measurements with the thermocouple sensor needs to penetrate the cover of the module and attach it properly on the chip. The sensor itself and the glue material add thermal resistance and capacitance which affect the measurement accuracy and response. Also special care should be taken to avoid EMI and short-circuits [45]. The use of IR camera is a possible solution. Another method to estimate the junction temperature indirectly is to calculate first the power losses of the IGBT (switching and conduction losses). Then, using the thermal impedance parameters R_{th} and Z_{th} of the IGBT assembly and the base plate or DBC temperature (usually in Infineon P3 modules a Negative Temperature Coefficient (NTC) resistor is attached on the baseplate), the determination of the chip temperature can be achieved. A schematic diagram of this process is given in Figure 5.1. The thermal impedance

parameters are provided by the manufacturer but these values can vary from one module to another [46]. Thus, a full dependency on these values could lead to inaccuracies. In addition, it should be considered that these values are changed as the degradation process goes on and the span life of the module is reduced. For this reason the parameters should firstly be extracted, and later be updated in different phases of the wear out [47].

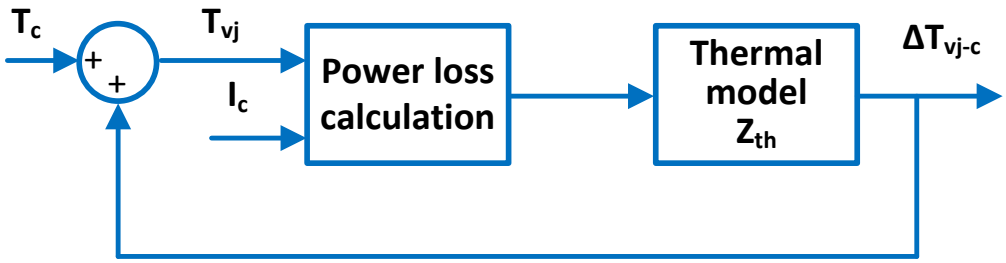


Figure 5.1. Schematic diagram for the junction temperature estimation using the thermal model of the IGBT module.

According to this method, the estimated junction temperature is given by Equation 5.1

$$T_{vj}(t) = \Delta T_{vj-c}(t) + T_c(t) \quad [^\circ C] \tag{5.1}$$

Where $T_{vj}(t)$ is the estimated junction temperature value, $T_c(t)$ is the measured value of the base plate and $T_{j-c}(t)$ is the temperature difference from junction to case which is calculated according to the power losses by the thermal model (rewritting Eq. 2.13):

$$\Delta T_{vj-c}(t) = P_d(t) \cdot Z_{th,j-c}(t) \quad [^\circ C] \tag{5.2}$$

The third approach, presented in the beginning of this section, uses the TSEP of the IGBT module to estimate the junction temperature. These parameters are temperature dependent and they can be used as temperatures indicators without any modification on the device package. Different TSEP such as the gate-emitter threshold voltage $V_{GE,th}$ [48], collector-emitter saturation voltage $V_{CE,sat}$ [23, 46, 47, 49, 50], turn on $t_{d,on}$ and off $t_{d,off}$ delay times [51], have been already used in research. Each of these parameters has different temperature dependency and in any case a calibration curve is needed to be applied in real operation conditions. Here, the method which uses the collector-emitter saturation voltage will be explained in more details.

The on-state voltage drop of an IGBT semiconductor is a function of the collector current I_c, the junction T_{vj} temperature and the gate-emitter voltage V_{GE}. By assuming that V_{GE} is maintained constant during the on-state, the T_{vj} can be estimated if the relation between V_{CE} and T_{vj} is found for a specific I_C: $T_{vj}= f(V_{CE}, I_C)$. In this case the V_{CE} shows a non-linear behaviour with respect to temperature and the collector current. Moreover, the temperature coefficient is negative for small current values and positive for higher collector currents [50]. This behaviour can be observed in Figure 5.2.

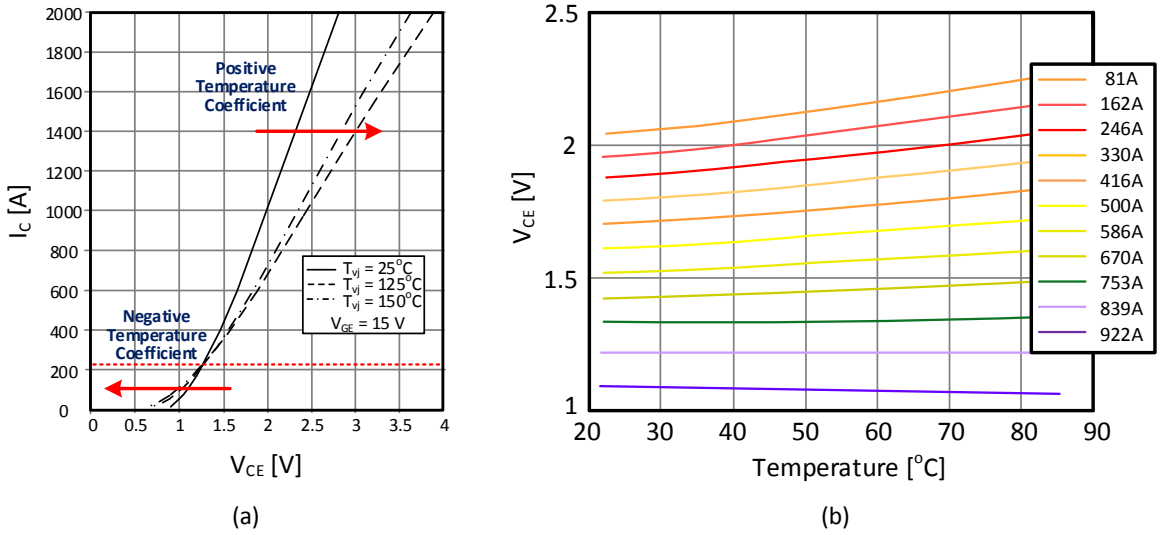


Figure 5.2. (a) I-V characteristic of 1700V-1000A IGBT module (FF1000R17IE4-Infineon) (b) Example of $V_{CE,sat}$ dependency on temperature for different load currents [50].

According to [46], the on-state voltage drop can be derived from the following equation (Eq. 5.3):

$$V_{CE,sat}(T_{vj}, I_C) = V_{CE,0} + k(I_C) \cdot (T_{vj} - T_{vj,0}) \quad [V] \tag{5.3}$$

where $V_{CE,0}$ is the collector-emitter voltage at a reference temperature T_{j0} and k is a value in function of the current, measured in $[V/K]$, and represents the ohmic resistance of the semiconductor.

Then, the junction temperature is calculated as in Eq. 5.4:

$$T_{vj} = \frac{V_{CE,sat}(T_{vj}, I_C) - V_{CE,0}}{k(I_C)} + T_{vj,0} \quad [°C] \tag{5.4}$$

In order to use the above relation, the $V_{CE,sat}$ voltage should be calibrated with respect to the T_{vj} temperature. Knowing the current level and measuring the V_{CE} voltage, the junction temperature can be found. This process is done by injecting small currents in range of milliamperes (e.g. 100mA) [17] or pulsing current values within the real operation range but which are not increasing the junction temperature [52]. For more accurate calibration, attention should be paid on knowing the real junction temperature during initial measurements. This can be done using a thermocouple attached on the chip. Moreover, the measurement system of the $V_{CE,sat}$ voltage has to provide the maximum accuracy for such small voltage levels and also be protected in case of high voltage transients during switching events, as already discussed in Chapter 3.

Finally, it was decided to implement two junction temperature estimation methods which are based on datasheet parameters. First of all, this decision was taken because of the ease to access the necessary data to implement the methods (I-V curves), which were not possible to obtain by means of experimental measurements, as will be explained in Section 5.2.4.

5.2 Implemented methods for junction temperature estimation

This section presents the implementation and validation of the 2 methods applied in the PC test setup. Additionally, a suggestion of the process to generate the I-V characteristics of the DUTs (FF1000R17IE4) is depicted.

5.2.1 Method 1: based on the I-V curves from datasheet

5.2.1.1 Overview

As initial approach, the junction temperature of the IGBT modules is estimated by using Eq. 5.3. For this equation, the reference temperature (T_{vjo}) is set at 25°C. The k factor and $V_{CE,o}$ are calculated as functions of the current (I_C) and these equations have been obtained after certain procedure based on the I-V characteristics which are provided in the datasheet [38]. Hence, the only unknown parameters for the temperature estimation are the I_C and $V_{CE,sat}$ which are measured continuously in this the setup.

The way that these relations have been extracted from the datasheet is explained as follows. Regarding $V_{CEo} = f(I_C)$ at 25°C, the function has been found using the Curve Fitting toolbox from MATLAB, approximated as ^{4th} order polynomial. Concerning the k factor calculation, three (V,T) points were extracted from the I-V curves, for each current level and for the three different temperature levels (25°C, 125°C, 150°C). Afterwards, the collected (V, T) pairs have been plotted as voltage versus temperature and they have been approximated linearly by Matlab Polyfit. Finally, the slope of each straight line corresponds to the k [V/T] factor for each current value. To calculate the k for any given current, the function $k = f(I_C)$ is approximated by a 3^{rd} order polynomial. The aforementioned steps are described visually in Fig.5.3 for better understanding.

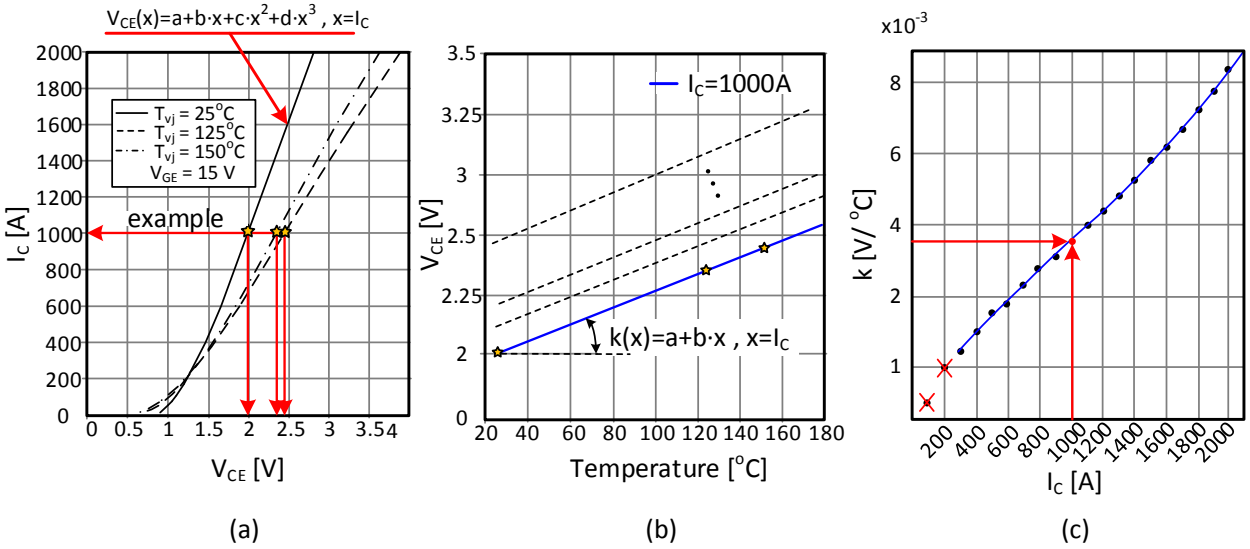


Figure 5.3. (a) I-V curves given in datasheet are found by CurveExpert tool, (b) The points taken from I-V curves are plotted in voltage to temperature graph, (c) k factor function is approximated by 4^{th} order polynomial.

It should be stated that this method is valid for current values above 300A. At 300A, the k factor is almost zero, therefore, Eq. 5.4 is not valid. This behaviour can be clearly seen in Fig.5.2a where the temperature coefficient is changed from negative to positive at currents around 300A. In addition, all curve fitting processes inserted small related errors (max.< 4%). The accuracy of the method is evaluated in Fig.5.4 which shows the calculated temperatures for different (I_C, V_{CE}) in comparison to the corresponding temperatures taken form the initial I-V curves. It can be observed that small errors of less than 7°C are achieved at high current values.

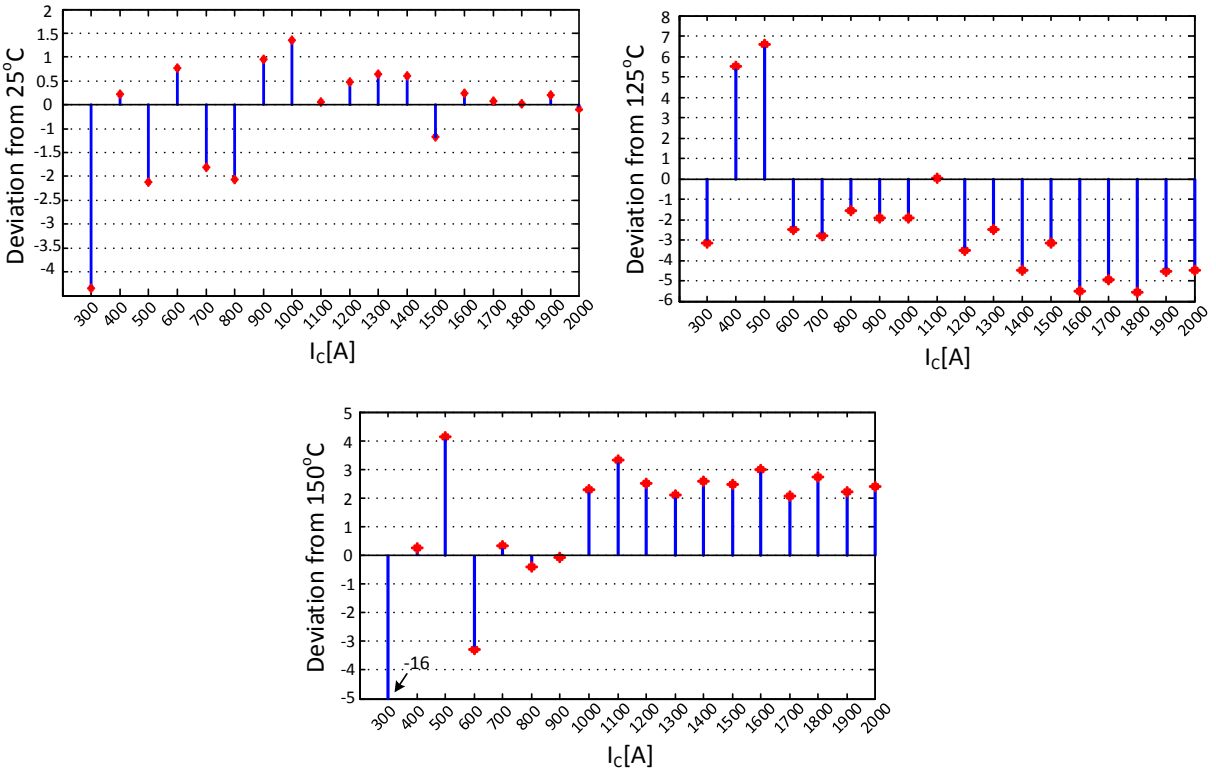


Figure 5.4. Temperature deviations in $^{\circ}C$ of the calculated values by Method1 from values given by datasheet.

5.2.1.2 Experimental results

The experiments have been carried out using 2 strings of the test setup (Fig. 3.13, page 41), which means 4 IGBT modules (DUTs 2, 3, 7 and 8), and the values of I_C and V_{CE} for high and low-side IGBTs have been measured as inputs for the temperature estimation method. The load current is set at 1000A, and the cooling system running at the rated operation point (VLT at 30 Hz, pump at 1720 rpm).

Resulted curves from the temperature estimation method based on the datasheet are shown in Fig. 5.5 and Fig. 5.6. They are referred to DUT8 and DUT2 respectively, both for high and low side IGBT chips, for 4 consecutive pulses of $T_{on} = 2$ sec and $T_{off} = 4$sec. Water temperature was measured at $T_{water} = 30^{\circ}C$ and the collector current I_C =600A for the DUT8 and $I_C = 1000A$ for DUT2. Tables 5.1 and 5.2 present the temperature variations observed during each pulse. It can be noticed that the low side IGBT chip at DUT8 has higher temperature levels and variations. One possible explanation for this behavior is that the low IGBT chip is at the upper side in the ShowerPower® where the water outlet is placed. Thus, an uneven heat distribution can cause temperature gradients even inside a single module.

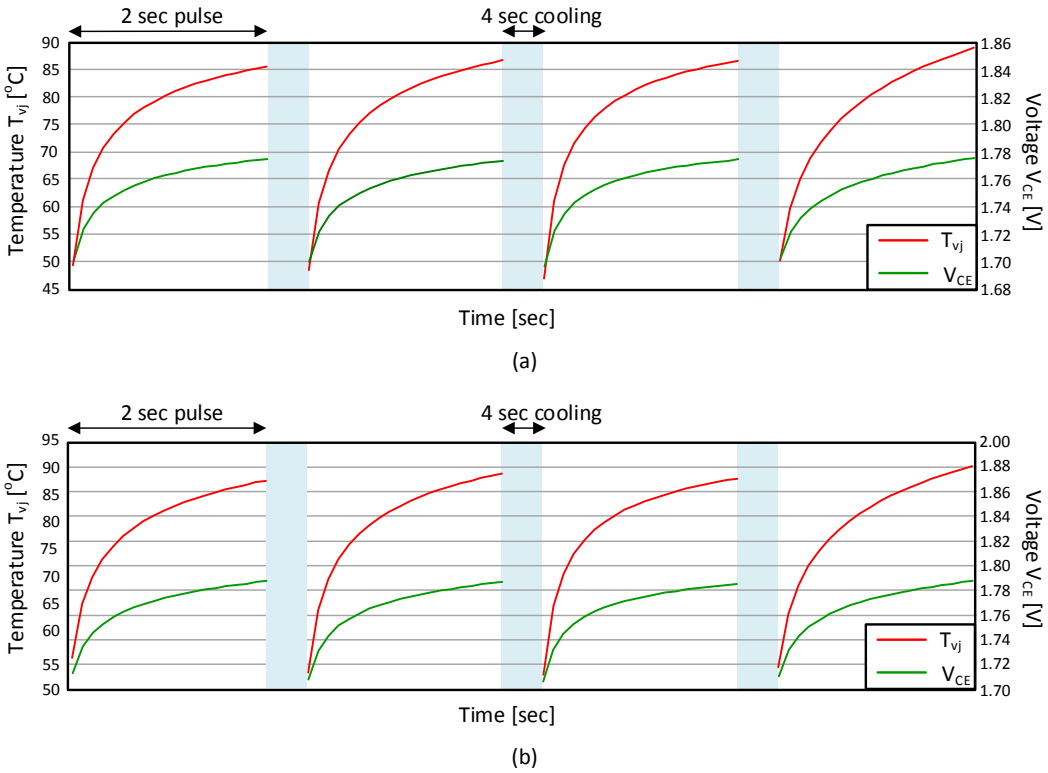


Figure 5.5. Junction temperature T_{vj} and collector-emitter voltage $V_{CE,sat}$ for: (a) DUT8 high-side IGBT chip, (b) DUT8 low-side IGBT.

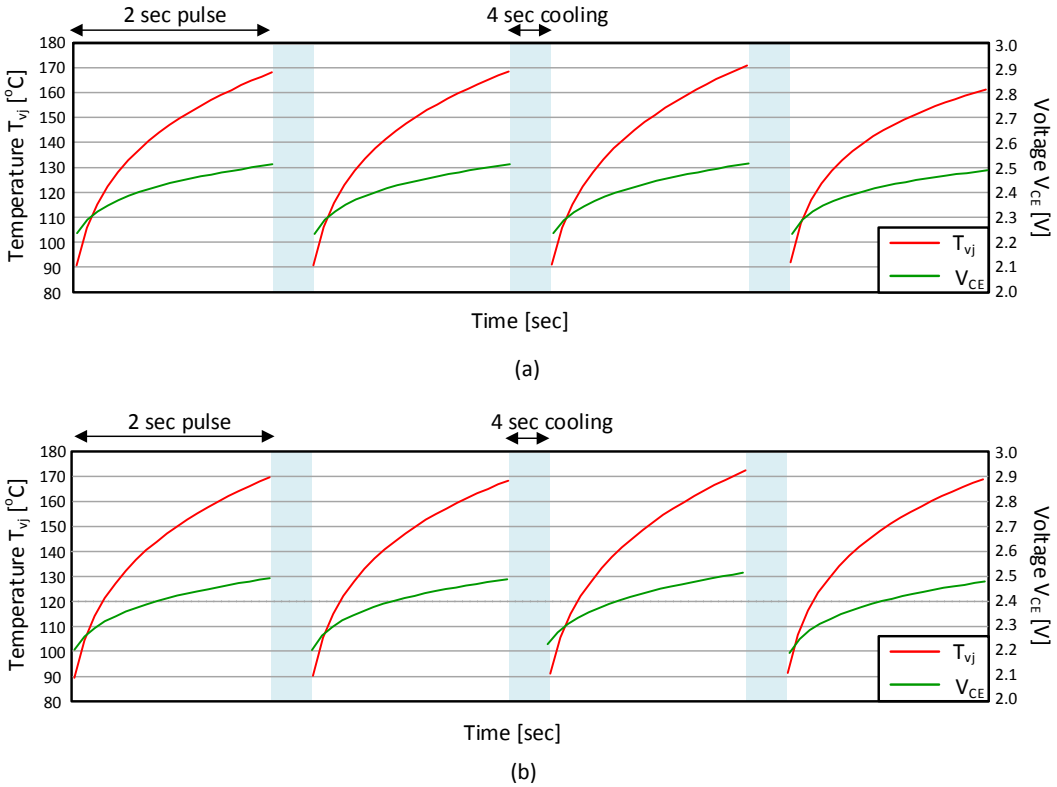


Figure 5.6. Junction temperature T_{vj} and collector-emitter voltage $V_{CE,sat}$ for: (a) DUT2 high-side IGBT chip, (b) DUT2 low-side IGBT.

Table 5.1. Temperature variations of DUT8 for 4 consecutive pulses, $T_{water,outlet} = 30°C$ and $I_C = 600A$

Temperature Swings ΔT_{vj} [°C]				
$\Delta T_{vj,high}$	36.1	38.1	39.5	38.6
$\Delta T_{vj,low}$	35.9	40.3	39.7	40.7

Table 5.2. Temperature variations of DUT2 for 4 consecutive pulses, $T_{water,outlet} = 30°C$ and $I_C = 1000A$

Temperature Swings ΔT_{vj} [°C]				
$\Delta T_{vj,high}$	77.2	77.5	79.9	69.2
$\Delta T_{vj,low}$	80.2	78.2	81.3	77.7

In addition, the power dissipations during a single current pulse for DUT8 and DUT2 respectively are shown in Fig. 5.7a and 5.7b, respectively. This power is dissipated from each IGBT chip and is responsible for the temperature increments.

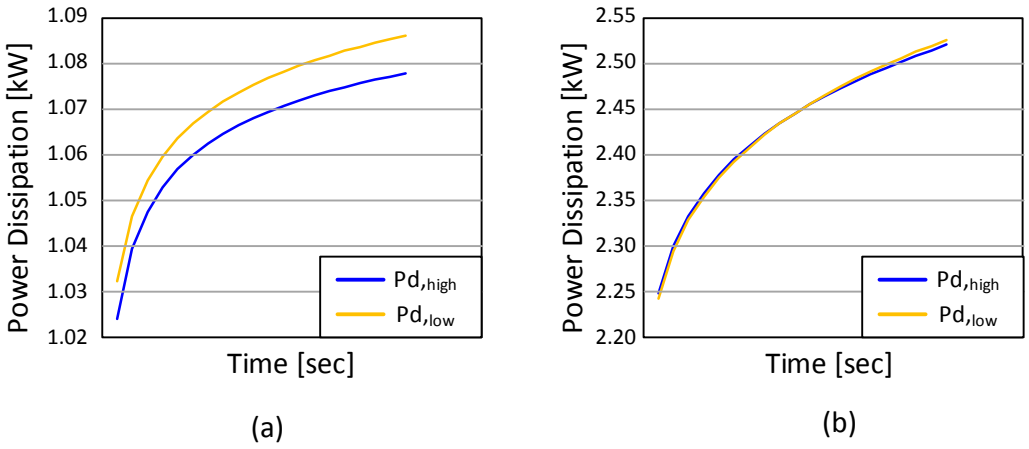


Figure 5.7. Power dissipated from high and low side IGBT chips during 2 sec single pulse of (a) DUT8, (b) DUT2.

Moreover, the thermal impedance $Z_{th,J-W}$ determines the temperature difference between junction and water for the corresponding power flow from chip to cooling device. Thus, in case that $Z_{th,J-W}$ and power dissipation are known, the chip temperature can be determined according to Eq. 5.2.

5.2.2 Method 2: based on the thermal impedance from datasheet

5.2.2.1 Overview

This method estimates the junction temperature taking into account the thermal impedance from junction to water ($Z_{th,J-W}$) which is resulted from the ShowerPower® cooling technology. According to Danfoss application note [53], the $Z_{th,J-W}$ at steady state conditions can be expressed by the empirical Eq. 5.5 for a single Infineon IGBT chip (SIGC186T170R3) as function of the water flow rate ($\dot{V}$ in l/min).

$$R_{th,J-W} = 0.48 \cdot \dot{V}^{-0.235} \quad [K/W] \tag{5.5}$$

The Infineon PrimePACK™3 IGBT modules consist of 6 parallel SIGC186T170R3 chips (Section 2.1) forming the one out of two IGBTs of the P3 package. The equivalent thermal network is given in Fig.5.8 without taking into account the transient response.

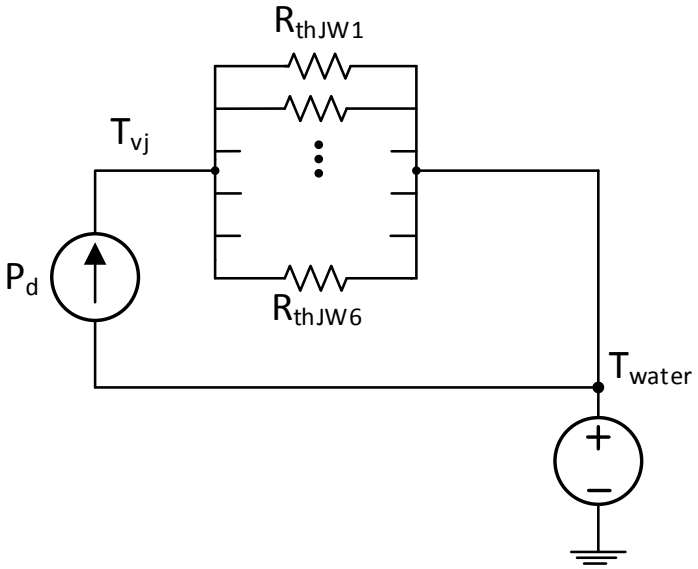


Figure 5.8. Simplified equivalent thermal network at steady state conditions for Infineon IGBT chip mounted on ShowerPower® module.

The water flow rates are continuously measured by flow sensors for each power module. An example is illustrated at Fig. 5.9b ($\dot{V}$=8.8 l/min). Hence, the R_{thJW} can be found using Eq. 5.5 or Fig. 5.9a.

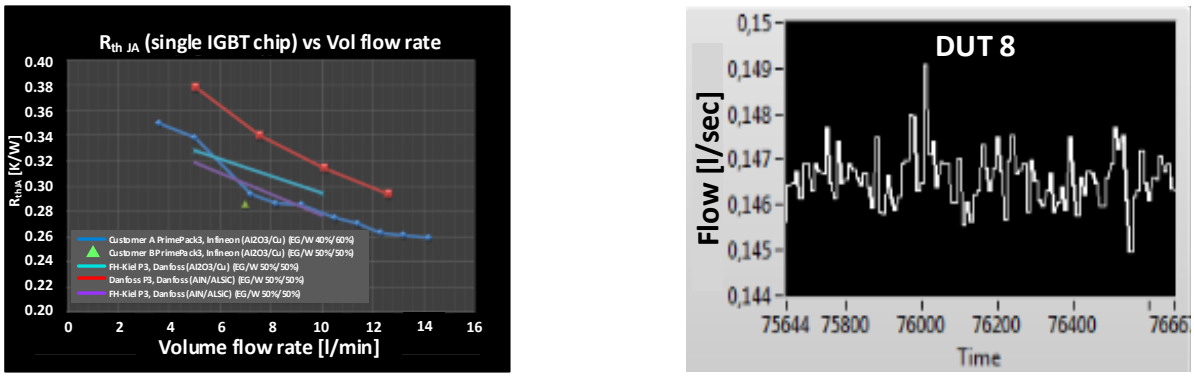


Figure 5.9. (a) Thermal resistance, junction to water for single IGBT chip [53], (b) Water flow measurement for DUT8 as seen from the cooling GUI (equivalent to 8.8 l/min).

5.2.2.2 Experimental results

The resulted maximum junction temperatures calculated according to Method 2 (using Eq. 5.2) are presented in Fig 5.10. They are referred to DUT8 which is loaded with $I_C = 1000A$ for $t_{on} = 2$ sec and duty cycle $D = 0.33$.

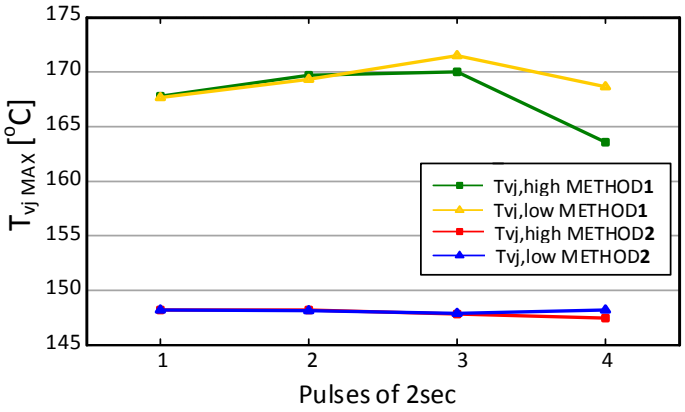


Figure 5.10. Maximum junction temperature of DUT8 calculated from Methods 1 and 2 for 4 consecutive pulses of 2 sec at $I_C = 1000A$.

5.2.3 Discussion on methods 1 and 2

At this point, a discussion on the results obtained from Methods 1 and 2 should be opened. As can be noticed from Fig. 5.10, the two implemented methods differ from one to another for about $25°C$, a fact that indicates an obvious inaccuracy of one of the two methods. Regarding method 1, it has already been proved that the method works properly for given datasheet I-V characteristics with an error of less than $7°C$ (Fig. 5.4). A possible explanation for this deviation is the obtainment of the V_{CE}, which in this setup is measured in the auxiliary terminals of the IGBT modules, taking into account all the voltage drops in the circuitry between chip and terminal. On the other hand, it is common practice of the manufacturers to measure on chip level. Therefore, the obtained V_{CE} on this setup will have a higher value than in reality. Similarly with method 2, higher junction temperatures than in reality are expected since the method uses as inputs V_{CE} and I_C (measured) and $R_{th,j-W}$ (obtained through the ShowerPower® application note, Eq. 5.5).

However, using the curves in Fig. 5.2b [52], which are experimentally generated for the same DUT, and extrapolating the relation of V_{CE}-T for an $I_C = 1000A$, a new operation point of DUT8 was estimated. This yielded a ΔT_{vj}= $70°C$ ($T_{vj,max} = 116°C$ and $T_{vj,min} = 46°C$), which approaches the result obtained with method 1, but offsetted to lower values.

5.2.4 $V_{CE,sat}$-T_{vj} calibration based on the generated I-V curves

5.2.4.1 Overview

The two previous methods allow the estimation of the junction temperature by measuring the V_{CE} and using the information provided in the datasheet. However, these methods can result in inaccuracies because of the differences between modules. Since all the modules are not 100 % identically manufactured, their I-V and Z_{th} characteristics may differ. Moreover, the ageing of the device leads to increase in V_{CE} and, therefore, a temperature estimation method which only relies on the initial measured values is not sufficient.

In order to have a proper thermal characterization of each module by means of the V_{CE} measurements, it is necessary to generate the above-mentioned I-V curves, or part of them, through experimental data. This method is known as calibration and it aims to measure the V_{CE} of the DUT at specific working temperatures for different current values. The procedure is as follows:

1. The device is heated up by means of an external heat source until the case temperature of the

device (T_C) has reached a constant value, i.e. steady-state conditions.

2. At the instant when the device starts to cool down, a current pulse is injected and V_{CE} is measured. The current pulse duration should be short enough ($\leq 100\mu s$) so that the device does not suffer any self-heating [45, 46].

3. The V_{CE} is measured again at the end of the cooling phase, prior to the new heating pulse.

4. Step 2 and 3 are repeated with different values of current for the same case temperature set in Step 1.

5. The entire process is repeated for different values of case temperature.

Regarding the above procedure, a few comments should be done in connection with the nature of the PC test setup presented in Chapter 3. Firstly, Step 1 cannot be performed by means of an external heat source with the actual layout of the setup. To overcome this issue, it has been decided to use the dissipated power in each of the devices as heat source of the entire system and, therefore, current will be continuously circulated through the system, until the necessary case temperatures are reached. In order to accelerate this process, the heat exchanger will be closed, so that heated coolant liquid flows through the different devices, achieving a more uniform heating. Secondly, as explained in the project limitations, the T_C of the module is not measured but the water temperature (T_{water}), which is measured by the flow and temperature sensor (Grundfoss VFS 1-20L G) placed in the outlet of the ShowerPower® (Section 3.3.4). Thus, T_C and T_{water} are assumed to be equal.

In addition, since the test setup is operated in a specific current level range for the accelerated wear-out of the IGBT modules, the calibration will be only carried out in the region marked in Fig. 5.11a. Besides the current range limitation (Y-axis), the working area for calibration is also limited by the maximum temperature that the cooling pipes can handle (80°C). Hence, the calibration will be performed for currents from 1000 to 1600A (200A steps) and for water temperatures from 25 to 80° (10° steps).

An overview of the calibration in a single module is shown in Fig. 5.11b.

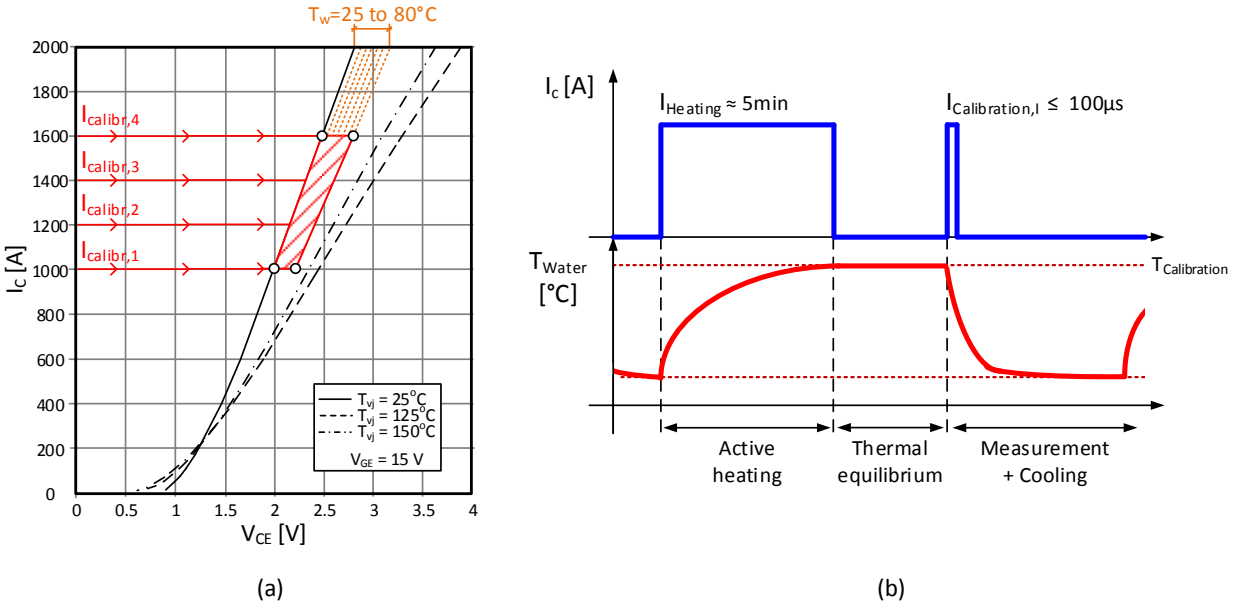


Figure 5.11. Overview of the calibration procedure: (a) Working area within the IGBT's I-V characteristics, (b) Load current and water temperature during calibration.

The load current is continuously injected until the entire system reaches the target temperature, or a few degrees above. At this moment, the current through the device under calibration is stopped so that the internal power dissipation does not keep increasing its junction temperature. If the water temperature across the device is kept constant during a few minutes, which is due to heating provided by the other strains, the calibration current pulse can be injected and V_{CE} is measured. This process is repeated for the different currents and different temperatures.

5.2.4.2 Implementation

The actual PC test setup topology consists in 5 parallel strings with 2 IGBT modules in each (10 modules). Therefore, in order to perform the calibration on all the modules in the most optimal way, the pulses shown in Fig. 5.12 are presented as concept.

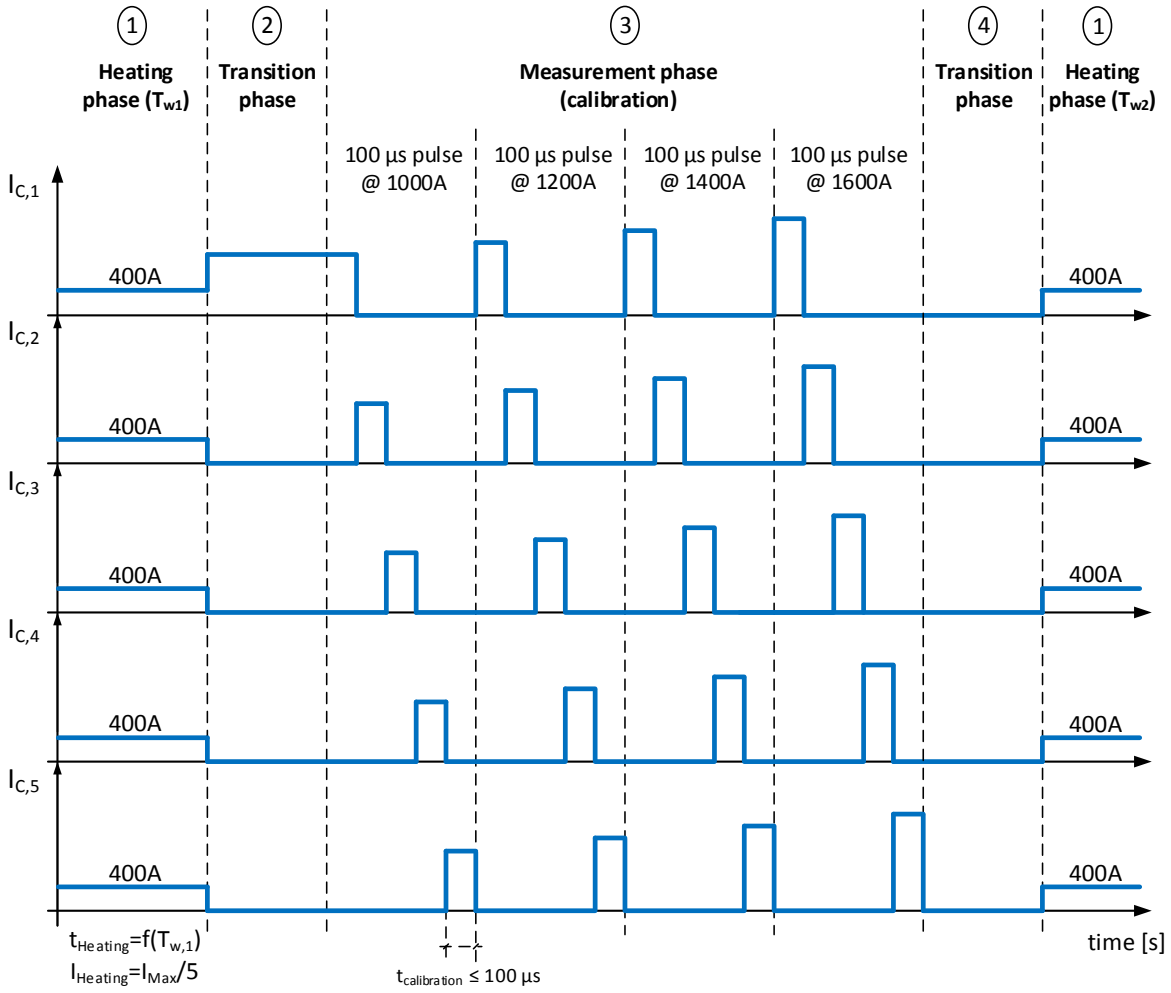


Figure 5.12. Testing routine (current pulses) in order to perform the V_{CE} calibration.

Regarding the above figure and its different phases, the process is described as:

1. **Heating phase (until $T_{water,1}$).**
   As described in the overview section, firstly, the water temperature should be increased by means of the circulating current which will cause power dissipation. This is done by turning on all the IGBTs at the same time (logic 1 in all the gates) and giving the maximum current of the supplies (2000A) which will be shared by 5 legs (400A each). Alternatively, the heating can also be performed by means of the typical PC pulses (2s on-time / 8s off-time). The water temperature is

measured by means of the VFS sensors placed in each of the outlets and monitored in LabVIEW.

2. **Transition phase**.
   Current level and gate control is modified during this phase. The supply current is adjusted from the previous 2000A for heating to the 1000A needed in the 1st calibration pulse. The gate control is changed from heating mode pulses to calibration mode pulses inside the LabVIEW program. Currently, this transition process is performed manually by the setup users.

3. **Measuring phase**.
   Once the current level is adjusted to the calibration target value (1000-1200-1400-1600), the 100 μs pulses are given. The value of V_{CE} is measured during the pulse. Due to limitations in the LabVIEW-based measuring system, which was designed to run in the Scan Engine ($\approx 500Hz$) and now μs sampling is needed, the monitoring is performed in a Tektronix DPO3014.

4. **Transition phase**.
   Similarly to phase 2, now the current and gate control is adjusted from measurement phase to heating phase. The gate control is automatically changed from calibration pulses to normal PC pulses.

5. **Heating phase (until $T_{water,2}$)**.
   Similarly to phase 1, the heating phase is performed until the new target T_{water} is reached. Then, the entire process is repeated.

The main contribution to this calibration is the generation of the PWM pulses for both heating and measurement phases. Therefore, 2 new modes have been added to the PWM pulses presented in Chapter 3 (Section 3.3.2.3, page 49).

The PWM pulses measured in the outputs of the NI 9401 module (DIO module) can be observed in Fig. 5.13. The PWM signal of Leg 5 is not included because of limited number of scope channels.

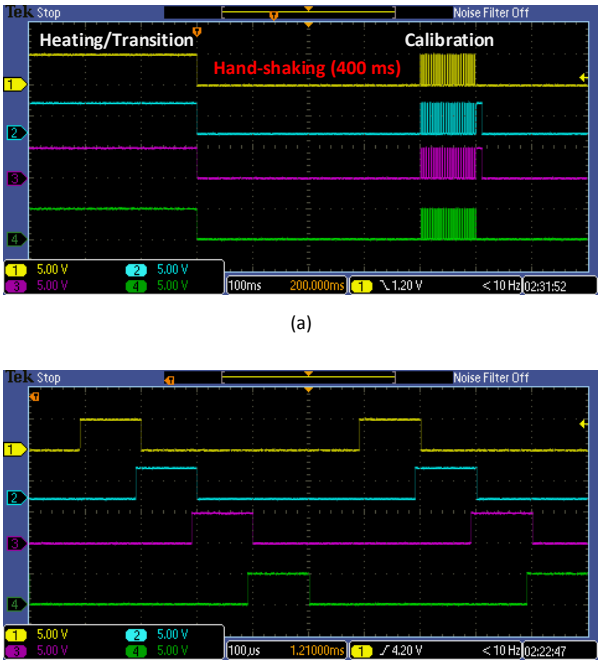


Figure 5.13. Measured PWM signals for calibration: (a) Complete pulse sequence including heating and calibration, (b) 100 μs pulses.

Preliminary tests of this method have been performed at 400 and 600A. However, a failure of one IGBT (DUT3 High-side) force to stop the test routine. The possible cause of failure is the handshaking shown in Fig. 5.13b which stop the current circulation during 400ms (between heating and calibration mode). Further investigations are needed for a more accurate diagnosis and for the modification of the PWM pulse generation code.

5.3 Determination of the thermal impedance

In Chapter 2, the thermal modelling of IGBT modules was presented. It has been shown that, using Eq. 2.13, the thermal impedance can be calculated for a given power dissipation P_d input and and for a known temperature difference ΔT. Usually, the thermal impedance given in datasheets is referred from junction to case, however, in this setup, the case temperature is not measurable by means of sensors but the water temperature is used as reference point. Therefore, Eq. 2.13 can be rewritten as:

$$Z_{th}(t) = \frac{\Delta T(t)}{P_d} = \frac{T_{vj}(t) - T_w(t)}{P_d} \quad [K/W] \tag{5.6}$$

This test setup is able to monitor P_d and T_w at any instant. At the same time, assuming that the actual junction temperature is obtained through the previously explained calibration method, the thermal impedance transient curve can be calculated. Subsequently, the $R_{th} - \tau_{th}$ parameters used for the Foster model (Section 2.2.2.2, page 18) can be extracted using, for example, the Curve Fitting toolbox from MATLAB.

Moreover, the obtainment of the thermal impedance could be used as validation of method 2, as the used thermal resistance ($R_{th,jw}$) has been taken from the experimental data given in the ShowerPower® datasheet. However, since the $V_{CE,sat}$-T_{vj} calibration process has not been completed in this report, the above procedure has not been carried out and, therefore, it is given only as a suggestion for future work.

Part III

Results and conclusions

Results on the wear-out of IGBT modules 6

In this chapter, the initial tests carried out in the power-cycling test setup regarding the wear-out of IGBT modules are presented. Firstly, the applied testing conditions are described and, subsequently, the obtained results are rendered.

6.1 Testing conditions

The power-cycling testing conditions for the wear-out of the IGBT modules are summarized in Table 6.1.

Table 6.1. Power-cycling test conditions applied for the wear-out tests

Power-cycling test conditions	
Load current, I_{dc}	1000 A
No. Active strings	2
No. Of DUTs	4
DUT	Infineon PrimePACK™3 (FF1000R17IE4)
t_{on}	2s
duty cycle	50%
VLT frequency	30 Hz

Compared to the test circuit shown in previous chapters, the number of DUTs has been reduced from 10 to 4 because of the breakdown of 3 IGBT modules during the preliminary testing period of the setup. The test circuit for the following wear-out tests is shown in Fig. 6.1.

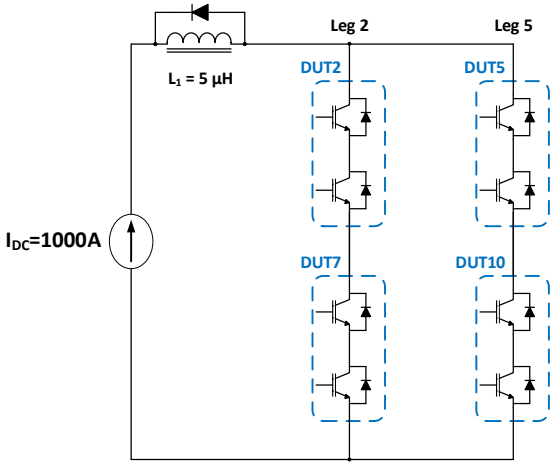


Figure 6.1. Test circuit for the initial tests on the IGBT modules

The process of wearing out the IGBT modules is strongly dependent on the applied temperature stresses, and previous results at Chapter 5 have shown that the temperatures differ from device to device. Table 6.2 summarizes the operating conditions for all the DUTs during the 4 days of testing period. The values in this table are representative of the whole period, however, slight variations may appear from one day to another.

Table 6.2. Testing conditions regarding the temperature stress in each of the DUTs. For each of the IGBTs in one DUT, the values are referred as High-side (H) and Low-side (L).

Wear-out operating point				
	DUT2 (H/L)	DUT5 (H/L)	DUT7 (H/L)	DUT 10 (H/L)
Load current, I_{dc} [A]	1000			
$T_{vj,max}[°C]$	113.99 / 114.28	111.70 / 112.70	112.27 / 114.99	112.12 / 111.24
$\Delta T_{vj}[°C]$	84.94 / 85.23	83.45 / 84.45	82.80 / 85.52	84.81 / 83.93
$T_{vj,mean}[°C]$	71.52 / 71.67	69.98 / 70.45	70.87 / 72.23	69.72 / 69.28
$T_{water}[°C]$	29.05 $°C$	28.25 $°C$	29.47 $°C$	27.31 $°C$
Flow rate [l/min]	8.90	8.70	8.70	8.80

The temperature estimation has been performed with the calibration curves from [52], as explained in Section 5.2.3, since this method based on experimental data gives more realistic results than the one based on the datasheet parameters. Moreover, it was assumed that the minimum junction temperature is equal to the case temperature, as it is described in the project limitations.

6.2 Experimental results

This section presents the first results regarding the wear-out of the IGBT modules. The results are presented in different sections for each of the DUTs (for both high-side and low-side IGBTs).

The tests have been carried out during 4 days, a total of 20.8 hours, which yields in 18746 cycles. These tests should be considered as a starting point to evaluate the performance of the whole system as a wearing-out platform and, therefore, debugging tasks were needed during this period. As a consequence, the results of Day 2 and 3 were affected by several system interruptions in order to fix minor issues (cooling system regulation, offset measurements, repair of cabling, etc.) and they have not been included.

In the figures below, the mean value of $V_{CE,sat}$ for each cycle (pulse on-time) has been plotted against the number of cycles. The measured values have been obtained through the LabVIEW data acquisition system. The raw data was collected in MS Excel files which were post-processed in a MATLAB script. Taking into account that each on pulse has 20 samples (2s duration at 100ms sampling), the principle of the script was to group the data in groups of 20 values, and reject the off time values. Afterwards, the mean value of each of the 20 on-state samples was calculated and stored in a vector.

6.2.1 IGBT module 2

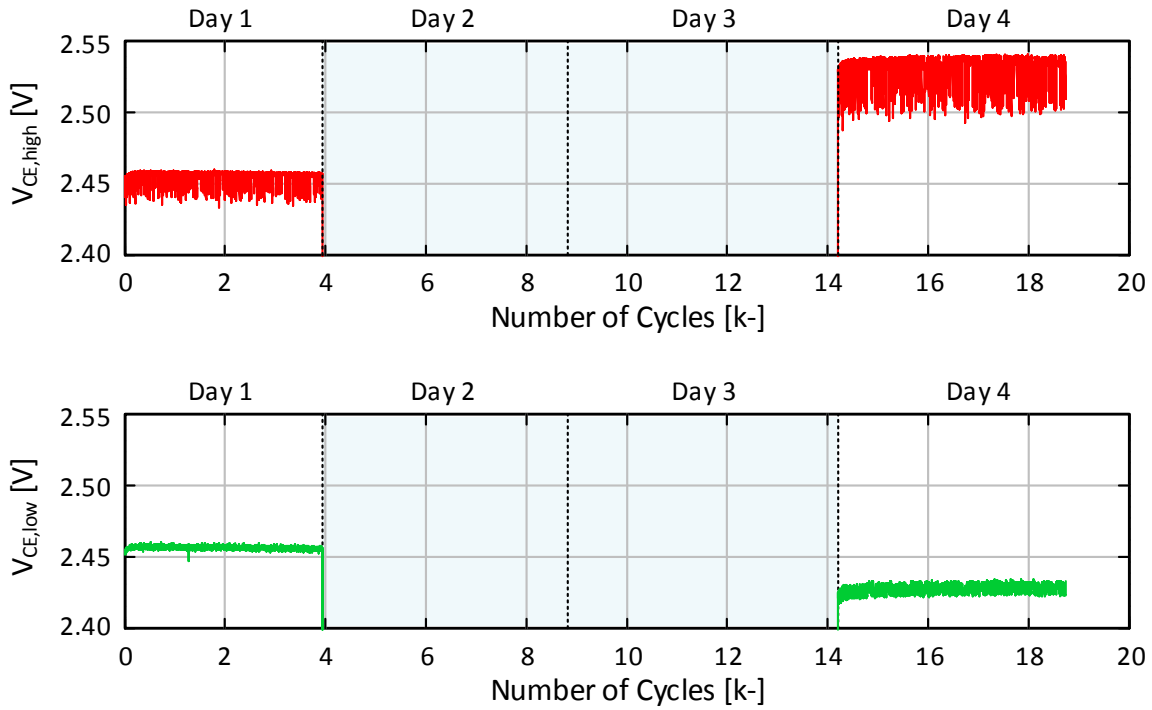


Figure 6.2. V_{CE} measurements for High-side and Low-side IGBTs of DUT2 during Day 1 and 4.

6.2.2 IGBT module 5

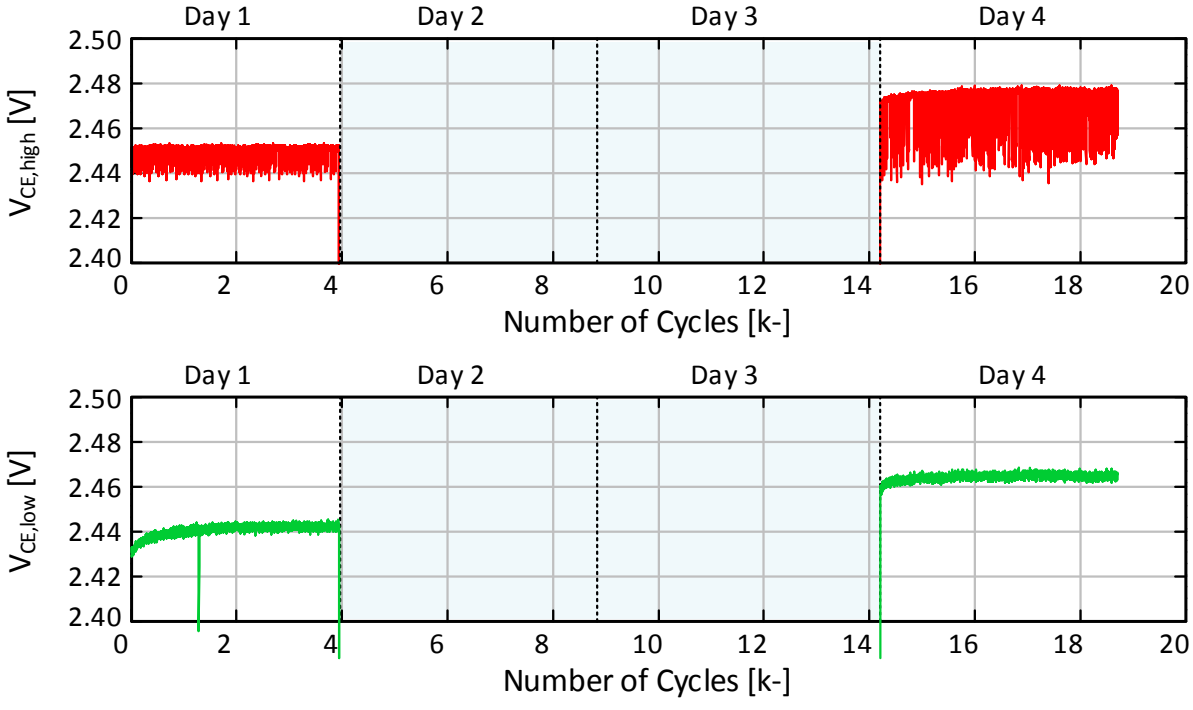


Figure 6.3. V_{CE} measurements for High-side and Low-side IGBTs of DUT5 during Day 1 and 4.

6.2.3 IGBT module 7

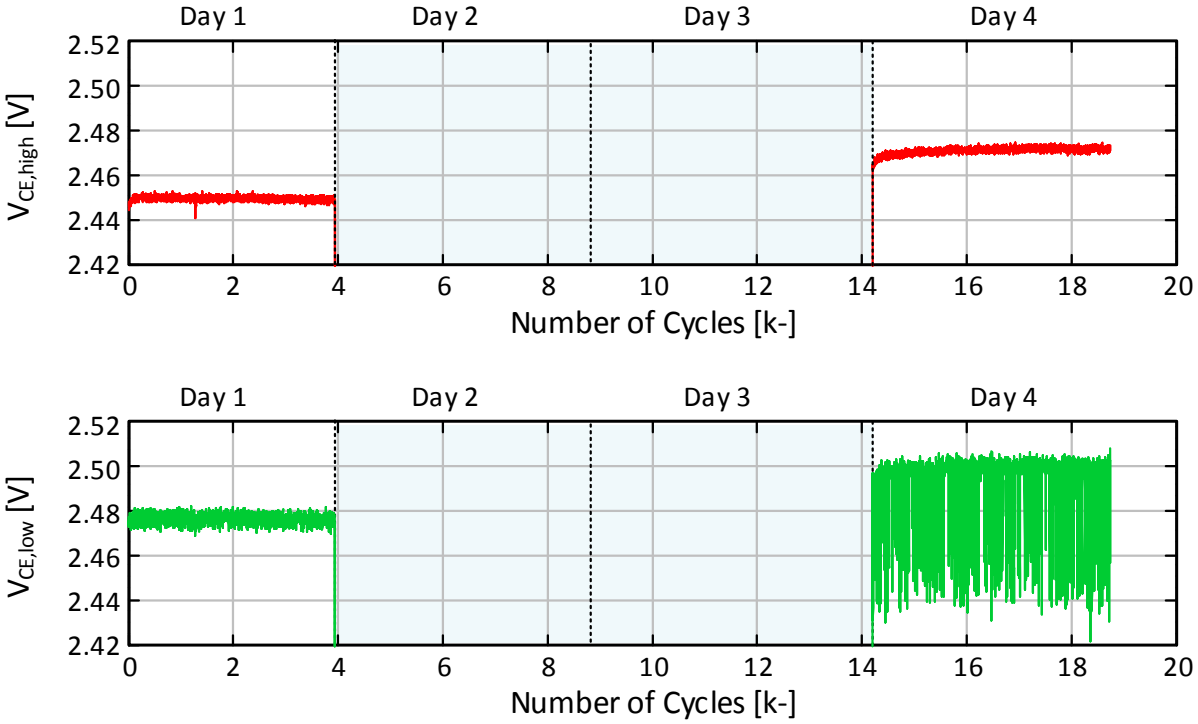


Figure 6.4. V_{CE} measurements for High-side and Low-side IGBTs of DUT7 during Day 1 and 4.

6.2.4 IGBT module 10

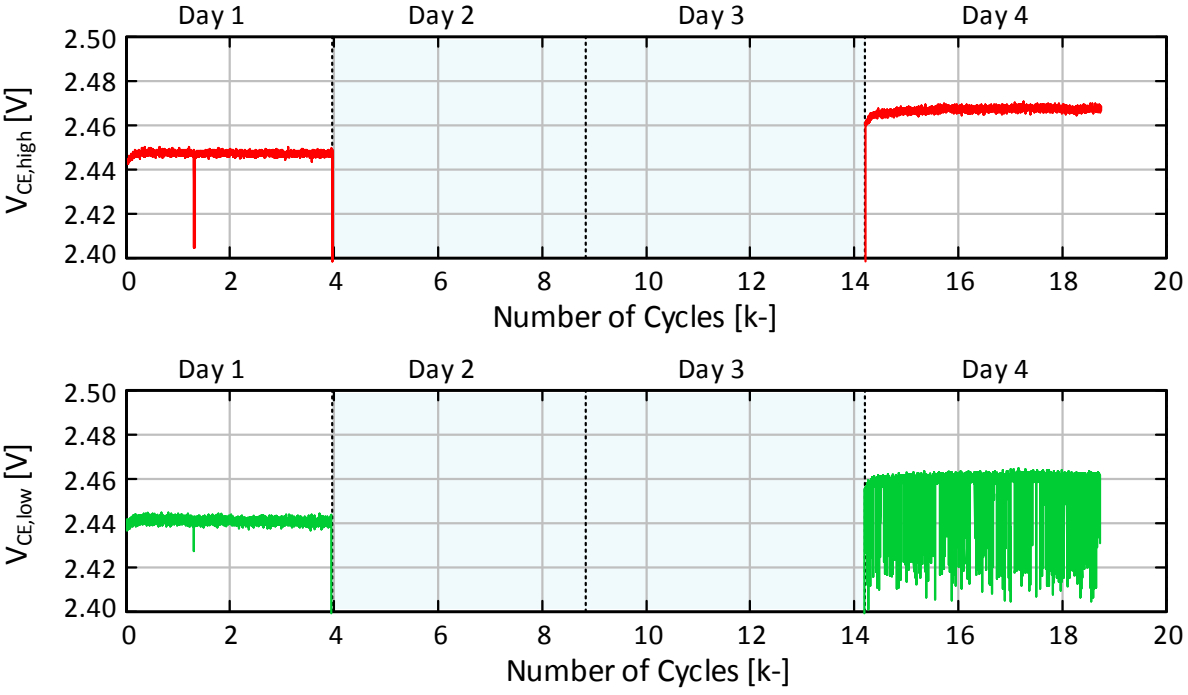


Figure 6.5. V_{CE} measurements for High-side and Low-side IGBTs of DUT10 during Day 1 and 4.

6.3 Discussion

During this short testing period, it was not expected any noticeable increment in the value of V_{CE}, however, a voltage increment between 20 and 90 mV was experienced in each of the IGBTs. This leaded to a further analysis of the operating conditions in order to investigate any possible divergences. Taking into account that the load current and pulse characteristics were kept constant during the entire testing period, the other factors that influenced the operating conditions was the performance of the cooling system. By observing Table 6.3, it can be realized that the value of the water temperature presents a higher value on Day, compared to Day 1, whereas the flow rates are constant. This fact justifies the difference on V_{CE} which is directly related with the thermal behaviour of the chip. A higher water temperature may offset the junction temperature swing and, therefore, the V_{CE}. On the other hand, this does not explain why the Low-side IGBT of DUT2 presents a lower value on Day 4 compared to Day 1. In order to address this problem, it is necessary to implement a closed-loop control on the cooling system which adjusts the flows according to a constant reference water temperature, fixed during the entire testing period.

Table 6.3. Water temperature and flow rate values for each DUT and test day

	DUT2		DUT5		DUT7		DUT 10	
	Day 1	Day 4	Day 1	Day 4	Day 1	Day 4	Day 1	Day 4
T_{water} [°C]	29,05	30,60	28,25	32,13	29,47	31,39	27,31	31,23
$Flowrate$ [l/min]	8,88	8,88	8,70	8,70	8,70	8,70	8,82	8,82

Conclusions and future work 7

In this chapter, the conclusions of this Master thesis, as well as suggestions on future work, are presented.

7.1 Conclusions

In the beginning of this report, it was emphasized that IGBT modules are one of the main components subjected to failures in high power converters. During converter operation thermal stresses are induced in the devices triggering failure mechanisms which lead to their final breakdown. The analysis carried out in Chapter 2 showed that power cycling (PC) test platforms are the most common setups to emulate thermal stresses and investigate the lifetime of the product. As a consequence of this analysis, certain objectives were established in order to develop a test setup which can wear-out IGBT modules in an accelerated way. These objectives were accomplished through the current work.

In this section, conclusions are drawn separately for each of the objectives and further discussions are opened.

- Design and implement a power-cycling test setup which is able to wear out IGBT power modules in an accelerated manner and describe its capabilities

First, the test setup was designed to be able to wear out up to 10 PrimePACK™3 IGBT modules and to provide DC current pulses up to 2000A so that multiple operating points could be applied in terms of ΔT_{vj}. The circuit topology and the gate driving system were designed to allow the adjustment of the on time and duty cycle of the pulses in order to have flexibility regarding the PC test conditions. Due to the switching with high current, a potential problem of this test setup was the appearance of overvoltages during the turn off transient. This problem was solved by designing and implementing laminated bus bars for the power circuitry of the DUTs, local overvoltage protection circuits for the measuring equipment and overlapping feature at the gate signals. The PWM pulses, as well as the data acquisition and monitoring system were implemented with NI LabVIEW. The logging system was designed to store a vast array of data which now is available for further processing. The high current level and scale of the setup implied many difficulties during the building process, both from mechanical and electrical point of view. However, all the above-mentioned capabilities were successfully applied.

- Conduct an acceptance test of the power-cycling test setup

In order to validate the proper operation of the test setup and to ensure that the PC requirements are fulfilled, several validation tests were performed. The overvoltages were measured and the results showed that they do not represent any critical issue for the setup operation. In addition, the protection circuits were tested and proved to work correctly. Regarding the gate signals, problems were encountered in the initial tests and they were solved after investigation. The data acquisition and

monitoring system implemented in LabVIEW behaves as expected and the most important parameters of the IGBT module can be constantly monitored and recorded in the host computer. The maximum current level that has been tested is 1200A which was shown to be safe from the thermal performance of the circuitry, verified by thermal camera measurements. Then, the current level was limited down to 1000A after a sudden breakdown of a DUT. Further investigation is still needed to figure out the root of the problem.

- Develop, implement and validate a junction temperature estimation method for IGBT power modules

From the experience gained during this project, it was realized that the determination of the junction temperature of the device is a crucial factor for the definition of PC test conditions and, furthermore, for the lifetime estimation of the DUT. Initially, the performed literature review suggested different methods to determine the junction temperature. Out of all, two methods were selected and implemented. The results indicated differences between the two methods, a fact that is believed to be caused not by the methods themselves but by the inputs obtained from the datasheets (I-V curves). Therefore, the I-V characteristics should be acquired from experimental data and for this purpose a possible approach has been suggested.

- Perform wearing out tests on the IGBT modules for subsequent lifetime investigation

The final goal of the PC test setup was to wear-out IGBT modules in an accelerated manner so that subsequent studies of the failure mechanisms can be performed. During the last stage of the thesis period, 4 IGBT modules have been tested under operation at 1000A for 18,740 cycles ($\approx$ 21h testing). However, it has been observed that interruptions during the test affect the consistency of the measurements and, therefore, continuous operation is suggested.

The estimated operating point, among the different DUTs, was $\Delta T_{vj} = 85°C$ ($T_{j,mean} = 70°C$) which was considered as a possible one to wear-out the modules in a short period. Until now, data has been collected and processed in MATLAB but no indication of failure or realistic V_{CE} increment has been observed. Hence, the wear-out process should be continued until a failure indication is appeared and more conclusions can be drawn.

7.2 Future work

The test setup is able to power cycle IGBT modules. From this point, new operating points with more extreme ΔT_{vj} should be tested and verified. Moreover, to validate the maximum current that can be provided from the DC power supplies (2000A), the testing of a more powerful DUT such as the 1400A PrimePACK™3 (FF1400R17IP4) is suggested. Furthermore, this setup was designed to simultaneously test 10 IGBT modules in approximately 1 week, which would lead to generate Coffin-Manson lifetime curves. The generation of these curves is another expected outcome which can be performed if the stress temperature operating point has been validated.

The implemented junction temperature estimation methods need to be validated. One solution that has been already suggested is to generate new I-V curves by means of this test bench using short pulses ($100\mu sec$) at the calibration current levels. However, a delay of the PWM generation code in LabVIEW during shifting from heating to calibration mode did not allow continuing this process. Therefore, more efficient and automated gate control system can be developed in order to calibrate during operation. Another approach is to perform direct measurements on chip level using a thermocouple or an infra-red camera.

Another capability of this test setup is the determination of the thermal impedance. As suggested in Section 5.3, if these temperature estimation methods are validated with experimental data, and the power dissipation and water temperature are monitored in LabVIEW, the implementation of the thermal impedance determination could be performed in software.

Regarding the hardware implementation, even though the laminated busbars have shown a proper performance, their design can be improved in order to have a more compact size. A suggestion on this design has been given in Fig. 3.18. As a limitation, enough space for the installation of the piping on inlet and outlet of the ShowerPower should be considered in new designs.

Also, the interface board of the CONCEPT gate drivers is currently used and it shows good performance during system operation. However, from the experience during the testing period, a few improvements are suggested both on the signal conditioning of the PWM signals and on the power supply of the drivers. The power supply of the gate drivers is set to 15V, however, the measured V_{GE} voltages on the 10 gate drivers differ by 100's of mV. The gate driver connectors are placed along the PCB with different distances between them, which is translated into different impedances and, therefore, different voltages. This fact is believed to affect the power dissipation of the IGBT module but it has not been experimentally validated. Regarding the hex buffer used to drive the signals, a similar IC but with open-collector outputs, such as the SN7407N, in combination with a pull-up resistor connected to 10-15V is recommended.

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Part IV

Appendices

Power-cycling test setup, Sven A

This brief appendix presents a picture, the equivalent diagram and the DUT designation of the test setup in order to familiarize the reader with the system layout. A part of the test setup implementation described in Section 3.3 (Chapter 3, page 41) can be observed in Fig. A.1.

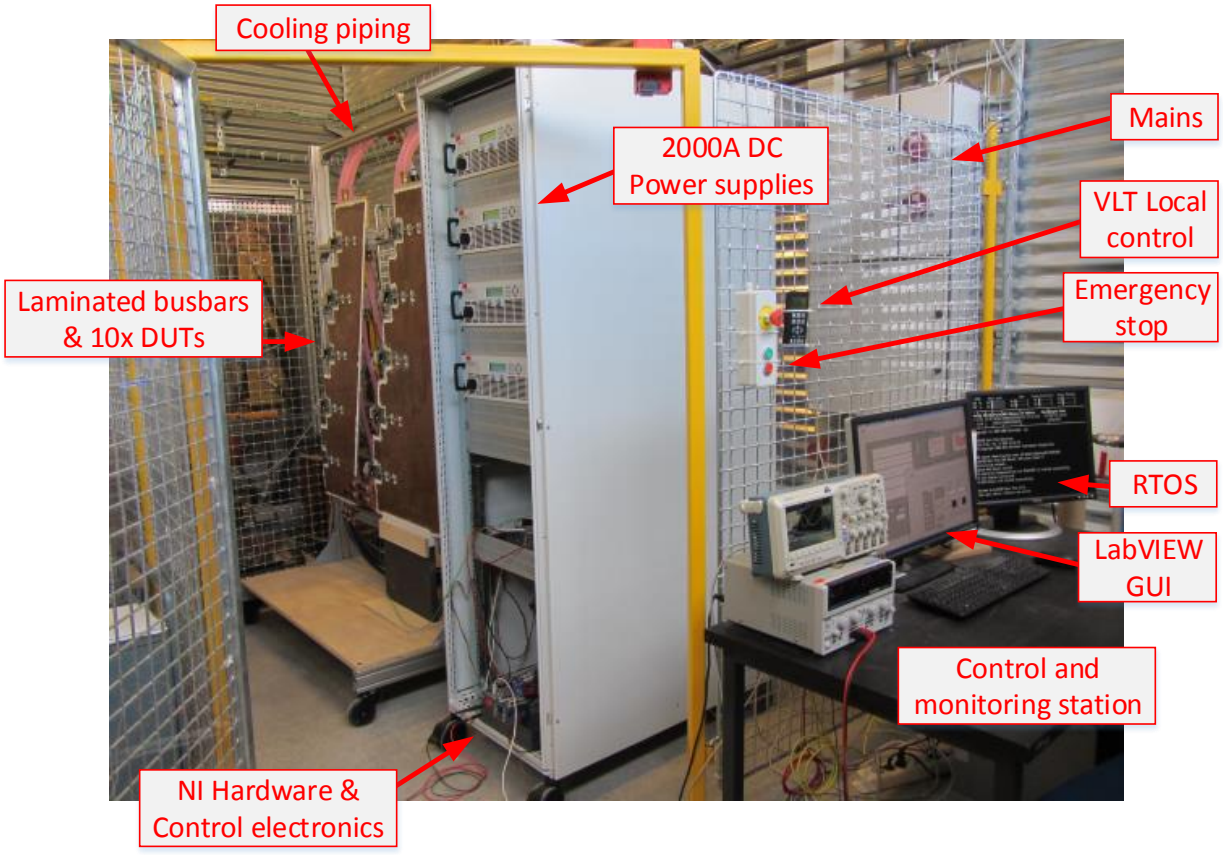


Figure A.1. Picture of the power-cycling test setup for accelerated wear-out of IGBT modules, Sven, with its different parts indicated.

As can be seen in the above figure, the test setup has been installed in a protection cage, which has been connected to the grounding of the Reliability laboratory. In case of malfunction of the system, an emergency stop has been installed next to the gate's door to disconnect the power from the electrical mains. The cooling system, the power circuitry (flexible and rigid busbars) and the decoupling inductor with snubber diode cannot be observed since these are located in the back part of the protection cage.

An equivalent diagram of the test setup, with a simplified layout of the acquired measurements and

sent signals on 1 single DUT, is shown in Fig. A.2. According to that diagram, the designation of DUTs in the implemented setup can be observed in Fig. A.3.

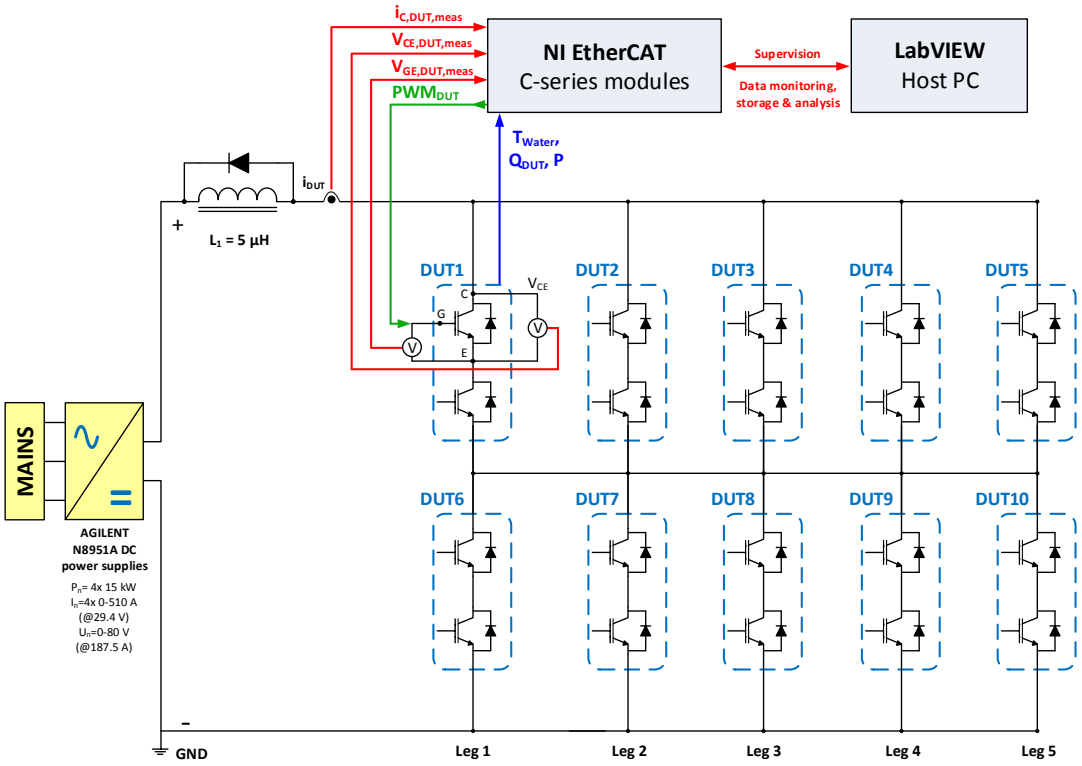


Figure A.2. Simplified diagram of the accelerated wear out test setup for IGBT modules (Sven).

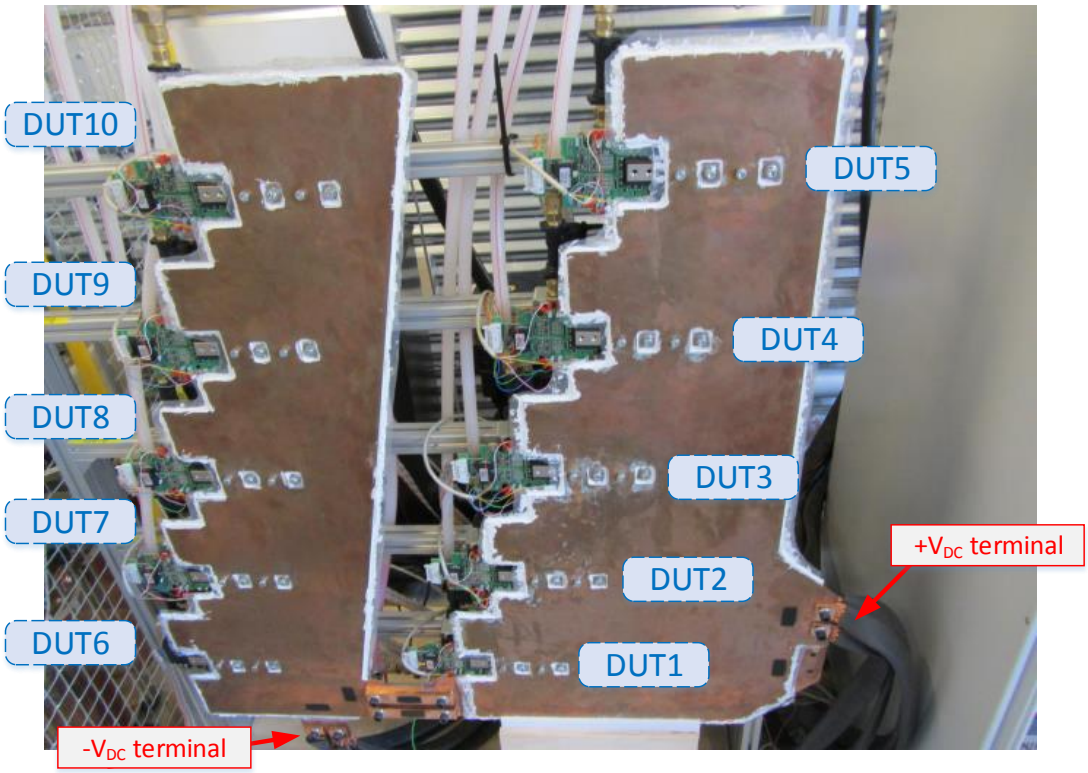


Figure A.3. Picture of the power-cycling test setup for accelerated wear-out of IGBT modules, Sven, with its different parts indicated.

Datasheets B

In this appendix the most relevant datasheets are presented. These are (in order of appearance):

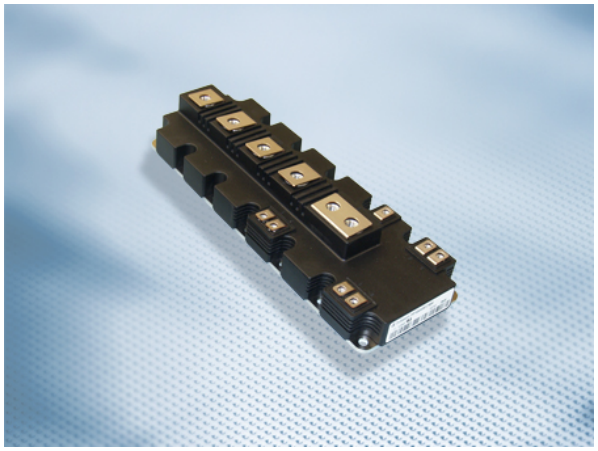
1. Infineon PrimePACK™3 IGBT module (FF1000R17IE4)
2. CONCEPT gate driver, 2SP0320T2A0-FF1000R17IE4

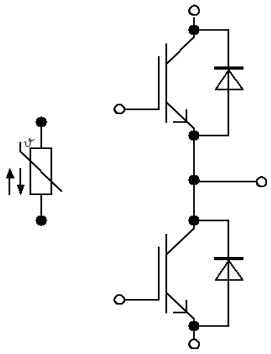
Technische Information / Technical Information

IGBT-Module
IGBT-modules

FF1000R17IE4

PrimePACK™3 Modul und NTC
PrimePACK™3 module and NTC





V_{CES} = 1700V
$I_{C\ nom}$ = 1000A / I_{CRM} = 2000A

Typische Anwendungen

- 3-Level-Applikationen
- Hilfsumrichter
- Hochleistungsumrichter
- Motorantriebe
- Windgeneratoren

Typical Applications

- 3-Level-Applications
- Auxiliary Inverters
- High Power Converters
- Motor Drives
- Wind Turbines

Elektrische Eigenschaften

- Erweiterte Sperrschichttemperatur $T_{vj\ op}$
- Große DC-Festigkeit
- Hohe Stromdichte
- Niedrige Schaltverluste
- $T_{vj\ op}$ = 150°C
- Niedriges V_{CEsat}

Electrical Features

- Extended Operation Temperature $T_{vj\ op}$
- High DC Stability
- High Current Density
- Low Switching Losses
- $T_{vj\ op}$ = 150°C
- Low V_{CEsat}

Mechanische Eigenschaften

- Gehäuse mit CTI > 400
- Große Luft- und Kriechstrecken
- Hohe Last- und thermische Wechselfestigkeit
- Hohe Leistungsdichte
- Kupferbodenplatte
- Standardgehäuse

Mechanical Features

- Package with CTI > 400
- High Creepage and Clearance Distances
- High Power and Thermal Cycling Capability
- High Power Density
- Copper Base Plate
- Standard Housing

Module Label Code

Barcode Code 128

Sample
00000123456000000000000

DMX - Code

Content of the Code	Digit
Module Serial Number	1 - 5
Module Material Number	6 - 11
Production Order Number	12 - 19
Datecode (Production Year)	20 - 21
Datecode (Production Week)	22 - 23

prepared by: TA	date of publication: 2013-11-05	
approved by: PL	revision: 3.2	

IGBT,Wechselrichter / IGBT,Inverter

Höchstzulässige Werte / Maximum Rated Values

Kollektor-Emitter-Sperrspannung Collector-emitter voltage	T_{vj} = 25°C	V_{CES}	1700	V
Kollektor-Dauergleichstrom Continuous DC collector current	T_C = 100°C, $T_{vj\,max}$ = 175°C T_C = 25°C, $T_{vj\,max}$ = 175°C	$I_{C\,nom}$ I_C	1000 1390	A A
Periodischer Kollektor-Spitzenstrom Repetitive peak collector current	t_P = 1 ms	I_{CRM}	2000	A
Gesamt-Verlustleistung Total power dissipation	T_C = 25°C, $T_{vj\,max}$ = 175°C	P_{tot}	6,25	kW
Gate-Emitter-Spitzenspannung Gate-emitter peak voltage		V_{GES}	+/-20	V

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Kollektor-Emitter-Sättigungsspannung Collector-emitter saturation voltage	I_C = 1000 A, V_{GE} = 15 V I_C = 1000 A, V_{GE} = 15 V I_C = 1000 A, V_{GE} = 15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$V_{CE\,sat}$		2,00 2,35 2,45	2,45 2,80	V V V
Gate-Schwellenspannung Gate threshold voltage	I_C = 36,0 mA, V_{CE} = V_{GE}, T_{vj} = 25°C		V_{GEth}	5,2	5,8	6,4	V
Gateladung Gate charge	V_{GE} = -15 V ... +15 V		Q_G		10,0		µC
Interner Gatewiderstand Internal gate resistor	T_{vj} = 25°C		R_{Gint}		1,5		Ω
Eingangskapazität Input capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{ies}		81,0		nF
Rückwirkungskapazität Reverse transfer capacitance	f = 1 MHz, T_{vj} = 25°C, V_{CE} = 25 V, V_{GE} = 0 V		C_{res}		2,60		nF
Kollektor-Emitter-Reststrom Collector-emitter cut-off current	V_{CE} = 1700 V, V_{GE} = 0 V, T_{vj} = 25°C		I_{CES}			5,0	mA
Gate-Emitter-Reststrom Gate-emitter leakage current	V_{CE} = 0 V, V_{GE} = 20 V, T_{vj} = 25°C		I_{GES}			400	nA
Einschaltverzögerungszeit, induktive Last Turn-on delay time, inductive load	I_C = 1000 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Gon} = 1,2 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,on}$		0,55 0,60 0,60		µs µs µs
Anstiegszeit, induktive Last Rise time, inductive load	I_C = 1000 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Gon} = 1,2 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_r		0,10 0,12 0,12		µs µs µs
Abschaltverzögerungszeit, induktive Last Turn-off delay time, inductive load	I_C = 1000 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Goff} = 1,8 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	$t_{d\,off}$		1,00 1,25 1,30		µs µs µs
Fallzeit, induktive Last Fall time, inductive load	I_C = 1000 A, V_{CE} = 900 V V_{GE} = ±15 V R_{Goff} = 1,8 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	t_f		0,29 0,50 0,59		µs µs µs
Einschaltverlustenergie pro Puls Turn-on energy loss per pulse	I_C = 1000 A, V_{CE} = 900 V, L_S = 30 nH V_{GE} = ±15 V, di/dt = 8000 A/µs (T_{vj} = 150°C) R_{Gon} = 1,2 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{on}		265 390 415		mJ mJ mJ
Abschaltverlustenergie pro Puls Turn-off energy loss per pulse	I_C = 1000 A, V_{CE} = 900 V, L_S = 30 nH V_{GE} = ±15 V, du/dt = 3000 V/µs (T_{vj} = 150°C) R_{Goff} = 1,8 Ω	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{off}		200 295 330		mJ mJ mJ
Kurzschlußverhalten SC data	$V_{GE} \leq$ 15 V, V_{CC} = 1000 V $V_{CEmax} = V_{CES} - L_{sCE} \cdot di/dt$	$t_P \leq$ 10 µs, T_{vj} = 150°C	I_{SC}		4000		A
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro IGBT / per IGBT		R_{thJC}			24,0	K/kW
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro IGBT / per IGBT λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		9,00		K/kW
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		150	°C

prepared by: TA	date of publication: 2013-11-05
approved by: PL	revision: 3.2

Diode, Wechselrichter / Diode, Inverter

Höchstzulässige Werte / Maximum Rated Values

Periodische Spitzensperrspannung Repetitive peak reverse voltage	T_{vj} = 25°C	V_{RRM}	1700	V
Dauergleichstrom Continuous DC forward current		I_F	1000	A
Periodischer Spitzenstrom Repetitive peak forward current	t_P = 1 ms	I_{FRM}	2000	A
Grenzlastintegral I²t - value	V_R = 0 V, t_P = 10 ms, T_{vj} = 125°C	I²t	140	kA²s

Charakteristische Werte / Characteristic Values

			min.	typ.	max.	
Durchlassspannung Forward voltage	I_F = 1000 A, V_{GE} = 0 V I_F = 1000 A, V_{GE} = 0 V I_F = 1000 A, V_{GE} = 0 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	V_F		1,85 1,95 1,95	2,25 2,35	V V V
Rückstromspitze Peak reverse recovery current	I_F = 1000 A, - di_F/dt = 8000 A/µs (T_{vj}=150°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	I_{RM}		1050 1200 1250		A A A
Sperrverzögerungsladung Recovered charge	I_F = 1000 A, - di_F/dt = 8000 A/µs (T_{vj}=150°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	Q_r		245 410 480		µC µC µC
Abschaltenergie pro Puls Reverse recovery energy	I_F = 1000 A, - di_F/dt = 8000 A/µs (T_{vj}=150°C) V_R = 900 V V_{GE} = -15 V	T_{vj} = 25°C T_{vj} = 125°C T_{vj} = 150°C	E_{rec}		115 205 245		mJ mJ mJ
Wärmewiderstand, Chip bis Gehäuse Thermal resistance, junction to case	pro Diode / per diode		R_{thJC}			48,0	K/kW
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Diode / per diode λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)		R_{thCH}		18,0		K/kW
Temperatur im Schaltbetrieb Temperature under switching conditions			$T_{vj\,op}$	-40		150	°C

NTC-Widerstand / NTC-Thermistor

Charakteristische Werte / Characteristic Values

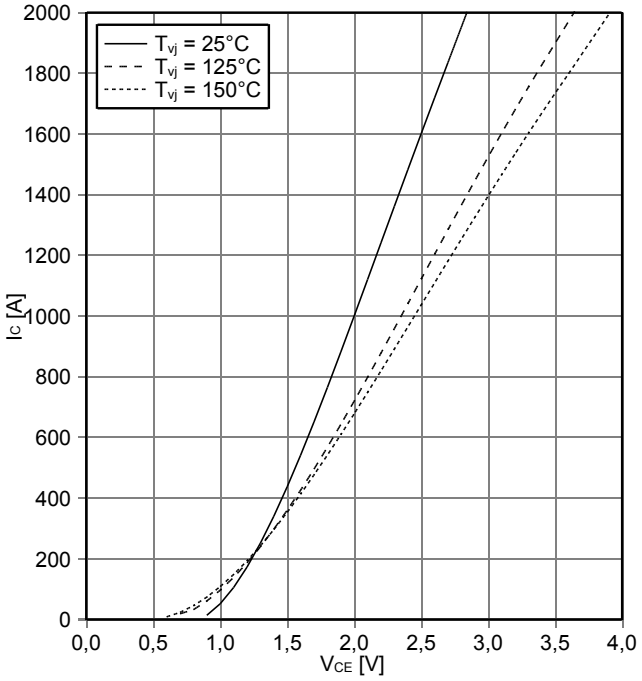
			min.	typ.	max.	
Nennwiderstand Rated resistance	T_C = 25°C	R_{25}		5,00		kΩ
Abweichung von R100 Deviation of R100	T_C = 100°C, R_{100} = 493 Ω	ΔR/R	-5		5	%
Verlustleistung Power dissipation	T_C = 25°C	P_{25}			20,0	mW
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/50}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/50}$		3375		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/80}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/80}$		3411		K
B-Wert B-value	$R_2 = R_{25} \exp [B_{25/100}(1/T_2 - 1/(298{,}15\ K))]$	$B_{25/100}$		3433		K

Angaben gemäß gültiger Application Note.
Specification according to the valid application note.

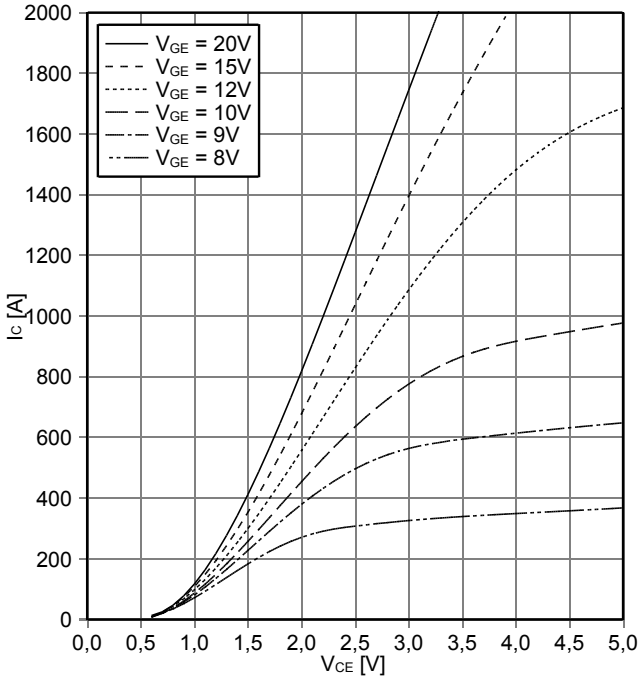
Modul / Module

Isolations-Prüfspannung Isolation test voltage	RMS, f = 50 Hz, t = 1 min.	V_{ISOL}		4,0		kV
Material Modulgrundplatte Material of module baseplate				Cu		
Innere Isolation Internal isolation	Basisisolierung (Schutzklasse 1, EN61140) basic insulation (class 1, IEC 61140)			Al_2O_3		
Kriechstrecke Creepage distance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			33,0 33,0		mm
Luftstrecke Clearance	Kontakt - Kühlkörper / terminal to heatsink Kontakt - Kontakt / terminal to terminal			19,0 19,0		mm
Vergleichszahl der Kriechwegbildung Comperative tracking index		CTI		> 400		
			min.	typ.	max.	
Wärmewiderstand, Gehäuse bis Kühlkörper Thermal resistance, case to heatsink	pro Modul / per module λ_{Paste} = 1 W/(m·K) / λ_{grease} = 1 W/(m·K)	R_{thCH}		3,00		K/kW
Modulstreuinduktivität Stray inductance module		L_{sCE}		10		nH
Modulleitungswiderstand, Anschlüsse - Chip Module lead resistance, terminals - chip	T_C = 25°C, pro Schalter / per switch	$R_{CC'+EE'}$		0,20		mΩ
Lagertemperatur Storage temperature		T_{stg}	-40		150	°C
Anzugsdrehmoment f. Modulmontage Mounting torque for modul mounting	Schraube M5 - Montage gem. gültiger Applikationsschrift Screw M5 - Mounting according to valid application note	M	3,00	-	6,00	Nm
Anzugsdrehmoment f. elektr. Anschlüsse Terminal connection torque	Schraube M4 - Montage gem. gültiger Applikationsschrift Screw M4 - Mounting according to valid application note Schraube M8 - Montage gem. gültiger Applikationsschrift Screw M8 - Mounting according to valid application note	M	1,8 8,0	- -	2,1 10	Nm Nm
Gewicht Weight		G		1200		g

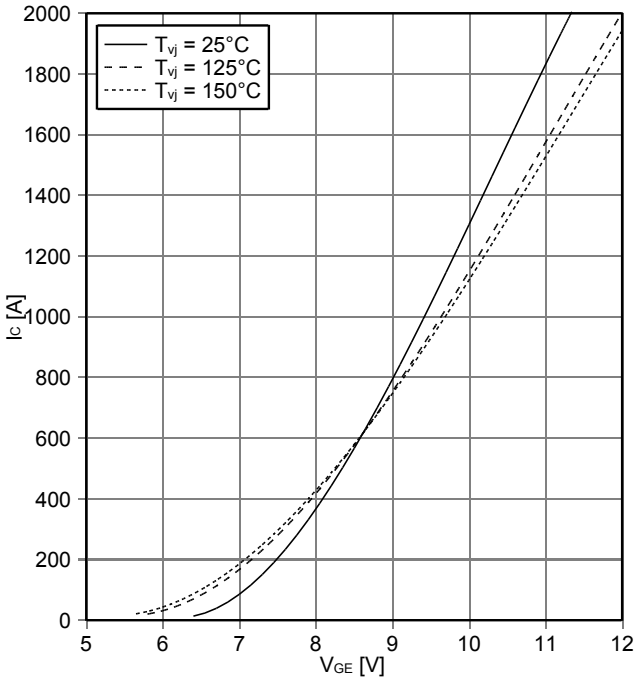
Ausgangskennlinie IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
V_{GE} = 15 V



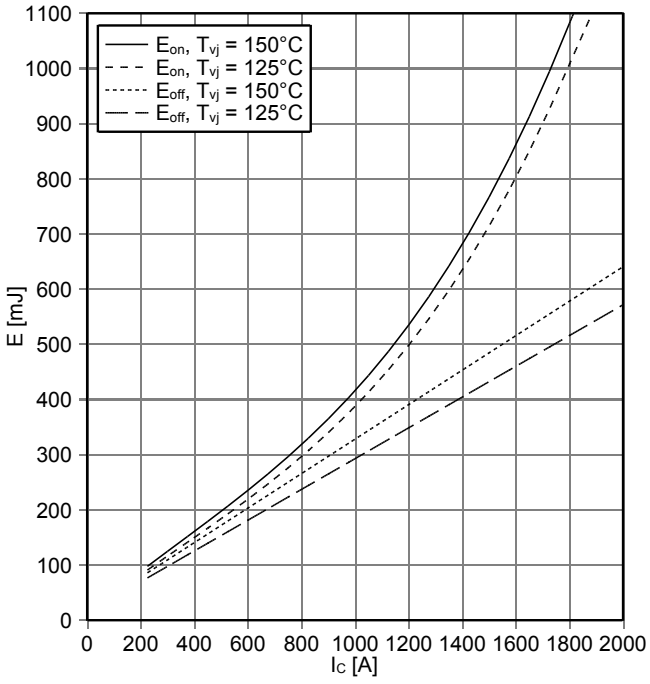
Ausgangskennlinienfeld IGBT,Wechselrichter (typisch)
output characteristic IGBT,Inverter (typical)
$I_C = f(V_{CE})$
T_{vj} = 150°C



Übertragungscharakteristik IGBT,Wechselrichter (typisch)
transfer characteristic IGBT,Inverter (typical)
$I_C = f(V_{GE})$
V_{CE} = 20 V

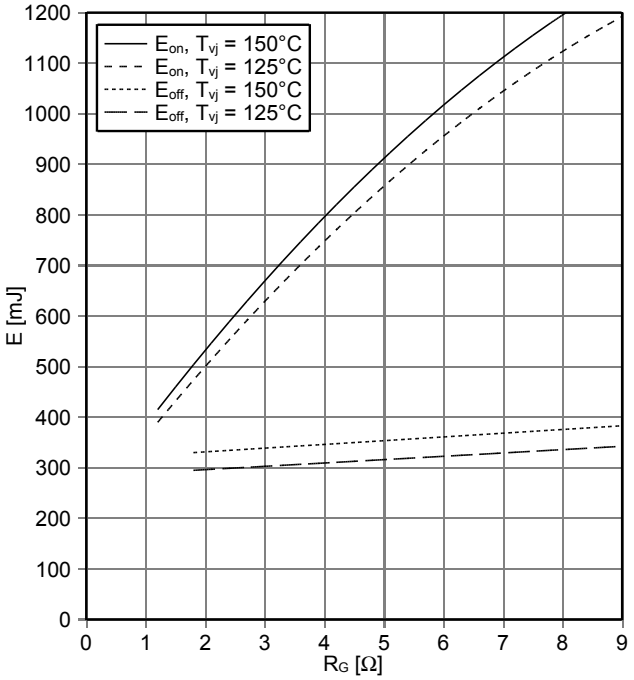


Schaltverluste IGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(I_C)$, $E_{off} = f(I_C)$
V_{GE} = ±15 V, R_{Gon} = 1.2 Ω, R_{Goff} = 1.8 Ω, V_{CE} = 900 V

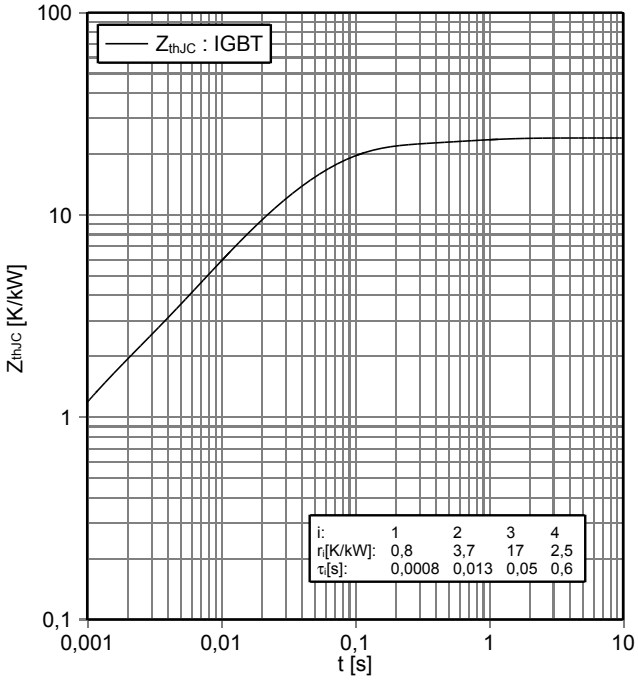


prepared by: TA	date of publication: 2013-11-05
approved by: PL	revision: 3.2

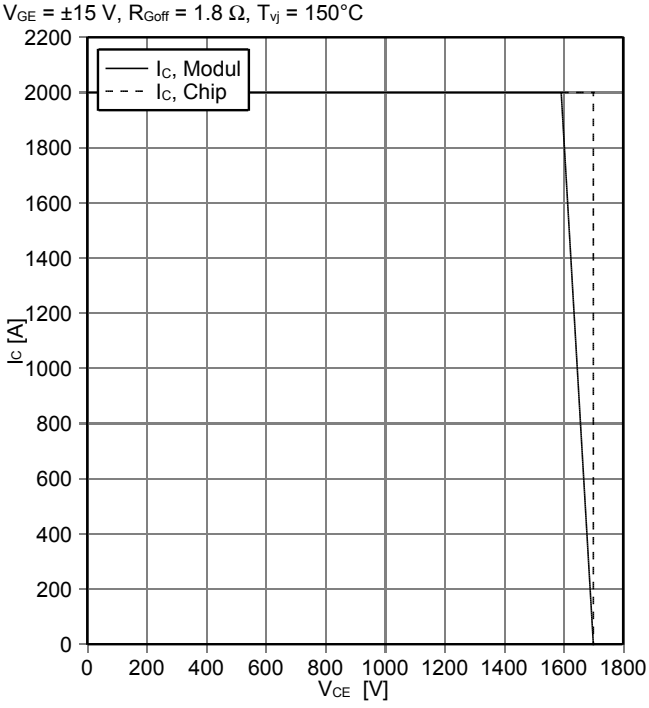
Schaltverluste IGBT,Wechselrichter (typisch)
switching losses IGBT,Inverter (typical)
$E_{on} = f(R_G)$, $E_{off} = f(R_G)$
V_{GE} = ±15 V, I_C = 1000 A, V_{CE} = 900 V



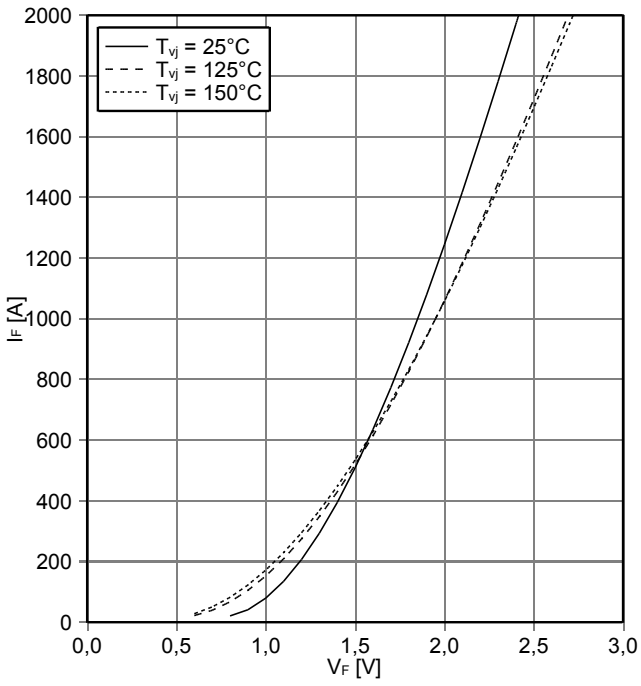
Transienter Wärmewiderstand IGBT,Wechselrichter
transient thermal impedance IGBT,Inverter
$Z_{thJC} = f(t)$



Sicherer Rückwärts-Arbeitsbereich IGBT,Wechselrichter (RBSOA)
reverse bias safe operating area IGBT,Inverter (RBSOA)
$I_C = f(V_{CE})$
V_{GE} = ±15 V, R_{Goff} = 1.8 Ω, T_{vj} = 150°C



Durchlasskennlinie der Diode, Wechselrichter (typisch)
forward characteristic of Diode, Inverter (typical)
$I_F = f(V_F)$



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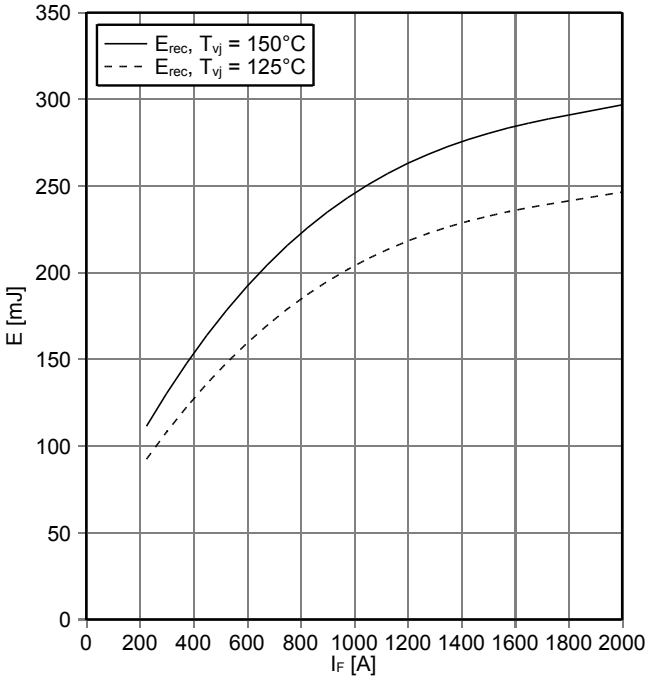
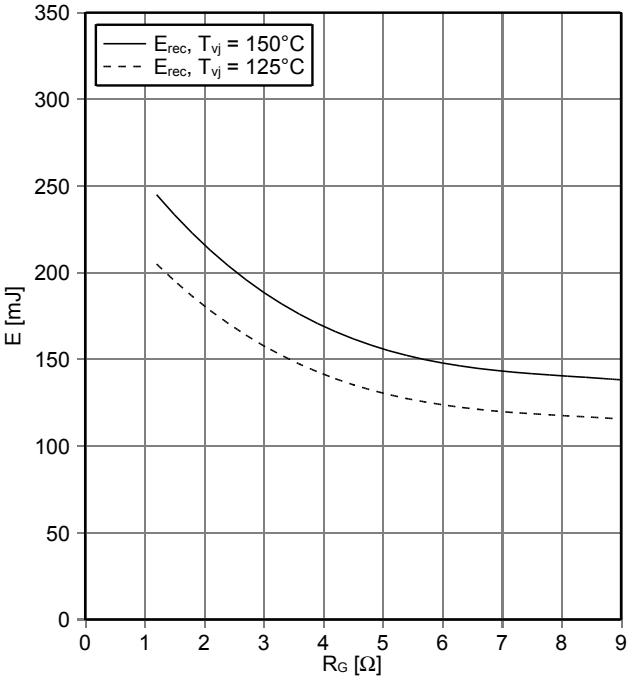
approved by: PL	revision: 3.2

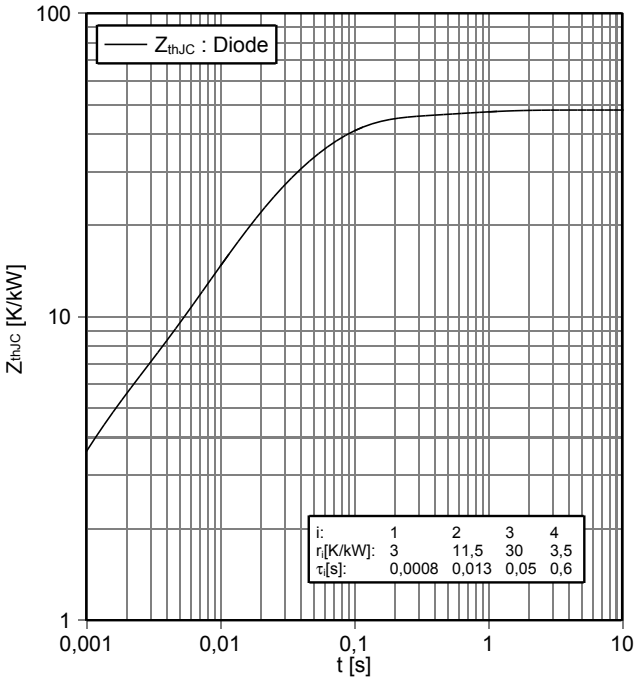
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(I_F)$
$R_{Gon} = 1.2\ \Omega$, $V_{CE} = 900$ V



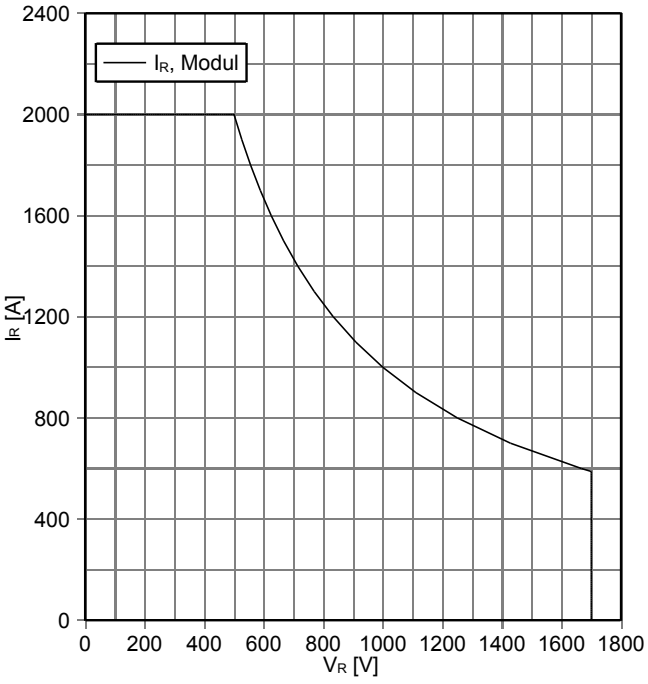
Schaltverluste Diode, Wechselrichter (typisch)
switching losses Diode, Inverter (typical)
$E_{rec} = f(R_G)$
$I_F = 1000$ A, $V_{CE} = 900$ V



Transienter Wärmewiderstand Diode, Wechselrichter
transient thermal impedance Diode, Inverter
$Z_{thJC} = f(t)$

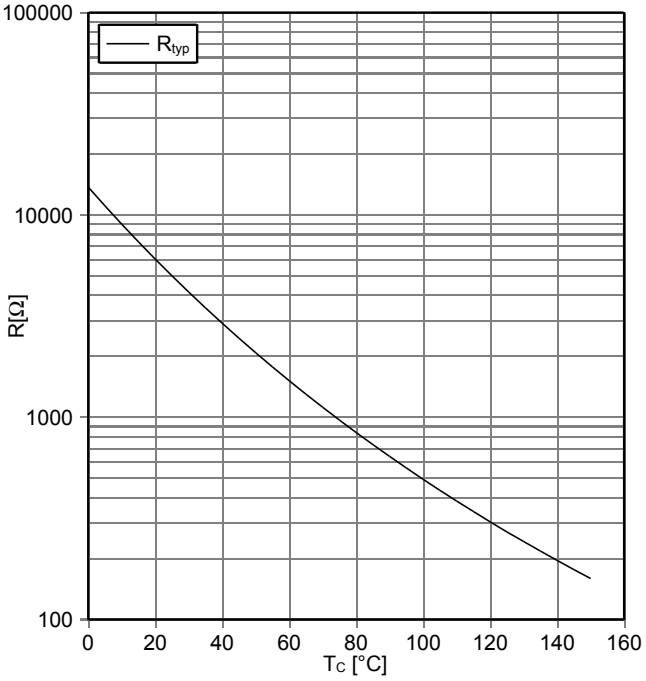


Sicherer Arbeitsbereich Diode, Wechselrichter (SOA)
safe operation area Diode, Inverter (SOA)
$I_R = f(V_R)$
$T_{vj} = 150$°C



prepared by: TA	date of publication: 2013-11-05
approved by: PL	revision: 3.2

NTC-Widerstand-Temperaturkennlinie (typisch)
NTC-Thermistor-temperature characteristic (typical)
R = f (T)



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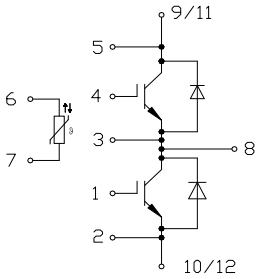
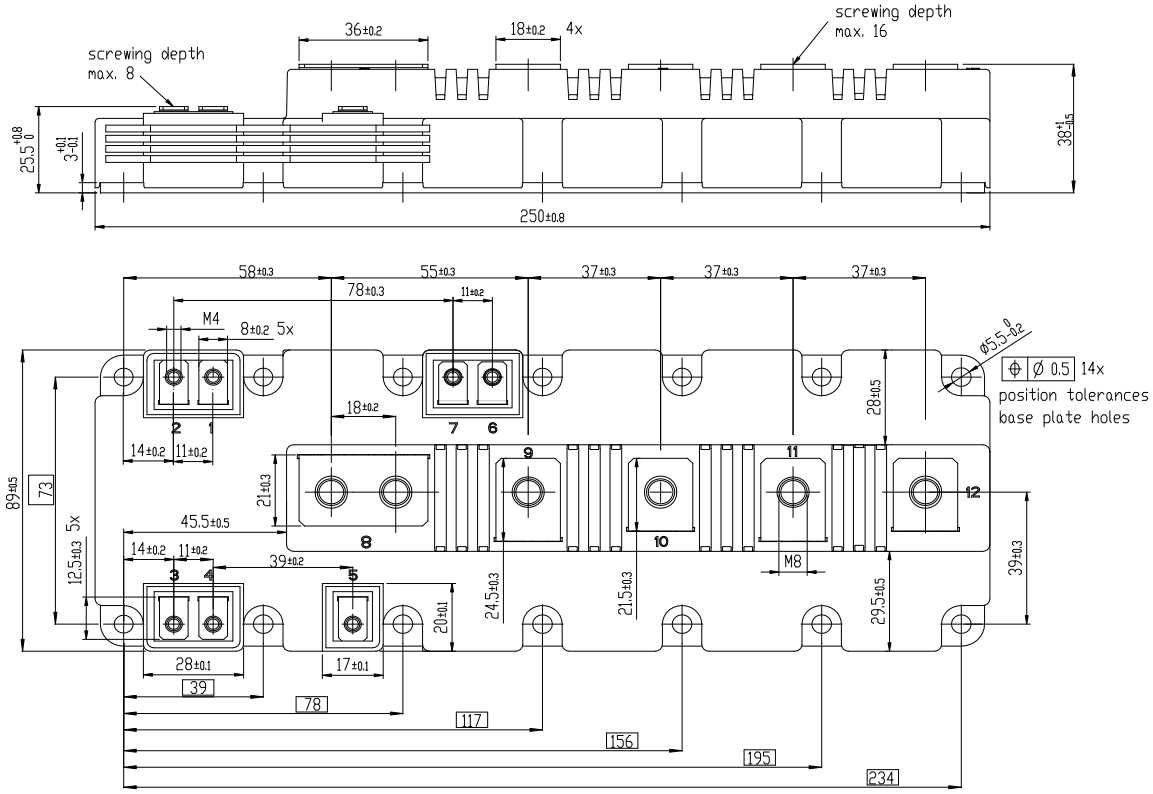
approved by: PL	revision: 3.2

Schaltplan / circuit_diagram_headline



Gehäuseabmessungen / package outlines



prepared by: TA	date of publication: 2013-11-05
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- the conclusion of Quality Agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery depended on the realization of any such measures.

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prepared by: TA	date of publication: 2013-11-05
approved by: PL	revision: 3.2

2SP0320x2Ax-FF1000R17IE4
Preliminary Data Sheet

Compact, high-performance, plug-and-play dual-channel IGBT driver based on SCALE-2 technology for individual and parallel-connected modules in 2-level, 3-level and multilevel converter topologies

Abstract

The SCALE-2 plug-and-play driver 2SP0320x2Ax-FF1000R17IE4 is a compact dual-channel intelligent gate driver designed for Infineon's PrimePACK™ IGBTs FF1000R17IE4. The driver features an electrical interface (2SP0320T) or a fiber-optic interface (2SP0320V and 2SP0320S) with a built-in DC/DC power supply.

For drivers adapted to other types of high-power and high-voltage IGBT modules, refer to

www.IGBT-Driver.com/go/plug-and-play

Features

- ✓ Plug-and-play solution
- ✓ Allows parallel connection of IGBT modules
- ✓ For 2-level, 3-level and multilevel topologies
- ✓ Shortens application development time
- ✓ Extremely reliable; long service life
- ✓ Built-in DC/DC power supply
- ✓ 20-pin flat cable interface (2SP0320T)
- ✓ Fiber-optic links (2SP0320V & 2SP0320S)
- ✓ Duty cycle 0... 100%
- ✓ Active clamping of V_{ce} at turn-off
- ✓ IGBT short-circuit protection
- ✓ Monitoring of supply voltage
- ✓ Safe isolation to EN 50178
- ✓ UL compliant
- ✓ Suitable for FF1000R17IE4

Applications

- ✓ Wind-power converters
- ✓ Industrial drives
- ✓ UPS
- ✓ Power-factor correctors
- ✓ Traction
- ✓ Railroad power supplies
- ✓ Welding
- ✓ SMPS
- ✓ Radiology and laser technology
- ✓ Research
- ✓ and many others

Preliminary Data Sheet

Safety Notice!

The data contained in this data sheet is intended exclusively for technically trained staff. Handling all high-voltage equipment involves risk to life. Strict compliance with the respective safety regulations is mandatory!

Any handling of electronic devices is subject to the general specifications for protecting electrostatic-sensitive devices according to international standard IEC 60747-1, Chapter IX or European standard EN 100015 (i.e. the workplace, tools, etc. must comply with these standards). Otherwise, this product may be damaged.

Important Product Documentation

This data sheet contains only product-specific data. For a detailed description, must-read application notes and common data that apply to the whole series, please refer to "Description & Application Manual for 2SP0320T SCALE-2 IGBT Drivers" (electrical interface) or "Description & Application Manual for 2SP0320V and 2SP0320S SCALE-2 IGBT Drivers" (fiber-optic interface) on www.IGBT-Driver.com/go/2SP0320.

When applying SCALE-2 plug-and-play drivers, please note that these drivers are specifically adapted to a particular type of IGBT module. Therefore, the type designation of SCALE-2 plug-and-play drivers also includes the type designation of the corresponding IGBT module. These drivers are not valid for IGBT modules other than those specified. Incorrect use may result in failure.

Mechanical Dimensions

Dimensions: See the relevant "Description and Application Manual"

Mounting principle: Connected to IGBT module with screws

Fiber-Optic Interfaces

Interface	Remarks	Part type #
Drive signal input	2SP0320V, fiber-optic receiver (Notes 21, 22)	HFBR-2522
Drive signal input	2SP0320S, fiber-optic receiver (Notes 21, 22)	HFBR-2412Z
Status output	2SP0320V, fiber-optic transmitter (Notes 21, 23)	HFBR-1522
Status output	2SP0320S, fiber-optic transmitter (Notes 21, 23)	HFBR-1412Z

Absolute Maximum Ratings

Parameter	Remarks	Min	Max	Unit
Supply voltage V_{DC}	VDC to GND	0	16	V
Supply voltage V_{CC}	VCC to GND (Note 1)	0	16	V
Logic input and output voltages	To GND	-0.5	VCC+0.5	V
SO_x current	Fault condition, total current		20	mA
Gate peak current I_{out}	Note 2	-20	+20	A
Average supply current I_{DC}	2SP0320T (Note 24)		600	mA
Average supply current I_{DC}	2SP0320V and 2SP0320S (Note 24)		690	mA
Output power per gate	Ambient temperature <70°C (Note 3)		3	W
	Ambient temperature 85°C (Note 3)		2	W
Switching frequency F			13	kHz
Test voltage (50Hz/1min.)	Primary to secondary (Note 19)		5000	$V_{AC(eff)}$
	Secondary to secondary (Note 19)		4000	$V_{AC(eff)}$
DC-link voltage	Note 4		1200	V
|dV/dt|	Rate of change of input to output voltage (Note 20)		50	kV/µs
Operating voltage	Primary/secondary, secondary/secondary		1700	V_{peak}
Operating temperature		-40	+85	°C
Storage temperature		-40	+90	°C

Recommended Operating Conditions

Power Supply	Remarks	Min	Typ	Max	Unit
Supply voltage V_{DC}	To GND (Note 1)	14.5	15	15.5	V
Supply voltage V_{CC}	To GND (Note 1)	14.5	15	15.5	V
Resistance from TB to GND	2SP0320T, blocking time≠0, ext. value	128		∞	kΩ
SO_x current	Fault condition, 3.3V logic			4	mA

Electrical Characteristics

Power Supply	Remarks	Min	Typ	Max	Unit
Supply current I_{DC}	2SP0320T, without load		37		mA
	2SP0320V and 2SP0320S, without load		145		mA
Efficiency η	Internal DC/DC converter		85		%
Supply current I_{CC}	Without load		19		mA
Coupling capacitance C_{io}	Primary side to secondary side, total, per channel				
	2SP0320T		20		pF
	2SP0320V and 2SP0320S		15		pF
Power Supply Monitoring	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Supply threshold V_{CC}	Primary side, clear fault	11.9	12.6	13.3	V
	Primary side, set fault (Note 5)	11.3	12.0	12.7	V
Monitoring hysteresis	Primary side, set/clear fault	0.35			V
Supply threshold V_{isox}-V_{eex}	Secondary side, clear fault	12.1	12.6	13.1	V
	Secondary side, set fault (Note 26)	11.5	12.0	12.5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.35			V
Supply threshold V_{eex}-V_{COMx}	Secondary side, clear fault	5	5.15	5.3	V
	Secondary side, set fault (Note 26)	4.7	4.85	5	V
Monitoring hysteresis	Secondary side, set/clear fault	0.15			V
Logic Inputs and Outputs	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Input impedance	2SP0320T, V(INx) > 3V (Note 6)	3.5	4.1	4.6	kΩ
Turn-on threshold	2SP0320T, V(INx) (Note 7)		2.6		V
Turn-off threshold	2SP0320T, V(INx) (Note 7)		1.3		V
SOx output voltage	Fault condition, I(SOx)<8mA			0.7	V
Short-circuit Protection	**Remarks**	**Min**	**Typ**	**Max**	**Unit**
Vce-monitoring threshold	Between auxiliary terminals		10.2		V
Response time	DC-link voltage > 550V (Note 8)		6.9		µs
Delay to IGBT turn-off	After the response time (Note 9)		1.4		µs
Blocking time	2SP0320T, after fault (Note 10)		90		ms

Timing Characteristics	Remarks	Min	Typ	Max	Unit
Turn-on delay $t_{d(on)}$	2SP0320T (Note 11)		90		ns
Turn-off delay $t_{d(off)}$	2SP0320T (Note 11)		90		ns
Jitter of turn-on delay	2SP0320T (Note 28)		±2		ns
Jitter of turn-off delay	2SP0320T (Note 28)		±2		ns
Turn-on delay $t_{d(on)}$	2SP0320V and 2SP0320S (Note 12)		120		ns
Turn-off delay $t_{d(off)}$	2SP0320V and 2SP0320S (Note 12)		100		ns
Output rise time $t_{r(out)}$	G_x to E_x (Note 13)		7		ns
Output fall time $t_{f(out)}$	G_x to E_x (Note 13)		25		ns
Dead time between outputs	2SP0320T, half-bridge mode		3		µs
Jitter of dead time	2SP0320T, half-bridge mode		±100		ns
Transmission delay of fault state	2SP0320T (Note 14)		450		ns
Transmission delay of fault state	2SP0320V and 2SP0320S (Note 25)		90		ns
Delay to clear fault state	2SP0320V and 2SP0320S (Note 15)		11		µs
Acknowledge delay time	2SP0320V and 2SP0320S (Note 16)		220		ns
Acknowledge pulse width	2SP0320V and 2SP0320S (on host side)		700	1050	ns

Outputs	Remarks	Min	Typ	Max	Unit
Turn-on gate resistor $R_{g(on)}$	Note 17		1.2		Ω
Turn-off gate resistor $R_{g(off)}$	Note 17		3.3		Ω
Gate voltage at turn-on			15		V
Gate-voltage at turn-off	2SP0320T / (2SP0320V & 2SP0320S)				
	P = 0W		-10.4/-9.9		V
	P = 0.3W		-10.2/-9.8		V
	P = 2.1W		-9.7/-9.5		V
	P = 3W		-9.6/-9.4		V
Gate resistance to COMx			4.7		kΩ

dV/dt Feedback	Remarks	Implementation
dV/dt feedback	Note 18	No

Electrical Isolation	Remarks	Min	Typ	Max	Unit
Test voltage (50Hz/1s)	Primary to secondary side (Note 19)	5000	5050	5100	V_{eff}
	Secondary to secondary side (Note 19)	4000	4050	4100	V_{eff}
Partial discharge extinction volt.	Primary to secondary side (Note 27)	1768			V_{peak}
	Secondary to secondary side (Note 27)	1700			V_{peak}
Creepage distance	Primary to secondary side	20			mm
	Secondary to secondary side	17			mm

All data refer to +25°C and V_{CC} = V_{DC} = 15V unless otherwise specified

Footnotes to the Key Data

1) Both supply voltages V_{DC} and V_{CC} should be applied in parallel.
2) The gate current is limited by the gate resistors located on the driver.
3) If the specified value is exceeded, this indicates a driver overload. It should be noted that the driver is not protected against overload. From 70°C to 85°C, the maximum permissible output power can be linearly interpolated from the given data.
4) This limit is due to active clamping. Refer to "Description & Application Manual for 2SP0320T SCALE-2 IGBT Drivers" (electrical interface) or "Description & Application Manual for 2SP0320V and 2SP0320S SCALE-2 IGBT Drivers" (fiber-optic interface).
5) Undervoltage monitoring of the primary-side supply voltage (VCC to GND). If the voltage drops below this limit, a fault is transmitted to the corresponding output(s) (2SP0320T/2SP0320V/2SP0320S) and the IGBTs are switched off (only 2SP0320T).
6) The input impedance can be modified to values < 18 kΩ (customer-specific solution).
7) Turn-on and turn-off threshold values can be increased (customer-specific solution).
8) The resulting pulse width of the direct output of the gate drive unit for short-circuit type I (excluding the delay of the gate resistors) is the sum of response time plus delay to IGBT turn-off.
9) The turn-off event of the IGBT is delayed by the specified time after the response time.
10) Factory set value. The blocking time can be reduced with an external resistor. Refer to "Description & Application Manual for 2SP0320T SCALE-2 IGBT Drivers".
11) Measured from the transition of the turn-on or turn-off command at the driver input to direct output of the gate drive unit (excluding the delay of the gate resistors).
12) Including the delay of the external fiber-optic links. Measured from the transition of the turn-on or turn-off command at the optical transmitter on the host controller side to the direct output of the gate drive unit (excluding the delay of the gate resistors).
13) Refers to the direct output of the gate drive unit (excluding the delay of the gate resistors).
14) Transmission delay of the fault state from the secondary side to the primary status outputs.
15) Measured on the host side. The fault status on the secondary side is automatically reset after the specified time.
16) Including the delay of the external fiber-optic links. Measured from the transition of the turn-on or turn-off command at the optical transmitter on the host controller side to the transition of the acknowledge signal at the optical receiver on the host controller side.
17) The gate resistors can be leaded or surface mounted. CONCEPT reserves the right to determine which type will be used. Typically, higher quantities will be produced with SMD resistors and small quantities with leaded resistors.
18) A dV/dt feedback can optionally be implemented in order to reduce the rate of rise of the collector emitter voltage of the IGBTs at turn-off (customer-specific solution).
19) HiPot testing (= dielectric testing) must generally be restricted to suitable components. This gate driver is suited for HiPot testing. Nevertheless, it is strongly recommended to limit the testing time to 1s slots as stipulated by EN 50178. Excessive HiPot testing at voltages much higher than $1200V_{AC(eff)}$ may lead to insulation degradation. No degradation has been observed over 1min. testing at $5000V_{AC(eff)}$. Every production sample shipped to customers has undergone 100% testing at the given value for 1s.
20) This specification guarantees that the drive information will be transferred reliably even at a high DC-link voltage and with ultra-fast switching operations.
21) The transceivers required on the host controller side are not supplied with the gate driver. It is recommended to use the same types as used in the gate driver. For product information refer to www.IGBT-Driver.com/go/fiberoptics
22) The recommended transmitter current at the host controller is 20mA. A higher current may increase jitter or delay at turn-off.
23) The typical transmitter current at the gate driver is 18mA. In case of supply undervoltage, the minimum transmitter current at the gate driver is 12mA: this is suitable for adequate plastic optical fibers with a length of more than 10 meters.
24) If the specified value is exceeded, this indicates a driver overload. It should be noted that the driver is not protected against overload.

25) Delay of external fiber-optic links. Measured from the driver secondary side (ASIC output) to the optical receiver on the host controller.
26) Undervoltage monitoring of the secondary-side supply voltage (Visox to Veex and Veex to COMx which correspond with the approximate turn-on and turn-off gate-emitter voltages). If the corresponding voltage drops below this limit, the IGBT is switched off and a fault is transmitted to the corresponding output.
27) Partial discharge measurement is performed in accordance with IEC 60270 and isolation coordination specified in EN 50178. The partial discharge extinction voltage between primary and either secondary side is coordinated for safe isolation to EN 50178.
28) Jitter measurements are performed with input signals INx switching between 0V and 15V referred to GND, with a corresponding rise time and fall time of 8ns.

Legal Disclaimer

This data sheet specifies devices but cannot promise to deliver any specific characteristics. No warranty or guarantee is given – either expressly or implicitly – regarding delivery, performance or suitability.

CT-Concept Technologie AG reserves the right to make modifications to its technical data and product specifications at any time without prior notice. The general terms and conditions of delivery of CT-Concept Technologie AG apply.

Ordering Information

The general terms and conditions of delivery of CT-Concept Technologie AG apply.

Interface	CONCEPT Driver Type #	Related IGBT
Electrical Interface	2SP0320T2A0-FF1000R17IE4	FF1000R17IE4
Fiber-Optic Interface [1)]	2SP0320V2A0-FF1000R17IE4	FF1000R17IE4
Fiber-Optic Interface [2)]	2SP0320S2A0-FF1000R17IE4	FF1000R17IE4

1) Fiber-optic interface with versatile link (HFBR-2522 and HFBR-1522)
2) Fiber-optic interface with ST (HFBR-2412Z and HFBR-1412Z)
See "Description & Application Manual for 2SP0320V and 2SP0320S SCALE-2 IGBT Drivers"

Product home page: www.IGBT-Driver.com/go/2SP0320

Refer to www.IGBT-Driver.com/go/nomenclature for information on driver nomenclature

Information about Other Products

For other drivers, evaluation systems product documentation and application support

Please click: www.IGBT-Driver.com

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Printed Circuit Boards C

This appendix presents all the Printed Circuit Boards (PCBs) that have been performed during the implementation of the test setup. These are:

1. Interface board for CONCEPT gate drivers.
2. Measurement interface board for NI9215 module (Overvoltage protection circuit).
3. Interface board for pressure sensors.

In the following pages, the above-mentioned PCBs are presented with their respective schematic and PCB layout.

These have been designed in Altium Designer® and built in the laboratories of the Department of Energy Technology.

C.1 Interface board for CONCEPT gate drivers

C.1.1 Schematics

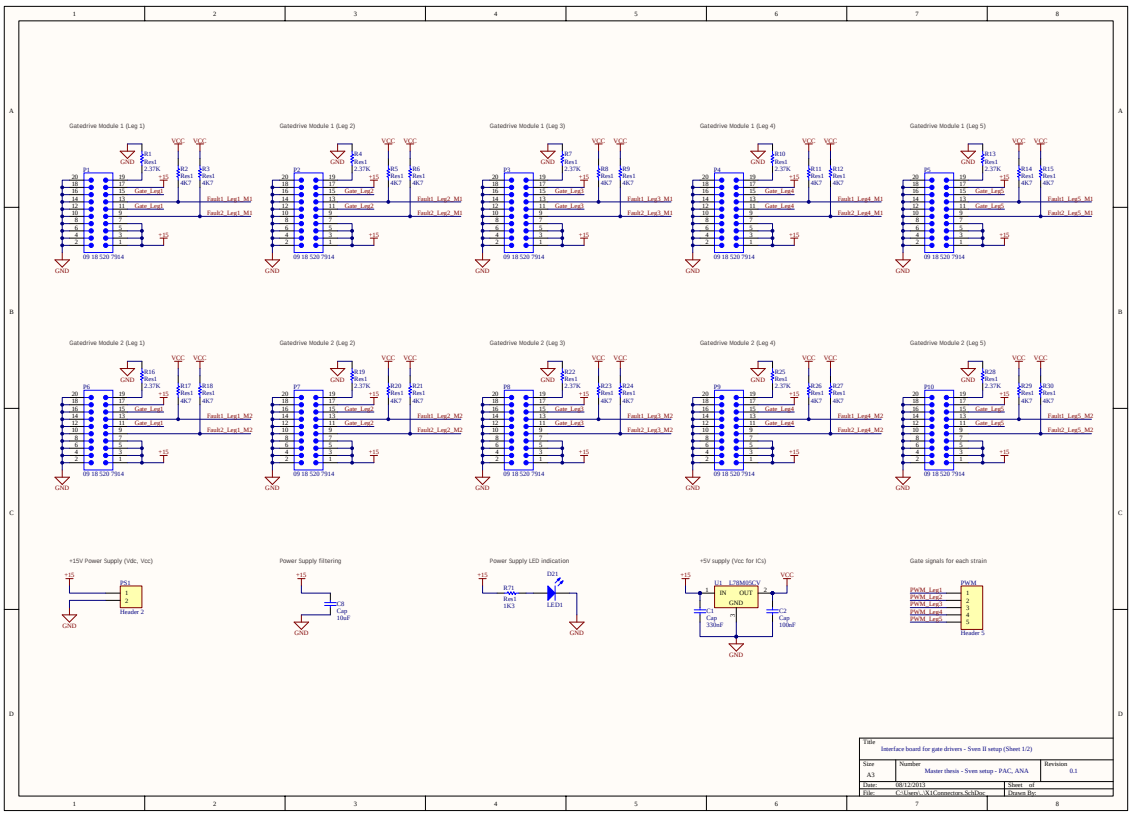


Figure C.1. Schematic of the X1 connectors.

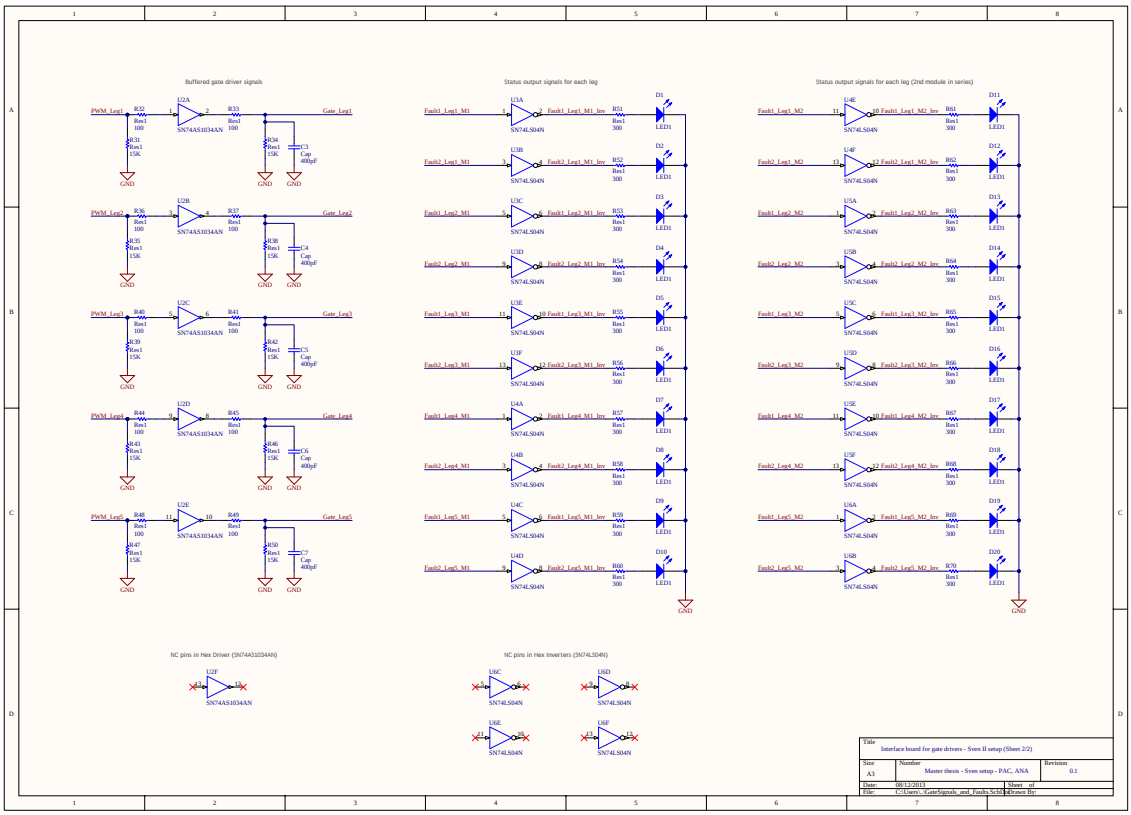


Figure C.2. Schematic of the gate signal buffer and fault signal inverters.

C.1.2 PCB layout

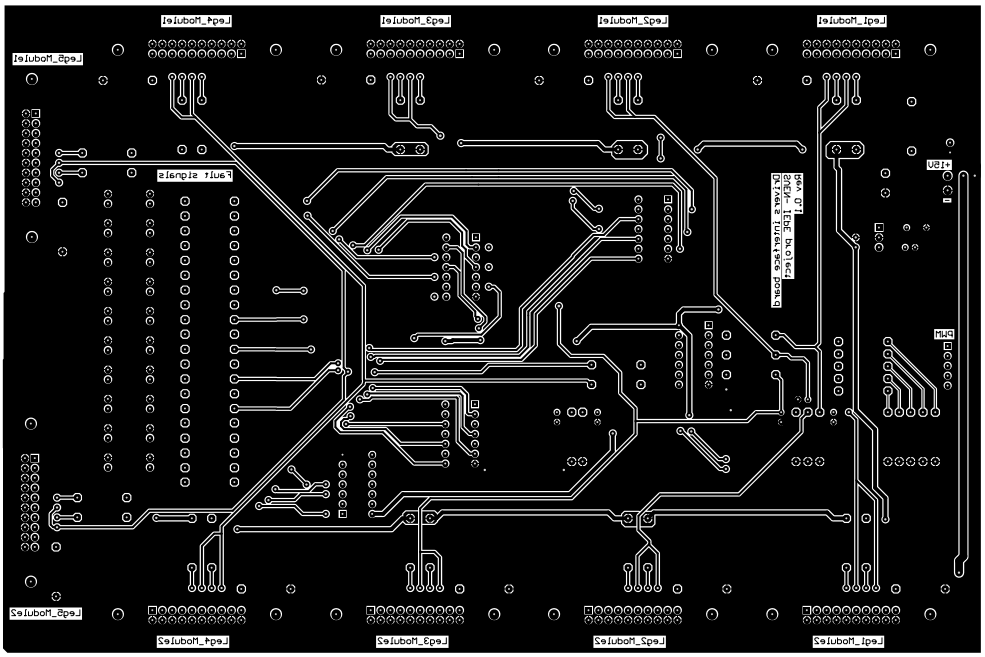


Figure C.3. Top layer of the gate driver's interface board.

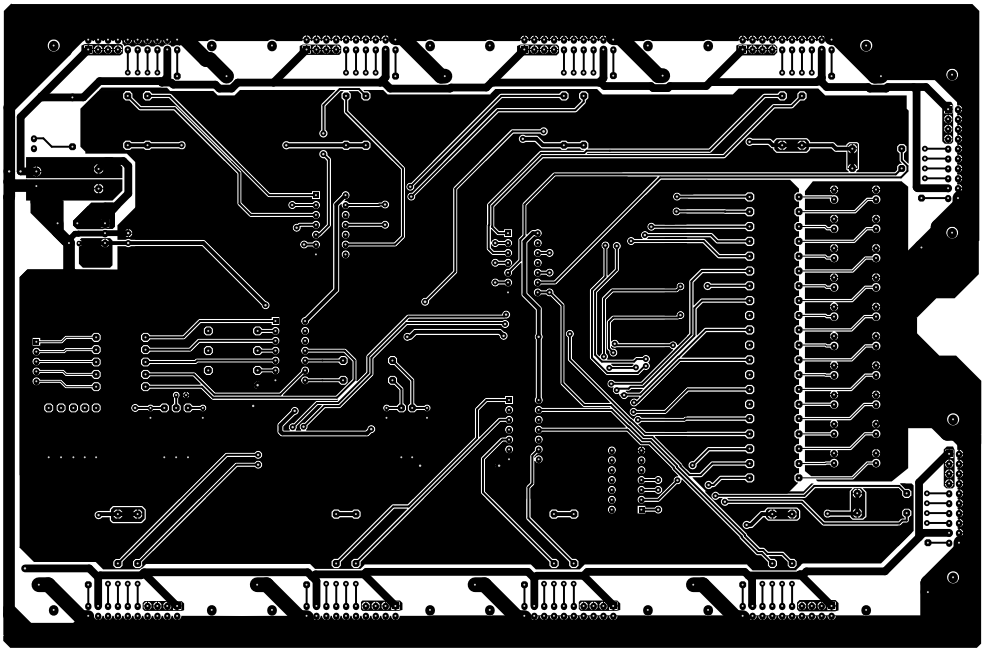


Figure C.4. Bottom layer of the gate driver's interface board.

C.2 Measurement interface board for NI9215 module (Overvoltage protection circuit)

C.2.1 PCB layout

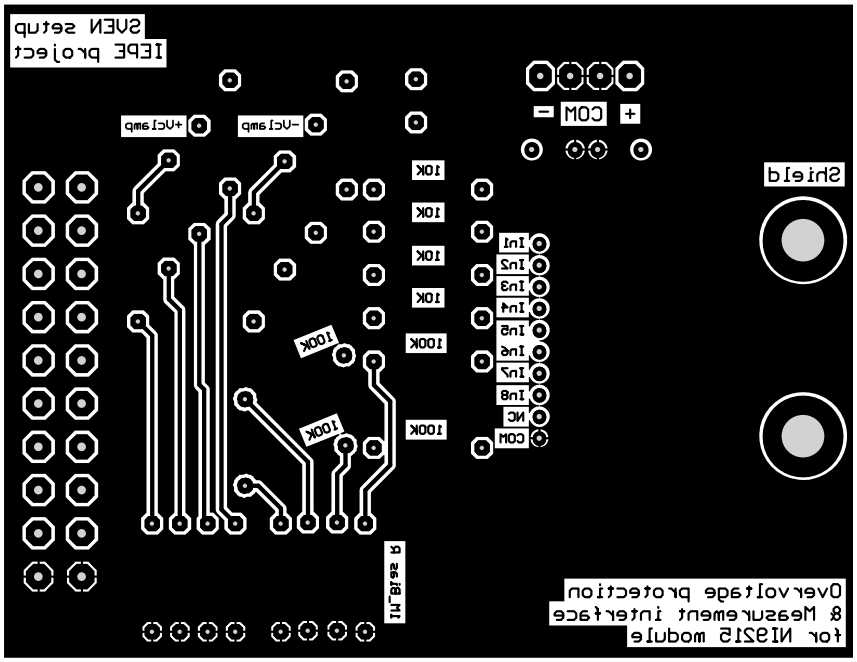


Figure C.5. Top layer of the Overvoltage protection circuit for the NI9215 module.

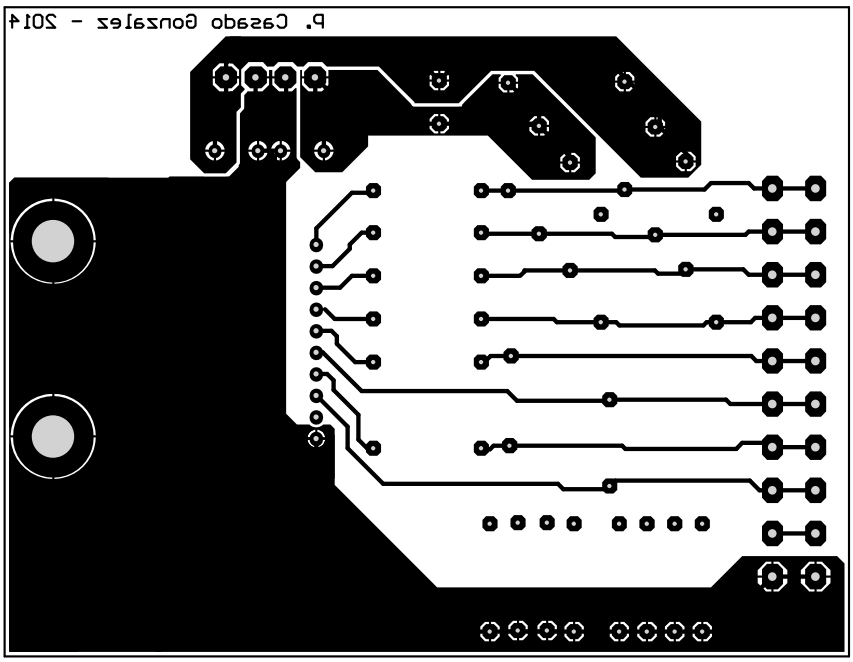


Figure C.6. Bottom layer of the Overvoltage protection circuit for the NI9215 module.

C.3 Interface board for pressure sensors

C.3.1 Schematics

C.3.2 PCB layout

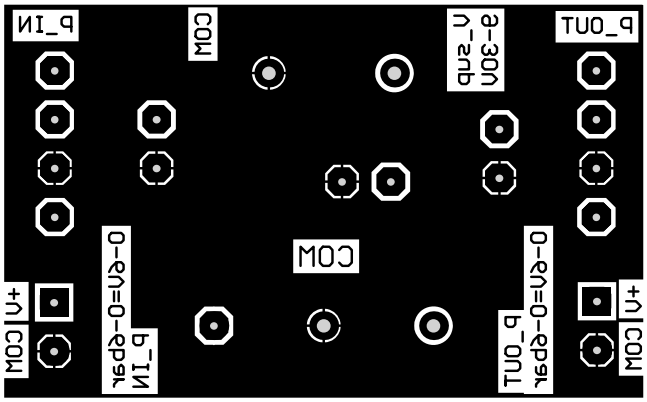


Figure C.7. Top layer of the interface board for the pressure sensors.

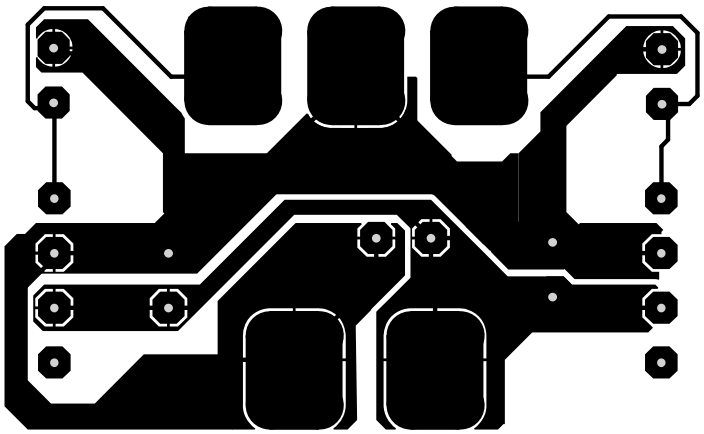


Figure C.8. Bottom layer of the interface board for the pressure sensors.

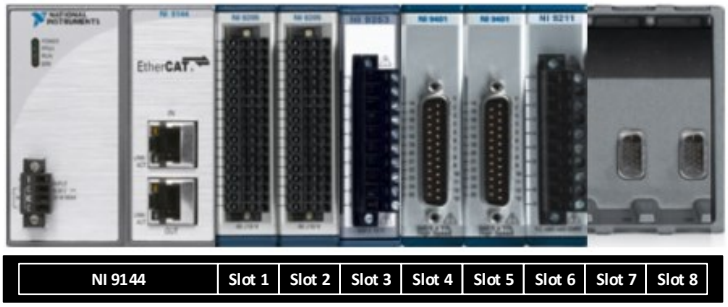
Additional description of the cooling system

D

This appendix is divided into three parts and it presents all the necessary information regarding hardware and software implementation of the cooling system for conducting the flow, pressure and temperature measurements.

D.1 Hardware implementation

In Fig. D.1, the layout of the used hardware is presented. It shows the designation of the channels for each of the NI modules according to the measurement quantities.



9205 (slot 1)	AI00	"Modul 00"	T retur
	AI01		Flow
	AI02	"Modul 01"	T retur
	AI03		Flow
	AI04	"Modul 02"	T retur
	AI05		Flow
	AI06	"Modul 03"	T retur
	AI07		Flow
	AI16	"Modul 04"	T retur
	AI17		Flow
	AI18		
	AI18		
	AI19		
	AI22		
	AI23	Manifold	p frem
	AI24		p retur

Differential Setup

9205 (slot 2)	AI00	"Modul 05"	T retur
	AI01		Flow
	AI02	"Modul 06"	T retur
	AI03		Flow
	AI04	"Modul 07"	T retur
	AI05		Flow
	AI06	"Modul 08"	T retur
	AI07		Flow
	AI16	"Modul 09"	T retur
	AI17		Flow
	AI18		
	AI18		
	AI19		
	AI22		
	AI23		
	AI24		

9211 (slot 6)	DO00	Manifold	Temperatur
	DO01		
	DO02		
	DO03		
	DO04		
	DO05		
	DO06		
	DO07		

9263 (slot 3)	AO00	"Modul 05"	Ventil
	AO01	"Modul 07"	VLT
	AO02		
	AO03		

Figure D.1. Instrumentation layout of the NI EtherCAT chassis with the installed NI modules.

D.2 Software implementation

This part of the appendix presents the software layout and its main parts, as they have been realized in NI LabVIEW. The Graphical User Interface where all the relevant quantities are monitored is shown in Fig. D.2, whereas the program structure together with the two main VIs,Host VI and Data Acquisition VI, are provided in Fig. D.3, D.4, D.5.

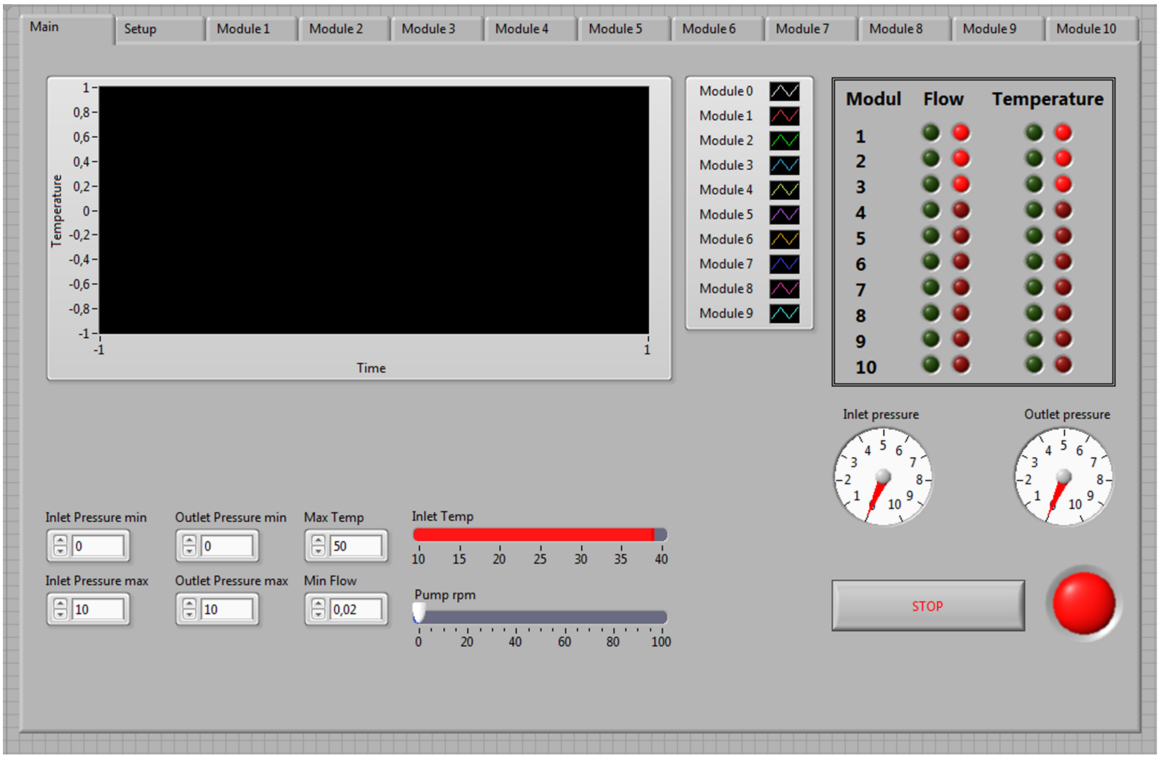


Figure D.2. Graphical User Interface panel for monitoring of the cooling quantities located at the Host PC.

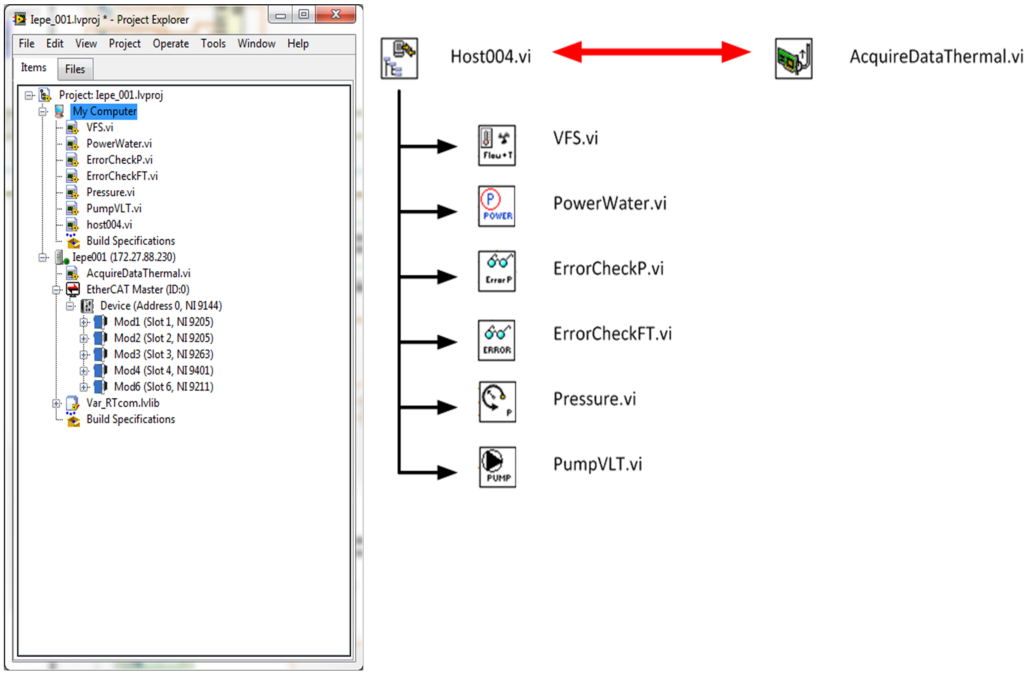


Figure D.3. Structure of the Project with all the relative sub VIs.

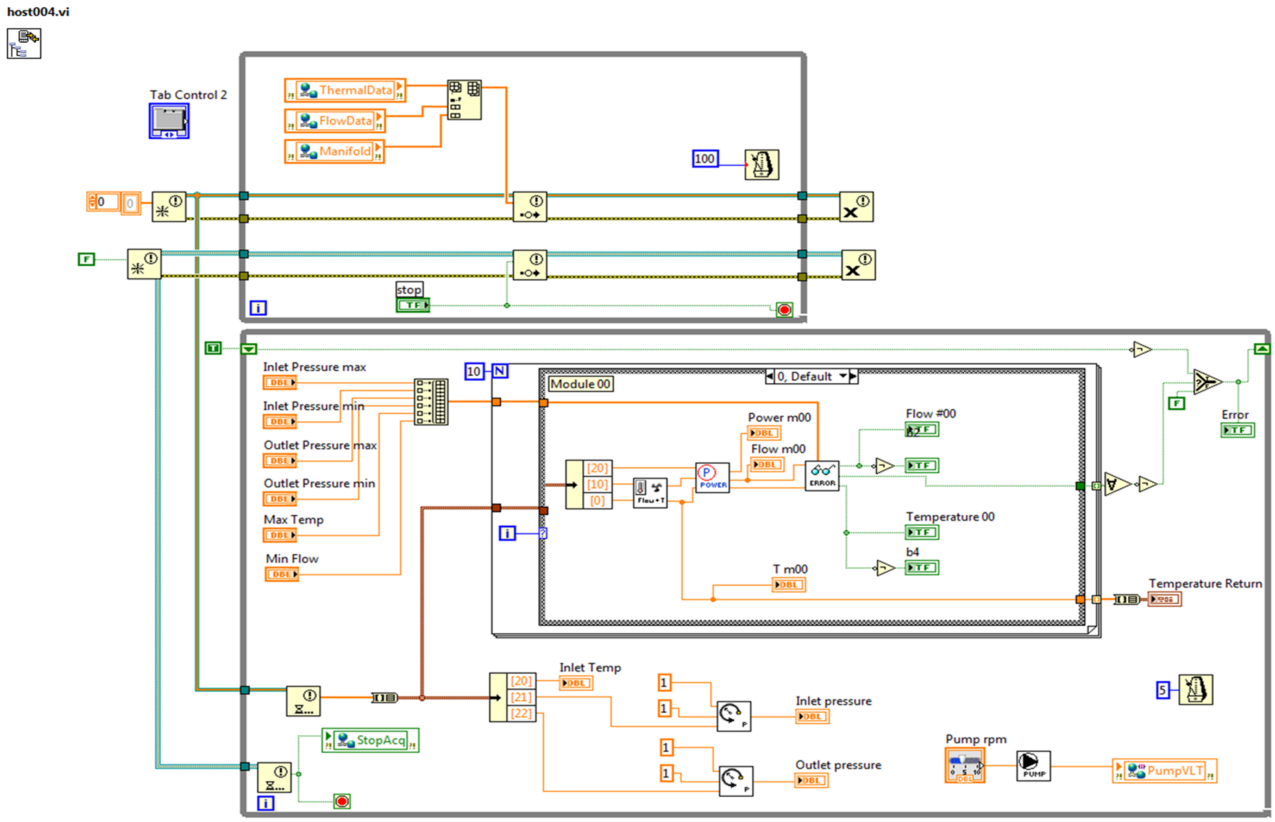


Figure D.4. Host VI used to handle all the signals for monitoring at the GUI.

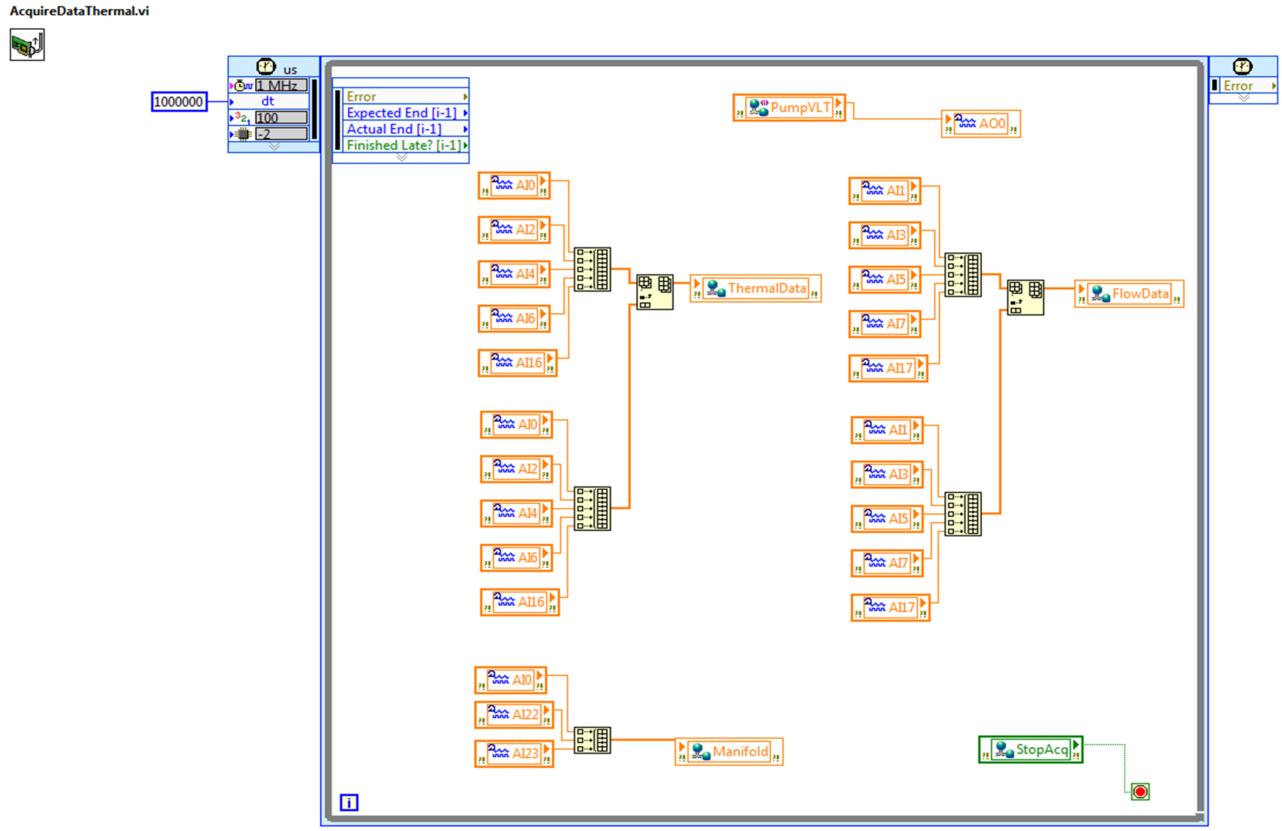


Figure D.5. Acquisition of signals from NI modules by means of Shared Variables.

D.3 Cooling system layout

The complete layout of the cooling system with the corresponding sensors is given in Fig. D.6.

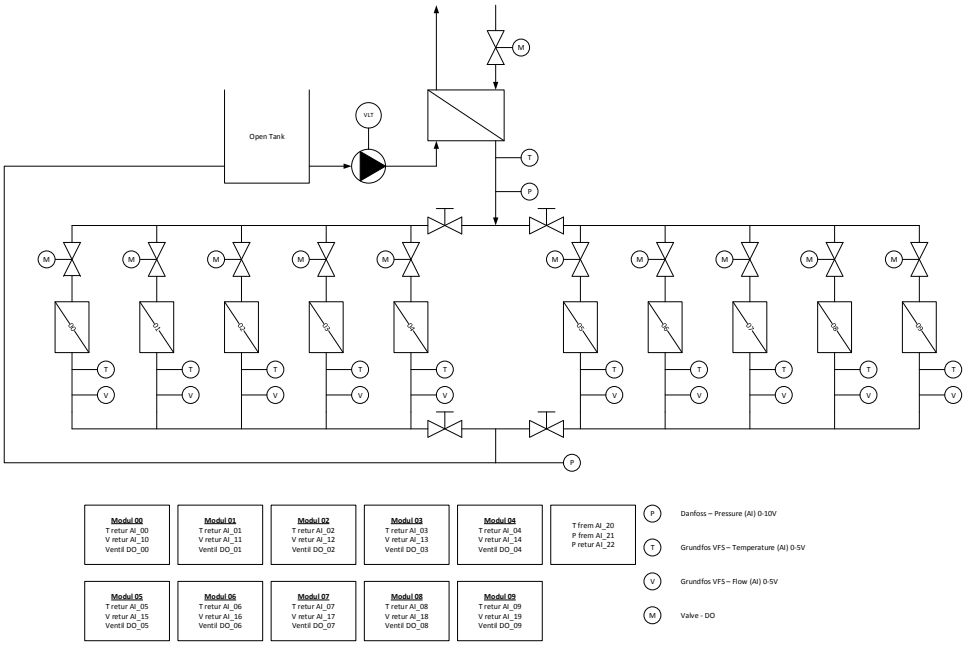


Figure D.6. Layout of the cooling system implemented in the PC test setup, Sven.

Contents of the CD E

The CD attached with the project contains the following documents and files:

- A PDF file containing this report, *Power cycling test setup for accelerated wear-out of high power IGBT modules*.
- The literature references used in this report.
- The screenshots of the experimental results obtained in the laboratory.
- A MATLAB file containing the PLECS model of the accelerated wear-out test setup (Sven).
- An LTspice file containing the electrical model of the accelerated wear-out test setup (Sven).