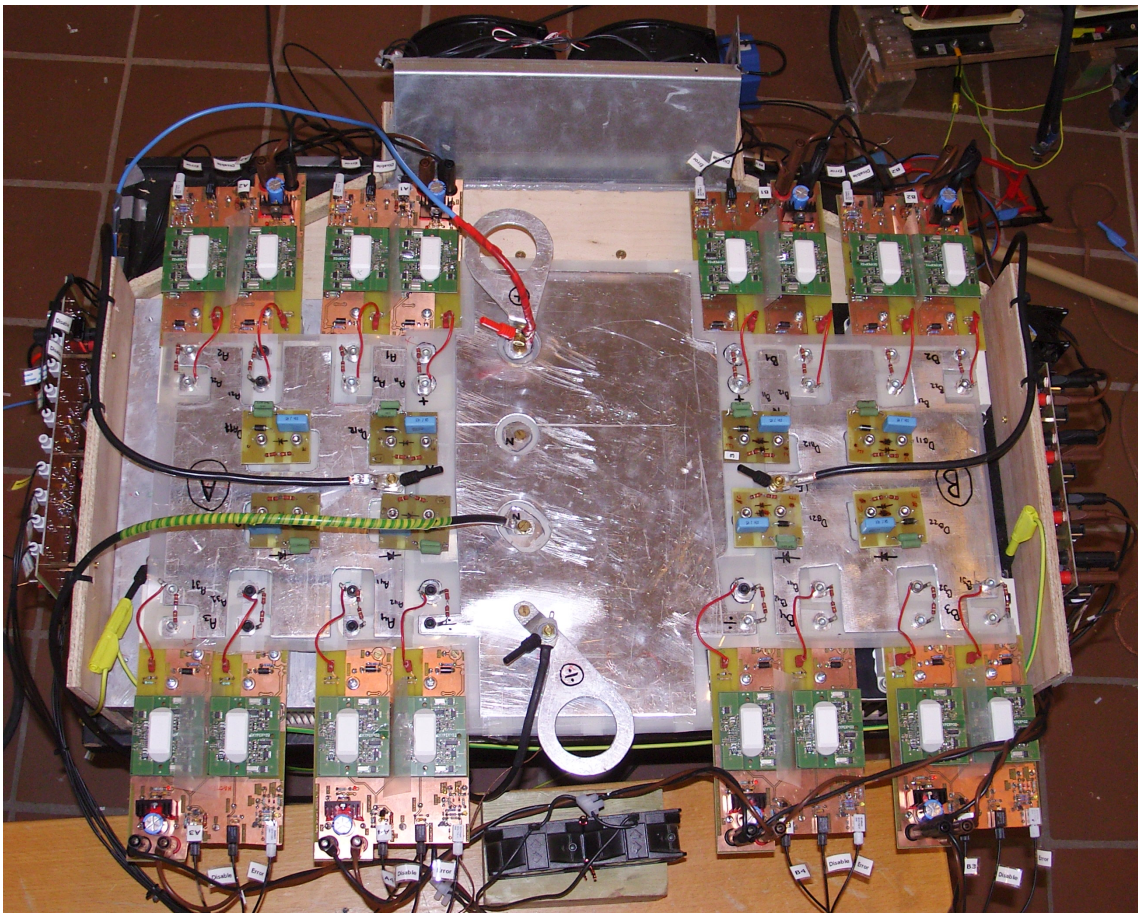
Three-Level Inverter for Medium Level Voltage Using Series Connected IGBTs

AALBORG UNIVERSITET

Institute of Energy Technology,
Master Thesis



Conducted by:
Mads Chr. Pilgaard Vaerens & Jan Sundvall
Group PED 1014 , Spring 2008

AALBORG UNIVERSITET

Institute of Energy Technology
Pontoppidanstrde 101
Telephone 96 35 92 40
Fax 98 15 14 11
http://www.iet.aau.dk

Summary:

Wind turbines of today reach power levels of more than $5MW$, and this puts large requirements to the used electrical components. If the wind turbine inverter setup is based on the back to back topology and full scale power conversion, then all the power is transferred across a common DC link. The voltage rating of the DC link is in the area of $1kV$, and this results in a high current rating, and hence large conductors are needed. If the voltage rating of the DC link can be increased, then the conduction losses, and hence the size of the conductors, could be reduced.
The goal of this master project is, to analyze the implementation of medium voltage level (+2.4kV) in the DC link, by means of standard IGBTs. The required increase in voltage rating is obtained, by utilizing the three-level inverter topology, and basing it on series connected standard IGBT modules. Also, protection schemes suited for the inverter is analyzed.
Based on the results from the analysis, a two phase three-level NPC inverter system rated for a DC link voltage of $2.4kV$, and a current rating of $200A$ was designed, realized and tested. To ensure equal voltage sharing and dynamic performance of the series IGBTs, snubber circuits was analyzed, designed and implemented in the setup. The protection scheme of the inverter was based on desaturation detection and voltage clamping. To perform the required tests of the system, a medium voltage DC power supply and an inductive load was build.
The results of the tests was, that by series connecting IGBTs, the voltage rating of an inverter can be increased with acceptable performance due to the incorporated zener clamped snubber circuits. The three-level topology is well suited for the medium voltage level, due to its voltage sharing nature. The voltage clamping protection did not have the expected performance, and therefore this method was not the optimal choice for this project.

Title:

"Three-Level Inverter for Medium Level Voltage Using Series Connected IGBTs"

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Participants:

Mads Christian Pilgaard Vaerens
Jan Sundvall

Supervisor:
Stig Munk-Nielsen, Associate professor

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Preface

This Master Thesis is conducted at the Faculty of Engineering, Science and Medicine at Aalborg University. It is written by group PED 1014 during the period from 5th of February to 4th of June 2008. The project title *Three-Level Inverter for Medium Level Voltage Using Series Connected IGBTs* is formulated by collaboration of the project group and supervisor Stig Munk-Nielsen. The report is directed to everyone with knowledge of electro physics, power electronics and interests in the given subject.

Thanks to supervisor Stig Munk-Nielsen for valuable guidance, and to Siemens Wind Power for believing in our ideas. A special thanks goes to Philip Waite and his team from Siemens Wind Power at Keele England, for input, inspiration and hardware support.

And to our wifes; Sorry!

Reading Instructions

- References in the text are specified in square parenthesis according to the Harvard method as for example [Ned Mohan, 2003]. The literature list is placed on page 151.
- Figures are numbered continuously in their respective chapters. For example figure 4.1 is the first figure in chapter 4.
- Equations are numbered in the same way as figures, but they are shown in brackets. For example equation (4.1).
- Appendices, source code and documents are attached on a CD-ROM on the last page. The contents of the CD-ROM is shown on page 148.
- Nomenclature list with used variables and notations is on page 147. Examples of the notation of the report is shown below.

Parameter:	**Notation:**
Time dependent current	i_{load}
RMS or DC current	I_{load}
Peak current	$\widehat{i}_{load} = \pm 100A$
Peak to peak current	$\widehat{i}_{load,pp} = 100A$

The Master Thesis is conducted by:

Mads Christian Pilgaard Vaerens

Jan Sundvall

Contents

Chapter 1

Introduction

The world's need for electrical energy is increasing every year, and large initiatives within alternative energy sources have been going on for years. One of these sources is wind. In this technology the winds kinetic energy is converted to electrical energy using wind turbines scaling from a few kW of output power up to $5MW$ in the largest turbines today (2008). And the tendency is going toward even greater output power in the future.

Figure 1.1 shows the evolution of the size and output power of commercial wind turbines over the past 20 years. The largest turbine on the market today is a $5MW$ model produced by German RePower.

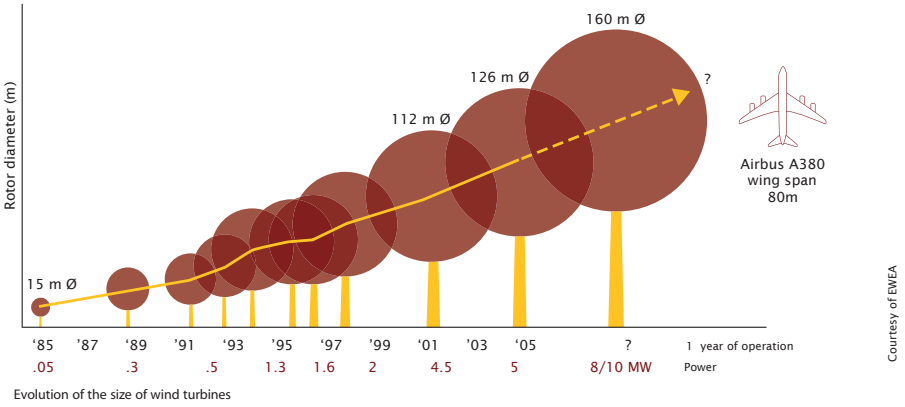


Figure 1.1: *History of physical size and output power of wind turbines [European_Commission, May 2006].*

Modern wind turbines are designed to operate at variable wind speeds and therefore at variable rotor angular speeds. This is realized by use of high power inverters made of power electronics devices. These inverters convert a voltage of variable frequency into a voltage with constant output frequency. Many different configurations have been developed and used for years, and three very popular systems, based on the back to back inverter topology, are shown on figure 1.2, 1.3 and 1.4.

Figure 1.2 shows a multi pole permanent magnet generator system, which is connected to the grid with a transformer and a full scale back to back inverter. The permanent magnet machine does not require external magnetization, and therefore the power only flows in one direction from the generator to the inverter. Often multi pole machines do not require the mechanical gear box.

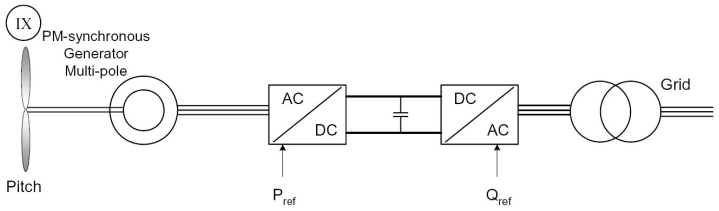


Figure 1.2: *Electrical system in a turbine with permanent magnet generator [Blaabjerg, 2006].*

Figure 1.3 shows a squirrel cage induction generator system with a full scale inverter. Squirrel cage machines require external magnetization from the grid, and because of this, the left side of the inverter is realized identically to the right side inverter. In this way, power can flow bidirectional controlled by the switching pattern of the semiconductors.

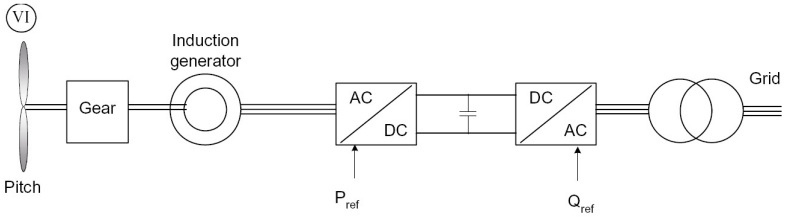


Figure 1.3: *Electrical system in a turbine with squirrel cage induction generator [Blaabjerg, 2006].*

Figure 1.4 shows a wounded rotor induction generator (slip ring) system. In this system, the stator carries the main part of power. The advantage is the possibility to use a small scale inverter to control the stator frequency by controlling the rotor frequency independently of rotor speed. Usually the power fraction between rotor and stator is $15 - 20\%$.

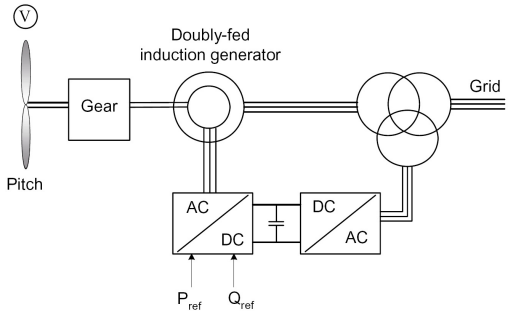


Figure 1.4: *Electrical system in a turbine with doubly fed induction generator [Blaabjerg, 2006].*

1.1 Scope of project

In this project, the main objective is to investigate the possibility of increasing the DC link voltage in full scale back to back inverter. The benefit of this is to be able to decrease the currents in the inverter and generator and by this lower the conduction losses. The project work is done in corporation with Siemens Wind Power, who is supplying the project with the hardware listed below:

- 36 Semikron SKM 600GA176D single pack IBGTs rated $1.7kV$ and $600A$.

- 24 Semikron Skyper 32 dual IGBT gate drivers.

Losses in modern turbines require great attention, though the losses in percentage seem to be rather low. Usually the inverter efficiency is in the approximately 97%, but for a $5MW$ turbine this leads to around $P_{loss} = 0.03 \cdot 5MW = 150kW$ of losses, and the heat produced must be distributed away from the turbine in one way or another, requiring additional cooling hardware and an increase in price.

When calculating conduction losses, the currents in the circuit are of great importance. The RMS phase to phase voltage from modern wind turbine generators is generally between $600V$ and $1kV$ depending on the output power. If the full scale topology described in figure 1.2 is used for the largest $5MW$ turbines power range, the phase currents will become

$$P = V \cdot I \cdot \sqrt{3} \quad \Rightarrow \quad I = \frac{P}{V \cdot \sqrt{3}} = \frac{5MW}{1kV \cdot \sqrt{3}} = 2.89kA \tag{1.1}$$

assuming unity power factor. These quantities of current require relatively large cross sectional area in the conductors used in the generator, inverter and the transformer primary windings.

The main motivation for increasing the generator phase to phase voltage to medium voltage level is due to the conduction losses given by:

$$P_R = I^2 \cdot R, \quad \text{with } R = \rho \cdot \frac{l}{A} \quad \Rightarrow \quad P_R = I^2 \cdot \underbrace{\rho \cdot \frac{l}{A}}_{constant} \tag{1.2}$$

where ρ is the resistivity of the material.

It's clear, that the losses will be proportional to the current squared for a given conductor. By increasing the generator voltage, the current can be decreased for a given power and lead to lower resistive losses in the electrical circuit.

However, increasing the voltage level of the generator does require either additional windings, higher flux density or higher rotor speed. And also the isolation level of the inverter, busbar, generator and transformer windings must be increased. But the cross sectional area of the windings can be reduced at the same time, so the increase in generator windings may not lead to a physically larger or heavier generator.

Another disadvantage of increasing the voltage rating of the inverter is , that the service of the wind turbine needs to be handled by specialists rather than electricians, due to safety regulations regarding medium and high voltage.

The medium voltage range

Regarding the medium voltage (MV) range, there is no universally accepted definition. The definitions vary by industry, country, and application.

- For AC motor drives, the range usually reaches from above $600V$ up to $15kV$. The MV threshold in Europe is $1kV$.
- DC drive products typically have a range from $2.3kV$ to $7.2kV$.
- Standard North American medium line voltages are $2.3kV$ and $4.16kV$, while predominating line voltages in Europe and the rest of the world are $3.3kV$ and $6.6kV$ for medium voltage.

In this project, the medium voltage range is defined as

$$\boxed{2.3kV_{DC} < V_{MV} < 7.2kV_{DC}}$$

1.2 Initial problem formulation

The goal of this project is, to design, build and test an inverter suited for medium voltage level using series connected IGBTs. The reason for using series connected IGBTs is, to reach the medium voltage level by means of standard components. A secondary goal of the project is, to analyze, design and implement a protection strategy for the inverter. From the goal of the project, the following initial problem can be stated:

How to design an inverter for medium voltage level using series connected IGBTs?

From this initial problem formulation, the following will be performed in part I of the report:

- Analysis and comparison of inverter topologies suitable for medium voltage range.
- Analysis and characterization of high power IGBTs.
- Analysis of series connection of IGBTs to obtain higher blocking capabilities.
- Analysis of snubbers for realizing the series connection.
- Analysis of IGBT fault mechanisms and protection.

The initial requirements and limitations of the project are chosen to:

- The DC link voltage value is chosen to $V_{DC} = 2.4kV \pm 10\%$ ripple. This is based on a project conducted by this group on 9th semester [Mads P. Vaerens, 2007].
- The load current is initially chosen to $\widehat{i}_{load} = \pm 200A$. This means, that only one third of the rated current for the IGBTs is applied, resulting in a 200% safety margin.
- Only the grid side inverter of the back to back topology is analyzed.

Part I:
Problem Analysis

Chapter 2

Three-level inverter

In this chapter, the three-level inverter is analyzed. This is done to identify the advantages and disadvantages of this inverter topology, especially regarding the medium voltage range. Section 2.1 covers the basics of the three-level neutral point clamped (NPC) inverter. In section 2.2, the three-level inverter is compared to the two-level inverter, and finally the sinusoidal PWM modulations strategies *carrier based modulation with third harmonic injection* and *space vector modulation* are analyzed in section 2.3.

2.1 Three-level NPC inverter basic

The three-level inverter is an alternative to the two-level inverter, and it has some advantages, that makes it better suited for a medium voltage application. Figure 2.1 shows the schematic of a three-level three phase inverter. One of the advantages of the three-level inverter is, that the transistors always turn on and off in pairs. This means, that the full DC link voltage will always be shared by two switches, where the two level inverter switches has to be able to block the full DC link voltage.

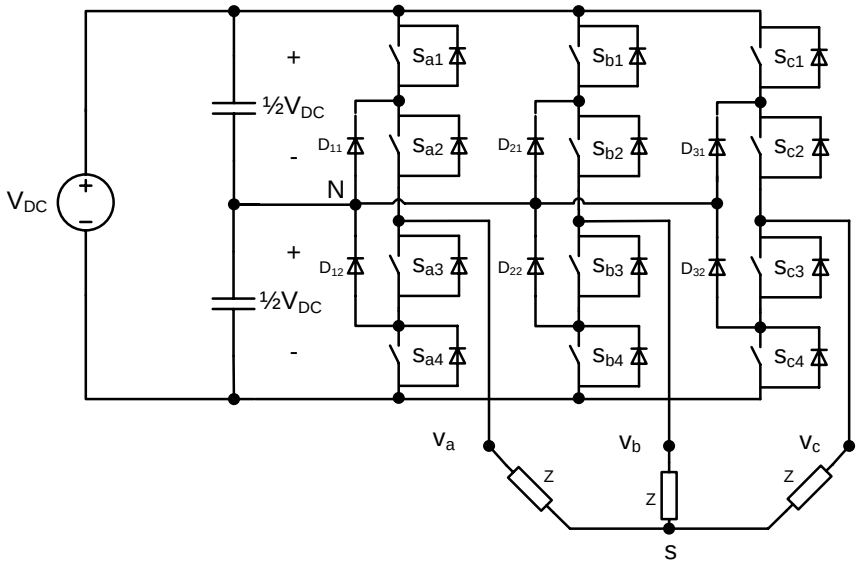


Figure 2.1: *Three-level three phase inverter schematic with star connected load.*

But a trade off is, that it consist of twice as many transistors as its two level counterpart plus the six neutral point diodes. The switching scheme of a three-level NPC inverter has three states; + where switch 1 and 2 are turned on, 0 where the middle switches 2 and 3 are on, and − where switch 3 and 4 are turned on. The +, 0 and − states are in some literature ex. [Lipo, 2003] denoted m_{x1}, m_{x2} and m_{x3}, where index x

refers to the leg. The m values then takes the values 1 or 0, if the switch states are on or off. A rule that must be obeyed is, that $m_{x1} + m_{x2} + m_{x3} = 1$, meaning that only one state is active at the time. For instance, the line to neutral point voltage v_{aN} can be written as:

$$v_{aN} = \frac{1}{2} V_{DC} \cdot (m_{a1} - m_{a3}) \tag{2.1}$$

which means, that if the upper two switches in leg a of figure 2.1 are turned on, then the two lower switches are turned off, and v_{aN} becomes:

$$v_{aN} = \frac{1}{2} V_{DC} \cdot (1 - 0) = \frac{1}{2} V_{DC} \tag{2.2}$$

This gives a phase voltage of three levels shown on figure 2.2.

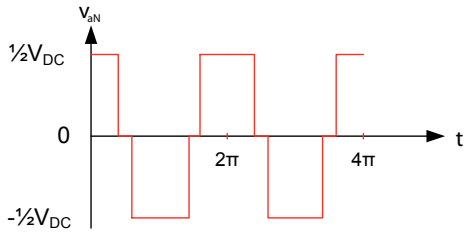


Figure 2.2: *v_{aN} voltage waveform.*

Because of the fact, that the switches are turned on in pairs, the phase voltage v_{aN} can never become larger than $\frac{1}{2} V_{DC}$. The phase to phase voltage v_{ab} can be written as:

$$v_{ab} = v_{aN} - v_{bN} = \frac{1}{2} V_{DC} \cdot (m_{a1} - m_{a3} - m_{b1} + m_{b3}) \tag{2.3}$$

This means, that if leg a is $+$ and leg b is $-$, v_{ab} is equal to V_{DC} because:

$$v_{ab} = v_{aN} - v_{bN} = \frac{1}{2} V_{DC} \cdot (1 - 0 - 0 + 1) = V_{DC} \tag{2.4}$$

So in total, the three-level inverter topology is capable of producing a phase to phase voltage v_{ab} of five voltage levels shown in figure 2.3.

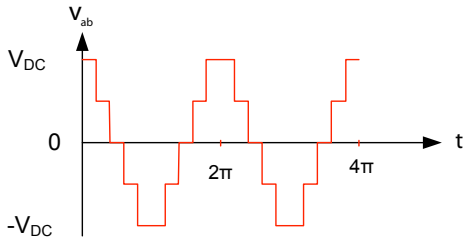


Figure 2.3: *v_{ab} voltage waveform.*

The voltage v_{sN} from the star point s to the neutral point N can be found from using the superposition principle.

On figure 2.4, the connection from N to s is illustrated. By using superposition on the circuit, v_{sN} can be written as:

$$v_{sN} = v_{aN} \frac{Z}{Z \| Z + Z} = \frac{1}{3} v_{aN} \tag{2.5}$$

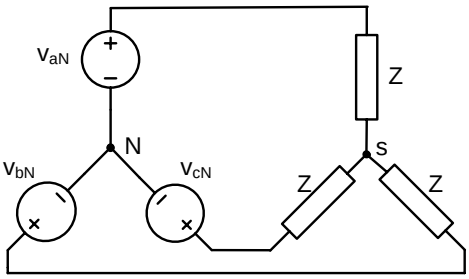


Figure 2.4: *Three phase voltage source with star connected load.*

By applying this to all three phases, v_{sN} becomes:

$$v_{sN} = \frac{1}{3}(v_{aN} + v_{bN} + v_{cN}) \tag{2.6}$$

The phase voltages can now be written as:

$$v_{as} = v_{aN} - v_{sN} \tag{2.7}$$
$$v_{bs} = v_{bN} - v_{sN} \tag{2.8}$$
$$v_{cs} = v_{cN} - v_{sN} \tag{2.9}$$

To find the relationship between the phase voltage and the switch states, the following is used.

$$v_{as} = v_{aN} - v_{sN} \tag{2.10}$$
$$v_{as} = v_{aN} - \frac{1}{3}(v_{aN} + v_{bN} + v_{cN}) \tag{2.11}$$
$$v_{as} = \frac{2}{3}v_{aN} - \frac{1}{3}v_{bN} - \frac{1}{3}v_{cN} \tag{2.12}$$
$$v_{as} = \frac{1}{2}V_{DC} \cdot \left(\frac{2}{3}m_a - \frac{1}{3}m_b - \frac{1}{3}m_c\right) \tag{2.13}$$
$$v_{as} = \frac{1}{3}V_{DC} \cdot \left(m_{a1} - m_{a3} - \frac{1}{2}\left(m_{b1} - m_{b3} + m_{c1} - m_{c3}\right)\right) \tag{2.14}$$

This shows, that the three-level inverter is capable of producing a phase to star point voltage of seven levels as shown on figure 2.5, which reduces the harmonic contents of the output compared to the two level inverter. The largest output voltage value is $\pm\frac{2}{3}V_{DC}$.

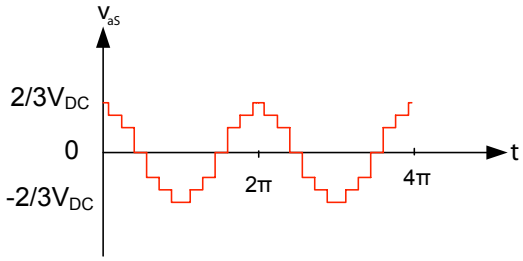


Figure 2.5: v_{as} *voltage waveform.*

However, all the voltage equations are only valid for a balanced DC link voltage across the neutral point of the inverter. This constrain makes the control of a three-level inverter more complex than the two level inverter, if not having a neutral point in the power supply. This will be further analyzed later in section 2.3.2.1.

2.2 Three-level vs. Two-level

After analyzing the three-level inverter, a comparison with the common two-level inverter is performed. From the previous section, it is clear, that the three-level inverter consists of twice the number of switches, and on top of this the six neutral point diodes. So one leg of a three-level inverter will consist of the same number of semiconductors as a three-phase two-level inverter. However, due to the switching nature of the three-level inverter, each device will only be subjected to half the DC link voltage. This means, that lower rated devices can be used for a three-level inverter. IGBTs for a lower voltage rating will typically have lower switching losses. This enables the inverter to either increase the switching frequency, or have less cooling. A higher switching frequency can in some applications lead to other components, ex. filters, to have smaller values. But the operating principle of the three-level inverter also means, that two switches is conduction at the same time, meaning two conductions losses instead of one, and typically a double rated IGBT device will not possess the double on-state voltage drop. This is further investigated in chapter 3, where IGBTs in series connections are analyzed.

The fact that each switch in the three-level inverter only requires half the voltage rating of a two-level inverter, also makes it a good choice in medium voltage applications, which is the main topic of this project. A disadvantage of the three-level inverter is unequal power dissipation in the switches due to the switching nature. Switch 2 and 3 is conducting for a longer time than 1 and 4, hence more conducting loss. This can lead to a difference in lifetime for the switches, and also complicate the cooling design. Another aspect of the three-level inverter vs. the two-level counterpart, is the harmonic contents of the output voltage which is investigated in the following.

2.2.1 Harmonic contents

Harmonic contents of the output voltage determines the fraction of the output energy, that is related to the fundamental waveform. For instance, how much of the energy is related to the harmonic contents in a PWM signal. To determine the power of the harmonic contents, the Total Harmonic Distortion or THD factor can be calculated. THD is defined as:

$$THD = \frac{Harmonic\,power}{Fundamental\ frequency\,power} = \frac{I \cdot V}{I_1 \cdot V_1} \quad [-] \tag{2.15}$$

Where I_1 and V_1 are fundamental RMS values. By applying Fourier series, a signal can be split into DC, fundamental and harmonic parts:

$$v(t) = V_{DC} + V_1 \cdot cos(\omega_1 t) + V_2 \cdot cos(\omega_2 t) + V_3 \cdot cos(\omega_3 t) + V_4 \cdot cos(\omega_4 t)..... \tag{2.16}$$

The V_{DC} term will be noted as $\frac{V_{DC}}{2}$ in the upcoming calculations. This is done to keep the notation from the previous section. All the capital variables are RMS values. Because inverters in most applications have a low pass filter on the output, it is important to have a small THD factor to preserve most of the energy. By dividing the output voltage into the DC, fundamental component and the harmonics, the following can be stated:

$$V = \sqrt{\left(\frac{V_{DC}}{2}\right)^2 + \sum_{n=1}^{\infty} V_n^2} = \sqrt{\left(\frac{V_{DC}}{2}\right)^2 + V_1 + \sum_{n=2}^{\infty} V_n^2} \tag{2.17}$$

By division of V_1 equation (2.17) becomes:

$$V = V_1 \cdot \sqrt{1 + \left(\frac{\frac{V_{DC}}{2}}{V_1}\right)^2 + \sum_{n=2}^{\infty} \left(\frac{V_n}{V_1}\right)^2} \tag{2.18}$$

Because the THD is defined as [Lipo, 2003]:

$$THD = \sqrt{\left(\frac{\frac{V_{DC}}{2}}{V_1}\right)^2 + \sum_{n=2}^{\infty} \left(\frac{V_n}{V_1}\right)^2} \tag{2.19}$$

then equation (2.18) can be rewritten to:

$$V = V_1 \cdot \sqrt{1 + THD^2} \tag{2.20}$$

And the THD can be isolated from this equation to:

$$THD = \sqrt{\left(\frac{V}{V_1}\right)^2 - 1} \tag{2.21}$$

Because the output voltage from power electronics is formed by square waves, the DC component and the even harmonics are cancelled out, so the following is obtained:

$$THD = \sqrt{\sum_{n=3,5,7..}^{\infty} \left(\frac{V_n}{V_1}\right)^2} \tag{2.22}$$

As an example, the THD of a square wave can be calculated by using the following series [Ned Mohan, 2003]:

$$1 + \frac{1}{3^2} + \frac{1}{5^2} + \frac{1}{7^2} + \frac{1}{9^2} + \frac{1}{11^2} .... = \frac{\pi^2}{8} \tag{2.23}$$

$$THD_{sqw} = \sqrt{\left(\frac{\pi^2}{8} - 1\right)^2} = 0.483 \tag{2.24}$$

To apply this to the two-level inverter, the levels of output voltage amplitudes is needed. To compare the two-level inverter with the three-level inverter, it is assumed that the two topologies have star-connected loads, and the base for comparison is the phase to star point voltage v_{as}, which for both inverters have the highest number of levels, and thereby is most quasi sinusoidal. The phase to neutral output voltage v_{as} from a two level inverter is seen on figure 2.6.

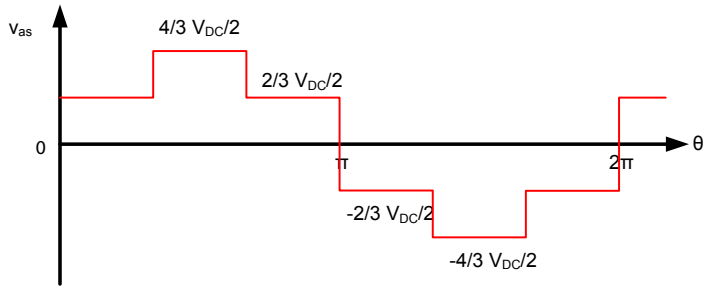


Figure 2.6: *Phase to star-point voltage v_{as} levels for two-level inverter. Freely after [Lipo, 2003].*

From figure 2.6 it is seen, that the numerical value of the output voltage is symmetrical around π. From this, the RMS value can be calculated as:

$$V_{as} = \sqrt{\frac{1}{T} \cdot \int_0^T v_{as}^2 dt} = \sqrt{\frac{1}{\pi} \cdot \int_0^\pi v_{as}^2 d\theta} \tag{2.25}$$

$$V_{as}^2 = \frac{1}{\pi}\left[\frac{\pi}{3}\left(\frac{4}{3}\right)^2 + \frac{2\pi}{3}\left(\frac{2}{3}\right)^2\right] \cdot \left(\frac{V_{DC}}{2}\right)^2 = \frac{8}{9} \cdot \left(\frac{V_{DC}}{2}\right)^2 \Rightarrow \tag{2.26}$$

$$V_{as} = \frac{2 \cdot \sqrt{2}}{3} \cdot \frac{V_{DC}}{2} \tag{2.27}$$

The fundamental output voltage RMS value is found in [Lipo, 2003] as $v_{as1} = 0.9 \cdot \frac{V_{DC}}{2}$. By using equation (2.21) the THD is found as:

$$THD_{2level} = \sqrt{\left(\frac{\frac{2\cdot\sqrt{2}}{3}}{0.9}\right)^2 - 1} = 0.311 \tag{2.28}$$

For the three level inverter, equation (2.21) is also useful for calculating the THD. From [Lipo, 2003], the RMS value of the fundamental output voltage for the three-level inverter can be calculated as:

$$V_{as1} = \frac{4}{\sqrt{2}\cdot\pi}\int_0^{5\pi/12} \frac{V_{DC}}{2}\cdot cos(\theta)d\theta \tag{2.29}$$

$$V_{as1} = \frac{2\cdot\sqrt{2}}{\pi}\cdot sin\left(\frac{5\cdot\pi}{12}\right)\cdot\frac{V_{DC}}{2} \approx 0.87\cdot\frac{V_{DC}}{2} \tag{2.30}$$

The total RMS output voltage can be calculated from the RMS definition.

$$V_{as} = \sqrt{\frac{1}{T}\cdot\int_0^T v_{as}^2 dt} \tag{2.31}$$

So

$$V_{as}^2 = \frac{1}{T}\cdot\int_0^T v_{as}^2 dt = \frac{2}{\pi}\cdot\int_0^{\pi/2} v_{as}^2 d\theta \tag{2.32}$$

The $\pi/2$ limit for the integral is chosen from figure 2.5 on page 8, because the waveform is periodic by this factor, if the numerical values of the voltage amplitude is used. From figure 2.5 the RMS output voltage can be calculated as:

$$V_{as}^2 = \frac{2}{\pi}\left[\frac{\pi}{12}\left(\frac{4}{3}\right)^2 + \frac{\pi}{6}(1)^2 + \frac{\pi}{6}\left(\frac{2}{3}\right)^2 + \frac{\pi}{12}(0)^2\right]\cdot\left(\frac{V_{DC}}{2}\right)^2 \Rightarrow \tag{2.33}$$

$$V_{as} = \frac{\sqrt{7}}{3}\frac{V_{DC}}{2} \tag{2.34}$$

Now, by applying equation (2.21), the THD can be calculated as:

$$THD_{3level} = \sqrt{\left(\frac{V_{as}}{V_{as1}}\right)^2 - 1} = \sqrt{\left(\frac{\frac{\sqrt{7}}{3}\cdot\frac{V_{DC}}{2}}{\frac{2\cdot\sqrt{2}}{\pi}\cdot sin\left(\frac{5\cdot\pi}{12}\right)\cdot\frac{V_{DC}}{2}}\right)^2 - 1} \tag{2.35}$$

$$THD_{3level} = 0.169 \tag{2.36}$$

This is an improvement over the two-level inverter with a THD of 0.311.
The THD comparison between the two topologies is based on an unmodulated output voltage.

2.3 Modulation of three level inverter

To connect an inverter to the grid or a machine, a sinusoidal output voltage is modulated. In this section, two of the most common PWM modulation strategies, carrier based modulation and space vector modulation, are analyzed in relation to the three level inverter. The common base for comparison of the two methods is the ability to modulate a sinusoidal output voltage.

2.3.1 Carrier based modulation

Carrier based modulation is a simple PWM based control strategy and is commonly used in inverters. The basic operation principle is, to compare a high frequency carrier wave, commonly a triangular or sawtooth waveform, to a modulation waveform, commonly a sinusoidal waveform. Figure 2.7 shows a carrier based modulation scheme for a three-level inverter.

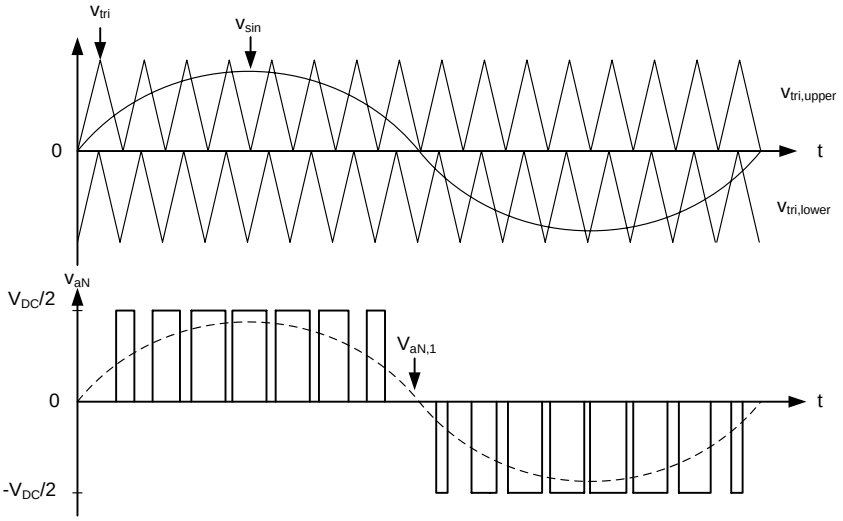


Figure 2.7: *Carrier based modulation scheme for three-level inverter. Top graph shows the modulation and carrier waveform and bottom graph is the generated output voltage pr. leg for a three-level inverter, and the first harmonic (dotted) waveform* $v_{aN,1}$.

One important aspect to notice from figure 2.7 is the double triangle. In a two level inverter, only one triangle is needed, because one leg only produces positive and zero voltage. In section 2.1 it is stated, that the three-level inverter can produce a v_{aN} of both positive, zero, and negative voltage. The upper triangle produce the positive to zero sequence when $v_{sin} > v_{tri,upper}$, and the lower triangle produce the zero to negative sequence of the v_{aN} voltage waveform when $v_{sin} < v_{tri,lower}$. The first harmonic of the output waveform shown on figure 2.7 was analyzed in the previous section, and is given by:

$$\widehat{v}_{aN,1} = Ma \cdot \frac{V_{DC}}{2} \cdot sin(\theta) \quad [V] \tag{2.37}$$

Where the modulation index Ma is given by:

$$Ma = \frac{\widehat{v}_{sin}}{\widehat{v}_{tri}} \quad [-] \tag{2.38}$$

From equation (2.37), it is seen that the maximum value of $\widehat{v}_{aN,1}$ is $\frac{V_{DC}}{2}$ for $Ma = 1$. Using a modulation index greater than one is known as over modulation, and can produce a larger peak value of the fundamental output voltage. However, over modulation is known to produce low-frequency baseband distortion [Lipo, 2003]. A common way of increasing the output voltage peak value, without the modulation indexes exceeding one is known as third harmonic injection and is analyzed in the following.

2.3.1.1 Third harmonic injection

Equation (2.37) can be rearranged to include a third harmonic modulation wave:

$$\widehat{v}_{aN,1+3} = \frac{V_{DC}}{2} \cdot (Ma_1 \cdot sin(\theta) + Ma_3 \cdot sin(3\theta)) \tag{2.39}$$

where Ma_1 and Ma_3 is the modulation index for the first and third harmonic waveform. The maximum value of $\widehat{v}_{sin,1+3}$ is still kept equal to one, but by choosing the relationship between Ma_1 and Ma_3 correct,

$\widehat{v}_{sin,1} > \frac{V_{DC}}{2}$. The optimal relationship can be found from the derivative of equation (2.39), and from the fact, that the third harmonic has no effect if $\theta = (k+1) \cdot \pi/3$ for $k = 0, 1, 2..$ since $sin(3[k+1]\pi/3) = 0$. This will ensure the maximum value for the fundamental component.

$$\frac{d\widehat{v}_{aN,1+3}}{d\theta} = \frac{V_{DC}}{2} \cdot (Ma_1 \cdot cos(\theta) + 3 \cdot Ma_3 \cdot cos(3\theta)) = 0 \quad \Rightarrow \tag{2.40}$$

$$\frac{-Ma_1}{Ma_3} = \frac{3cos(3\theta)}{cos(\theta)} \tag{2.41}$$

For $\theta = \frac{\pi}{3}$, when $\widehat{v}_{aN,3} = 0$:

$$\frac{-Ma_1}{Ma_3} = -6 \quad \Rightarrow \quad Ma_3 = Ma_1 \cdot \frac{1}{6} \tag{2.42}$$

Now, inserting this in equation (2.39) the maximum Ma_1 can be found at $\theta = \frac{\pi}{3}$.

$$\widehat{v}_{aN,1+3} = \frac{V_{DC}}{2} \cdot \left(Ma_1 \cdot sin(\theta) + \frac{Ma_1}{6} sin(3\theta) \right) = \frac{V_{DC}}{2} \quad \Rightarrow \tag{2.43}$$

$$Ma_1 = \frac{2}{\sqrt{3}} \approx 1.16 \tag{2.44}$$

The waveforms is shown in figure 2.8, and the PWM output voltage on figure 2.9, and here it can be seen, that the first harmonic is larger than one, but the output voltage $\widehat{v}_{aN,1+3}$, and thereby the modulation index is still one, meaning that the first harmonic can be higher than one without the base band distortion caused by over modulation.

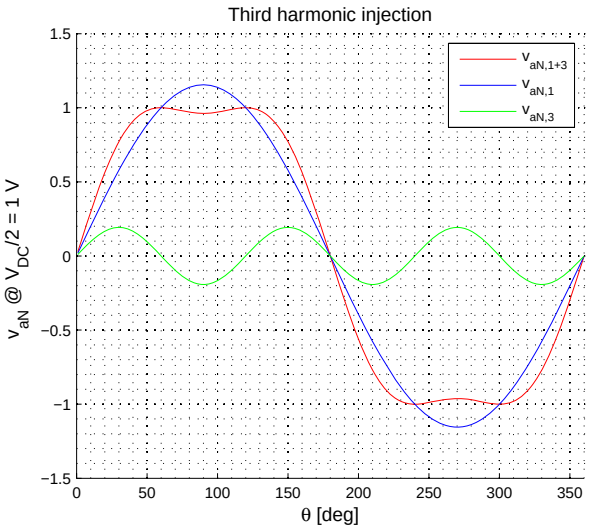


Figure 2.8: *First harmonic, third harmonic and resulting waveform for* $Ma_1 = 1.16$.

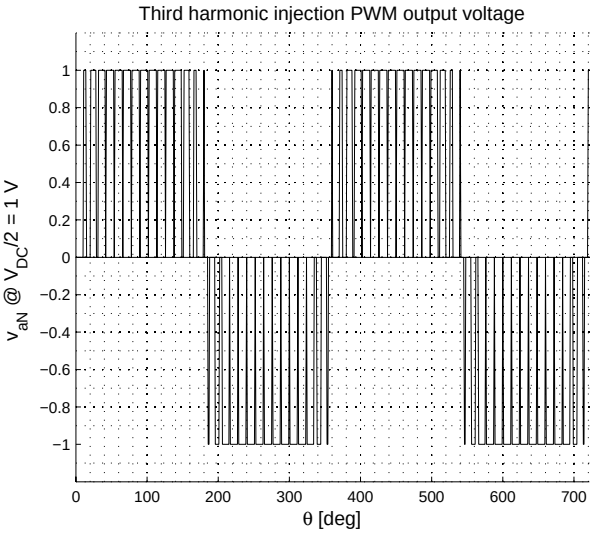


Figure 2.9: *PWM output voltage for carrier based modulation.*

In some literature ex. [Lipo, 2003], a third harmonic of $Ma_3 = \frac{Ma_1}{4}$ is suggested to give the minimum THD. However, this is at cost of the gain in the fundamental waveform, because the modulation index still has to be kept lower than or equal to one to avoid base band distortion.

Even though the resulting waveform of figure 2.8 does not look sinusoidal, the third harmonic, and divisions of the third harmonic is canceled out phase to phase, and hence the output is purely sinusoidal. This can be seen by the following equation:

$$v_{ab} = v_{aN} - v_{bN} \tag{2.45}$$

$$
\begin{aligned}
&= \frac{V_{DC}}{2}[Ma_1 \cdot sin(\theta) + Ma_3 \cdot sin(3\theta)] - \frac{V_{DC}}{2}\left[Ma_1 \cdot sin \cdot \left(\theta + \frac{2\pi}{3}\right) + Ma_3 \cdot sin\left(3\left(\theta + \frac{2\pi}{3}\right)\right)\right] \\
&= \frac{V_{DC}}{2}\left[Ma_1 \cdot sin(\theta) - Ma_1 \cdot sin\left(\theta + \frac{2\pi}{3}\right) + \underbrace{Ma_3 \cdot sin\left(3\theta\right) - Ma_3 \cdot sin\left(3\left(\theta + \frac{2\pi}{3}\right)\right)}_{=0}\right] \\
v_{ab} &= \frac{V_{DC}}{2}\left[Ma_1 sin(\theta) - Ma_1 sin\left(\theta + \frac{2\pi}{3}\right)\right] \qquad (2.46)
\end{aligned}
$$

This means that, even though a third harmonic is injected to give a higher gain, it is cancelled in the phase to phase output voltage. This is also valid for the phase to starpoint voltage v_{as} as shown:

$$
\begin{aligned}
v_{as} &= v_{aN} - \frac{v_{aN} + v_{bN} + v_{bN}}{3} \qquad (2.47) \\
&= \frac{2 \cdot v_{aN}}{3} - \frac{v_{bN}}{3} - \frac{v_{cN}}{3} \\
&= \frac{V_{DC}}{2}\left[\frac{2}{3}\left(Ma_1 \cdot sin(\theta) + Ma_3 \cdot sin(3\theta)\right) - \frac{1}{3}\left(Ma_1 \cdot sin\left(\theta + \frac{2\pi}{3}\right) + Ma_3 \cdot sin\left(3\left(\theta + \frac{2\pi}{3}\right)\right)\right)\right] \\
&\quad -\frac{V_{DC}}{2}\left[\frac{1}{3}\left(Ma_1 \cdot sin\left(\theta - \frac{2\pi}{3}\right) + Ma_3 \cdot sin\left(3\left(\theta - \frac{2\pi}{3}\right)\right)\right)\right] \\
&= \frac{V_{DC}}{2}\left[\frac{2}{3}\left(Ma_1 \cdot sin(\theta)\right) - \frac{1}{3}\left(Ma_1 \cdot sin\left(\theta + \frac{2\pi}{3}\right)\right) - \frac{1}{3}\left(Ma_1 \cdot sin\left(\theta - \frac{2\pi}{3}\right)\right)\right] \\
&\quad \underbrace{-\frac{V_{DC}}{2}\left[\frac{2}{3}\left(Ma_3 \cdot sin(3\theta)\right) - \frac{1}{3}\left(Ma_3 \cdot sin\left(3\left(\theta + \frac{2\pi}{3}\right)\right)\right) - \frac{1}{3}\left(Ma_3 \cdot sin\left(3\left(\theta - \frac{2\pi}{3}\right)\right)\right)\right]}_{=0} \\
v_{as} &= \frac{V_{DC}}{2}\left[\frac{2}{3}\left(Ma_1 \cdot sin(\theta)\right) - \frac{1}{3}\left(Ma_1 \cdot sin\left(\theta + \frac{2\pi}{3}\right)\right) - \frac{1}{3}\left(Ma_1 \cdot sin\left(\theta - \frac{2\pi}{3}\right)\right)\right] \qquad (2.48)
\end{aligned}
$$

The carrier based modulation strategy analyzed in this subsection has the advantage of easy implementation and the possibility of increasing the peak value of the fundamental output by an easy implemented third harmonic reference. This third harmonic sine wave is cancelled out in a balanced system, but gives an ampltude gain to the first harmonic waveform.

2.3.2 Space vector modulation

Another method commonly used is space vector modulation SVM. The voltage space vector $\overline{V}_s$ arises from the sum of the individual voltage vectors in a balanced three phase system, and can be defined according to [Marian P. Kazmierkowski, 2002] as the complex number:

$$
\overline{V}_s = \frac{2}{3}\left(v_a + v_b \cdot e^{-j\frac{2\pi}{3}} + v_c \cdot e^{-j\frac{4\pi}{3}}\right) \qquad (2.49)
$$

In the case of the two-level inverter, there are eight states, including two zero states, as illustrated on figure 2.10.

By applying a duty cycle to two following states ex. (100)-(110), the position of the space vector in quadrant 1 is determined as:

$$
\overline{V_s} = \frac{T_1}{T_s/2}\overline{V}_{100} + \frac{T_2}{T_s/2}\overline{V}_{110} = |\overline{V_s}|\angle\theta \qquad (2.50)
$$

where T_1 and T_2 is the time, that decides the fraction of the half switching period $T_s/2$, hence what duty cycle each state is given. The reason for choosing $T_s/2$ will be explained later in this subsection. The maximum

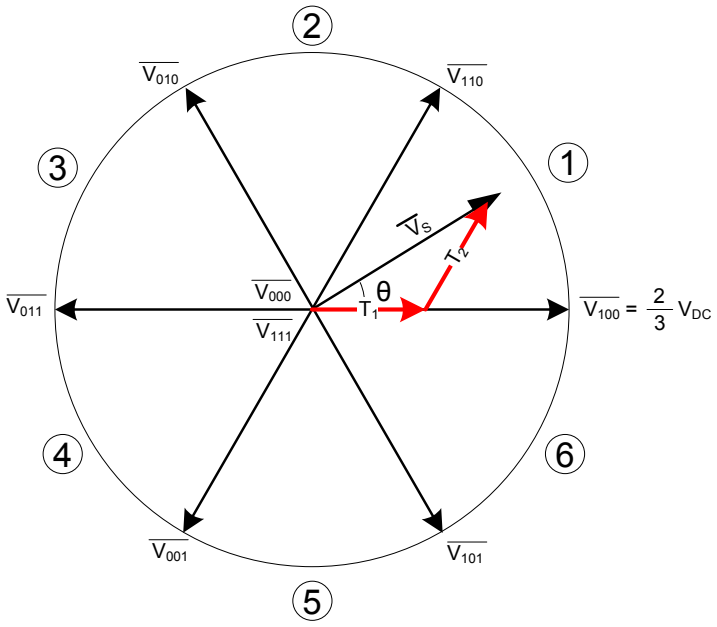


Figure 2.10: *SVM states in the two-level inverter.*

value of the space vector can be calculated as:

$$\begin{aligned} \overline{V}_s = |\overline{V}_s|(cos(\theta) + jsin(\theta)) &= \frac{T_1}{T_s/2}|\overline{V}_{100}|\,(cos(0) + jsin(0)) + \frac{T_2}{T_s/2}|\overline{V}_{110}|\left(cos\left(\frac{\pi}{3}\right) + jsin\left(\frac{\pi}{3}\right)\right) \\ |\overline{V}_s|(cos(\theta) + jsin(\theta)) \cdot T_s/2 &= T_1 \cdot |\overline{V}_{100}| + T_2 \cdot |\overline{V}_{110}| \cdot \left(cos\left(\frac{\pi}{3}\right) + jsin\left(\frac{\pi}{3}\right)\right) \end{aligned} \tag{2.51}$$

The magnitude of the two space vectors is $\frac{2}{3} \cdot V_{DC}$, which can easily be seen by inserting $\overline{V}_{100}$ in equation (2.49). This gives the following results of T_1 and T_2:

$$T_1 = \frac{V_s \cdot sin\left(\frac{\pi}{3} - \theta\right)}{\frac{2}{3} \cdot V_{DC} \cdot sin\left(\frac{\pi}{3}\right)} \cdot \frac{T_s}{2} \quad [s] \tag{2.52}$$

$$T_2 = \frac{V_s \cdot sin(\theta)}{\frac{2}{3} \cdot V_{DC} \cdot sin\left(\frac{\pi}{3}\right)} \cdot \frac{T_s}{2} \quad [s] \tag{2.53}$$

This means, that the time given to the space vectors states are dependent of θ. A constrain in space vector modulation is, that $T_1 + T_2 \leq \frac{T_s}{2}$, meaning that $\overline{V}_s$ can not become larger then $\frac{2}{3} \cdot V_{DC}$.

$$\frac{T_1 + T_2}{T_s/2} = \frac{\left(\frac{V_s \cdot sin\left(\frac{\pi}{3} - \theta\right)}{\frac{2}{3} \cdot V_{DC} \cdot sin\left(\frac{\pi}{3}\right)} \cdot \frac{T_s}{2}\right) + \left(\frac{V_s \cdot sin(\theta)}{\frac{2}{3} \cdot V_{DC} \cdot sin\left(\frac{\pi}{3}\right)} \cdot \frac{T_s}{2}\right)}{T_s/2} \leq 1 \tag{2.54}$$

The value of θ maximizing equation (2.54) is $\theta = \frac{\pi}{6}$ giving:

$$\frac{T_1 + T_2}{T_s/2} = \frac{2 \cdot V_s \cdot sin\left(\frac{\pi}{6}\right)}{\frac{2}{3} \cdot V_{DC} \cdot sin\left(\frac{\pi}{3}\right)} \leq 1 \tag{2.55}$$

$$|\overline{V}_{s,max}| = \frac{3}{\sqrt{3}} \cdot \frac{2}{3} \cdot \frac{V_{DC}}{2} \approx 1.16 \cdot \frac{V_{DC}}{2} \tag{2.56}$$

This results shows, that space vector modulation and carrier based modulation with third harmonic injection yields the same maximum value.

To improve the THD, the two zero vectors $\overline{V}_{000}$ and $\overline{V}_{111}$ can be incorporated in the switching sequence, according to [Lipo, 2003] such as:

$$\frac{T_s}{2} = T_1 + T_2 + 2 \cdot T_0 \tag{2.57}$$

where T_0 is the time given to each zero state. Each zero state is applied for the same amount of time. By placing a zero state in the beginning and the end of a sequence, a symmetrical sequence is obtained by centering the active vectors. This sequence can be written for $0 \leq \theta \leq \frac{\pi}{3}$ as:

$$\underbrace{\overline{V}_{000} + \overline{V}_{100} + \overline{V}_{110} + \overline{V}_{111}}_{\frac{T_s}{2}} + \underbrace{\overline{V}_{111} + \overline{V}_{110} + \overline{V}_{100} + \overline{V}_{000}}_{\frac{T_s}{2}} \tag{2.58}$$

This can be visualized as figure 2.11.

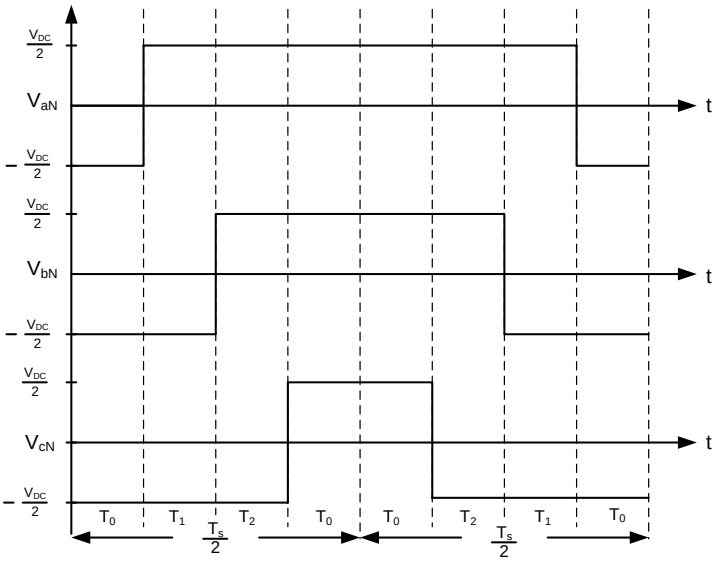


Figure 2.11: *Phase voltage representation of equation (2.58).*

Because of the fact, that $T_s/2$ is chosen, the times T_1 and T_2 given to each vector in equation (2.58) can be recalculated each $T_s/2$, and this gives advantages regarding the THD of the output [Lipo, 2003]. T_1 and T_2 can be calculated for $0 \leq \theta \leq \frac{\pi}{3}$ as:

$$T_1 = \frac{\overline{V}_s}{V_{DC}} \cdot \sqrt{3} \cdot cos\left(\theta + \frac{\pi}{6}\right) \cdot T_s/2 \tag{2.59}$$

$$T_2 = \frac{\overline{V}_s}{V_{DC}} \cdot \sqrt{3} \cdot cos\left(\theta - \frac{\pi}{2}\right) \cdot T_s/2 \tag{2.60}$$

The average space vector for phase a, b and c can be written based on figure 2.11 as:

$$v_{aN} = \frac{V_{DC}}{2} \cdot \left(\frac{T_1}{T_s/2} + \frac{T_2}{T_s/2}\right) \tag{2.61}$$

$$v_{bN} = \frac{V_{DC}}{2} \cdot \left(\frac{-T_1}{T_s/2} + \frac{T_2}{T_s/2}\right) \tag{2.62}$$

$$v_{cN} = \frac{V_{DC}}{2} \cdot \left(\frac{-T_1}{T_s/2} - \frac{T_2}{T_s/2}\right) \tag{2.63}$$

This result gives the following average phase voltages for $0 \leq \theta \leq \frac{\pi}{3}$. The modulation index Ma is included in the equations.

$$v_{aN} = \frac{V_{DC}}{2}\left(\frac{T_1}{T_s/2} + \frac{T_2}{T_s/2}\right) = \frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2} \cdot \left[cos\left(\theta + \frac{\pi}{6}\right) + cos\left(\theta - \frac{\pi}{2}\right)\right] \tag{2.64}$$

$$= = \frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2} \cdot sin\left(\theta + \frac{\pi}{3}\right) \tag{2.65}$$

$$v_{bN} = \frac{V_{DC}}{2}\left(-\frac{T_1}{T_s/2} + \frac{T_2}{T_s/2}\right) = \frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2} \cdot \left[-cos\left(\theta + \frac{\pi}{6}\right) + cos\left(\theta - \frac{\pi}{2}\right)\right] \tag{2.66}$$

$$= \frac{3}{2} \cdot Ma \cdot \frac{V_{DC}}{2} \cdot cos\left(\theta - \frac{2\pi}{3}\right) \tag{2.67}$$

$$v_{cN} = \frac{V_{DC}}{2}\left(-\frac{T_1}{T_s/2} - \frac{T_2}{T_s/2}\right) = \frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2} \cdot \left[-cos\left(\theta + \frac{\pi}{6}\right) - cos\left(\theta - \frac{\pi}{2}\right)\right] \tag{2.68}$$

$$= \frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2} \cdot \left(-sin\left(\theta + \frac{\pi}{3}\right)\right) \tag{2.69}$$

For the other remaining six quadrants, the space vector can be calculated in a similar manner. This is shown i table 2.1. These results are taken from a similar table in [Lipo, 2003].

θ	$\frac{v_{aN}}{\frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2}}$	$\frac{v_{bN}}{\frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2}}$	$\frac{v_{cN}}{\frac{\sqrt{3}}{2} \cdot Ma \cdot \frac{V_{DC}}{2}}$
$0 \leq \theta \leq \frac{\pi}{3}$	$sin\left(\theta + \frac{\pi}{3}\right)$	$\sqrt{(3)} \cdot cos\left(\theta - \frac{2\pi}{3}\right)$	$-sin\left(\theta + \frac{\pi}{3}\right)$
$\frac{\pi}{3} \leq \theta \leq \frac{2\pi}{3}$	$\sqrt{3} \cdot cos(\theta)$	$sin(\theta)$	$-sin(\theta)$
$\frac{2\pi}{3} \leq \theta \leq \pi$	$cos\left(\theta - \frac{\pi}{6}\right)$	$cos\left(\theta + \frac{5\pi}{6}\right)$	$\sqrt{3} \cdot cos\left(\theta + \frac{2\pi}{3}\right)$
$\pi \leq \theta \leq \frac{4\pi}{3}$	$cos\left(\theta - \frac{\pi}{6}\right)$	$\sqrt{3} \cdot cos\left(\theta - \frac{2\pi}{3}\right)$	$cos\left(\theta + \frac{5\pi}{6}\right)$
$\frac{4\pi}{3} \leq \theta \leq \frac{4\pi}{3}$	$\sqrt{3} \cdot cos(\theta)$	$sin(\theta)$	$-sin\theta$
$\frac{5\pi}{3} \leq \theta \leq 2\pi$	$cos\left(\theta + \frac{\pi}{6}\right)$	$cos\left(\theta - \frac{5\pi}{6}\right)$	$\sqrt{3} \cdot cos\left(\theta + \frac{2\pi}{3}\right)$

Table 2.1: *Space vector placement for* $0 \leq \theta \leq 2\pi$.

The graphical interpretation of the space vector calculated in similar fashion for $0 \leq \theta \leq 2\pi$ is plotted on figure 2.12 and the PWM output voltage is plotted on figure 2.13.

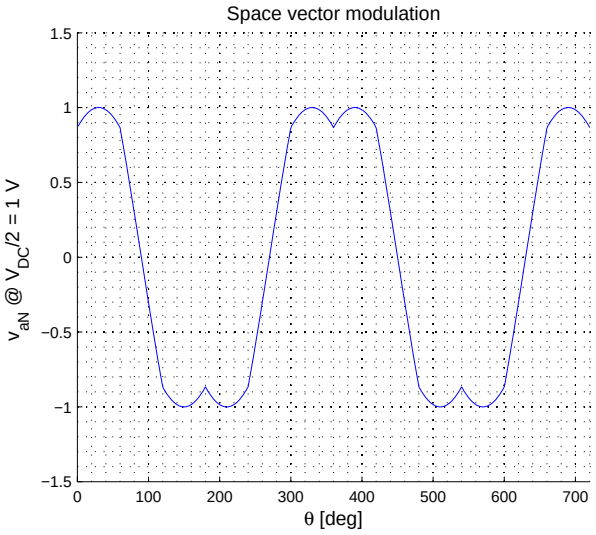


Figure 2.12: *Space vector output wave form for* v_{aN}.

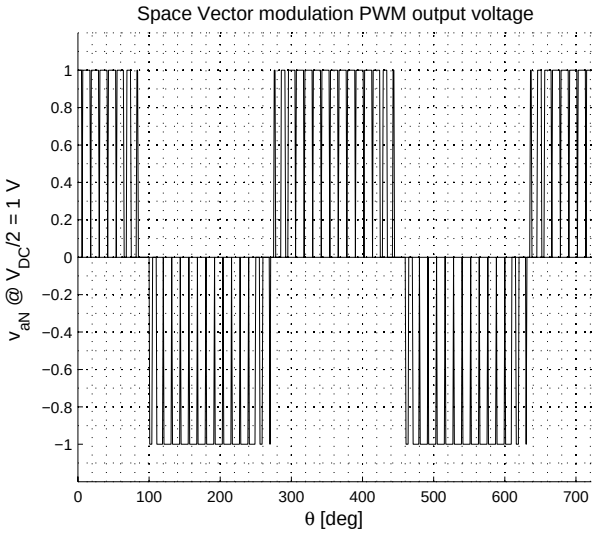


Figure 2.13: *PWM output voltage for space vector modulation.*

The output for the three-level SVM is generated in the same way as for the carrier based modulation by comparing the waveform from figure 2.12 to two triangular waveforms as was illustrated in figure 2.7.

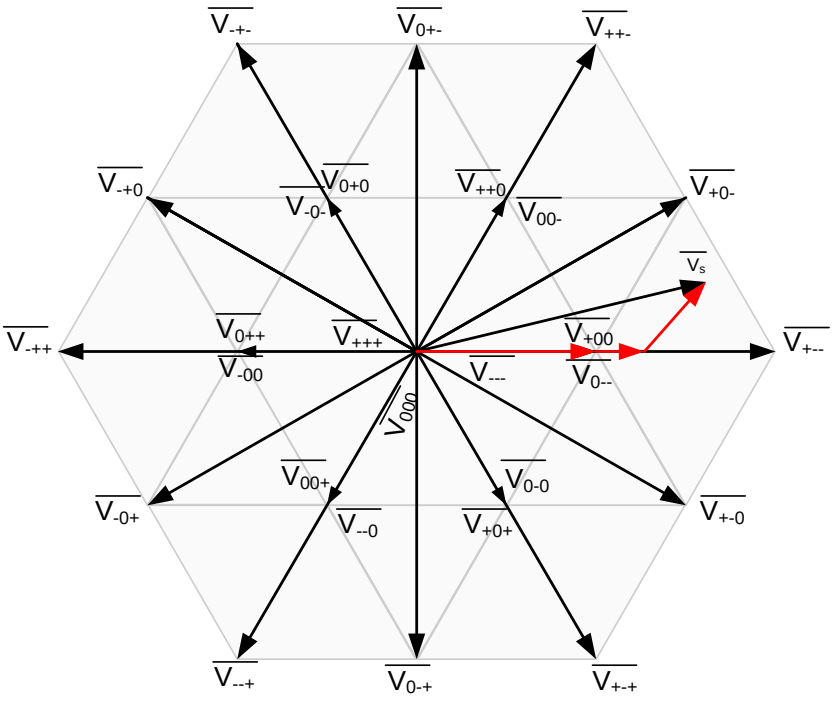


Figure 2.14: *SVM states in the three-level inverter.*

The three level inverter offers some advantages to the two-level inverter in the nature of SVM. The three-level inverter has 27 states, 12 of these states are redundant and the zero vector is triple redundant. The space vector diagram can be presented like figure 2.14.

It can be seen from figure 2.14, that the space vector $\overline{V_s}$ originates in zero, but the vector sequence needed to produce $\overline{V_s}$ does not need to, as is the case for the two-level inverter. Because of the redundant states, the vector sequence needed to produce $\overline{V_s}$ can instead be produced as:

$$\underbrace{\overline{V}_{+00} + \overline{V}_{+--} + \overline{V}_{+0-} + \overline{V}_{0--}}_{\frac{T_s}{2}} + \underbrace{\overline{V}_{0--} + \overline{V}_{+0-} + \overline{V}_{+--} + \overline{V}_{+00}}_{\frac{T_s}{2}} \tag{2.70}$$

This principle is also known as the "nearest three" space vector (NTS), and has the ability to create a more accurate representation of $\overline{V_s}$. This fact can also be linked to the results of section 2.1, where it is stated, that the three-level inverter was able to produce more voltage levels. Another very important aspect of the nearest three space vector (NTS) is, that is has the ability to balance the voltage across the neutral point capacitors as explained in the following.

2.3.2.1 Neutral point balancing

For the basic three level equations in section 2.1 to be exact, the neutral point capacitor voltages are required to be very stable. If the capacitor voltage is allowed to deviate, such that two switches experience a higher voltage than intended, the voltage distribution in the output is compromised. This can cause a current offset, and worst case the switches could be destroyed. This puts high demands, and thereby cost, to the DC link capacitors, because these have to be able to prevent a large voltage drop, when current flows from or to the neutral point. The rate of change of the capacitor voltage can be calculated as:

$$i_c = \frac{dv_c}{dt} \cdot C \quad [A] \tag{2.71}$$

$$dv_c = \frac{dt \cdot i_c}{C} \quad [V] \tag{2.72}$$

This means, that a larger capacitance leads to a lower rate of change in the neutral point voltage, and hence decreased sensitivity.

This is an issue with the three-level and multi-level inverters in general, and a weakness in the NPC topology. However, using the NTS aproach, this problem can be limited. The current flows from or to the neutral point, when a zero state is present in one leg (except from $(0,0,0)$). In order to keep the neutral point balanced, the average current must be zero. The three-level inverter has $3^3 = 27$ different stages, but because the output voltage only has seven levels, there is some redundancy of the switching states. For example, $(0,+,+)$ and $(-,0,0)$ both give an output voltage of $-\frac{1}{3}V_{DC}$ according to equation (2.14) and figure 2.14:

$$\begin{aligned} v_{as} &= \frac{1}{3}V_{DC} \cdot \left(m_{a1} - m_{a3} - \frac{1}{2}\left(m_{b1} - m_{b3} + m_{c1} - m_{c3}\right)\right) \\ v_{as(0++)} &= \frac{1}{3}V_{DC} \cdot \left(0 - 0 - \frac{1}{2}\left(1 - 0 + 1 - 0\right)\right) = -\frac{1}{3}V_{DC} \qquad (2.73) \\ v_{as(-00)} &= \frac{1}{3}V_{DC} \cdot \left(0 - 1 - \frac{1}{2}\left(0 - 0 + 0 - 0\right)\right) = -\frac{1}{3}V_{DC} \qquad (2.74) \end{aligned}$$

The current flow in the three-level inverter in these states are shown in figure 2.15 and 2.16.

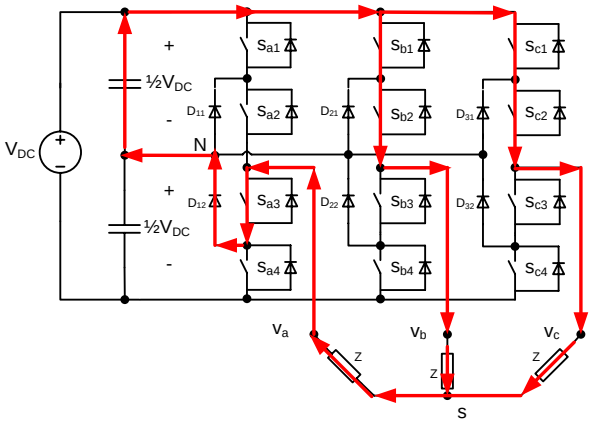


Figure 2.15: *Current flow for state* $(0,+,+)$*. Notice that the current is entering the neutral point, hence discharging the top capacitor.*

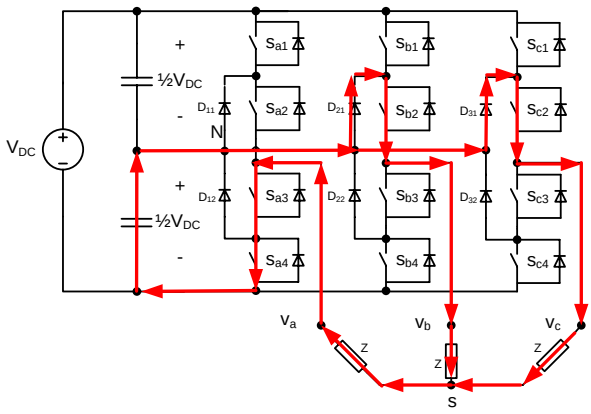


Figure 2.16: *Current flow for state* $(0,+,+)$*. Notice that the current is leaving the neutral point, hence discharging the bottom capacitor.*

The figures show, that the current flows into the neutral point in $(0,+,+)$, and out from the neutral point in $(-,0,0)$. So for the same output voltage, the control scheme of the inverter decides, which direction the current is flowing through the neutral point, and hence if the upper or lower capacitor is charging. So by choosing the NTS, control of the neutral point voltage balance is easy to implement by simply choosing which redundant switch state that is applied, based on voltage feedback from the capacitors.

The space vector modulation analyzed in this subsection has the overall same performance as the carrier based modulation, but also an easy implementation of neutral point balancing. However, according to [Bruckner, 2005], the approach described in this subsection has some issues when the double triangle is applied. The problem is, that the redundant switch states can be activated at the wrong times, hence compromising the NTS approach by not centering the redundant vectors. This is because the analyzed SVM approach is developed for the two-level inverter, where only one redundant (zero) vector exists, and then applied to the three-level inverter. To ensure that the vector sequence for the three-level inverter is optimal, three-level SVM can be used for better performance. However, this subject is not within the time-frame of this project.

2.4 Conclusion

In this section, the three-level inverter has been analyzed. The goal of the analysis was to gain knowledge about the three-level inverter, and also pinpoint the advantages and disadvantages of this topology. The base for comparison was the commonly used two-level inverter. Also two modulations strategies suited for implementation of the three-level inverter was analyzed. One key feature of the three-level inverter, that makes it well suited for the medium voltage levels is the fact, that the DC link voltage is always shared by two switches. This lowers the requirements for the semiconductors used for the inverter. As later chapters of this report will show, higher voltage ratings for a single device leads to higher switching losses, hence limiting the upper switching frequency.

A disadvantage is twice the amount of semiconductors and the unequal loss distribution of the switches. This could lead to issues regarding efficient cooling and lifetime of the inverter system. Also the neutral point balancing is a disadvantage for the three-level inverter.

A great advantage of the three-level inverter instead of the two-level inverter is the THD. It was calculated in section 2.2 that the THD of the three level inverter was 0.169 against 0.311 for the two-level inverter. A lower THD leads to higher efficiency. Due to the extra voltage level per phase, the output voltage of the three-level inverter can reach seven levels (phase to star point), which makes the output more quasi-sinusoidal compared to the two-level inverter. Table 2.2 sums up the advantages and disadvantages.

	Two-level inverter	**Three-level inverter**
Advantages	Simple, few switches, no NPC balancing	Low THD, seven voltage levels, lower voltage rating for switches,
Disadvantages	Double the THD of a three-level, high voltage rating for switches	Unequal loss distribution, neutral point balancing Twice the Switches + diodes for neutral NPC topology.

Table 2.2: *Comparison of two-level inverter and NPC three-level inverter.*

Finally the analysis of the modulation schemes for the three-level inverter showed, that the two standard modulation strategies; Carrier Based Modulation and Space Vector Modulation both could be implemented in a three-level inverter by using two triangular carriers in phase instead of one. Also neutral point balancing could easily be implemented in the Space Vector Modulation scheme. From these analysis, it is concluded that the three-level inverter is well suited for medium voltage applications, and even surpasses the two-level inverter in performance.

Chapter 3

Series connection of IGBTs

In this chapter advantages and disadvantages of series connections of IGBTs are analyzed with respect to unequal voltage sharing due to parameter deviations in IGBTs, switching and conduction losses. Finally reliability in series and parallel connected IGBTs are compared from a statistical point of view.

Inverter operation at medium voltages can be obtained by either using single high voltage switches or by series connecting two or more lower rated switches in series. IGBTs capable of blocking up to $6.5kV$ are available today, however they are not industry standard, as the $1.7kV$ devices used for the project.

IGBTs have characteristics, that in practice deviate from one device to another. This is typically due to small deviations in the silicon, from which the IGBT is produced. The deviations affect the switching times of the devices, and can be subject to changes over time depending on the history of the device, such as unequal temperature, improper environment or aging.

In many applications, small deviations do not matter, but when series connecting switches, small deviations become significant, because the deviations affect the switching times. The switches must turn on and off very closely together, otherwise the switches may not share the voltage equally in the on and off transitions, and eventually damaging one or more of the devices. Figure 3.1 (a) shows the switch voltages for two switches with unequal voltage sharing, because of delayed gate signals, with the fastest switch exceeding the maximum allowed voltage. Figure 3.1 (b) shows the situation, when the switch voltage does not exceed the maximum voltage $v_{ce,max}$, even though the switches are not turned on simultaneously.

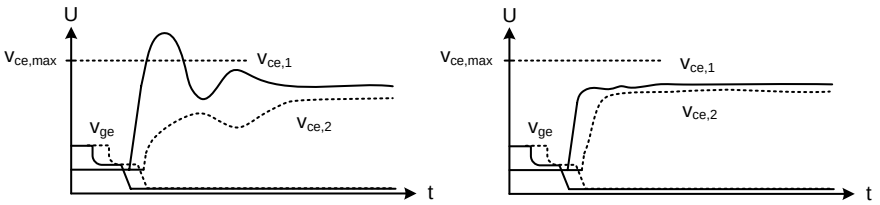


Figure 3.1: *Switch voltages for two switches with (a) unequal voltage sharing, and (b) equal voltage sharing.*

To avoid unequal voltage sharing and IGBT destruction, the switching must be very closely controlled, also when temperature and aging changes the switch characteristics compared to one another. This control is usually obtained by adding auxiliary circuits to the switches, called snubbers. This topic is discussed in more detail in chapter 4.

3.1 Parameter dependence

The unequal voltage sharing depends on the differences in device parameters as mentioned above. The parameter dependence of the turn on and off can be shown by simulations and used for comparison between the individual dependencies.

In this section simulations are performed using OrCad for a simple circuit containing two series connected IGBTs with additional deviation in selected parameters. The actual parameter values are chosen from the data sheet for a Mitsubishi CM400HA-34H IGBT and a Semikron SKHI 21A gate driver. The Mitsubishi IGBT device is chosen, because a Pspice model is available from the producer, and because it holds parameters similar to the used Semikron SKM600GA125D IGBT. The relative parameter deviations are chosen according to the Semikron data sheet.

Parameters for the SKHI 21A gate driver is used for the simulations, because the deviations in propagation delay is a known quantity, that are obtained from [Mads P. Vaerens, 2007].

The gate emitter and collector emitter capacitances C_{ge} and C_{ce} of the IGBT are derived in equations (3.1) to (3.3) based on the input, output and reverse transfer capacitances (Miller capacitance) from the data sheet. Generally these are dependent on the collector emitter voltage, but for this simulation they are assumed to be constant for simplicity.

$$C_{gc} = C_{res} = 15nF \tag{3.1}$$
$$C_{ge} = C_{ies} - C_{gc} = 85nF - 15nF = 70nF \tag{3.2}$$
$$C_{ce} = C_{oes} - C_{gc} = 20nF - 15nF = 5nF \tag{3.3}$$

The capacitances, gate resistances and the corresponding deviations are listed is table 3.1.

Parameter	Default value	Value with deviation	Deviation
Gate capacitance C_{ge}	$70.0nF$	$91nF$	30%
Collector emitter capacitance C_{ce}	$5nF$	$6.5nF$	30%
Gate resistor R_g	5Ω	5.25Ω	5%
Gate signal delay t_d	$0s$	$170ns$	

Table 3.1: *Chosen parameters for a Mitsubishi CM400HA-34H IGBT and Semikron gate driver - default and deviated values.*

3.1.1 Simulation results

Figures 3.2 to 3.5 show the four OrCad schematics used for the simulations. Figure 3.2 is added with 30% collector emitter capacitance, figure 3.3 with 30% gate emitter capacitance, figure 3.4 with 5% gate resistance and figure 3.5 with $170ns$ of difference between the gate signals. These are all the expected parameter deviations according to data sheets. The switching frequency is chosen to $f_s = 5kHz$ according to appendix A.4.

The corresponding simulation results are shown in figures 3.6 to 3.13. These show the collector emitter voltage v_{ce} for each series connection.

It's clear in any of the four figures, that deviations in parameter values affect the voltage sharing between the devices, but there is a large difference in the significance of the deviations.

Generally an addition of capacitance or resistance increases the time constant of the device and makes it turn off and on slower than the other device. Because of this, the slowest device is exposed to a higher collector emitter voltage at turn on, and opposite at turn off. Here the quickest device is exposed to a higher voltage. In both cases, the high voltage may damage the devices.

The least significant parameter is the collector emitter capacitance, which is also numerically the smallest according to table 3.1. Deviations in this parameter has almost no influence on the device dynamics as seen in figure 3.6 and 3.7.

Deviations in the gate emitter capacitance and the gate emitter resistance leads to almost the same behavior. The on transition becomes slightly longer with addition of gate capacitance leading to a small voltage spike across the slowest switch as seen in figure 3.8 to 3.11.

The most significant deviation is the delay between the gate signals leading to a large voltage difference between the switches as seen in figure 3.12 and 3.13. This fact must be taken into consideration in the choice and design of the voltage balancing topology, because not every topology may be able to handle an unbalance of this magnitude. Methods of voltage balancing is discussed in more detail in chapter 4.

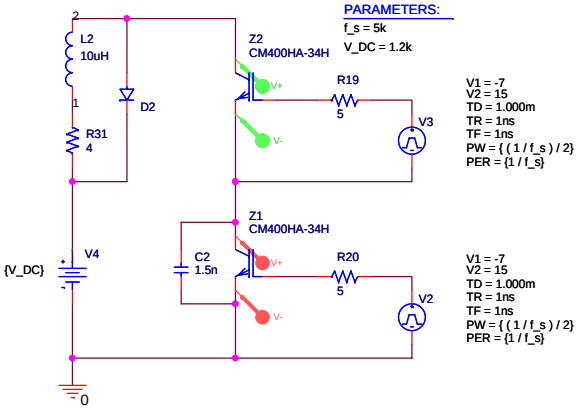


Figure 3.2: *Schematic with added collector emitter capacitance shown as $C_2 = 2.7nF$. Results are shown in figures 3.6 and 3.7.*

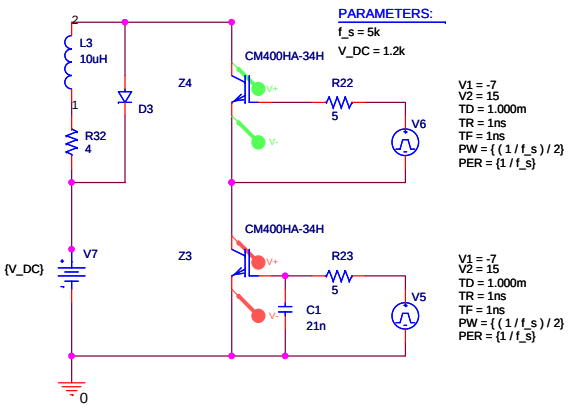


Figure 3.3: *Schematic with added gate emitter capacitance shown as $C_1 = 3.3nF$. Results are shown in figures 3.8 and 3.9.*

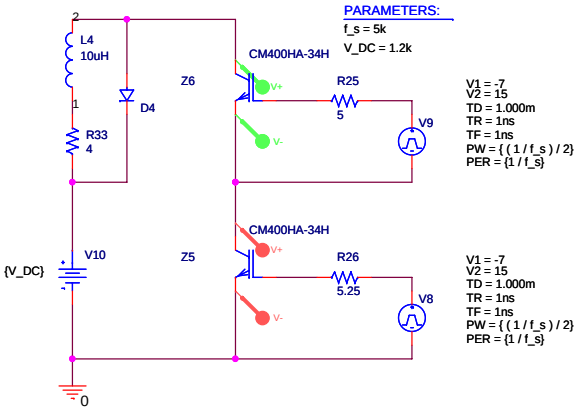


Figure 3.4: *Schematic with added gate resistance shown as $R_{26} = 5.25\Omega$. Results are shown in figures 3.10 and 3.11.*

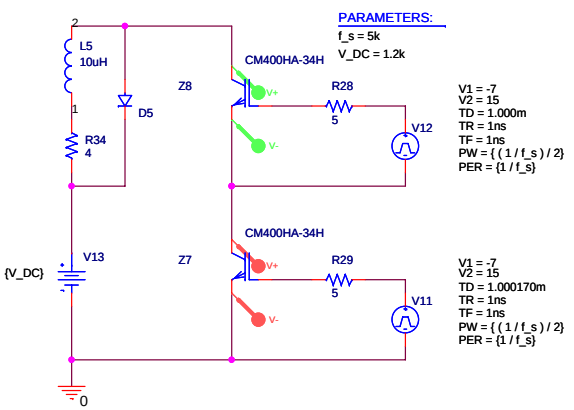


Figure 3.5: *Schematic with added gate signal delay $TD = 170ns$ in the gate signal source V_{11}. Results are shown in figures 3.12 and 3.13.*

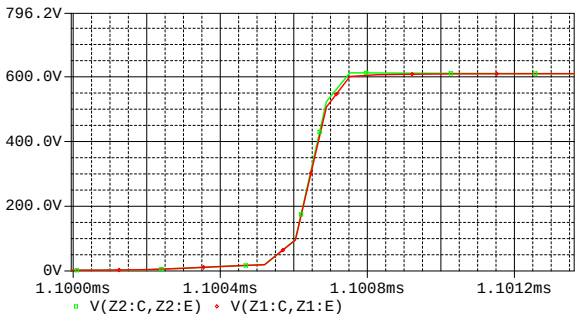


Figure 3.6: *Turn off transition with added collector emitter capacitance. See schematic in figure 3.2.*

Figure 3.7: *Turn on transition with added collector emitter capacitance. See schematic in figure 3.2.*

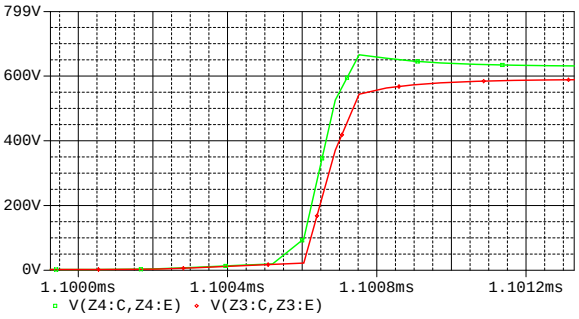


Figure 3.8: *Turn off transition with added gate emitter capacitance. See schematic in figure 3.3.*

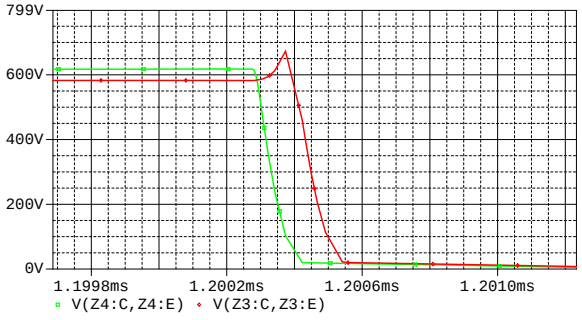


Figure 3.9: *Turn off transition with added gate emitter capacitance. See schematic in figure 3.3.*

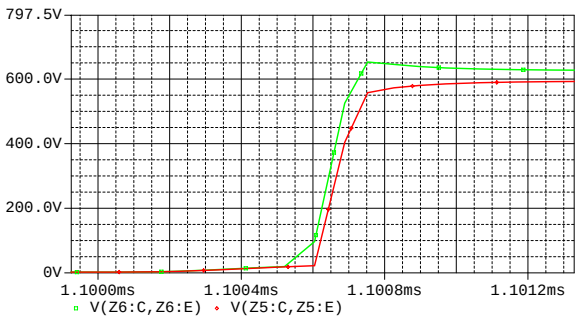


Figure 3.10: *Turn off transition with added gate resistance. See schematic in figure 3.4.*

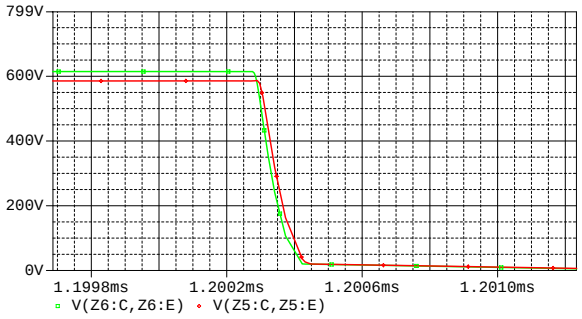


Figure 3.11: *Turn on transition with added gate resistance. See schematic in figure 3.4.*

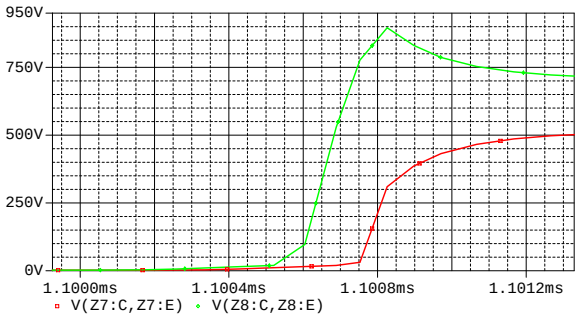


Figure 3.12: *Turn off transition with added gate signal delay. See schematic in figure 3.5.*

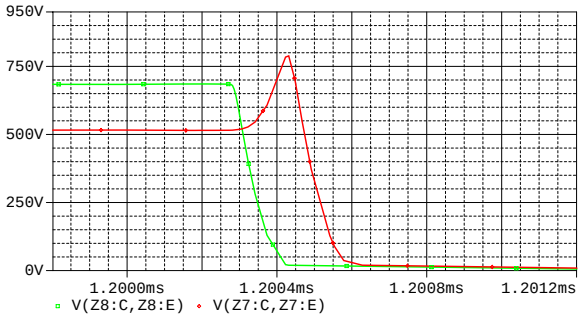


Figure 3.13: *Turn on transition with added gate signal delay. See schematic in figure 3.5.*

3.1.2 Conclusion

The simulations show, that the gate signal delay is the most significant contributor to voltage unbalance, and therefore it is convenient to use this delay as reference in the design of a given balancing circuitry. The worst case value is chosen according to the gate driver data sheet and to [Mads P. Vaerens, 2007].

It must be noticed, that combinations of parameter deviations are not examined here, and therefore no estimate on this is given, even though a combination may lead to even larger voltage differences.

The simulation results are also only valid for the specific IGBTs chosen for the project and can not be directly related to other types or manufacturers. If other devices are used, similar simulations must be performed for these devices.

3.2 Losses Comparison for Series Connections

The main objective to series connect a number of devices is to increase the off state voltage capabilities of the inverter. Series connecting a number of low voltage IGBTs devices can be shown to lower the total losses, compared to using only one high voltage device. The losses of the series connection are dependent of the switching frequency, and in fact there exist a given frequency, below which the losses become lower for the single device setup. This is because the switching losses become less significant compared to the conduction losses, which are independent of the switching frequency.

In this section, a comparison is performed by comparing losses for one $3.3kV$ IGBT with series strings of two $1.7kV$ and three $1.2kV$ IGBTs. The losses are calculated based on typical loss energy values from the data sheets for the device. The devices used are summarized below:

- Dynex DIM400BSS12 ($1.2kV/400A$)
- Dynex DIM400BSS17 ($1.7kV/400A$)
- Dynex DIM400NSM33 ($3.3kV/400A$)

The reason for not using data and comparing three different Semikron devices, is because Semikron do not produce $3.3kV$ IGBTs. To make a fair comparison, all three devices are chosen from Dynex, because Dynex produces devices for all three voltage levels and Dynex supplies sufficiently detailed data sheets. The Dynex $1.7kV$ and the Semikron $1.7kV$ devices have similar loss characteristics and current ratings.

The relevant parameters for the comparison obtained from the device data sheet are the switching energies E_{on}, E_{off}, E_{rec} and on state voltage drop $v_{ce,on}$ and current i_c, and these are summarized in table 3.2.

The losses for the three different cases are calculated using equations (3.4), (3.5) and (3.6). The losses are divided into turn on, turn off, reverse recovery and conduction losses.

$$P_{tot,3.3kV} = P_{rise} + P_{fall} + P_{rec} + P_{cond} \quad [W] \tag{3.4}$$

Parameter:	**1.2kV IGBT:**	**1.7kV IGBT:**	**3.3kV IGBT:**
T = 25°C			
On state voltage drop $v_{ce,on}$	$2.2V$	$2.7V$	$2.8V$
Collector current I_c	$400A$	$400A$	$400A$
Off state voltage $v_{ce,off}$	$600V$	$900V$	$1800V$
Turn off energy E_{off}	$45mJ$	$120mJ$	$520mJ$
Turn on energy E_{on}	$45mJ$	$150mJ$	$620mJ$
Reverse recovery energy E_{rec}	$17mJ$	$70mJ$	$150mJ$
T = 125°C			
On state voltage drop $V_{ce,on}$	$2.6V$	$3.4V$	$3.6V$
Collector current I_c	$400A$	$400A$	$400A$
Off state voltage $V_{ce,off}$	$600V$	$900V$	$1800V$
Turn off energy E_{off}	$60mJ$	$180mJ$	$600mJ$
Turn on energy E_{on}	$60mJ$	$170mJ$	$870mJ$
Reverse recovery energy E_{rec}	$32mJ$	$100mJ$	$300mJ$

Table 3.2: *Loss parameters for three differently rated IGBTs at $T = 25°C$ and $125°C$. All values are for $v_{ge} = \pm 15V$ and load inductance $L \approx 100nH$.*

$$P_{tot,1.7kV} = 2 \cdot (P_{rise} + P_{fall} + P_{rec} + P_{cond}) \quad [W] \tag{3.5}$$
$$P_{tot,1.2kV} = 3 \cdot (P_{rise} + P_{fall} + P_{rec} + P_{cond}) \quad [W] \tag{3.6}$$

where

$$P_{rise} = f_{sw} \cdot E_{on} \quad [W] \tag{3.7}$$
$$P_{fall} = f_{sw} \cdot E_{off} \quad [W] \tag{3.8}$$
$$P_{rec} = f_{sw} \cdot E_{rec} \quad [W] \tag{3.9}$$
$$P_{cond} = i_c \cdot v_{ce,on} \quad [W] \tag{3.10}$$

The figures 3.14 and 3.15 show the calculated losses as function of switching frequency for a junction temperature of $T = 25°C$ and $T = 125°C$, because the losses depend on the junction temperature as well.

The figures show a clear difference in losses for the single $3.3kV$ device and the two series strings of $1.7kV$ and $1.2kV$ devices. Two factors here are obvious. One is the general dependence on the switching frequency both for the single device and for the series strings, which is explained by equations (3.7) to (3.9), where f_s is a parameter. The second fact is the difference in losses between the single and the series strings, which is explained by the relationship between the turn on and turn off energy loss for the individual devices.

For the lower rated devices, the individual loss energy is relatively small compared to the higher rated devices In fact even the sum of the individual losses in the series string becomes smaller, than for the single high voltage device. This can also be seen from table 3.2.

As figure 3.15 shows, the losses for the series string is not lower for all switching frequencies. In this case, the single device becomes more efficient at frequencies below approximately $900Hz$, when the duty cycle is $D = 0.5$.

The figures also show, that the losses depend on the duty cycle. With an increase in duty cycle, the conduction losses increase more rapidly for the series string, because the total on state voltage drop is higher for the series string than for the single device, but the total losses still remain significantly lower for the series string.

For high voltage applications, it is clear, that the losses can be lowered by connecting more IGBTs, with more gate drivers and protection circuits, in series by applying a sufficient switching frequency, but a drawback here is the increased volume and mass of the inverter. For a wind turbine application, where space in the nacelle is limited, it may not be an option. But at same time lower losses require smaller cooling systems, which may compensate for the mass increase of IGBTs. This discussion is out of further focus in this report.

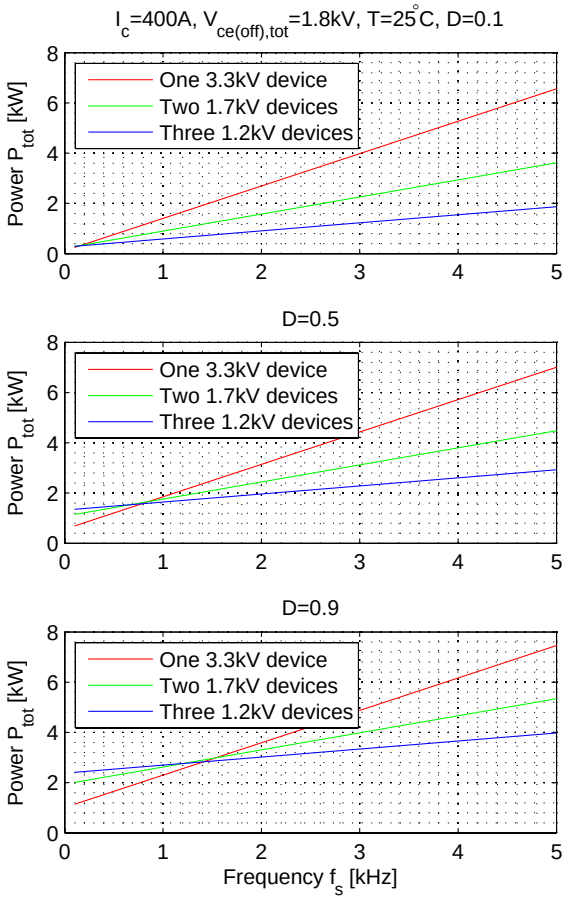


Figure 3.14: *Total losses at $T = 25°C$ with duty cycle $D = 0.1$, $D = 0.5$ and $D = 0.9$.*

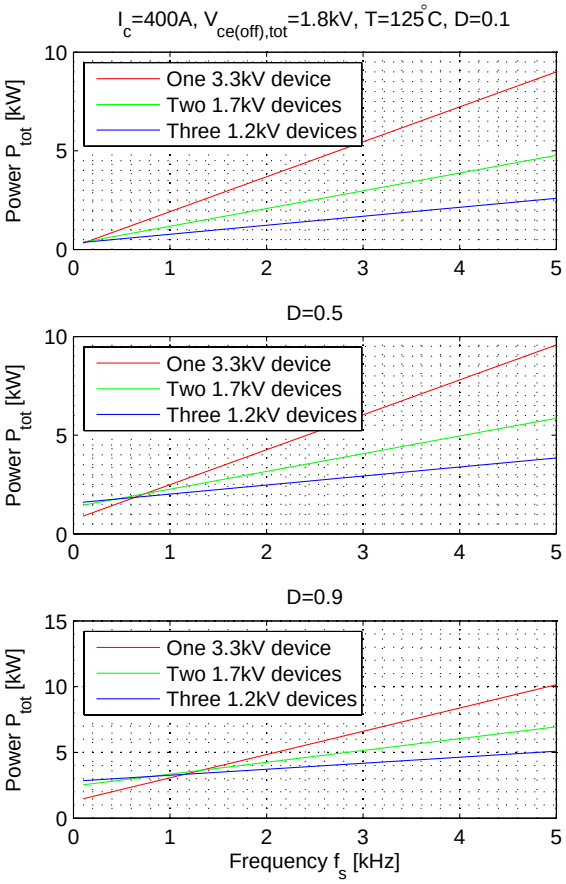


Figure 3.15: *Total losses at $T = 125°C$ with duty cycle $D = 0.1$, $D = 0.5$ and $D = 0.9$.*

3.3 Reliability in Series Connected IGBTs

In many applications, the overall reliability of operation is given high priority. In the case of an off shore wind turbine, reliability is crucial, both seen from a competition and maintainance point of view. Wind turbines with known low reliability will have a poor position on the market, and maintainance of off shore turbines is a costly affair, in case of vital and heavy parts braking down. In this section, the reliability of the power semiconductors is described and compared for parallel and series connected devices.

The motivation for series connecting devices is the advantage of operating at higher off state voltage and though higher DC link voltage. The increase in DC link voltage allows either to decrease the current for a given output power, or for a given current to increase the the output power. But adding a higher number of devices into a circuit may degrade the reliability, because the probability of one single device failing increases with the amount of devices - the more devices, the higher statistical risk of failure.

The probability of a fault vs. success for one device can be described by the random variable x. This can take values zero for failure or one for success, and the probability p of a single device not breaking down is given as

$$P\{x = 1\} = p \tag{3.11}$$

According to (3.11), for a inverter with n devices in total, the probability of no devices of the n not breaking down becomes

$$P\{(x_1 = 1), (x_2 = 1), (x_3 = 1), ..., (x_n = 1)\} = p^n \tag{3.12}$$

The variable p is always smaller than or equal to one, and therefore equation (3.12) shows, that the probability of success decreases with the number of devices. Therefore series connecting IGBTs may not be an optimal and more reliable choice from a statistical point of view.

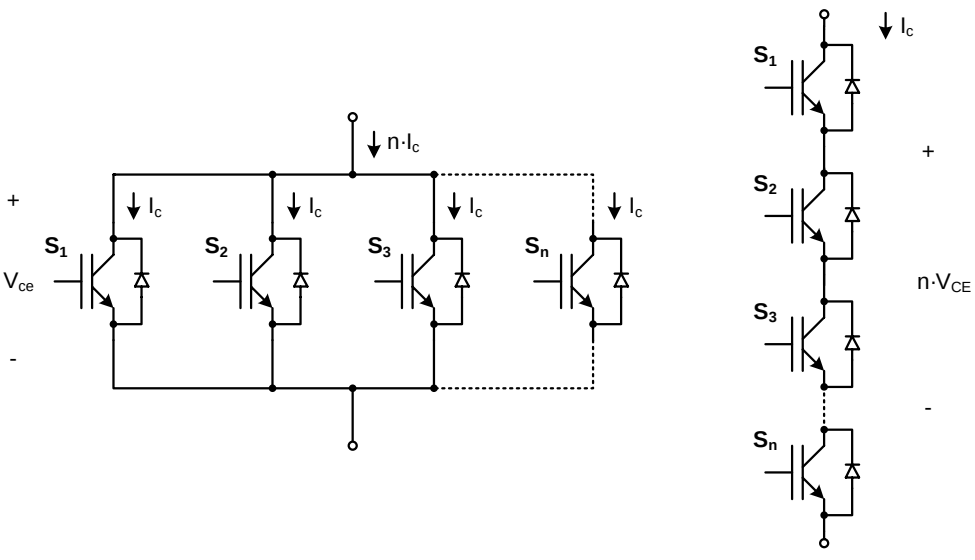


Figure 3.16: *IGBTs in parallel (left) and series connections (right).*

Another way to increase the output power capabilities of a inverter is to keep the DC link voltage low, and instead increase the total current. This can be realized by paralleling a number of switches of the same type in the inverter, as shown on figure 3.16. The amount of devices is equal in both configurations because

of the power $P = U \cdot I$, and hence the power density will be the same for a given topology. According to equation (3.11), the probability of device failure will be the same for both the series and the parallel connected setups. This means, that from a reliability point of view, the series connected devices can be considered an alternative to the parallel connection scheme, when focusing on the power devices only.

Though the reliability is shown to be the same for the series and parallel connection, the series connection has some advantages from a redundancy point of view. In the case, that one device in a series string breaks down and short circuits, the remaining devices can keep the inverter operating, as longs as the voltage ratings of the individual devices are not violated. If the same happens for a parallel connection, then the short circuited device will clamp all of the paralleled devices, and render the rest of the paralleled IGBTs useless.

The break down of an IGBT in the series string may not always create a short circuit internally as described, but instead break the internal wiring on the silicon or between two individual devices. In this case, the discussion about redundancy in a series string becomes irrelevant, because the entire string will be shut off.

On the other hand, if using paralleled IGBTs, then broken internal wirings in one IGBT does not prevent the inverter operation, as longs as the current ratings of the individual devices are not exceeded.

3.4 Conclusion

In this chapter, advantages and disadvantages of connecting two or more IGBTs in series are analyzed with respect to the unequal voltage sharing, that is a consequence of parameter deviations in IGBTs. The conclusion of this is, that for the Mitsubishi IGBT and Semikron gate driver chosen for the simulations, the parameter deviation, that affects the voltage unbalance most significantly, is a delay between two or more gate signals.

Also switching and conduction losses are analyzed for series strings containing one, two or three IGBTs. Here the conclusion is, that the conduction losses increase for the series string, because the total on state voltage drop becomes larger than for one single device. But lower rated IGBTs have smaller capacitances in the junction, and therefore the switching losses decrease significantly, and therefore the total losses becomes smaller compared to using fewer higher rated IGBTs in series.

A short analysis shows, that the statistical reliability of the IGBTs does not decrease, when connecting these in series in stead of parallel to obtain a given output power of the inverter. This is because the total amount of IGBTs stay the same for the series and the parallel connected setups for a given inverter topology.

Chapter 4

Voltage Balancing Methods

4.1 Voltage balancing methods

In this chapter, different methods to balance the voltage across series connected semiconductors are described, based on a state of the art analysis. The scientific literature proposes and describes numerous methods based in different techniques, each one with their own advantages, disadvantages and requirements. Selected methods are described in this chapter, and among these three methods are selected for further analysis.

The asymmetry in the collector emitter voltage v_{ce} can be divided into two groups, the static and the dynamic asymmetry as described below.

- **The static asymmetry** is mainly caused by the off state characteristics of the devices connected in series. The higher the leakage current $i_{c,off}$ of the transistor, the lower is the off state resistance $R_{ce,off}$ and the lower becomes the voltage across the transistor. If two devices in series do not share the same off state resistance, the voltages will differ.
- **The dynamic asymmetry** is caused by different factors, such as delays in the gate drivers and differences in the IGBT's switching times, as the simulations show on page 24.

The factors affecting the static and dynamic asymmetry are summarized in table 4.1.

Factor	**Static asymmetry**	**Dynamic asymmetry**
Leakage current $i_{c,off} = f(v_{ce}, v_{ge}, T_j)$	x	
Gate emitter threshold voltage $v_{ge,th}$		x
Switching times $t_{d,on}, t_{d,off}, t_{rise}, t_{fall}$		x
Output impedance of gate driver R_g		x
Total loop impedance		x
Driver circuit inductance carrying collector current		x
Gate driver signal propagation time t_d		x

Table 4.1: *Static and dynamic asymmetry factors [Semikron, -].*

Careful selection and matching of devices with low parameter difference and synchronizing the gate drive signals will minimize the problems associated with voltage sharing. But this alone may not be sufficient, because temperature and aging also affect the parameters, and this may corrupt a mating of initially identical devices. Three main methods exist to solve voltage unbalance [N.Y.A. Shammas & Chamud, February 2006], and these are the

- *Passive Snubber*
- *Active Gate Control*

- *Voltage Clamping*

Figure 4.1 shows the relation between the methods, and these are described in more detail in section 4.1.1.

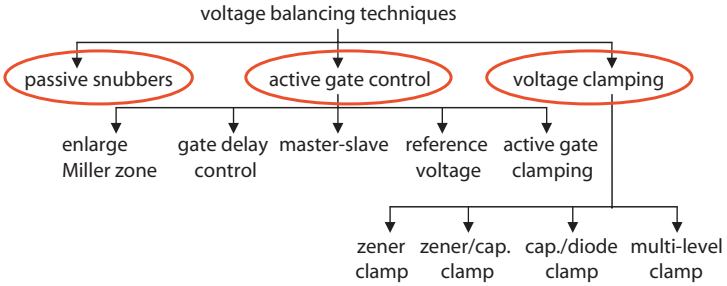


Figure 4.1: *Classification of different voltage balancing methods for series connected semiconductors [N.Y.A. Shammas & Chamud, February 2006].*

4.1.1 Passive Snubber Method

The passive snubber is one of the three main topologies shown in figure 4.1 and is one of the most commonly used methods in series connection of semiconductors because of its simplicity. It can be used both for series connected diodes and transistors, because it is not dependent on the gate emitter side of the device. The basic schematic of the snubber is shown in figure 4.2.

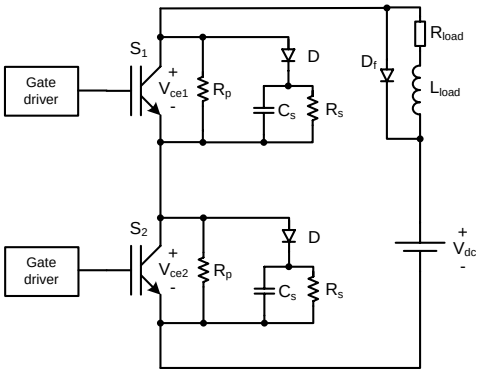


Figure 4.2: *Schematic of two series connected IGBTs with passive snubbers.*

The voltage divider made by the two R_p resistors is used for static balancing. The resistance of these is chosen to be dominant compared to the off state resistance. The RDC circuit is for the dynamic sharing in the turn off and on transitions. This network constitute a larger time constant compared to the IGBT's internal time constant. The IGBT's switching times t_{sw} therefore are small compared to the time constant of the network, making it insignificant as shown in equation (4.1).

$$\tau_{R_s C_s} >> t_{sw(S1,S2)} \tag{4.1}$$

In that way, the total time constant of the IGBTs connected in series is the same, only affected by the component tolerances of the snubber. Although the circuit is simple, it has some disadvantages. Increasing the capacitance C_s for higher time constant makes the voltage unbalance decrease, but the snubber's power losses and the on and off time increases, and therefore the device switching frequency has to be kept comparably low. Another disadvantage is, that the snubber is placed in the power side, and the energy stored in the capacitance C_s is dissipated into the resistance R_s in every turn on transition, because the RC network

is short circuited.

As shown in the simulations on page 24, a delay between gate signals affects the voltage sharing significantly. This expected gate delay must be taken into consideration in the choice of the RC network time constant. For a long delay, the RC time constant must be increased, and with this the losses also increase.

4.1.2 Active Gate Control Methods

The active gate control methods are commonly operating by affecting the gate emitter voltage, thus working on the small signal side of the devices. Therefore the methods are not suited for balancing diodes in a series connection, because these do not have gate emitter access. The literature proposes several active gate control methods as described shortly in the following.

- **The voltage balancing by enlarging the Miller effect zone.** This method balances the collector emitter voltages during the transient state. A positive gate pulse is injected by inserting a precharged capacitor to the fastest device to switch off, or the slowest device to switch on. The result is a small transient voltage unbalance, that may be acceptable for particular applications. The static balancing is done by connecting large resistors in parallel with each device [N.Y.A. Shammas & Chamud, February 2006].

- **The gate signal delay control method**. The gate signal of each device is adjusted to control the transient and steady state voltage unbalances. Controlled delays of gate signals can manipulate the voltage balance. The gate delay times are decided according to the level of voltage unbalance by monitoring the collector emitter voltage continuously in a closed loop. One gate signal is used as reference for the other gate signals. The method requires additional voltage feedback and processing power to generate the gate delays [N.Y.A. Shammas & Chamud, February 2006].

- **Master-slave approach method.** In this method one device behaves as master and the other ones are slaves. The slaves' collector-emitter voltage are controlled by referring to the master device collector emitter voltage. The control signal enables the current sources to charge the gate capacitance depending on the voltage unbalance of the slave devices. The power losses and the switching time does not increase significantly, but the control for more than two devices is complex [N.Y.A. Shammas & Chamud, February 2006].

- **The reference voltage method.** is based on controlling all the series connected devices with a common reference. The collector emitter voltage reference (v_{ce} voltage slope) is chosen by the designer and does not depend on the device. High speed controls are needed in series connected devices in order to follow the reference voltage. The power losses depends on the rate of rise of the reference voltage. Static balancing is reached with parallel voltage sharing networks [N.Y.A. Shammas & Chamud, February 2006].

- **The voltage clamping by active gate control.** This is an active voltage clamping with closed loop feedback by passive components. The collector emitter voltage is controlled. If it becomes larger than the reference voltage across C_{11} or C_{21}, a positive gate charge is injected into the gate. The proposed schematic is shown in figure 4.3.

  One of the main advantages of this method is the lack of complexity of gate side circuits. R_1 and R_2 are the components in charge of the static voltage sharing, while C_a, C_b, D and R_g are the components that ensure the transient voltage balancing [N.Y.A. Shammas & Chamud, February 2006].

- **The gate voltage reference clamping.** Here v_{ce} is converted to a gate signal reference and the control circuit clamps the collector emitter voltage at the desired level. The active gate control circuit consists of many functional units and therefore the gate drive circuit is complex and less reliable [N.Y.A. Shammas & Chamud, February 2006].

- **The gate balancing core method.** This method is shown in figure 4.4. here all the gate signal wires of the series connected IGBTs are coupled magnetically with iron cores. Each gate driver circuit is coupled

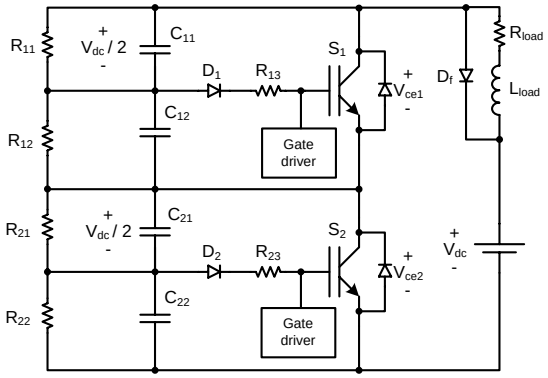


Figure 4.3: *Active gate control by closed loop feedback with passive components [N.Y.A. Shammas & Chamud, February 2006].*

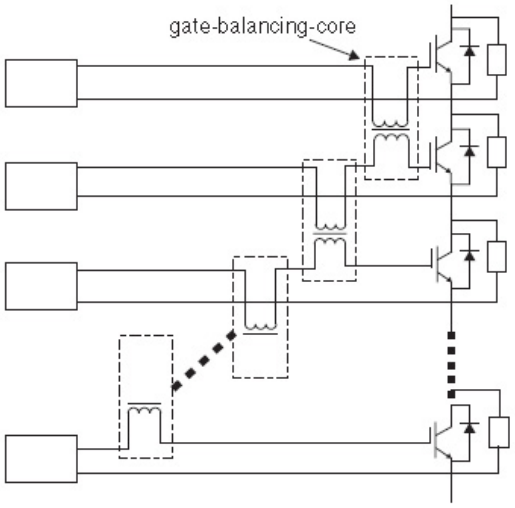


Figure 4.4: *Gate balancing core method [N.Y.A. Shammas & Chamud, February 2006].*

with a gate balancing core, that induces gate currents whenever the switching signal is delayed. The circuit becomes relatively complex for more than two switches in series. The static balancing is achieved with a parallel resistive voltage balancing network [N.Y.A. Shammas & Chamud, February 2006].

These methods described all belong to the active gate control methods. The methods are commonly characterized by affecting the gate emitter voltage to obtain one out of two different transient v_{ce} behaviors.

- The **Gate Signal Delay method** and **Master-slave approach method** is balancing the switches by matching the individual collector emitter voltages very precisely, both in steady state and transients.
- The remaining methods are protecting the switches being exposed to higher voltages, by defining a given maximum voltage limit, that may not be exceeded. This means, that in the transients, they are actually not balancing the voltages, rather working as over voltage protection.

The static balancing is in each case obtained by a resistive voltage divider.

4.1.3 Voltage Clamping Methods

The voltage clamping methods described here are basically operating by fixing the maximum collector emitter voltage to a defined level. Some of the methods are not balancing the switch voltage equally as some of the the active gate control methods do, but more acting as a clamping circuit to avoid over voltages across collector and emitter. There are four main topologies as described here.

- **Zener diode clamping.** The collector emitter voltage is limited to the maximum acceptable voltage defined by a zener diodes Z_1 and Z_2 connected between collector and gate. Whenever the collector emitter voltage reaches the zener breakdown voltage, the zener diode conducts. This makes the gate emitter voltage increase, and the device is turned on slightly for a short while, until the other device turns off also. The static balancing is obtained by parallel resistors R_p. Basically this method is not trying to balance the switch voltages in the transient states, like the active gate control method in figure 4.3, but more acting as a over voltage protection [N.Y.A. Shammas & Chamud, February 2006].

  The break down voltage level of the zener diodes must be chosen larger than the DC link voltage divided by the amount of switches in series. Otherwise the devices will be clamped on permanently in the off state.

This method is the most simple and easy to implement, because it does not require complex circuitry. The schematic is shown in figure 4.5.

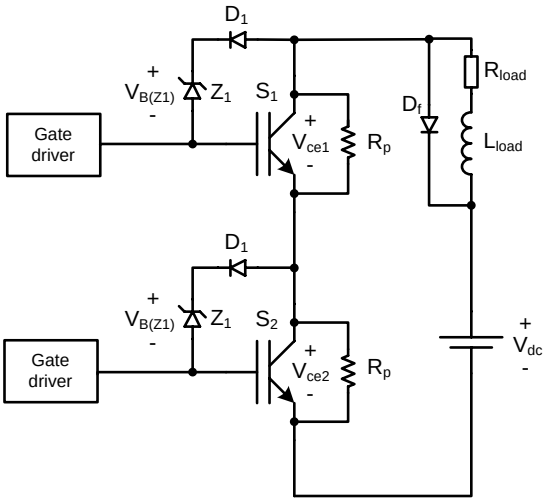


Figure 4.5: *Voltage clamping by a zener diode between collector and gate.*

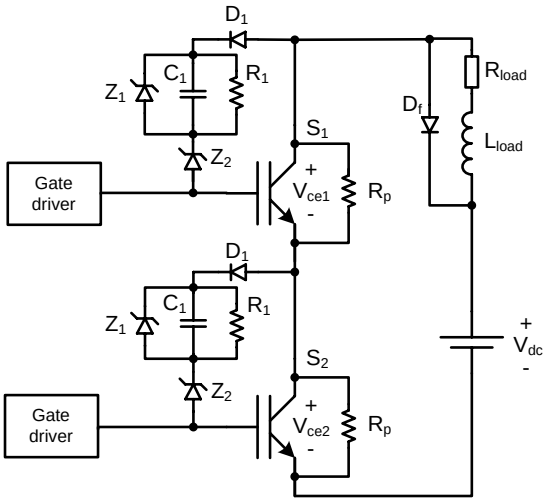


Figure 4.6: *Voltage clamping by two zener diodes and an RC network [N.Y.A. Shammas & Chamud, February 2006].*

- **Voltage clamping by two zener diodes and an RC network.** This method is an extension of the *Zener diode clamping* and clamps in two steps. When the collector emitter voltage increases above the breakdown of Z_2 in the turn off transition, Z_2 clamps and the charging of C_1 slows down the quickest transistor. The operation of Z_1 will ensure, that the IGBT voltage is clamped at the desired level, working as over voltage protection. The schematic is shown in figure 4.6 [N.Y.A. Shammas & Chamud, February 2006].

  The RC network of R_1 and C_1 operates by the same principals as the passive snubber on page 31 by slowing down the quickest transistor, but for this one, the power losses and the switching time is improved, because the RC network works on the small signal side.

- **Voltage clamping by capacitors and diodes.** This circuit is shown in figure 4.7 and basically behaves as a passive snubber. C_1 / D_1 and C_2 / D_2 work as a clamping circuit. The excess energy stored in the clamping capacitors is transferred to an external load by a circuit similar to a flyback converter. In that way, there is only one place to transfer the excess energy. The load can also be the DC link of the inverter. The complexity of the circuit is considerable. As in many other methods, the static voltage balancing is achieved by parallel voltage balancing network R_1 and R_2 [N.Y.A. Shammas & Chamud, February 2006].

- **Multi-level voltage clamping.** This balancing method uses three levels of feedback for the clamping, as shown in figure 4.8. The signals from each feedback block is used to affect the actual gate signal.

  The three levels are the $\frac{dv}{dt}$ clamp circuit (DVC) to control the voltage slope, the peak voltage clamp circuit (PC) to protect against over voltages and finally the tail current period clamp circuit (TCC). Because of the three different clamping levels, the method requires external devices for the current and voltage measurement, and this adds considerably to the complexity compared to the other methods described here [N.Y.A. Shammas & Chamud, February 2006].

These methods described, all belong to the voltage clamping methods. These are commonly characterized by clamping the collector emitter voltage to a given maximum limit by injecting current into the gate, when

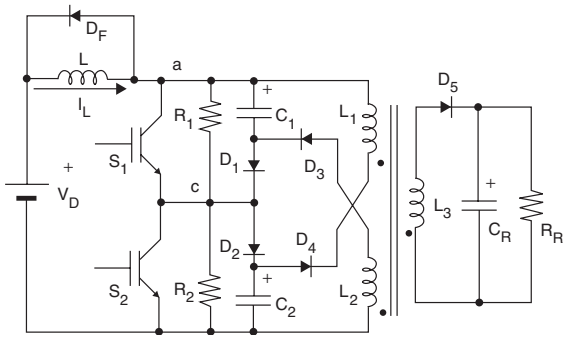


Figure 4.7: *Voltage clamping by diodes and capacitors [N.Y.A. Shammas & Chamud, February 2006].*

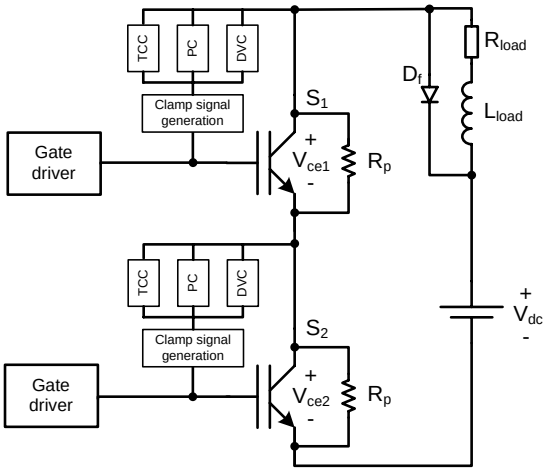


Figure 4.8: *Multi level voltage clamping [N.Y.A. Shammas & Chamud, February 2006].*

the voltage limit is reached.

The clamping methods are acting more as over voltage protection than voltage balancing like the gate signal delay method described on page 32. In the transients, the individual collector emitter voltages are allowed to deviate from each other, but one switch will not be exposed to higher voltages than the clamping voltage.

The static balancing is in each case obtained by a resistive voltage divider.

4.2 Analysis of chosen methods

In this section deeper analysis of the *passive snubber*, the *active gate control* and the *zener clamped snubber* is performed. These three methods are chosen for analysis mainly because of their simplicity. They work in an intuitive way and do not require complex circuitry or any external devices, such as DSP's or current and voltage measurement devices. The main difference between the passive snubber and the active gate control / zener clamped snubber is, that the passive snubber is operated on the power side of the device, and the two others operate at the small signal gate side. Beside of this, zener clamped snubber is not balancing the switches perfectly, but protecting against over voltages. Each method shows its advantages and disadvantages, and these are explained in this section.

The *gate signal delay* method is an interesting method also, but the time requirements for this one are considered non realistic for this project.

4.2.1 Passive snubber

The passive snubber is known to be one of the most simple voltage balancing topologies. It is independent of any extra control circuit, because the voltage balancing is obtained by passive components. The passive snubber is shown in figure 4.9. The main disadvantage is, that the components are placed on the power side of the IGBT, and therefore the components have to be able to handle high voltages. Also energy stored in the capacitor is dissipated in the series resistor and the IGBT for every turn on transient.

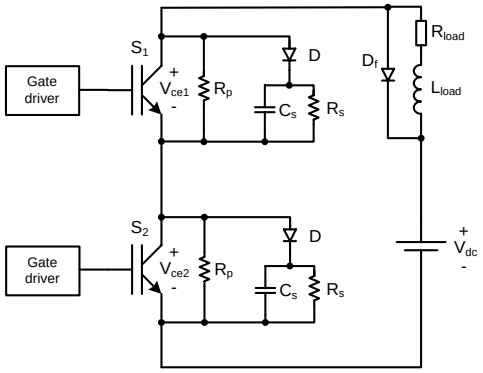


Figure 4.9: *Schematic of two passive snubbers.*

4.2.1.1 Design of passive snubber

The balancing is divided into static and dynamic balancing. The static voltage unbalance can be minimized by connecting a resistor R_p in parallel with each device in the string. The resistance must be chosen much lower, than the device off state resistance. According to the IGBT producer [Semikron, -], the current in the parallel resistors is required to be three to five times higher than the IGBT leakage current, following the inequality (4.2). In this way, the parallel resistors will be dominant, and the leakage current may be neglected.

$$\frac{v_{ce,off}}{5 \cdot i_{c,off}} \quad < \quad R_p \quad < \quad \frac{v_{ce,off}}{3 \cdot i_{c,off}} \quad [\Omega] \tag{4.2}$$

where $v_{ce,off}$ is the off state voltage and $i_{c,off}$ is the leakage current.

The transient voltage balancing is obtained by an RCD snubber network consisting of R_s, C_s and D. The capacitor C_s charges in the turn off transient, and discharges when the IGBT is turned on. The diode D forms a low impedance path during charging. The resistor R_s acts as current limiter, when the IGBT turns

on, and short circuits the capacitor. Because of this, the energy stored in the capacitor is mainly dissipated into the resistor instead of the IGBT. The capacitor is used to prevent a steep change of the voltage v_{ce}. It will cause v_{ce} to rise relatively slow, because the capacitance is chosen much larger than the internal collector emitter capacitance C_{ce} of the device - see figure 4.10. This makes the voltage difference Δv_{ce} between the two switches decrease in the transient states, even when having differences in device parameter. At the same time, a good choice of the capacitor is important to avoid affecting the switching time too much, because this will add to the switching losses, and may also conflict with the dead timing between complementary switches.

The simplified switching waveforms of the voltage across the capacitor v_{Cs} and the current through the load i_{load}, the transistor i_c and the capacitor i_{Cs}, when the IGBT is turning off, are shown in figure 4.11. Notice, that the load current i_{load} is assumed to flow continuously through the capacitor, when the switch turns off and the collector current decreases. This is because the load is assumed to be inductive, and the collector tail current is ignored. These simplifications allows approximations for simple design rules.

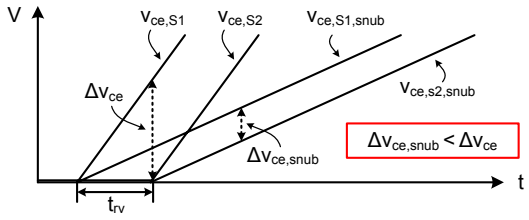


Figure 4.10: *Voltage waveforms in turn off transient with and without snubber.*

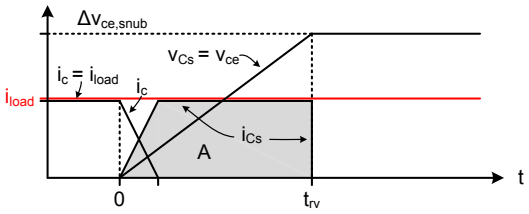


Figure 4.11: *Voltage and current waveforms for IGBT and snubber in figure 4.9.*

Figure 4.12 shows the current path, when transistor S_2 turn off earlier than S_1.

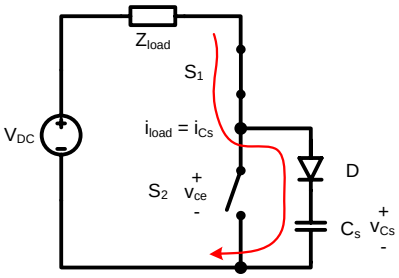


Figure 4.12: *Current path when lower switch is off.*

For the RCD network design many design rules are developed. In this case the design rulers are inspired by [Jiann-Fuh Chen & Ai, 1996], added by some corrections and additional deeper explanations.

The voltage across the capacitor at any time t can be calculated as function of the capacitor current i_{Cs}:

$$v_{Cs} = \frac{1}{C_s}\int_0^t i_{Cs}\ dt \quad \Rightarrow \quad v_{Cs} = \frac{1}{C_s}\int_0^t \frac{I_{load}}{t_{rv}} \cdot t\ dt \tag{4.3}$$

where $\frac{I_{load}}{t_{rv}} \cdot t$ is the average current during t. i_{load} is the instantaneous load current, t_{rv} is the fall time of the capacitor voltage, and I_{load} is the maximum load current. The capacitor reaches a designed voltage value Δv_{ce} as in equation (4.4), which is a fraction of the voltage source, at time $t = t_{rv}$. This voltage is chosen to be the maximum acceptable difference $\Delta v_{ce,snub}$ as shown in figure 4.10. In the case of series connected IGBTs, t_{rv} can be dimensioned from a known worst case gate driver delay t_d and the current fall time t_{fi}. In the case of series connected diodes it is chosen from the worst case difference in voltage rise and fall times.

$$I_C = \frac{q}{t}, \quad V_C = \frac{q}{C} \quad \Rightarrow \quad \Delta v_{ce} = \frac{I_C \cdot t_{rv}}{C_s} \quad [V] \tag{4.4}$$

where $I_C \cdot t_{rv}$ $[C]$ is the approximate area A shown on figure 4.11, which is the electrical charge entering the capacitor. To ensure, that the voltage across the capacitor does not exceed the designed value Δv_{ce}, equation (4.5) must to be fulfilled. It is here assumed, that the switch is off and high impedant.

$$C_s > \frac{I_L \cdot t_{rv}}{\Delta v_{ce}} \quad [F] \tag{4.5}$$

In a serial resonant RLC circuit the damping ratio is defined by ξ as:

$$\xi = \frac{R_{load}}{2} \cdot \sqrt{\frac{C_s}{L_{load}}} \quad [-] \tag{4.6}$$

In this case the damping ratio is chosen to be smaller than unity, to avoid slow switching times, but not too small to counter large voltage peaks. With $\xi < 1$, some degree of overshoot is allowed, and the circuit appears as second order. Equation (4.6) is reorganized to

$$\xi = \frac{R_{load}}{2}\sqrt{\frac{C_s}{L_{load}}} < 1 \quad \Rightarrow \quad C_s < \frac{4 \cdot L_{load}}{R_{load}^2} \quad [F] \tag{4.7}$$

With the conditions in equations (4.5) and (4.7), the value of the capacitor must fulfill the following specifications.

$$\frac{I_L \cdot t_{rv}}{\Delta v_{ce}} \quad < \quad C_s \quad < \quad \frac{4 \cdot L_{load}}{R_{load}^2} \quad [F] \tag{4.8}$$

The resistor R_s in series must be chosen so, that the capacitor discharges completely within the minimum on time $T_{on,min}$ (minimum possible duty cycle D_{min}). Complete discharge occurs within five times the time constant τ_{RC}. The complete discharge is very important for reliable operation, because any voltage across the capacitor in the following turn off transient will add to the voltage difference and over time corrupt the balancing. The actual minimum on time depends among other things on the switching frequency and duty cycle.

$$T_{on,min} \quad > \quad 5 \cdot R_s \cdot C_s \quad \Rightarrow \quad R_s \quad < \quad \frac{T_{on,min}}{5 \cdot C_s} \quad [\Omega] \tag{4.9}$$

These preceding steps are followed in the design of the passive snubber.

4.2.2 Simulation of passive snubbers

Here the passive snubber is designed and simulated to verify proper operation. The simulation is performed in two different stages. One simulation for a circuit with two IGBTs in series, and secondly for a pair of free wheeling diodes in series as the NPC three level inverter.

The two setups are shown in figure 4.13 and 4.22, and they are simulated using *OrCad*. In the case for two diodes in series, the parameter difference is obtained by adding $C = 1.5nF$ to the lower diode between anode and cathode according to table 3.1 on page 22. In the IGBT case, the gate signal of the lower switch is delayed by $t_d = 170ns$. The reason for using a delay in gate signals in stead of addition of gate resistance or capacitance is due to the conclusion of section 3.1.1, that states, that a delay in gate signals is the most significant contributor to voltage unbalance, when operating within the given tolerances.

The passive snubbers for both setups are designed following the steps in equations (4.2) to (4.9). The IGBT and diode model used for simulations is a Mitsubishi CM400HA-34H IGBT.

4.2.2.1 Simulation of passive snubber for IGBTs

The numeric data required for the snubber design for the IGBTs in series are:

- Data specifically from the IGBT data sheet:
  - Leakage current $i_{c,off}$ @ $(v_{ce,off} = 1.7kV, T_j = 125°C) = 4mA$.
  - Current fall time $t_{fi} = 160ns \quad \Leftrightarrow \quad t_{rv} = t_d + t_{fi} = 170ns + 160ns = 330ns$.
- Data chosen for the circuit design:
  - $V_{DC} = 1.2kV$
  - $R_{load} = 4\Omega$
  - $L_{load} = 10mH$
  - Modulation frequency $f_{mod} = 50Hz$
  - $i_{load,max} = \frac{v_{load,max}}{|Z_{load}|} = \frac{V_{DC}}{|4+j\cdot 2\pi\cdot 50Hz\cdot 10mH|} = 236A$
  - $T_{on,min}$ is chosen from the switching frequency and the smallest possible duty cycle. In this case, these are chosen to $f_{sw} = 5kHz$ and $D = 1\% \Rightarrow T_{on,min} = 2\mu s$.
- Design value for the maximum acceptable voltage difference Δv_{ce}.
  - $\Delta v_{ce} = 200V$

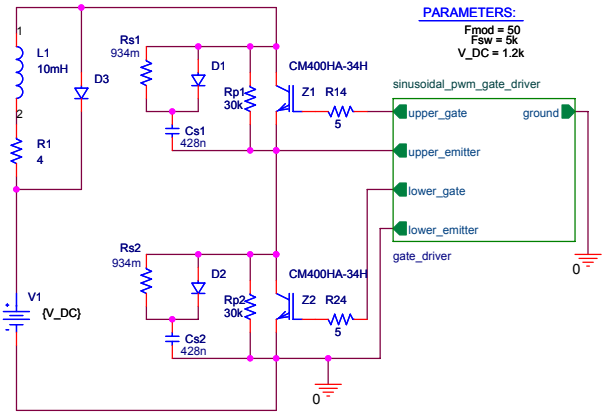


Figure 4.13: *Simulation schematic for passive snubber.*

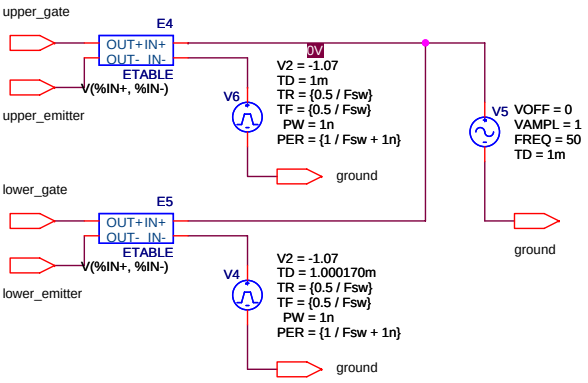


Figure 4.14: *Simulation schematic for sinusoidal PWM circuit with $t_d = 170ns$ and $f_{mod} = 50Hz$.*

For the static voltage balancing, the current through the parallel resistor R_p must be three to five times higher than the IGBT leakage current. From this, the resistance becomes:

$$R_{p,min} = \frac{v_{ce,off}}{5 \cdot i_{c,off}} = \frac{600V}{5 \cdot 4mA} = 30k\Omega \tag{4.10}$$

$$R_{p,max)} = \frac{v_{ce,off}}{3 \cdot i_{c,off}} = \frac{600V}{3 \cdot 4mA} = 50k\Omega \tag{4.11}$$

The numeric values for the components of the RCD network are obtained following equation (4.8) .

$$C_{s,min} = \frac{I_{load} \cdot t_{rv}}{\Delta v_{ce}} = \frac{236A \cdot 360ns}{200V} = 428nF \tag{4.12}$$

$$C_{s,max} = \frac{4 \cdot L_{load}}{R_{load}^2} = \frac{4 \cdot 10mH}{4^2} = 2.5mF \tag{4.13}$$

From this, the capacitance has to fulfill the following requirements:

$$428nF < C_s < 2.5mF \tag{4.14}$$

The series resistance R_s is calculated according to equation (4.9) as:

$$R_s \quad < \quad \frac{T_{on,min}}{5 \cdot C_{s,min}} = \frac{2\mu s}{5 \cdot 428nF} \quad = \quad 934m\Omega \tag{4.15}$$

These component values are added to the simulation circuits. For summary, the chosen values are $C_s = 428nF$, $R_p = 30k\Omega$ and $R_s = 934m\Omega$.

The simulation results are shown in figures 4.15, 4.16 and 4.17. Important aspects to notice is, that the capacitor and IGBT collector currents and capacitor voltages waveforms in figure 4.16 follow the ones used as background for the design guide in figure 4.11. Also the voltage $\Delta v_{ce,snub}$ does not exceed the designed value of $\Delta v_{ce} = 200V$, which means acceptable performance of the snubber.

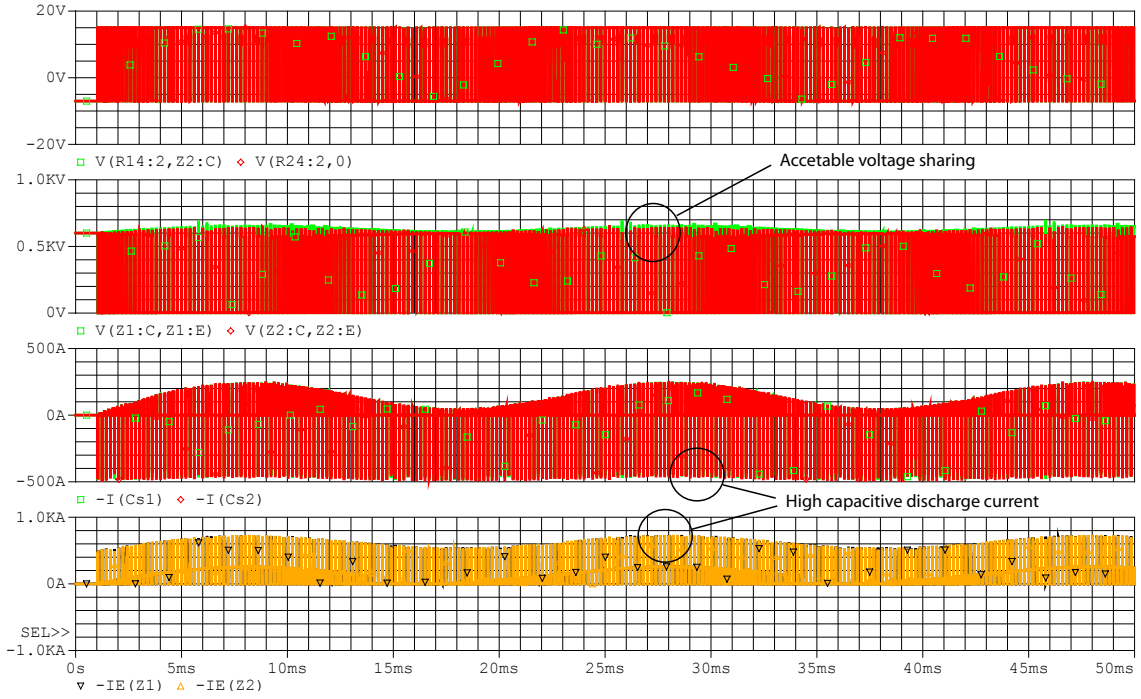


Figure 4.15: *Simulation of passive snubber for series connected IGBTs. (1) v_{ge1} and v_{ge2}, (2) $v_{ce,Z1}$ and $v_{ce,Z2}$, (3) i_{Cs1} and i_{Cs2} and (4) $i_{c,Z1}$ and $i_{c,Z2}$.*

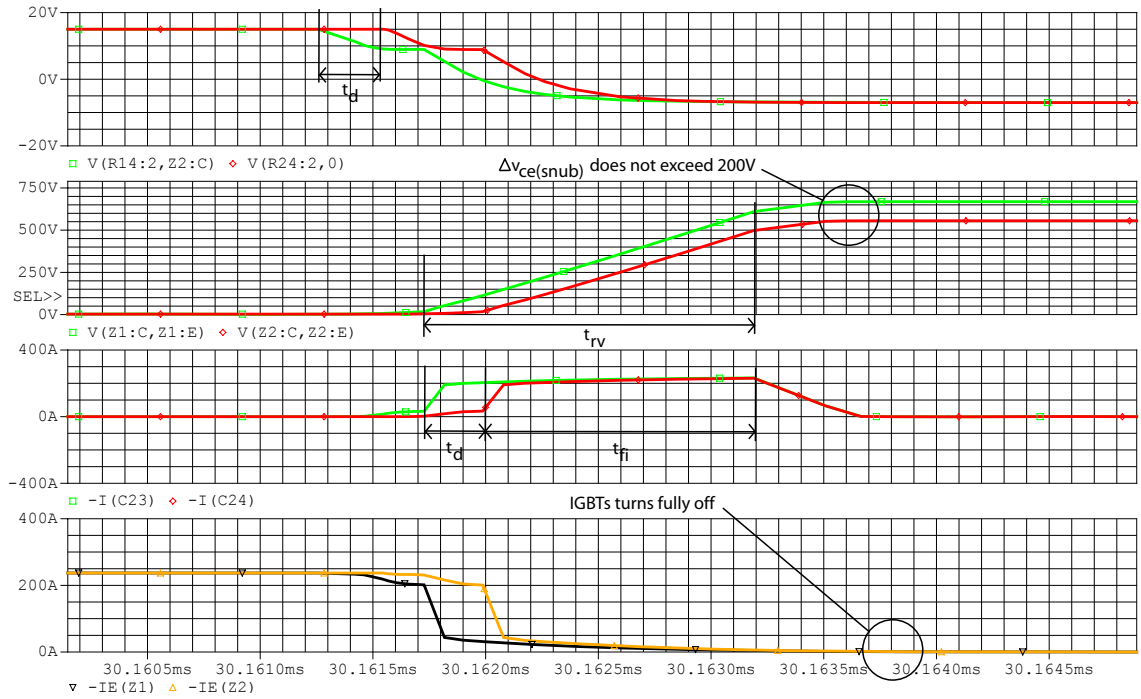


Figure 4.16: *Simulation of off transition of passive snubber for series connected IGBTs. (1) v_{ge1} and v_{ge2}, (2) $v_{ce,Z1}$ and $v_{ce,Z2}$, (3) i_{Cs1} and i_{Cs2} and (4) $i_{c,Z1}$ and $i_{c,Z2}$.*

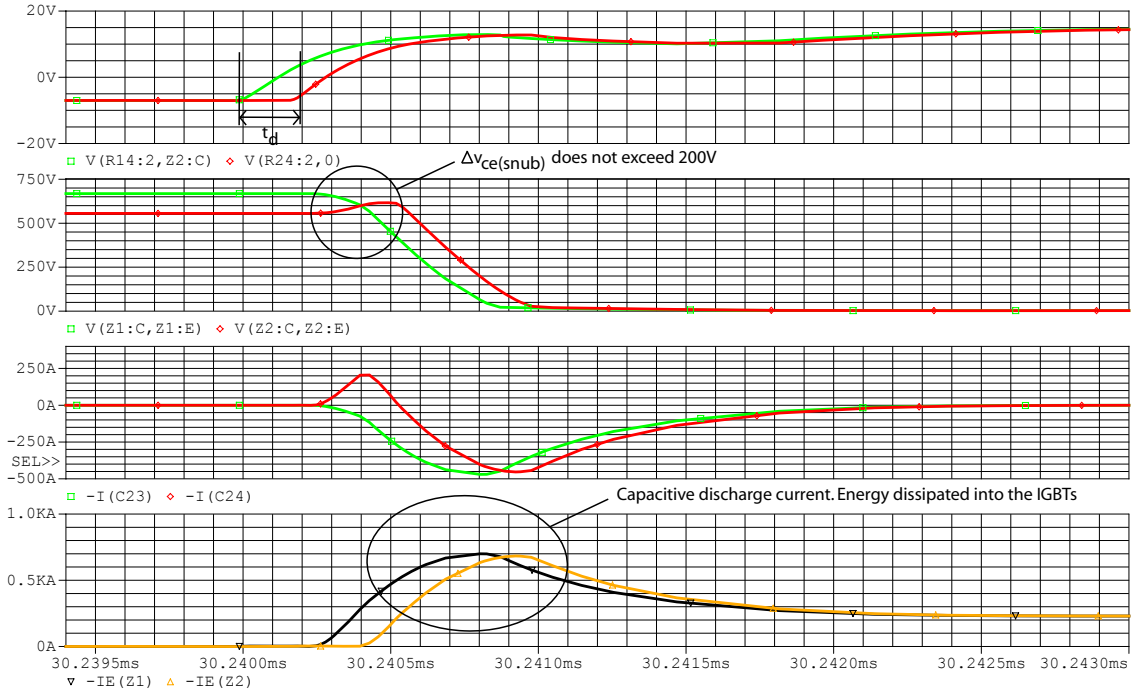


Figure 4.17: *Simulation of on transition of passive snubber for series connected IGBTs. (1) v_{ge1} and v_{ge2}, (2) $v_{ce,Z1}$ and $v_{ce,Z2}$, (3) i_{Cs1} and i_{Cs2} and (4) $i_{c,Z1}$ and $i_{c,Z2}$.*

4.2.2.2 Simulation of passive snubber for diodes

Here the passive snubber is simulated for a series string of two diodes in stead of IGBTs. This is of interest, because the diodes are required for the neutral point clamping in the three level inverter topology.

The simulation schematic is shown in figure 4.18 and 4.19. Here the free wheeling diode is replaced by two diodes D_3 and D_4 in series. The Pspice model used is the *Dbreak* diode. In the model, the anode cathode capacitance C_{jo} is chosen equal to the collector emitter capacitance C_{ce} for the Semikron IGBT used in the project. This is done because the IGBTs reverse diode is used in stead of a regular diode rated for the same voltage and current as the IGBTs.

$$C_{jo} = C_{ce} = 5nF \tag{4.16}$$

The lower diode D_4 in the schematic is added with $1.5nF$ of capacitance C_p according to the deviated values in table 3.1 on page 22.

The static voltage balancing resistances R_p are calculated according to equation (4.2) on page 36 and summarized here:

$$R_{p,max} = \frac{v_{ce,off}}{5 \cdot i_{c,off}} = \frac{600V}{5 \cdot 600\mu A} = 200k\Omega \tag{4.17}$$

$$\tag{4.18}$$

The numeric values for the components of the RCD network are obtained by following equation (4.8). The acceptable voltage difference Δv_D is chosen to $\Delta v_D = 200V$ as for the simulation of the IGBTs in series, though this can be chosen freely within the off state voltage limitations of the diodes.

The required capacitor voltage rise time t_{rv} can be determined from the difference in the time constants for the diodes internal parameters; the junction capacitance C_{jo} and the forward series resistance R_F as in equation (4.19). The numeric values are in the ranges $C_{jo} = [5; 6.5nF]$ and $R_F = [1.3; 1.5m\Omega]$ according to

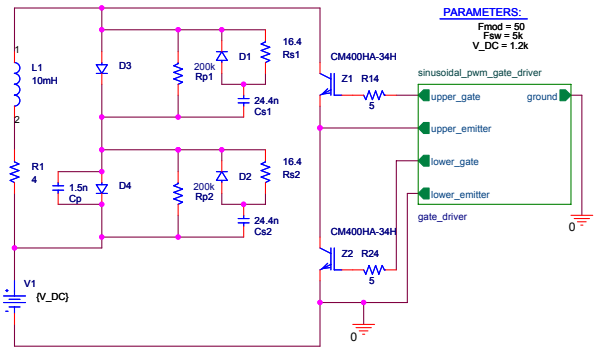


Figure 4.18: *Simulation schematic for the passive snubber for diodes - here used for two free wheeling diodes.*

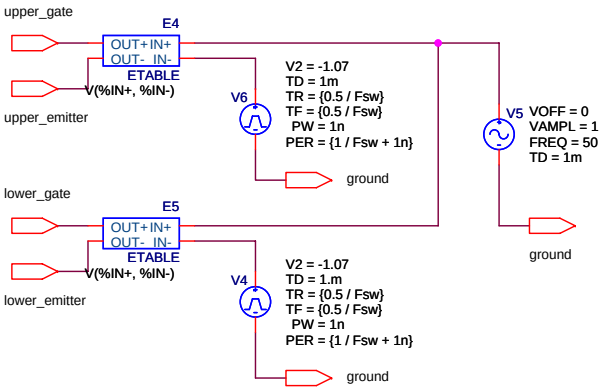


Figure 4.19: *Simulation schematic for sinusoidal PWM circuit.*

the data sheet for the Semikron IGBT. From these values, the minimum and maximum rise time can be determined as in equation (4.19). See figure 4.20 for the circuit model for two diodes in series.

$$t_{rise,min} = 5 \cdot \tau_1 = 5 \cdot C_{jo,1} \cdot R_{F,1} = 5 \cdot 5nF \cdot 1.3m\Omega = 32.5ns \tag{4.19}$$

$$t_{rise,max} = 5 \cdot \tau_2 = 5 \cdot C_{jo,2} \cdot R_{F,2} = 5 \cdot 6.5nF \cdot 1.5m\Omega = 48.8ns \tag{4.20}$$

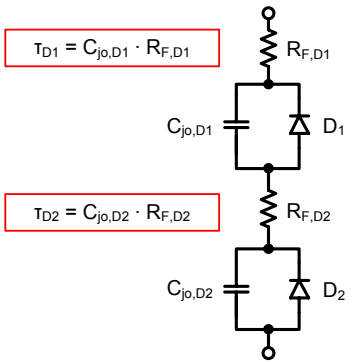


Figure 4.20: *Circuit model of two diodes in series, each with individual forward resistance R_F and junction capacitance C_{jo}.*

The difference in rise time become $\Delta t_{rise} = 48.8 - 32.5 = 16.3ns$. Within this period the voltage inequality between the diodes emerge, and therefore the rise time is used to estimate the appropriate minimum capacitance according to equation (4.13). t_{rv} is set to $t_{rv} = \Delta t_{rise}$.

$$C_{s,min} = \frac{I_L \cdot t_{rv}}{\Delta v_D} = \frac{300A \cdot 16.3ns}{200V} = 24.4nF \tag{4.21}$$

$$\tag{4.22}$$

The maximum capacitance is not calculated, because it is of interest to determine only the smallest possible capacitance, because of the losses associated with the energy stored in the capacitor.

The maximum series resistance R_s is calculated according to equation (4.9) as:

$$R_{s,max} = \frac{T_{on,min}}{5 \cdot C_{s,min}} = \frac{2\mu s}{5 \cdot 24.4nF} = 16.4\Omega \tag{4.23}$$

The component values calculated are added to the simulation circuits in figure 4.18. For summary, the chosen values are $C_s = 24.4nF$, $R_p = 200k\Omega$ and $R_s = 16.4\Omega$. The simulation results are shown in figures 4.22, 4.23 and 4.24.

Figure 4.21 shows the voltage and current waveforms, when a passive snubber is not applied to the series connected diodes. This is done to show the need of snubber circuits, when parameter deviations are present in the diodes. In this case the diode D_3 is exposed to a high voltage of $v_{D3} = 1.05kV$, and the voltage difference between the two diodes is $\Delta v_D \approx 900V$. The Semikron reverse diode used for the realization, can block a maximum of $V_{D,max} = 1.7kV$, so the voltage seen by the diode here is within the upper limit, and not in direct danger of destruction. But the simulation clearly shows the consequence of the parameter differences and the need to add balancing circuitry, because the parameters change with temperature that may lead to even larger voltage difference.

Figure 4.22 shows the voltage and current waveforms, when passive snubbers are applied to the series connected diodes. The results show, that for the given parameter deviations Δt_{rise} and the used design guide, the required voltage balancing can be obtained. The maximum voltage difference is $\Delta v_{D,snub} \approx 50V$, which is within the chosen requirement and design parameter of $200V$, and therefor the snubber can be accepted. The losses associated with the snubber are explained in section 4.2.2.3.

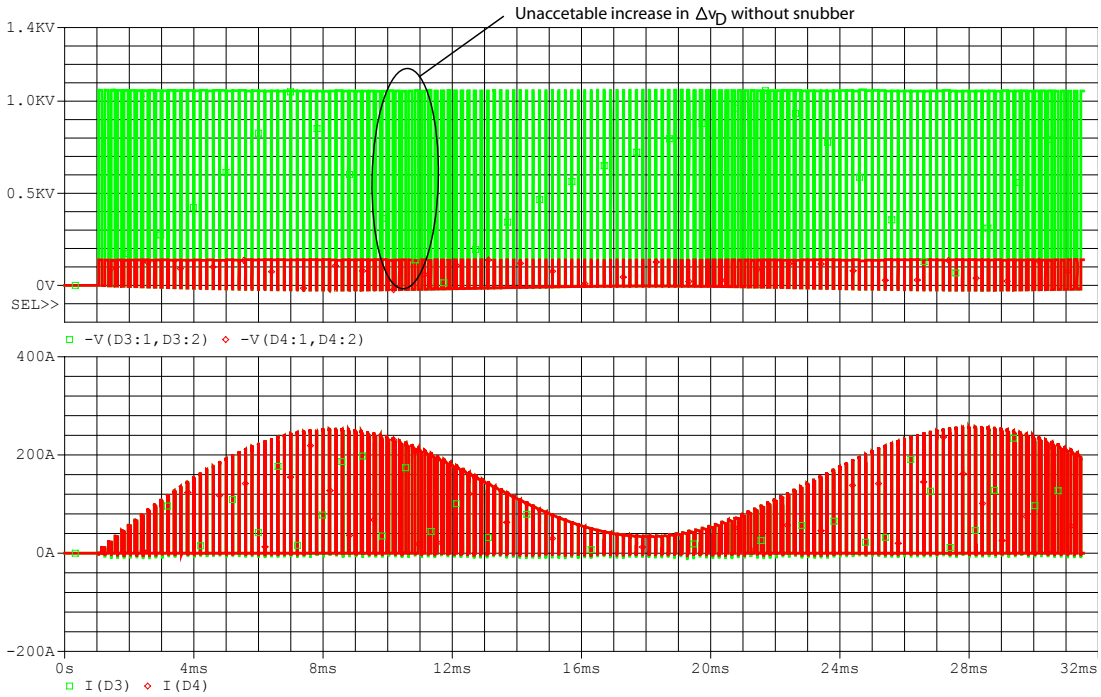


Figure 4.21: *Simulation of series connected diodes* ***without*** *passive snubbers. (1) v_{D3} and v_{D4}, (2) i_{D3} and i_{D4}.*

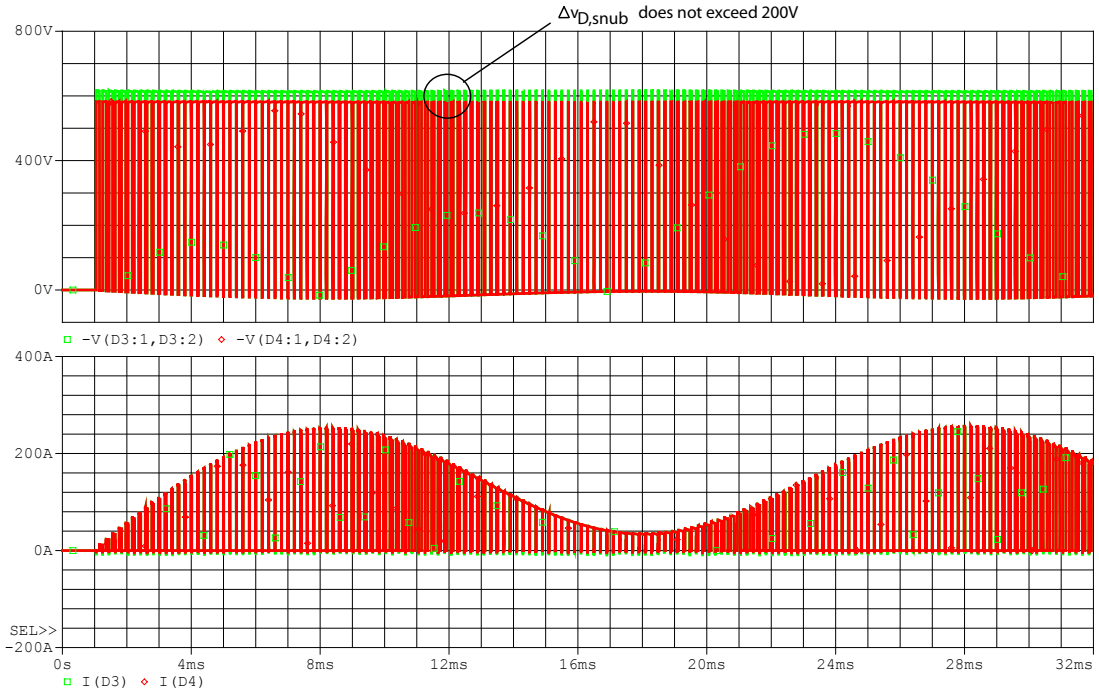


Figure 4.22: *Simulation of passive snubber for series connected diodes. (1) v_{D3} and v_{D4}, (2) i_{D3} and i_{D4}.*

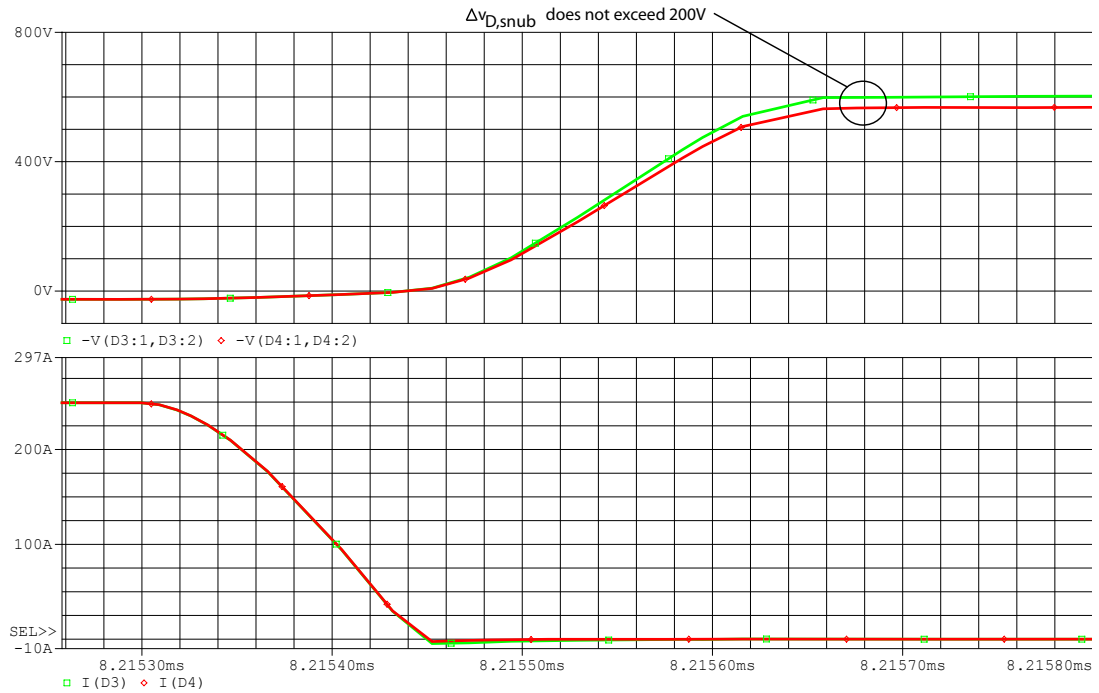


Figure 4.23: *Simulation of off transition of passive snubber for series connected diodes. (1) v_{D3} and v_{D4}, (2) i_{D3} and i_{D4}.*

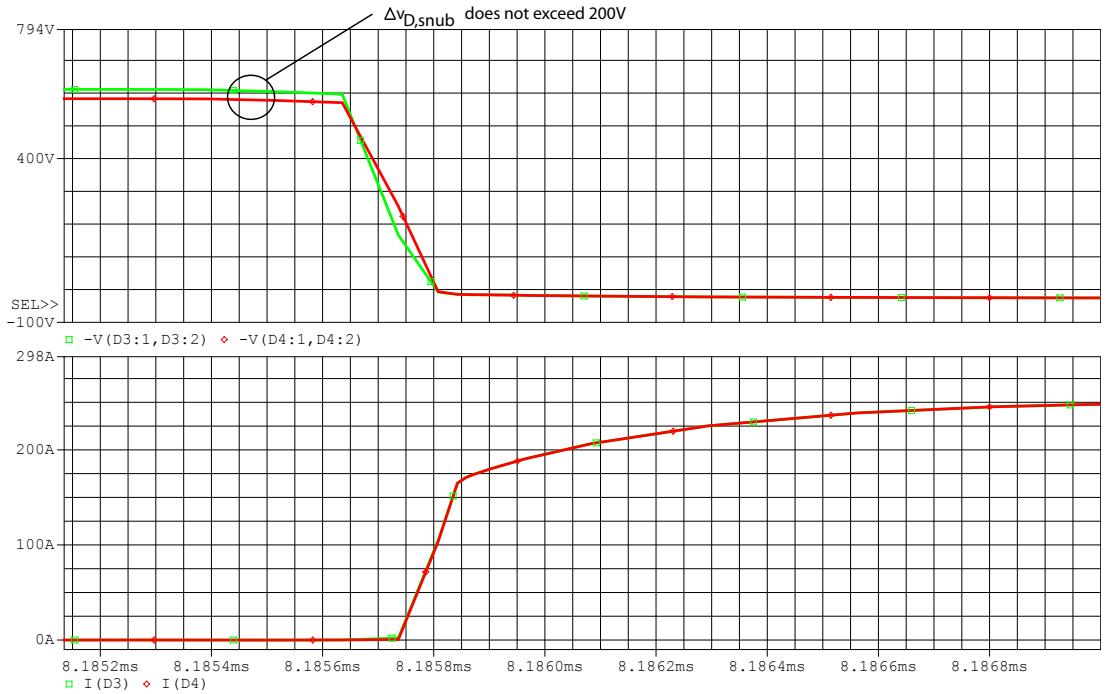


Figure 4.24: *Simulation of on transition of passive snubber for series connected diodes. (1) v_{D3} and v_{D4}, (2) i_{D3} and i_{D4}.*

4.2.2.3 Losses in passive snubber

As mentioned in the introduction, the main disadvantage of the passive snubber is the power losses related to the snubber capacitors being discharged into the IGBTs in every on transition.

The total losses can be compared to the maximum acceptable voltage difference between the IGBTs in off state, and from this an eventual optimum or trade off can be found. The losses depend on the switching frequency, the capacitance and the voltage according to

$$P_{loss} = f_{sw} \cdot \frac{1}{2} \cdot C_s \cdot V_{Cs}^2 \quad [W] \tag{4.24}$$

Having two capacitors C_{s1} and C_{s2} sharing the DC supply voltage V_{DC} with individual voltages, the losses become

$$\begin{aligned} P_{loss} &= P_{Cs1} + P_{Cs2} = f_{sw} \cdot \frac{1}{2} \cdot C_s \cdot \left(V_{Cs1}^2 + V_{Cs2}^2\right) && (4.25)\\ &= f_{sw} \cdot \frac{1}{2} \cdot C_s \cdot \left[\left(\frac{V_{DC}}{2} + \frac{\Delta v_{ce,snub}}{2}\right)^2 + \left(\frac{V_{DC}}{2} - \frac{\Delta v_{ce,snub}}{2}\right)^2\right] && (4.26)\\ &= f_{sw} \cdot \frac{1}{2} \cdot C_s \cdot \left(\frac{V_{DC}^2 + \Delta v_{ce,snub}^2}{2}\right) \quad [W] && (4.27) \end{aligned}$$

Equation (4.8) and (4.27) are used here to estimate the minimum capacitance required to obtain a given maximum voltage difference between the IGBTs in off state and the related losses. The capacitor voltage rise time is chosen to $t_{rv} = 330ns$ according to the simulation parameters on page 39. The maximum load current and switching frequency are $I_{load} = 300A$ and $f_{sw} = 5kHz$. The results are shown in figure 4.25.

As can be seen from the figure, the losses increase with decreasing voltage difference, because the required capacitance becomes larger. For the specific voltage difference of $\Delta v_{ce,snub} = 200V$ as used for the simulation

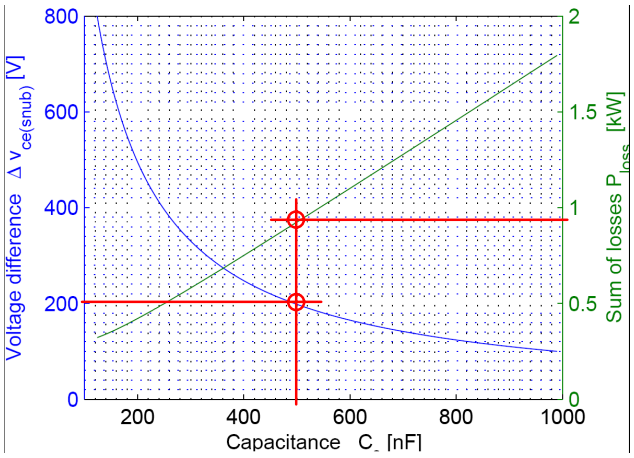


Figure 4.25: *Plot of acceptable voltage difference $\Delta v_{ce,snub}$ between two switches in off state, required snubber capacitance C_s and related losses P_{loss}. Fixed parameters are $I_{load} = 300A$ and $f_{sw} = 5kHz$.*

design and results shown in figure 4.16, the total losses become $P_{loss} \approx 1kW$. Another point worth noticing is, that the distribution of snubber losses become unequal according to equation (4.24), whenever the voltage difference becomes significant, meaning unequal heating of the devices.

The losses may be lowered for a given application, but here the trade off is an increase in the switch voltage difference. And for a high difference, the switch voltages approach the maximum limit, and the safe zone decreases.

Another way to lower the losses is to choose gate drivers and IGBTs, that are closely matched with respect to signal propagation delays and parameter differences. Finally the switching frequency is directly proportional to the losses.

4.2.3 Conclusion on the passive snubber

In this section the passive snubber is analyzed, designed and simulated for a pair of IGBTs in series and for a pair of diodes in series. The simulation results show, that acceptable performance is obtainable for both applications, because the device off state voltages do not exceed the designed values. But for the case with series connected IGBTs with a significant gate driver delay time, the losses related to the energy stored in the snubber capacitors, becomes unacceptably large, easily reaching the kW range. For this reason the passive snubber is rejected as an option for voltage balancing for IGBTs in a series string.

In the case with series connected diodes, voltage balancing can be obtained using the same topology and design rules an for the IGBT based snubber. In this case, the required snubber capacitance become significantly smaller, also with much smaller power dissipation. Because of this, the passive snubber is accepted as solution for balancing the voltage across the neutral point clamped diodes.

4.2.4 Clamping by active gate control method

This method belongs to the active gate control schemes, because the balancing is obtained by controlling the gate emitter voltage independent of the gate driver signal. The topology is proposed in an article by [Ju Won Baek & Kim, December 2001]. In this topology a relatively simple circuit compares the voltage across two or more switches, and if a significant voltage difference appears, the circuit tries to equalize them by affecting the gate emitter voltage. In the turn on transition, the slowest switches are turned on by injecting additional gate current, and in the turn off transition, the fastest switches are turned on for a while, until the slowest switch follows. This means, that the snubber is always on state dominant, meaning that no switch

in a series string is allowed to turn off until the slowest switch gate signal goes low.

The circuit is only monitoring v_{ce}, and therefore the topology is operating the same way, no matter, if the slowing down of one switch is due to a delayed gate driver, difference in gate resistance, difference in gate capacitance or difference in switch on resistance etc. The balancing in any case is obtained by affecting the gate emitter voltage, depending on, if a given switch is turning on or off.

The circuit with two series connected switches is shown in figure 4.26. The snubber consists of six resistors, four capacitors, and two diodes. R_{11}, R_{12}, R_{21} and R_{22} form resistive voltage dividers and are used for static voltage balancing only. The capacitors C_{11} and C_{21} are used as reference voltages and are in the ideal case assumed to carry the same constant DC voltage $V_{C11} = V_{C21} = V_{dc}/2$, even during transitions. This means, that initially the capacitors have to charge up before operation, and they must be chosen large enough to keep the voltage constant, even when the circuit tries to balance the switches. The diodes D_1 and D_2 are used to block the gate currents from flowing into the capacitors, when the switch voltages are balanced perfectly.

The voltages across the capacitors C_{12} and C_{22} are not constant. They are varying between zero and $-V_{dc}/2$ in on and off transitions in a balanced situation, because the voltage across C_{11} and C_{21} is constant. When an unbalance appears, the capacitor voltage for the slowest switch becomes positive - in worst case equal to $V_{dc}/2$, and the diode begins to conduct a current into the gate of the slowest switch to turn it on. A detailed description is below.

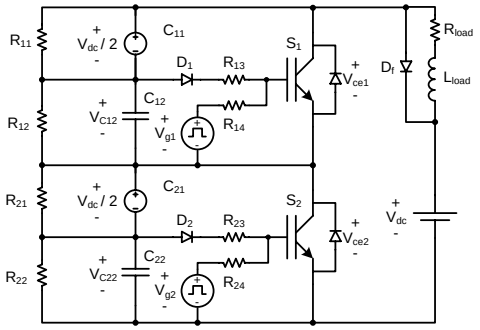


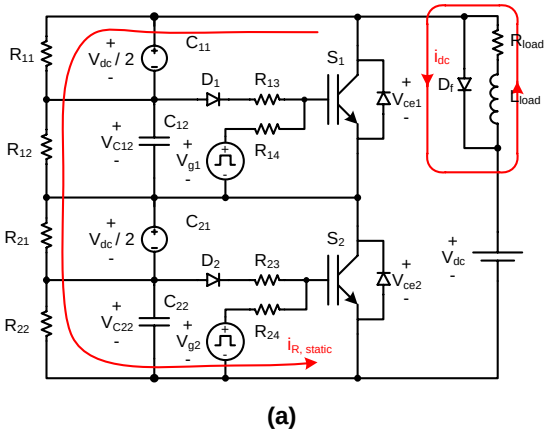
Figure 4.26: *Schematic of the balancing circuit for two switches.*

4.2.5 Operation principle

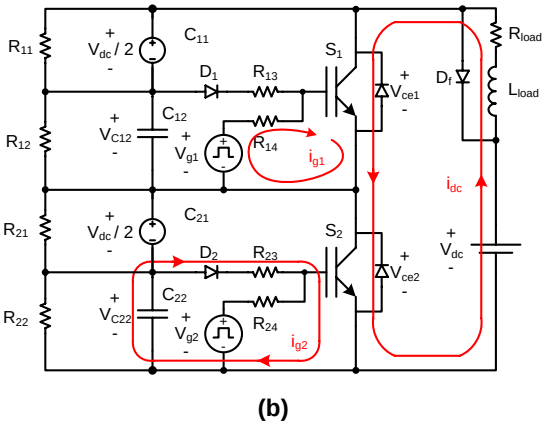
The operation of the balancing circuit is most easily described in the ideal case, when the capacitor voltage of C_{11} and C_{21} is assumed to be constant and exactly $V_{DC}/2$ at any time. In this case, the operation is divided into six periods for one cycle as described below. Later in this section non ideal behavior and consequences of this are described closely. In both cases, the unbalance is assumed to be generated by a delayed gate signal. In the transient periods, the static balancing resistors can be ignored.

Ideal operation

The ideal operation is shown in six periods in figures 4.27 to 4.32.



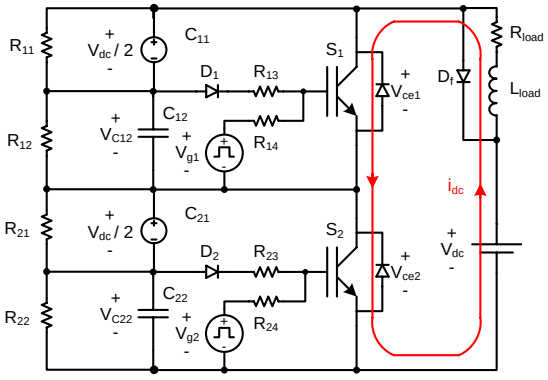
(a)



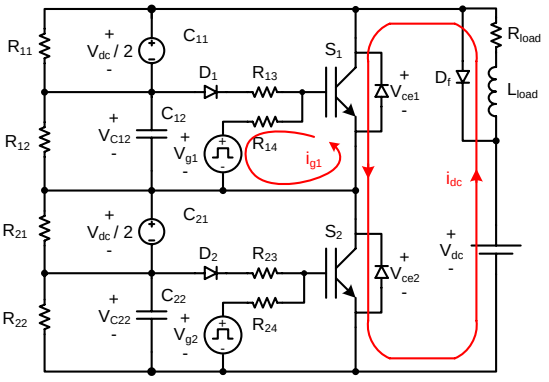
(b)

Figure 4.27: ***Period (a)****. Here both of the switches are completely turned off, and the load current flows through the inductive load L_{load} and the freewheeling diode D_f. The voltage across C_{12} and C_{22} is zero.*

Figure 4.28: ***Period (b)****. Here the gate driver of S_1 is turned on earlier than S_2, and the voltage across S_1 decreases quickly, thus increasing the voltage across the capacitor C_{22}. Before any gate signal is applied to S_2, current flows through D_2 into the gate turning S_2 on together with S_1, in this way trying to balance v_{ce1} and v_{ce2}.*



(c)



(d)

Figure 4.29: ***Period (c)****. Finally both gate drivers are in the on state. The capacitors C_{12} and C_{22} reach $-V_{dc}/2$, and both switches turns fully on.*

Figure 4.30: ***Period (d)****. Here an on to off transition has just started. Only the driver v_{g1} goes low, and current is flows out from the gate of S_1, discharging the gate capacitance. Current i_{dc} still flows from collector to emitter, because the switches are not turned fully off yet.*

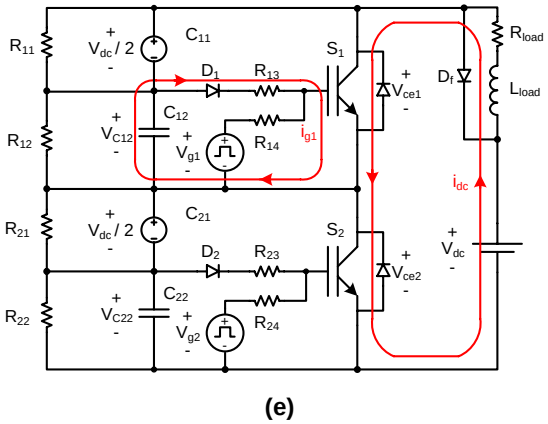


Figure 4.31: ***Period (e)****. Here the voltage across* S_1 *increases to a level above* $V_{DC}/2$*, and the capacitor voltage* v_{C12} *becomes positive, and* D_1 *becomes forward biased. Therefore current flows into the gate of* S_1 *even though it is just turned off. In this way the voltage across* S_1 *does not increase above* $V_{DC}/2$*. In this state, the switches do not see the same voltage yet, that means they are not balanced. This happens in period (f).*

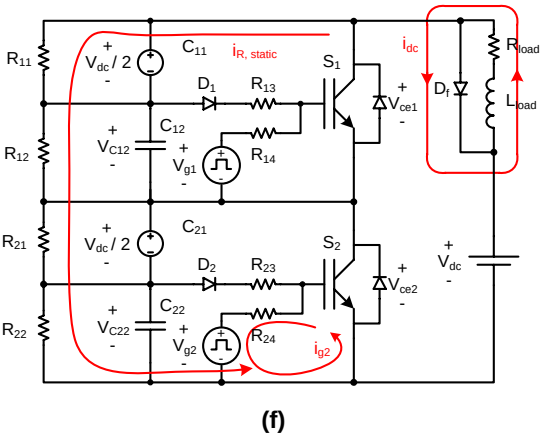


Figure 4.32: ***Period (f)****. In this period, the gate driver* v_{g2} *goes low, and current flow out of the gate emitter capacitance of* S_2*.* v_{ce2} *starts to increase, and at the end of this period, the voltage of* S_2 *also reaches* $V_{dc}/2$ *and both switches become high impedant and the static balancing is obtained by the resistive network* R_{11}*,* R_{12}*,* R_{21} *and* R_{22}*.*

The voltage waveforms $v_{ge1,ge2}$, $v_{ce1,ge2}$, $v_{C12,C22}$ and the current waveforms $i_{R13,R23}$ and $i_{R14,R24}$ are shown in figure 4.33.

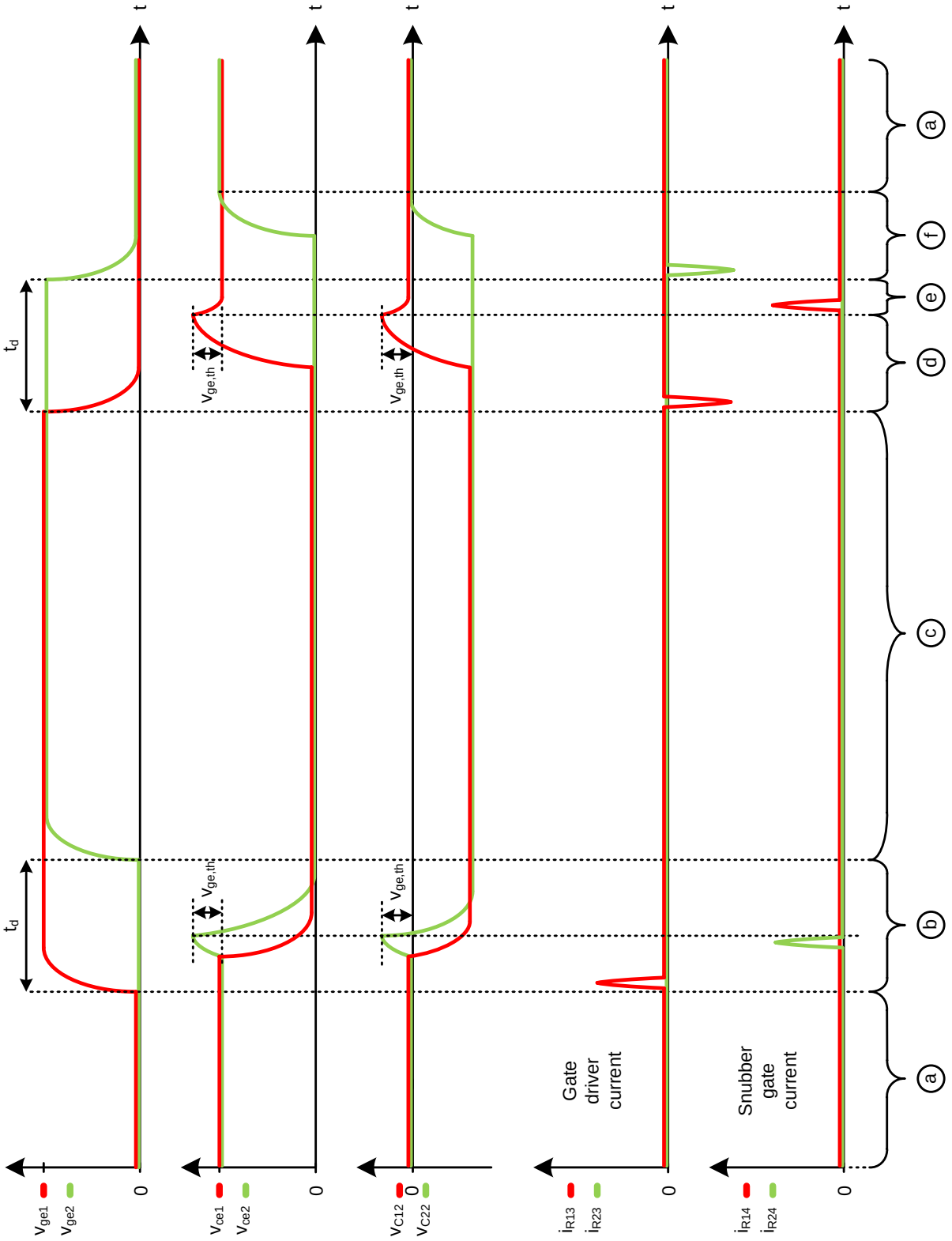


Figure 4.33: *Waveforms for the ideal active gate control snubber.*

Non ideal operation

In the preceding section, the operation was described assuming, that the voltage across C_{11} and C_{21} is constant at any time and equal to exactly $V_{DC}/2$. This is only possible, if the capacitors are infinitely large, and the voltage drop across the resistors R_{12} and R_{22} is zero, which requires zero resistance. This would in fact oppose the operation of the snubber, because the snubber balancing function is dependent on a voltage across the resistor R_{12}, and to obtain this across a zero resistance would require infinitely high current.

The consequences of non ideal operation, design rules regarding the resistive network and the capacitors, are presented here to show disadvantages and limitations with this type of snubber. The circuit containing one active gate snubber is shown in figure 4.34. For two transistors, two circuits are needed.

Design of resistive network

The resistive network for the steady state balancing R_{11} and R_{12} is needed in the off state, and the sum of resistance is designed based on the IGBT leakage current. Here the requirement is, that the current in the off state is required to be approximately five times the IGBT leakage current to make the resistive network dominate [Semikron, -]. By voltage division one obtains:

$$\sum R = R_{11} + R_{12} = \frac{v_{ce,off}}{5 \cdot i_{c,off}} \quad [\Omega] \tag{4.28}$$

The design would be simplified by having $0V$ off state gate emitter voltage $v_{ge,off}$, as in the ideal case. But in practical cases, this is negative to ensure proper turn off. The used Semikron gate drivers, applies $v_{ge,off} = -7V$.

Because of a negative $v_{ge,off}$, the resistor R_{12} may start to conflict with the gate driver, if chosen too small. The diode D_1 is included to apply gate current, when v_{ce12} becomes positive, but when v_{ge} is negative, the diode is forward biased and the gate driver will conduct a constant off state current, which is not desirable [1].

On the other hand, the resistor R_{12} should be chosen very small to ensure, that the voltage across the capacitor C_{11}, that acts as reference, is as close as possible to $V_{DC}/2$. But this would draw high current from the gate driver in off state, and this creates a conflict.

As can be seen from figure 4.35, the off state current $5 \cdot i_{c,off}$ will find an alternative path trough the diode and the gate driver in the off state, and that allows to put R_{12} to a high resistance without corrupting the static sharing.

[1] Because the average gate current capabilities of the Skyper driver is only $I_{g,avg} = 50mA$.

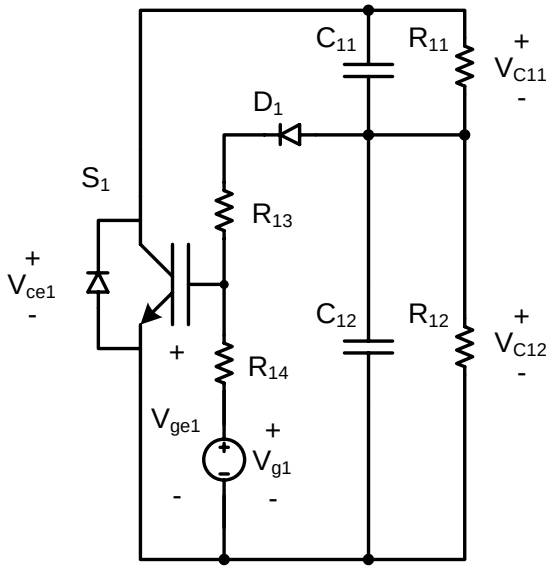


Figure 4.34: *Schematic of one single active gate snubber.*

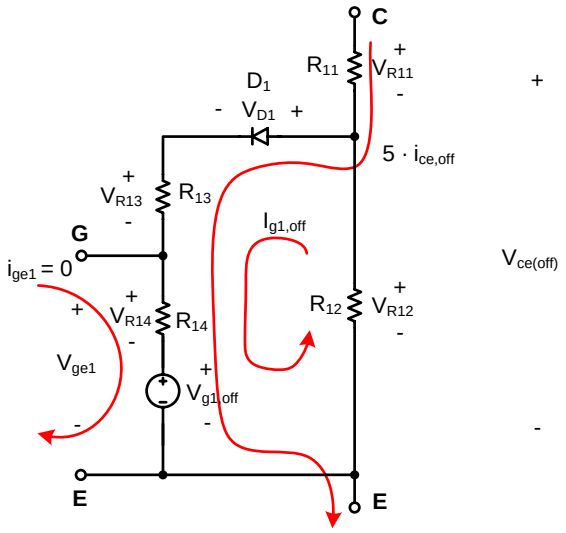


Figure 4.35: *Schematic of current paths with gate driver in off state.*

From this, the resistance of R_{11} is determined as

$$R_{11} = \frac{v_{ce,off} - v_{D1} - v_{R13} - v_{R14} - v_{g1}}{5 \cdot i_{c,off}} \quad [\Omega] \tag{4.29}$$

Because $v_{ce,off}$ typically is large and $i_{c,off}$ is in the mA range, the voltage drop across D_1, R_{13}, R_{14} and the gate driver may be ignored. Equation (4.29) therefore simplifies to

$$R_{11} = \frac{v_{ce,off}}{5 \cdot i_{c,off}} \quad [\Omega] \tag{4.30}$$

The resistor R_{12} is kept in the circuit to ensure the static sharing on case of the gate driver going high impedant. The actual resistance is determined from the acceptable current, that the gate driver can source in off state. This should be set in the low mA range.

$$R_{12} = \frac{v_{ge,off} - v_{D1}}{i_{g1,off(max)}} \quad [\Omega] \tag{4.31}$$

Here the voltage drop across R_{13} and R_{14} is ignored, because they are typically small.

The feedback resistor R_{13} is included in the design to limit the current through the diode D_1, to protect the diode. Within these constraints it can be chosen freely. But the choice of resistance also has great influence on the snubber dynamics. The smaller resistance chosen, the quicker and better voltage balancing is obtained, because the snubbers ability to deliver high peak current into the gate, will make the switches turn on faster. A proper balancing function is highly dependent of fast response of the switches and though high peak gate current $\hat{i}_{ge1}$.

In practice, the optimal feedback resistance R_{13} is very hard to determine analytically and is better determined iteratively by simulation and tests to assure, that the diode is not destroyed by over current and that the balancing is obtained with the chosen resistance. It's worth noticing, that fast snubber response requires fast switching and this in term increases reverse recovery losses, so a trade off in this field must be found, if minimization of losses is of concern. Also the optimum resistance found for a given switch may not

stay optimal for a long period, because aging and temperature generally changes the device parameters, and this may put a new set of requirements to the optimal resistance. In this particular case, the resistance is chosen equal to R_{14}, which is normally only a few ohms.

Design of capacitive network

For the design of capacitors, the upper capacitor C_{11} must be chosen as large as possible, to fix the voltage as reference for the snubber. The lower capacitor must be chosen much smaller than the upper for two reasons. In the first case, a part of the power dissipation of the snubber depends on the energy stored in C_{12}. The voltage shifts from $-V_{DC}/2$ to ≈ 0 in every turn off transition giving a change in stored energy as in equation (4.32).

$$\Delta W_{C12} = \frac{1}{2} \cdot C_{12} \cdot \Delta V_{C12}^2 \quad [J] \tag{4.32}$$

This energy is dissipated into R_{12} every time the switch in turned off, and the larger capacitance, the larger power dissipation. Secondly the capacitance must be small enough to ensure fast response of the snubber in the turn off transitions. The response depends on, how fast C_{12} charges, related to the time constant τ of the RC circuit C_{12} and R_{11}.

$$\tau_{RC,lower} = R_{11} \cdot C_{12} \quad [-] \tag{4.33}$$

$\tau_{RC,lower}$ must be much smaller, than the corresponding τ for the upper capacitor RC network

$$\tau_{RC,upper} = R_{12} \cdot C_{11} \quad [-] \tag{4.34}$$

In the practical application, the upper capacitance is chosen as large as possible, only limited by the available voltage ratings and the physical size. The lower capacitance is chosen very small or left out of the circuit totally, because the energy delivered to the gate is flowing from the upper capacitance anyway.

Variations in reference voltage

In this section, the consequences of the non ideal reference voltage across the upper capacitors C_{11} and C_{21} is analyzed. For ideal operation of the snubber, these voltages must remain constant, but in the practical case, this is not possible. In the on and off transitions, the capacitor voltages start to deviate from one another, if devices have different parameters. And more important, the voltages start to drop below $V_{DC}/2$, when the duty cycle stays below $D = \frac{1}{2}$, because in this case the discharge time is longer than the charging time. The mechanism and consequences of this is described in detail in the following.

Figure 4.36 shows the interaction of the switch and the two RC networks during balanced off (a) and on state (b) and during a non balanced off transition (c), where switch S_2 turns off earlier than S_1. The resistors R_{11}, R_{21} and the capacitors C_{12} and C_{22} can be ignored here, because they are high impedant compared to the other resistors and capacitors.

Figure 4.36 (a) shows the balanced off state, where neither switch is conducting. Here the capacitors are charged through the resistors R_{12} and R_{22}. The final capacitor voltage depends on the RC time constant τ_{upper} and the off state time for the switches, meaning the duty cycle. In the best case, the voltage reaches the full $V_{DC}/2$ and stays there as in the ideal case. This only happens with an appropriate off state time.

Figure 4.36 (b) shows the on state, where both switches are conducting. The consequence of the switches being on is the discharging of the capacitors C_{11} and C_{21} through the resistors R_{12} and R_{22}. The final capacitor voltage depends on the RC time constant and the on state time for the switches. In the worst case with a long on state time, the capacitors discharge completely.

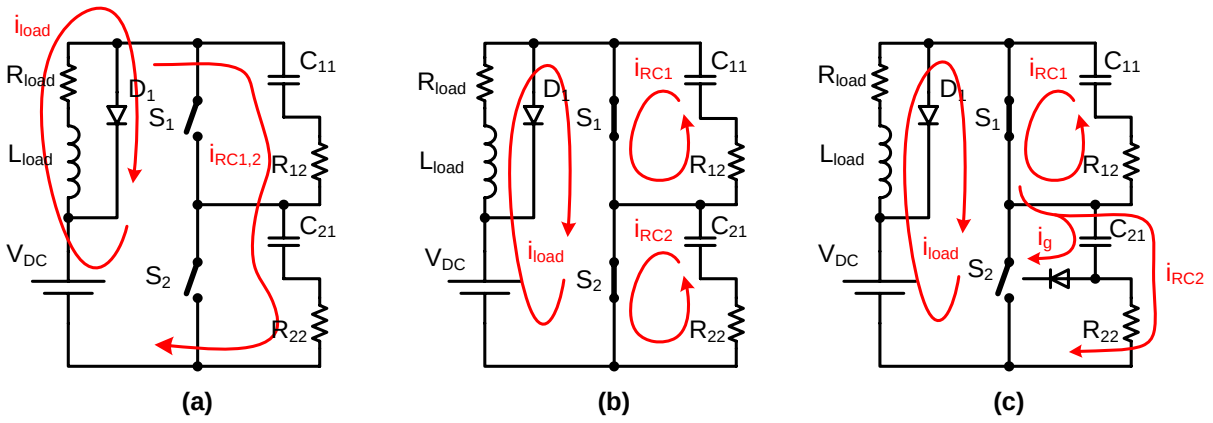


Figure 4.36: *(a) Balanced off state, (b) Balanced on state and (c) Non balanced turn off transient. Switch S_2 turns off earlier than S_1.*

The capacitors not carrying the constant voltage of $V_{DC}/2$, does not corrupt the balancing function of the snubber as such, but when both switches turn from on to off state, the capacitor voltages must be charged to a voltage close to $V_{DC}/2$ very quickly. Otherwise both switches will be turned on again by the snubber, even though both gate signals are low. This happens because a positive voltage appears across R_{12} and R_{22}, and is caused by the transistor dynamics being faster than the RC network.

Figure 4.36 (c) shows the non balanced on to off transition, where switch S_2 turns off earlier than S_1. Here simultaneously, the upper RC network continues to discharge, while the lower RC network is charged again through S_1, because the S_2 is turned off. When the voltage across the switch becomes larger than the voltage across C_{21}, current starts to flow into the gate of S_2, in this way turning the device on again to balance the two switch voltages. At the end of the transient period, the voltage across C_{11} ends up being smaller than C_{21}, and the voltages do not reach the same level again in the preceding off state, if the off state time is too short. This is because both RC networks share identical time constants.

This means, that the capacitors will charge and discharge identically, but with a DC offset, that increases over time. This may corrupt the balancing function, because one of the switches will be turned on all of the time by the snubber, when the capacitor voltages become heavily deviated.

4.2.6 Simulations of active gate control

The ideal and non ideal active gate snubber is simulated by *OrCad* with two switches in series using snubber component values calculated according to the design rules specified. Both cases are simulated to show the operation of the snubber and to show the problems associated with the non ideal behavior. In the ideal case, the upper capacitors are replaced by voltage sources carrying a constant half of the DC link voltage as shown in figure 4.43. Both simulations are performed with a sinusoidal PWM generator supplying both the upper and lower switches with signals, that are delayed by $t_d = 170ns$ according to the device deviation parameters defined on page 22. The reason for using a sinusoidal PWM is to apply variable duty cycle in the whole range $[0; 1]$.

The non ideal control schematic is shown in figure 4.42. Here the capacitance for the upper capacitors is chosen to $C = 10\mu F$, because this is a realistic value for capacitors rated for a voltage of $600V$.

The used component values are calculated here according to equations (4.30) and (4.31) and the data sheet value for the SKM600GA176D leakage current. The DC link voltage is chosen to $V_{DC} = 1.2kV$.

$$R_{11} = \frac{v_{ce,off}}{5 \cdot i_{c,off}} = \frac{600V}{5 \cdot 0.6mA} = 200k\Omega \tag{4.35}$$

$$R_{12} = \frac{v_{ge,off} - v_{D1}}{5 \cdot i_{c,off}} = \frac{7V - 0.7V}{5 \cdot 1mA} = 6.3k\Omega \tag{4.36}$$

$$R_{13} = R_{14} = 5\Omega \tag{4.37}$$

Simulation of ideal active gate control

The simulation schematics of the ideal snubber and the PWM circuit used are shown in figures 4.37 and 4.38. Figure 4.39 shows four periods of operation and figures 4.40 and 4.41 show the zoomed on and off transitions.

Figures 4.40 (4) and 4.41 (4) clearly show, that the balancing of the voltage between the two switches is obtained regardless of the delay in gate signals, because any of the two switches never are exposed to voltages higher than $V_{DC}/2$. Figure 4.40 (2) and Figure 4.41 (2) show, how the snubber inject current into the gate of the particular switch, that is about to be exposed to a voltage greater than $V_{DC}/2$.

The conclusion based on the actual simulations is, that given a constant voltage across C_{11} and C_{21}, the ideal active gate control snubber shows acceptable performance. The challenge is to fix the voltage constantly $V_{DC}/2$, also in situations with variations in the DC link voltage.

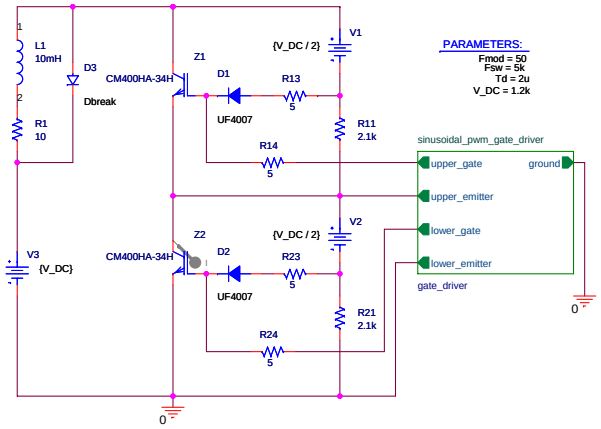


Figure 4.37: *Simulation schematic for ideal active gate control snubber.*

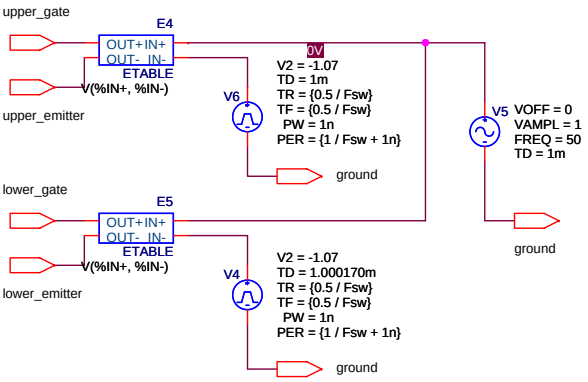


Figure 4.38: *Simulation schematic for sinusoidal PWM circuit with $t_d = 170ns$ and $f_{mod} = 50Hz$.*

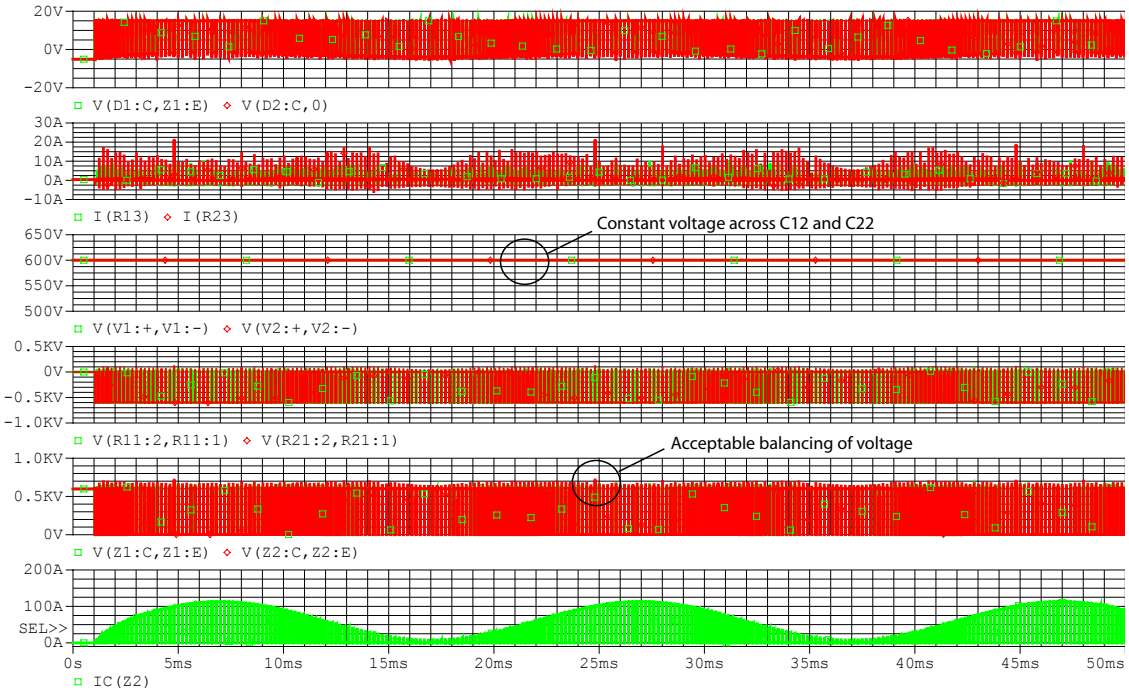


Figure 4.39: *Simulation of the ideal active gate control with constant voltage across C_{11} and C_{21}. (1) v_{ge1} and v_{ge2}, (2) i_{R13} and i_{R23}, (3) v_{C12} and v_{C22}, (4) v_{R11} and v_{R21}, (5) $v_{ce,Z1}$ and $v_{ce,Z2}$ and (6) $i_{c,Z1}$.*

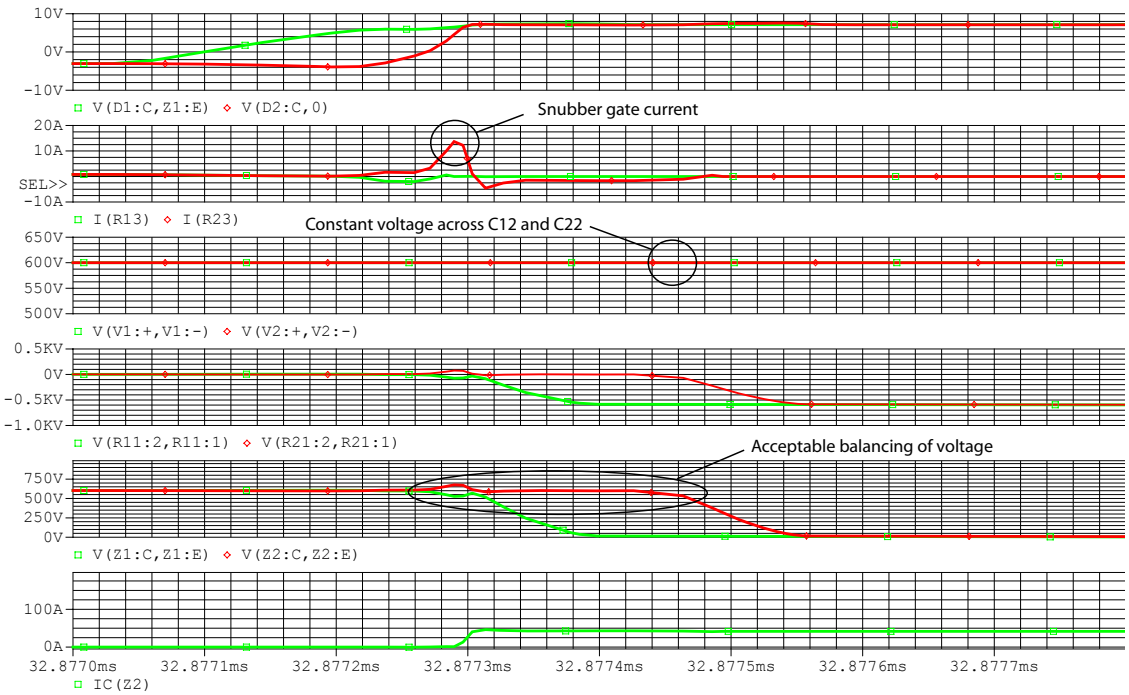


Figure 4.40: *Zoom in of simulation of an on transition by the ideal active gate control (constant voltage across C_{11} and C_{21}). (1) v_{ge1} and v_{ge2}, (2) i_{R13} and i_{R23}, (3) v_{C12} and v_{C22}, (4) v_{R11} and v_{R21}, (5) $v_{ce,Z1}$ and $v_{ce,Z2}$ and (6) $i_{c,Z1}$.*

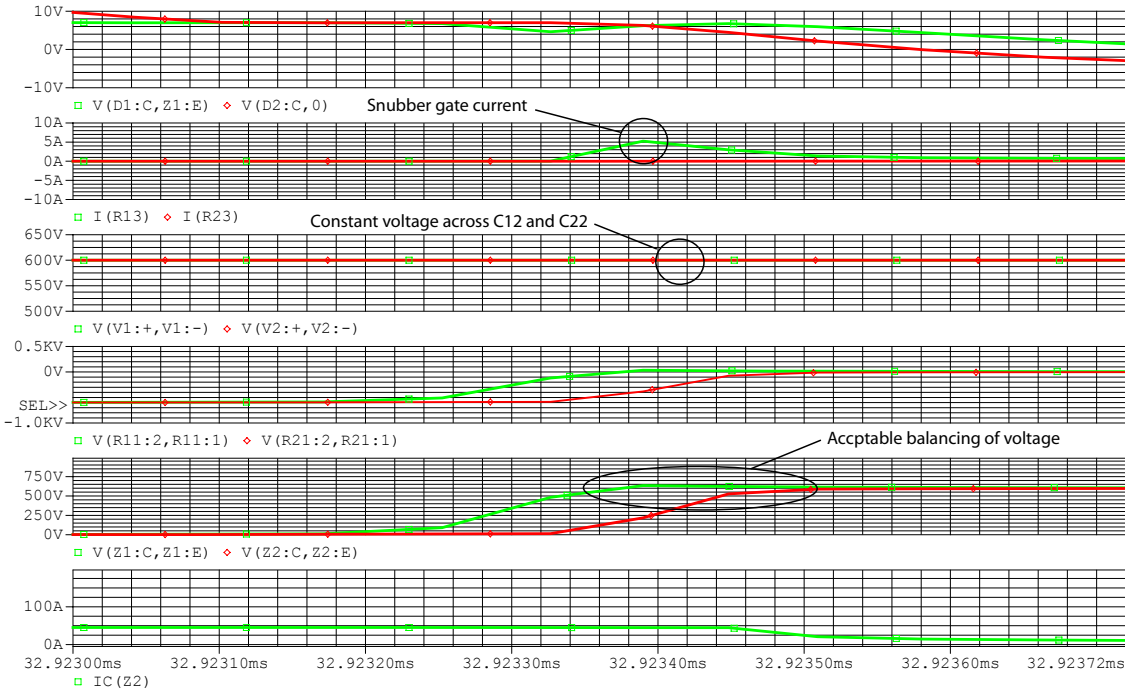


Figure 4.41: *Zoom in of simulation of an off transition by the ideal active gate control (constant voltage across C_{11} and C_{21}). (1) v_{ge1} and v_{ge2}, (2) i_{R13} and i_{R23}, (3) v_{C12} and v_{C22}, (4) v_{R11} and v_{R21}, (5) $v_{ce,Z1}$ and $v_{ce,Z2}$ and (6) $i_{c,Z1}$.*

Simulation of non ideal active gate control

The simulation schematics of the non ideal snubber and the PWM circuit used are shown in figures 4.42 and 4.43. Figure 4.44 shows three periods of operation in $t = [0; 50ms]$, and figures 4.45 and 4.46 show the zoomed on and off transitions.

From figure 4.44 the consequences of the non ideal circuit are clear. In sub figure (3), the voltage across C_{11} and C_{21} starts to drop, when the duty cycle is $D > 0.5$. This is because the discharge time here is longer than the charging time. And also a voltage difference appears between the two capacitors, because the charge required by the snubber to balance the voltages is drawn from the capacitor associated with the slowest switch.

Figures 4.45 (5) and 4.46 (5) clearly show, that the balancing of the voltage between the two switches is obtained regardless of the delay in gate signals and regardless of the capacitor voltages starting to deviate.

Conclusion for active gate control

The conclusion for this snubber based on the actual simulations is, that the deviation of the capacitor voltages v_{C11} and v_{C21} does not directly corrupt the voltage balancing, which is desirable. But the deviation increases over time, and at some instant it will start to affect the balancing, because the difference appears across the switches also. Therefore the active gate control snubber is considered not reliable and not an option.

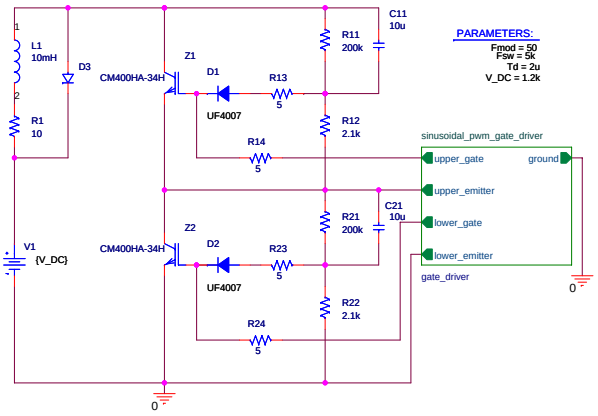


Figure 4.42: *Simulation schematic for non ideal active gate control snubber.*

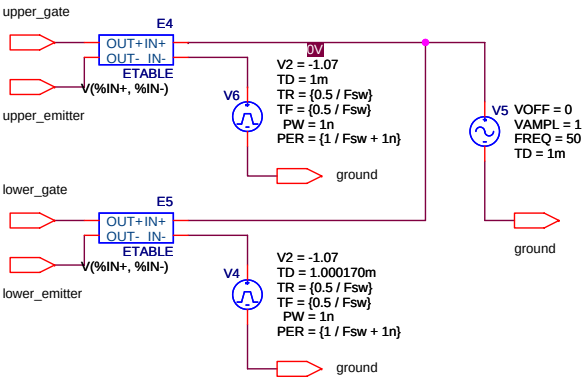


Figure 4.43: *Simulation schematic for sinusoidal PWM circuit with* $t_d = 170ns$ *and* $f_{mod} = 50Hz$.

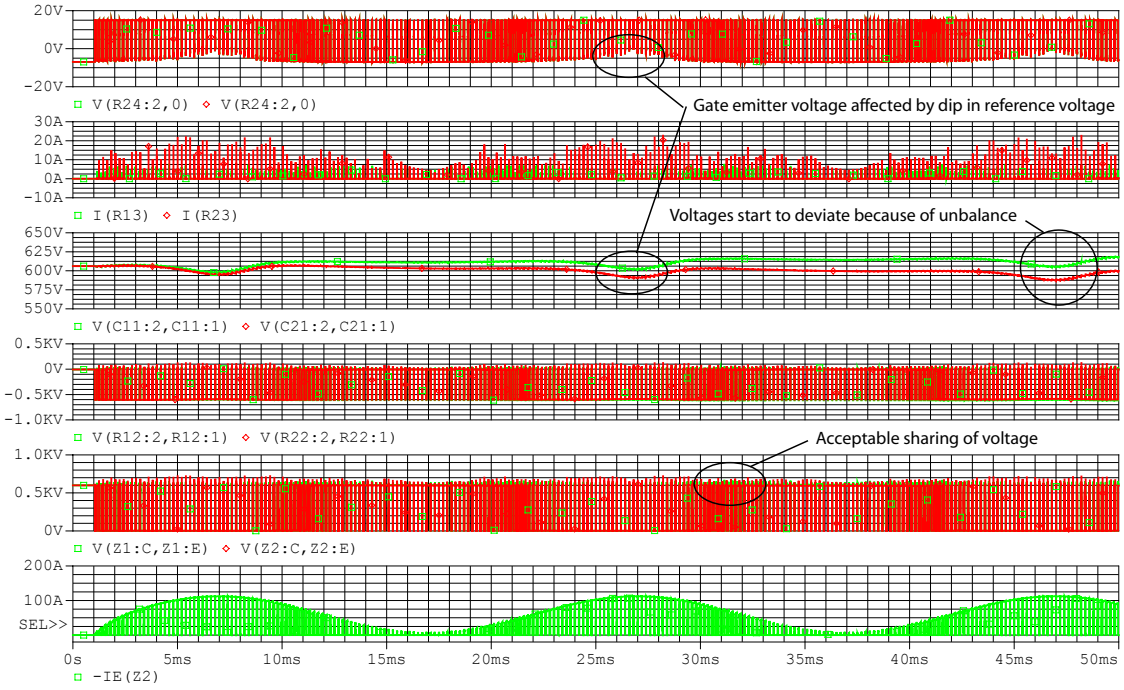


Figure 4.44: *Simulation of the non ideal active gate control. (1)* v_{ge1} *and* v_{ge2}*, (2)* i_{R13} *and* i_{R23}*, (3)* v_{C12} *and* v_{C22}*, (4)* v_{R11} *and* v_{R21}*, (5)* $v_{ce,Z1}$ *and* $v_{ce,Z2}$ *and (6)* $i_{c,Z1}$.

4.2.7 Capacitor voltage stabilization

As described, the decrease in the capacitor voltage across C_{11} and C_{21} leads to non acceptable performance. This decrease can be due to the non intended discharging of the capacitors, but also a quick increase of the DC link voltage will lead to the same consequences, because the mechanism is the same.

One possibility of decreasing the deviation is to increase the capacitance of C_{11} and C_{21} from the $10\mu F$ used here, but here practical limitations and availability becomes an issue. Capacitors with large capacitance for high voltages are available, but they are generally expensive, bulky, heavy and generally based on

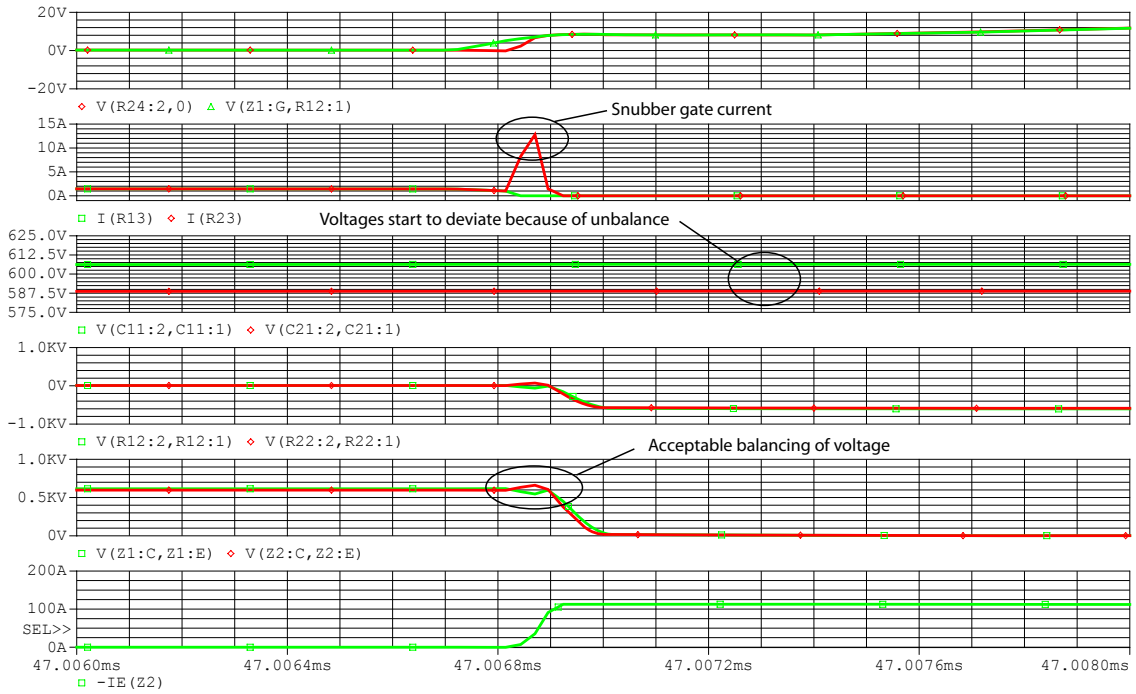


Figure 4.45: *Zoom in of on transition simulation of the non ideal active gate control. (1)* v_{ge1} *and* v_{ge2}*, (2)* i_{R13} *and* i_{R23}*, (3)* v_{C12} *and* v_{C22}*, (4)* v_{R11} *and* v_{R21}*, (5)* $v_{ce,Z1}$ *and* $v_{ce,Z2}$ *and (6)* $i_{c,Z1}$*.*

electrolytic technology with limited lifetime.

Also the capacitance must be chosen very large to ensure long term balancing and reliability, even though the device parameter deviations exceed the expected ones or the ones used in the simulations here. And by using very high capacitance, the RC time constant easily becomes much longer than the eventual rise time in an increase of the DC link voltage, and this will once again turn the switches on in the off state.

Another solution could be to replace the capacitors by isolated constant voltage sources with a constant voltage of $V_{DC}/2$ like in the simulation shown on page 56. In the ideal case the voltage sources must follow the DC link voltage closely even during transients. This solution in practice requires the same amount of isolated PSU's as power switches though adding to the complexity. And these sources are required to possess fast and especially identical dynamics, so that transients do not corrupt the balancing. This solution is not analyzed in more detail here.

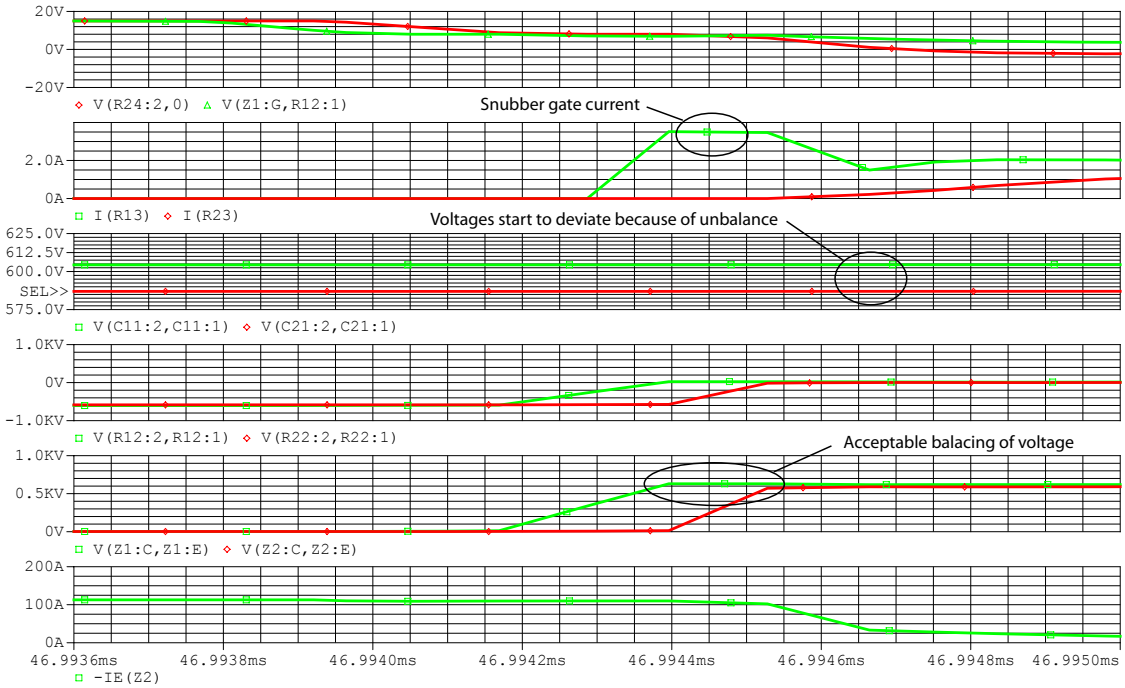


Figure 4.46: *Zoom in of off transition simulation of the non ideal active gate control. (1)* v_{ge1} *and* v_{ge2}*, (2)* i_{R13} *and* i_{R23}*, (3)* v_{C12} *and* v_{C22}*, (4)* v_{R11} *and* v_{R21}*, (5)* $v_{ce,Z1}$ *and* $v_{ce,Z2}$ *and (6)* $i_{c,Z1}$*.*

4.2.8 Zener clamped snubber

The zener clamped snubber is the most simple method analyzed in this report, because it contains only three passive components D_n, Z_n and $R_{p,n}$. Here the collector gate voltage v_{cg} is limited to a maximum level defined by the zener diodes Z_1 and Z_2 break down voltage $v_{B,Z}$ as shown on figure 4.47. Whenever the collector gate voltage v_{cg} increases above the zener break down voltage, the zener diode conducts, as shown in figure 4.48. This increases the gate emitter voltage, and the device is turned on slightly. In this way the IGBT is protected against over voltages. The static balancing is obtained by parallel resistors R_p.

Basically this method is not trying to balance the switch voltages in the transient states, like the gate signal delay method does, but more acting as a over voltage protection.

The diodes D_1 and D_2 are included in the circuit to avoid a constant gate current, that will be conducted by Z_1 or Z_2 through the switches in the on state.

From the zener break down voltage and the maximum gate emitter voltage, the maximum collector emitter voltage becomes

$$v_{cg,max} = V_{B,Z} \quad \Leftrightarrow \tag{4.38}$$

$$v_{ce,max} = v_{ge,max} + V_{B,Z} \tag{4.39}$$

Typically the maximum gate emitter voltage is limited by protection to $v_{ge,max} \approx \pm 20V$.

To ensure proper functionality, the zener break down voltage must be chosen larger than the maximum DC link voltage divided by the amount of devices in series, added with safety headroom for the eventual voltage ripple ΔV_{DC}.

$$V_{B,Z(min)} = \frac{V_{DC} + \Delta V_{DC}}{n}, \quad n = \text{number of devices} \tag{4.40}$$

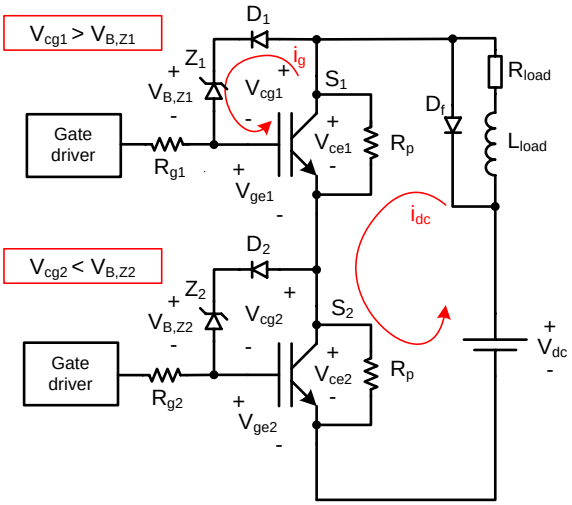


Figure 4.47: *Zener clamped snubber schematic showing current paths in a turn off transient with S_1 turning off quicker than S_2.*

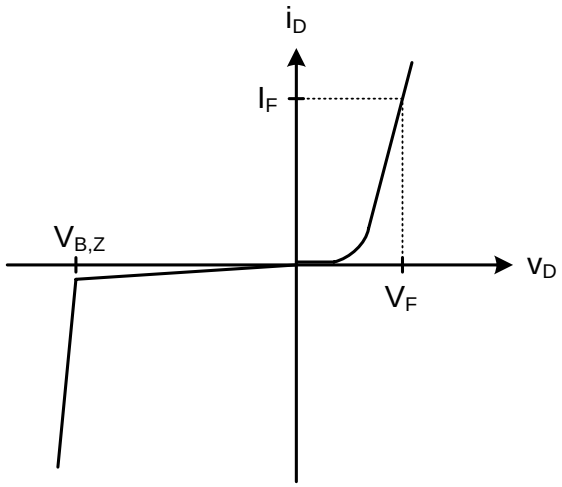


Figure 4.48: *i/v curve for a zener diode.*

If the headroom is ignored, even a small increase in the DC link voltage will clamp all of the switches at the same time leading to a short circuit, which becomes critical, if the voltage increase duration is very long.

In practical applications the zener break down voltage can be chosen arbitrarily, as long as the voltage is kept within the borders of nominal DC link voltage and maximum collector emitter voltage for one IGBT. In this case, unintended clamping of all switches into a short circuit or over voltage break down will not appear. But from a loss point of view, the clamping voltage should be chosen as close as possible to the minimum value according to equation (4.40), because a large difference in the collector emitter voltages between switches leads to unequal distribution of the switching losses. This is because the collector current through the switches always is the same for all switches in the series string, but for large voltage difference, the individual losses begin to differ according to equation (4.41).

$$P_{tot}(t) \quad = \quad P_{S1}(t) + P_{S2}(t) + ... + P_{Sn}(t) \quad = \quad i_c(t) \cdot (v_{ce,S1}(t) + v_{ce,S2}(t) + ... + v_{ce,Sn}(t)) \quad (4.41)$$

where $v_{ce,S1}(t) \neq v_{ce,S2}(t) \neq v_{ce,Sn}(t)$, and $i_c(t)$ is the same for all switches. The total switching losses P_{tot} in a series string stay the same, regardless of the losses being unequally distributed. This is because the sum of switch voltages $v_{ce,Sn}$ always equals the DC link voltage and the collector current i_c for all switches is the same. This can be shown by simulation.

The on state conduction losses $P_{on,Sn}$ will always stay equal for every switch in the series string, because the on state voltages drops are low, and do not differ significantly. Therefore the on state does not contribute to any unequal distribution of losses in a series string.

4.2.9 Simulation of the zener clamped snubber

Here the zener clamped snubber is simulated. As mentioned above, a voltage head room must be included in the zener break down voltage $V_{B,Z}$ to avoid unintended short circuit of the switches.

In the introduction on page 4, the DC link voltage is chosen to $V_{DC} = 2.4kV$ with $\pm 10\%$ ripple giving $\Delta V_{DC} = \pm 240V$. This means, that $60V$ is to be expected across each switch pair, when ΔV_{DC} is divided by the four switches being exposed to the full DC link voltage, as for the three level inverter. Because of this, the zener break down voltage is chosen with additional safety to $V_{B,Z} = 700V$.

The parallel resistors $R_p = 30k\Omega$ are calculated on page 39. The resistors R_3, R_4, R_7 and R_8 are included in the simulation to ensure a defined potential in the junction between the diodes. These resistors are not included in the realization.

The simulation schematic is shown in figure 4.49 and 4.50.

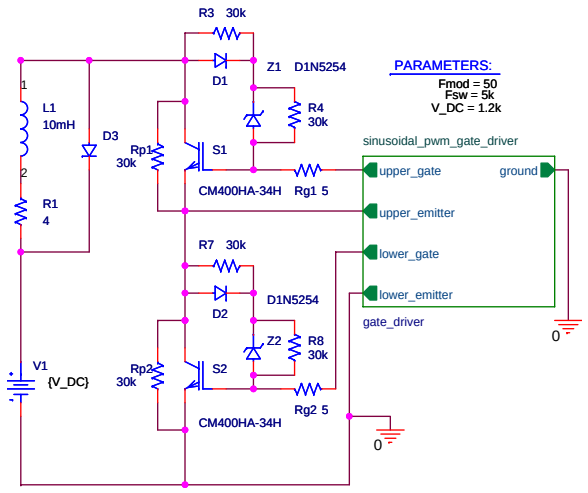


Figure 4.49: *Zener clamped snubber simulation schematic. The zener break down voltage is defined to* $v_{B,Z} = 700V$.

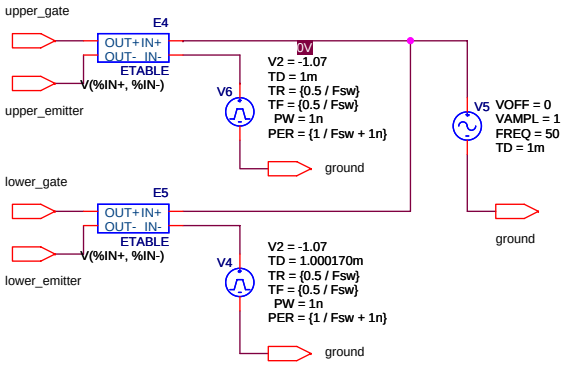


Figure 4.50: *Simulation schematic for sinusoidal PWM circuit with* $t_d = 170ns$ *and* $f_{mod} = 50Hz$.

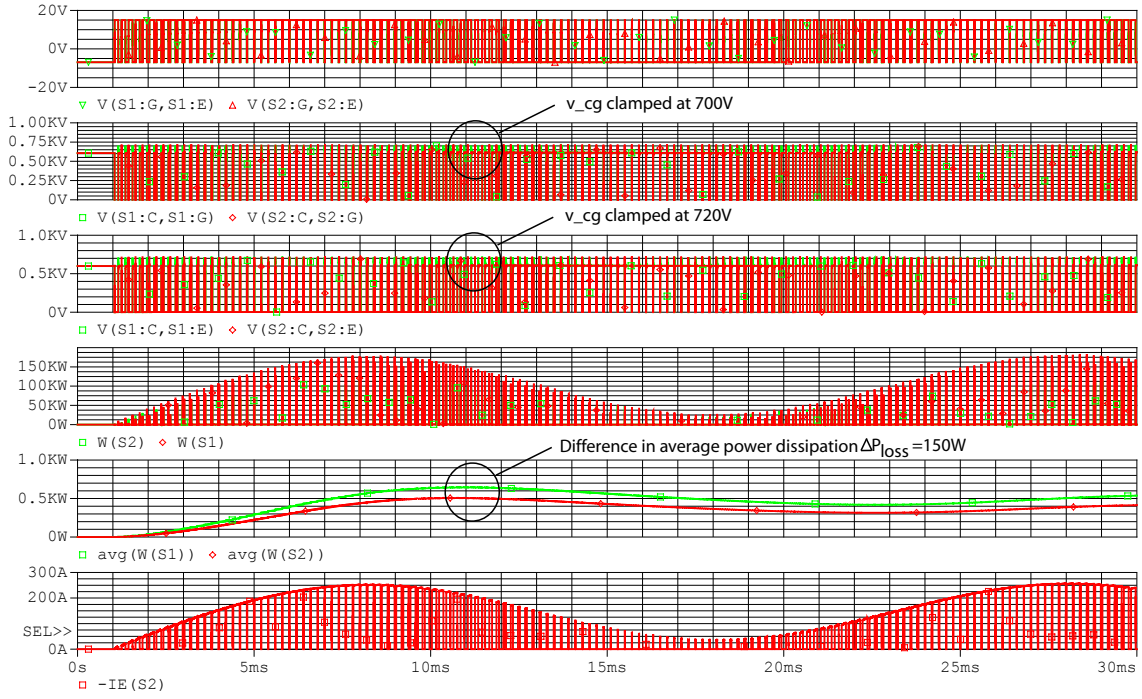


Figure 4.51: *Simulation of the zener clamped snubber. (1)* v_{ge1} *and* v_{ge2}*, (2)* v_{cg1} *and* v_{cg2}*, (3)* v_{ce1} *and* v_{ce2}*, (4)* W_{S1} *and* W_{S2}*, (5)* $W_{S1,avg}$ *and* $W_{S2,avg}$ *and (6)* $i_{c,S2}$.

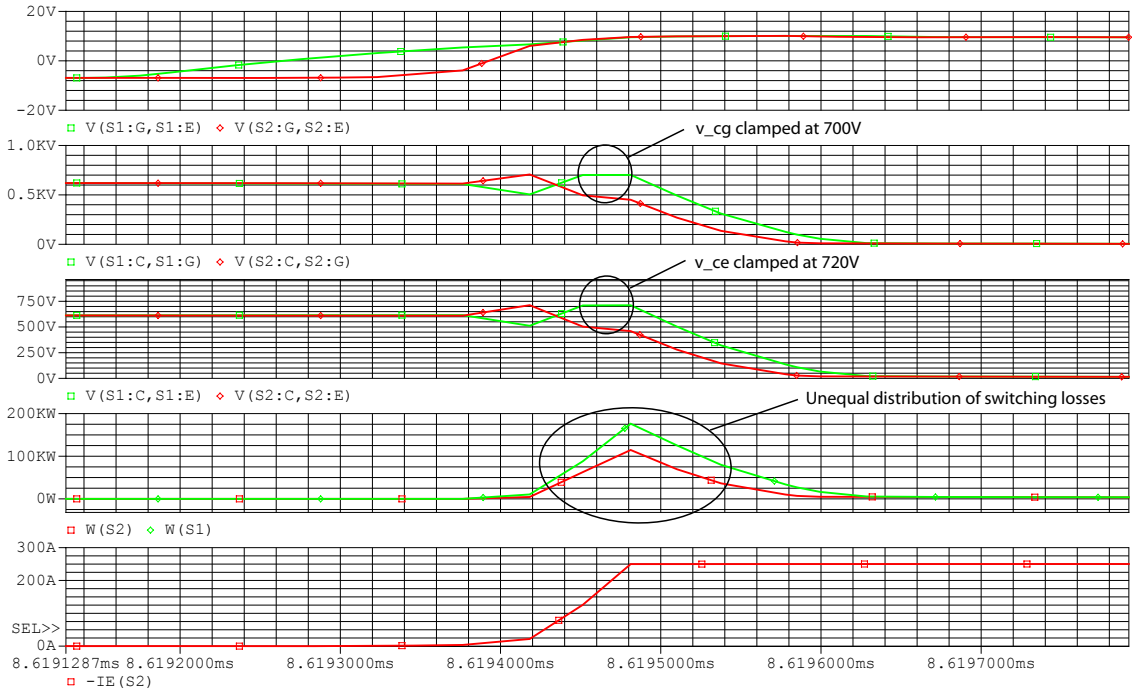


Figure 4.52: *Zoom in of simulation of an on transition by the zener clamped snubber. (1) v_{ge1} and v_{ge2}, (2) v_{cg1} and v_{cg2}, (3) v_{ce1} and v_{ce2}, (4) W_{S1} and W_{S2} and (5) $i_{c,S2}$.*

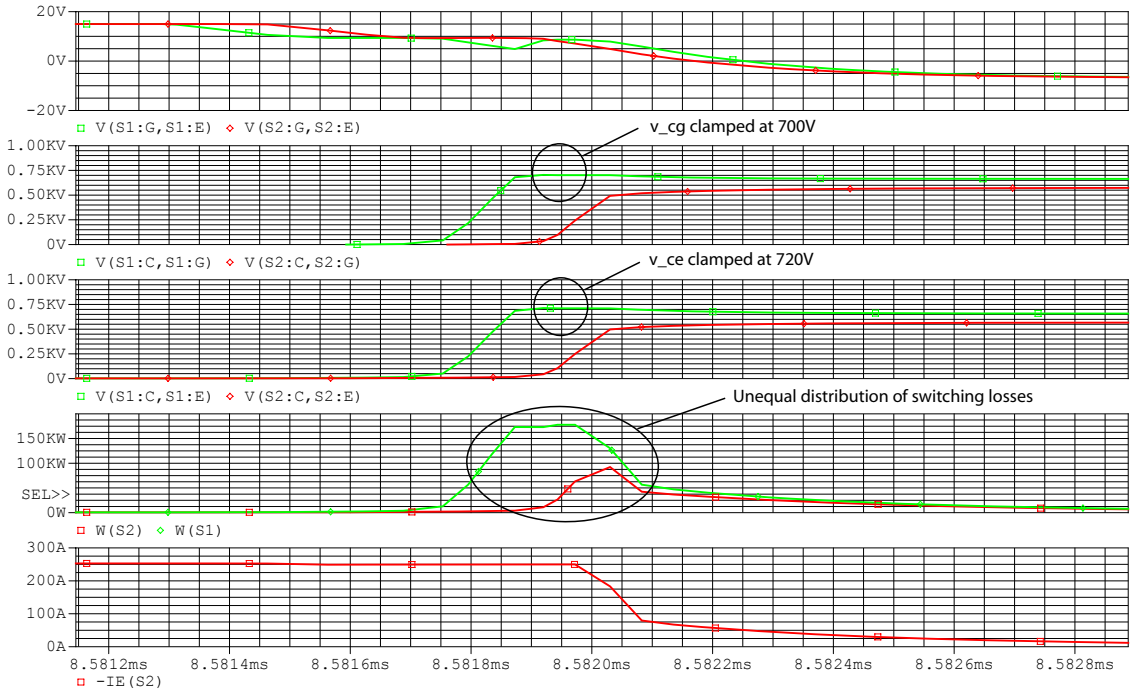


Figure 4.53: *Zoom in of simulation of an off transition by the zener clamped snubber. (1) v_{ge1} and v_{ge2}, (2) v_{cg1} and v_{cg2}, (3) v_{ce1} and v_{ce2}, (4) W_{S1} and W_{S2} and (5) $i_{c,S2}$.*

The simulation results on figure 4.51, 4.52 and 4.53 show two important aspects.

1. First the collector gate voltages and the collector emitter voltages are clamped at $v_{cg} = 700V$ and

$v_{ce} = 720V$, and this satisfies equation (4.39). This means, that the clamping action works properly.

2. Secondly the switching losses are unequally distributed, because the two switches do not share the same voltage in the transients, and this in fact is the main disadvantage of this method. Figure 4.51 (5) shows, that the difference in average power dissipation $\Delta P_{loss} \approx 150W$ meaning, that S_1 dissipates $\approx 30\%$ more power than S_2.

   The quantity of the difference is heavily dependent on the difference in off state voltage $\Delta v_{ce,off} = 200V$ and the gate signal delay t_d, which in this simulation is chosen to $t_d = 170ns$. The smaller theses two values become, the smaller the loss difference also will be.

4.3 Choice of snubber topology for IGBTs

In this chapter three selected methods for balancing voltages between IGBTs and diodes are analyzed in detail. The first method is the passive *RC* snubber, that works by increasing the slope of v_{ce}, and in this way matching the voltages. The other methods are the active gate control and the zener clamped snubber,a dn these work by clamping any over voltage seen in v_{ce}.

The methods are analyzed regarding to ability to balance the collector emitter voltages, power losses and losses distribution between switches. The advantages and disadvantages are summarized in table 4.2.

Method	**Advantages**	**Disadvantages**
Passive snubber	Simple - four passive components Low power dissipation with diodes Accepts transients in DC link voltage Applicable for both IGBTs and diodes	High and unequal power dissipation with IGBTs
Active gate control	Simple - five passive components	Difficult to stabilize reference voltage Not applicable for diodes
Zener clamped snubber	Most simple - three passive components	Non uniform power dissipation Not applicable for diodes

Table 4.2: *Comparison of methods for voltage balancing.*

Based on the analysis and the advantages and disadvantages in table 4.2, the best choice considered for this project is the zener clamped snubber for the IGBTs. This is because of its simplicity and because the snubber power dissipation is low compared to the passive *RC* snubber. The non uniform distribution of losses can be kept at an acceptable level by choosing a clamping level close to the maximum expected voltage according to equation (4.40).

For the neutral point diodes, the only possibility among the analyzed methods is the passive snubber, and therefore this is chosen.

The active gate control is disregarded, because the capacitor voltages, that acts as clamping reference, start to deviate whenever device parameter differences appear. This affects the reliability if the snubber, and this can not be accepted.

Chapter 5

IGBTs under fault conditions

One of the main goals of this project is to analyze and design a protection scheme to prevent a faults from destroying any of the IGBTs in the three-level inverter.

To obtain an over all protection scheme, that prevents destruction of any device in the total inverter system, incl. the power supply, DSP and gate driver boards etc. under any circumstance, then individual protection systems have to be incorporated in all sub systems. This is a complex task and beyond the time frame of the project, and therefore the protection scheme of the inverter is focused on IGBT protection only.

The following definitions are used:

- **Fault situation:** This means, that one or more IGBTs are operated above rated values.
- **Break down:** This means, that one or more IGBT is destroyed as consequence of wrong handling of the fault described above

The break down of an IGBT can happen due to one or more of the following faults mechanisms:

- **Over voltage:** IGBT break down because collector emitter voltage limit exceeded.
- **Over current:** Current range between rated current and short circuit current.
- **Short circuit:** When the current reaches maximum values, as shown on figure 5.5.

The over current fault can happen due to heavy loading of the inverter, whereas a short circuit will appear as a fast fault, characterized by a high current rise, because the short circuit impedance is small. In this project the fast fault is defined, as reaching short circuit level within one switching period, as shown on figure 5.1. The slow fault is characterized by significant line inductance, that leads to small rate of change in current, as shown on figure 5.2.

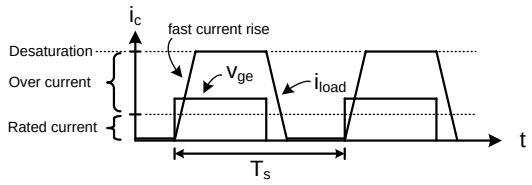


Figure 5.1: *Desaturation by fast fault with small inductance. Desaturation occurs immediately after short circuit.*

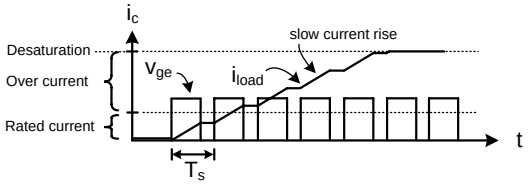


Figure 5.2: *Desaturation by slow fault with large inductance. Desaturation occurs after a sequence of switching periods.*

The two fault types are shown, for the three-level inverter topology, in figures 5.3 and 5.4, and described in more detail in appendix B.

To be able to design protection schemes, the fault mechanisms are analyzed in detail in section 5.1.

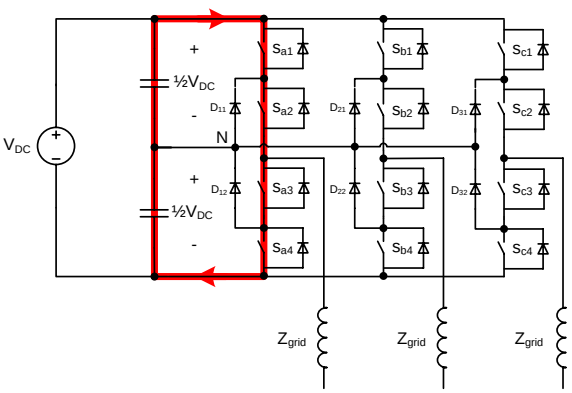


Figure 5.3: *Fast fault with shoot through in one phase leg. Characterized by very fast current rise.*

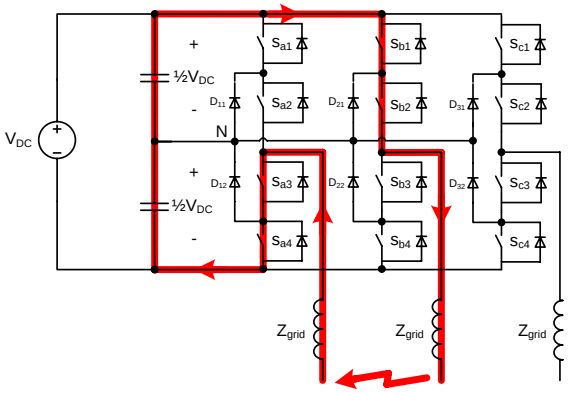


Figure 5.4: *Slow fault with phase to phase short circuit. Characterized by slow current rise.*

5.1 Fault mechanisms

The used Semikron SKM600GA176D IGBT is robust in short circuit situations. According to the data sheet, the rated current is $I_c = 600A@25°C$, and the short circuit current is limited by the IGBT to six times the rated current $I_{c,sc} = 3.6kA@v_{ge} = 20V$. This makes the IGBT a good choice in high power systems.

One way to analyze the IGBT under short circuit conditions, is to extend the graph from figure A.3 on page 155 to the one shown on figure 5.5. This figure shows, that the voltage will start to increase rapidly, if the current reaches high magnitudes for a given gate emitter voltage. This is known as desaturation of the IGBT device. The figure also shows the relationship between rated current range, the over current range and the desaturation level.

The desaturation current is highly dependent on the on v_{ge} as figure 5.5 shows. For a low v_{ge}, desaturation will occur for a low current and opposite.

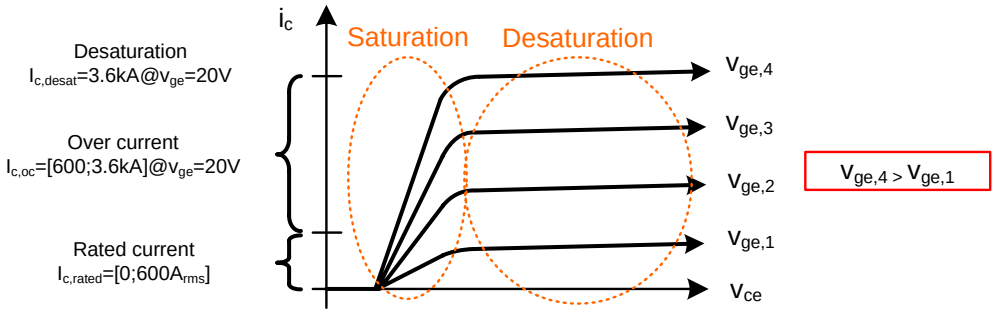


Figure 5.5: *i/v characteristic under fault conditions for the Semikron IGBT.*

Desaturation will subject the IGBT device, to a high short circuit current, if v_{ge} is high, at a high v_{ce}[1], resulting in power dissipations, that can reach the MW range. This power dissipation can not be handled by the device for more than a few μs, and at some point the internal temperature of the device exceeds $250°C$ [Rahul S. Chokhawala, April 1995] and the silicon becomes intrinsic, meaning that the doping disappears. At approximately $900°C$ the silicon breaks down, and this happens very quickly in desaturation.

The short circuit characteristic of a Toshiba MG100Q2YS40 IGBT is seen on figure 5.6. The figure shows, that desaturation occurs when the current is at maximum. If the short circuit is detected in time, steps can be taken to prevent device destruction. However, due to the stray inductance in an inverter circuit, over voltages can be generated if the IGBT is hard switched off. The over voltage can be described by the inductor terminal law that states:

[1] which in medium voltage level can be in the kV range

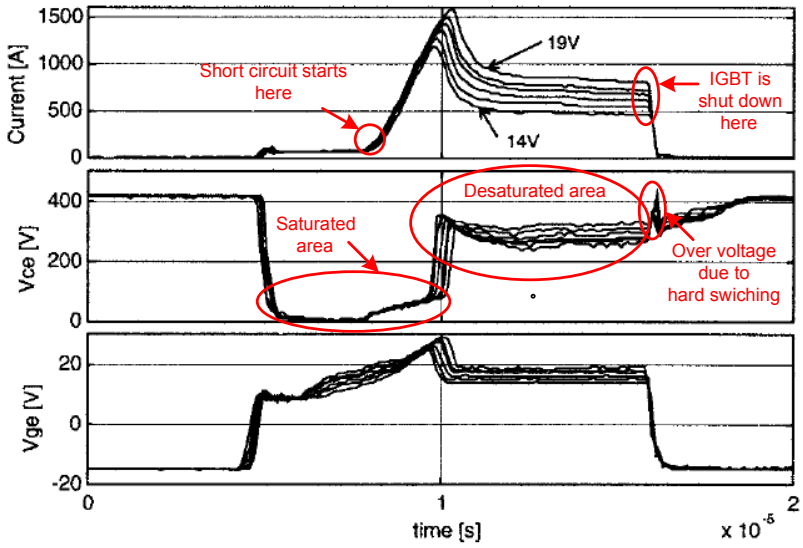


Figure 5.6: *Short circuit characteristic of a Toshiba MG100Q2YS40 IGBT rated* $1.2kV/100A$ *[Vinod john, April 1999].*

$$v = L \cdot \frac{di}{dt} \quad [V] \tag{5.1}$$

So even if the stray inductance L is in the nH range, the $\frac{di}{dt}$ part of the equation will generate an over voltage, that can destroy the device. Eventough the IGBT is robust in regards to high currents, it is very sensitive to over voltages. This means, that both an over voltage and an over current protection must be incorporated in a protection scheme, if hard swithing is used to turn the device off.

Another fault mechanism of great importance for the IGBT under fault conditions is the *latch up* phenomena. Latch up can occur at high currents, and results in the IGBT being unable to turn off. Latch up happens due to a parasitic thyristor across the collector emitter of the IGBT illustrated on figure 5.7. If this thyristor is turned on, the IGBT can no longer be turned off by the gate, and control over the device is lost.

As an extension to the circuit model from figure A.1 on page 154, the latch up is included on figure 5.8.

Here the latch up is modelled by the extra transistor T_1, which turns on when the current, and hence the voltage across the Body Region spread resistance R_s becomes high. If this transistor turns on, it is clear from figure 5.8, that the MOSFET controlling the gate is clamped, meaning that control over the IGBT is lost until the transistor turns off again due to external circumstances. In latch up, the IGBT can break down due to excessive power dissipation if not shut off.

To summarize, the fault mechanisms of the IGBT is the excessive power dissipation in the desaturation and latch up modes. Also the over voltage at hard switching from figure 5.6 needs to be taken into consideration, because the IGBT device is very sensitive to over voltages.

5.2 Fault detection

To prevent device break down because of a fault, it must be detected, and it must be detected fast. According to [Semikron, -], their devices have to be shut down within $t_{sd,max} = 10\mu s @ (v_{ce} = 1.2kV, v_{ge} = 20V)$ after the desaturation occurs to ensure the functionality of the IGBT module. Even though one IGBT used in this project is not expected be subjected to a collector emitter voltage of $1.2kV$, and the on state gate emitter

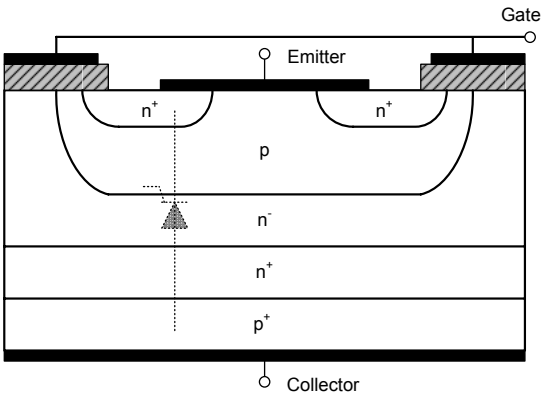


Figure 5.7: *Physical structure of IGBT (freely after [Ned Mohan, 2003]).*

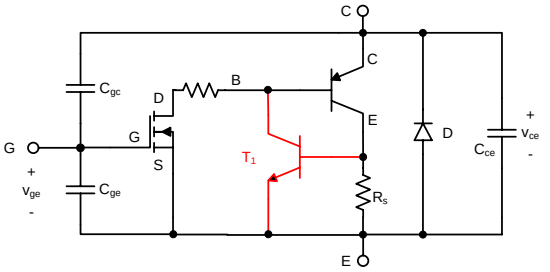


Figure 5.8: *Circuit model including latch up transistor T_1.*

voltage is $v_{ge,on} = 15V$ in stead of $20V$, the $10\mu s$ is used as maximum rating and as design guide. Because of the $v_{ge} = 15V$, the current will not reach $3600A$. In the following, three detection methods related to the fast and the slow faults will be analyzed.

5.2.1 Over current detection

The over current can be detected by simply monitoring the load current. This is due to the fact, that the over current situation is highly dependent on the line impedance.

5.2.2 Desaturation detection

A common way of detecting a short circuit is to monitor, when the device enters desaturation, meaning high v_{ce}, v_{ge} and i_c at the same time, as illustrated on figure 5.6. Measuring i_c directly is not always an option because of confined spaces, and therefore desaturation is commonly detected by high v_{ce} and v_{ge}. But only monitoring for high v_{ce} and v_{ge} at the same time is not enough. This is because of the switching scheme of the IGBT, explained in figure A.4 on page 156. Here it is seen, that v_{ge} rises before v_{ce} drops, and this could trigger an unintended desaturation error. However, the on and off times of the used IGBT are well defined, and this knowledge can be used to set op the following rule for the desaturation detection:

If v_{ce} and v_{ge} is high for longer time than t_{on}, then desaturation has occurred.

In practical applications, a safety margin can be added to t_{on} to minimize the risk of unintended fault detection.

When desaturation happens, the current, and the power dissipation in the device, has been high for a while, because of high conduction losses as seen on figure 5.6.

5.2.3 Error detection by monitoring emitter kelvin-emitter voltage

The Semikron power IGBT used for this project, has an additional small signal emitter terminal, intended for the gate emitter voltage v_{ge}. This is called the kelvin emitter terminal [Vinod john, April 1999].

This kelvin-emitter is physically connected to the real emitter on the silicon by a wire. The extra terminal is included to avoid the relatively low gate emitter voltage of being affected by voltage drop due to the impedance between the emitter on the silicon and the power emitter terminal. The impedance is denoted Z_{eke}, and a schematic view of this is shown on figure 5.9, and the Z_{eke} in the real IGBT is shown on figure 5.10.

The thesis behind the *error detection by emitter / kelvin emitter voltage* is, that if the collector current becomes high, then a voltage drop will occur across the emitter kelvin-emitter terminals, because of the impedance.

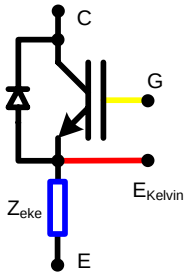


Figure 5.9: *Schematic view of the impedance Z_{eke} impedance.*

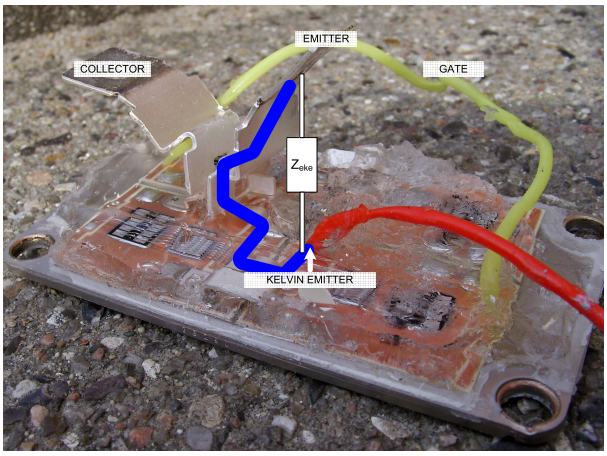


Figure 5.10: *Picture of the Semikron IGBT internal. Z_{eke} is shown by the blue line.*

To test this thesis, a measurement is set up, where similar graphs from figure 5.6 is sought for the Semikron SKM600GA176D together with the emitter kelvin-emitter voltage v_{eke}. The purpose of the test is, to analyze if any characteristics of the v_{eke} can be used to detect the short circuit before desaturation happens. The test report describing the fast short circuit test is found in appendix D.1 on page 170, and the results are shown on figure 5.11 and 5.12. The negative voltage spike in v_{eke} is due to the impedance in the red kelvin emitter wire from figure 5.9.

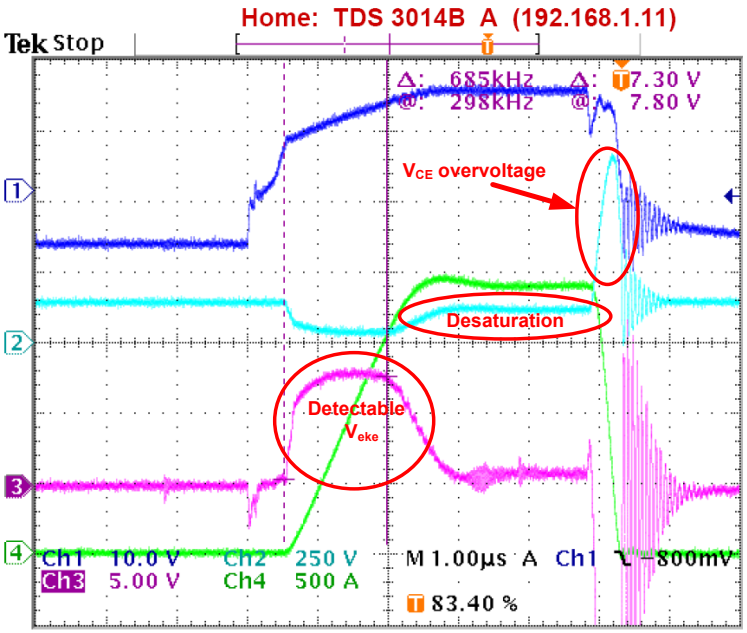


Figure 5.11: *Short circuit test for $V_{in} = 150V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_c.*

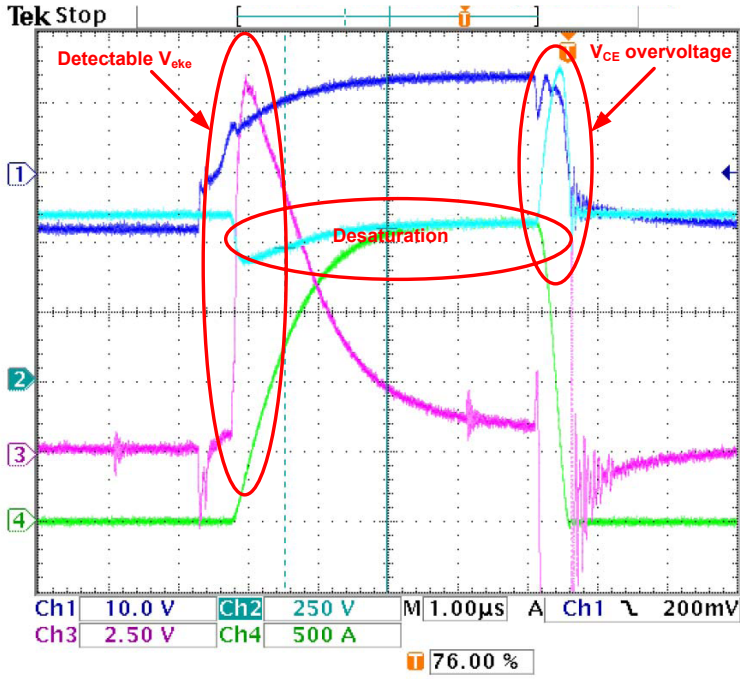


Figure 5.12: *Short circuit test for $V_{in} = 600V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_c. Notice that the offset for v_{ce} has changed. Also notice that the desaturation occurs immediately.*

The conclusion of the test is, that a *fast short circuit* can be detected by using the v_{eke}. In the $150V$ test, the measured voltage stays constant at $v_{eke} \approx 8V$ during the current rise. And in the $600V$ test, the same voltage peaks at $v_{eke} \approx 13V$.

Also, the over voltage due to hard switching can cause device destruction and needs to be taken into account in a protection scheme. The inductance and resistance of Z_{eke} is found to be $L_{eke} = 7.5nH$ and $R_{eke} = 277\mu\Omega$.

From the two tests shown in detail on figure 5.11 and 5.12, an important aspect can be identified;
For the $V_{in} = 150V$ test, v_{ce} reaches zero and then enters desaturation. This is the equivalent of having a short circuit occur while the IGBT is on. In this case, the v_{eke} method will be the fastest way of detecting the error by a margin of approximately $2\mu s$. For the $V_{in} = 600V$ test from figure 5.12, the desaturation is detectable almost immediately. This is the equivalent of turning the IGBT on, while a short circuit is present in the inverter.

These results show, that using both v_{eke} and desaturation detection at the same time to detect an error, will increase the effectiveness of the protection, due to the fact, that the fastest detector will trigger the error. If the IGBT short circuit during on state, the non zero v_{eke} will trigger the protection, and if the IGBT turns on into a short circuit, the error is detectable in both v_{eke} and v_{ce} at the same time. Also, choosing two detectors pr. IGBT, will add redundancy to the inverter protection scheme, meaning that a backup system is in place, in case of a defect in the detector. It must be mentioned, that the redundancy can only be guaranteed with a fast fault.

The v_{eke} test is only performed on a fast short circuit with marginal bus bar stray inductance. In this case, a clearly measurable voltage appears across Z_{eke}, because the current rise is fast. It is suggested, that an implementation of v_{eke} detection is based on integration of the waveform, rather than peak voltage detection due to the fact, that peak voltage detection is sensitive to noise. Because of time constrains, the corresponding slow fault test with large line inductance is not performed. It is expected, that the voltage v_{eke} will be hard to detect according to equation (5.1), because $\frac{di}{dt}$ will become smaller.

5.3 Break down prevention schemes

In the previous section, the consequences of a short circuit have been clarified. It was concluded, that the over voltage caused by hard switching the IGBT needed to be taken into account. Also it was critical, that the short circuit was brought to an end within $t_{sd,max} = 10\mu s$. To prevent the transient voltage, that occurs at a hard switched shut down, illustrated in the previous section, a soft shut down of the IGBT or clamping of the over voltage can be utilized. In the following, these break down prevention methods are analyzed and tested either by simulation or laboratory test.

5.3.1 Soft shut down

Soft shut down is performed, by slowing down the turn off of the IGBT. In the previous section, equation (5.1) stated that the transient voltage was dependent on the inductance and the $\frac{di}{dt}$, hence the rate of change of the current. The rate of change in i_c and the resulting over voltage in v_{ce} was deemed a damaging factor in a hard switched turn off of a short circuit. From the transfer characteristic of an IGBT shown on figure 5.5, it is seen that the gate voltage v_{ge} is a current limiting factor. This can also be verified by the tests of appendix D.1, where the tests are performed at the same v_{ge}. By slowing down the gate turn off time, it is in theory possible to limit the $\frac{di}{dt}$, and hence limit the transient v_{ce} voltage. As described in chapter A, the turn off time of an IGBT is decided by the discharge time for the gate capacitance dependent on the the gate resistance. According to appendix A.3, the Semikron SKM600GA176D turn off time is $t_{off} = 480ns$ at $R_g = 3\Omega$. To increase the turn off time, an additional resistor for soft shut down R_{SS} can be switched in between the gate and $v_{ge,off}$. To prevent, that the gate driver sinks the gate discharge current, the connection between the gate and the gate driver needs to be severed, because the Skyper 32 driver used in the project is low impedant in both on and off state. A simple implementation of the protection is shown in figure 5.13.

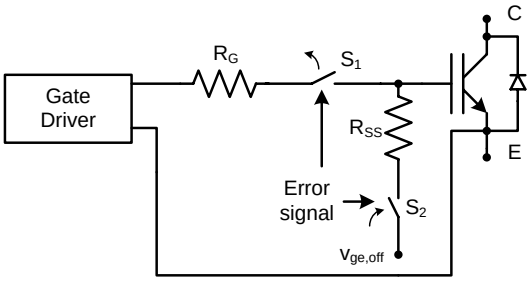


Figure 5.13: *Soft shut down implementation schematic.*

The error signal turns off the switch S_1 and turns on S_2 [2], and the gate capacitance is discharged through the soft shut down resistor R_{SS}. The value of R_{SS} can be estimated from the wanted soft shut down discharge time t_{SS} of the gate capacitance. As mentioned, Semikron states a maximum shut down time of $10\mu s$ after desaturation occurs. From this, the following demand can be set:

$$10\mu s \geq t_{SS} + t_{detect} + t_{delay} \tag{5.2}$$

where t_{delay} is covering S_2 and S_1 turn off time and propagation delays. These needs to be known. t_{SS} can be found from τ for the RC circuit consisting of the gate capacitance $C_{ge} = 70nF$ and R_{SS}. The threshold $v_{ge,th}$ for the IGBT is $5.8V$, but v_{ge} has the range $\Delta v_{ge} = [15V; (-7V)]$, and from this range, the $\Delta v_{ge,th} = 22 - (15 - 5.8) = 12.8V$. So the following discharge equation can be stated.

$$\Delta v_{ge,off,th} = \Delta v_{ge} \cdot e^{\frac{-t_{SS}}{\tau}} = \Delta v_{ge} \cdot e^{\frac{-t_{SS}}{R_{SS} \cdot C_{ge}}} \tag{5.3}$$

Under ideal circumstances, the maximum time is $t_{SS} = 10\mu s$, meaning that the error is detected before desaturation, and no propagation delay is in the system, and then $R_{SS,max}$ can be found from:

$$\Delta v_{ge,off-th} \quad = \quad \Delta v_{ge} \cdot e^{\frac{-t_{SS}}{R_{SS} \cdot C_{ge}}} \Rightarrow 12.8V = 22V \cdot e^{\frac{-10\mu s}{R_{SS,max} \cdot 70nF}} \Rightarrow \tag{5.4}$$

[2] S_1 needs to be a MOSFET due to voltage control, high speed and the need for bi-directional current.

$$R_{SS,max} = 263\Omega \tag{5.5}$$

To test, if the soft shut down method works properly, an OrCad simulation is used. The purpose of this test is, to repeat the short circuit test from the previous section, but with protection. The simulation schematic is shown on figure 5.14. The gate driver puts out a $10\mu s$ pulse, that turns on the IGBT. $5\mu s$ into this pulse, the error signal is triggered by the *error* pulse generators. The sequence is shown on figure 5.15. The added line impedance is used to simulate the non ideal laboratory setup.

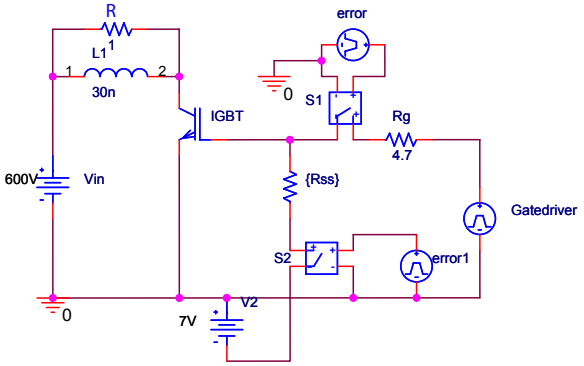


Figure 5.14: *Simulation schematic of soft shut down protection.* $R_{SS} = 4.7(Y)$,$15(\diamond)$, $50(\nabla)$, $75(\Delta)$, $100(*), 263(+)[\Omega]$ *used for parameter sweep analysis.*

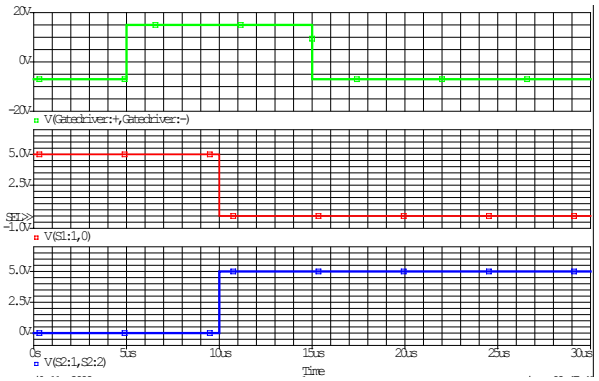


Figure 5.15: *Control signals for soft shut down simulation. From the top* v_{ge}, v_{error} *for* $S1$ *and* v_{error} *for* $S2$.

The results of the simulation are shown on figure 5.16.

The simulation is also here performed by using the *Mitsubishi CM400HA-34H* IGBT Pspice model used in the previous chapters of the rapport. From figure 5.16 it can be seen, that the soft shut down works. The first value of $R_{SS} = 4.7\Omega(Y)$ is the same as the gate resistor in the test from last section on figure 5.12. It can also be seen, that the over voltage at $R_{SS} = 4.7\Omega(Y)$ reaches approximately the same value in the simulation, as it did in the short circuit test from the laboratory, which verify that the simulation results and the lab results are comparable. Figure 5.16 shows, that the over voltage can be controlled by the gate discharge time. It can also be seen, that the calculated maximum value for $R_{SS} = 263(+)[\Omega]$ turns of the IGBT within the $10\mu s$, because the gate voltage reaches its threshold voltage. The transient over voltage at this value of R_{SS} is measured to $624V$, which is within safety limits. At $R_{SS} = 50\Omega(\nabla)$, the IGBT is turned of after $4\mu s$, and the over voltage reaches $746V$, which is still very acceptable, but much faster. So to determine the optimal for R_{SS} for the three-level inverter system, all the propagation delays in the system and also the stray inductance of the inverter needs to be taken in to account, but the method can be used to safely shut down the IGBT within the time frame and prevent the destructive over voltage associated with hard switching.

5.3.2 Voltage clamping

Another method of preventing the transient over voltage from the hard switching is, to clamp the voltage at a reasonable level. This method is very simple, and does not require active components, such as the transistors used for the soft shut down method. An even bigger benefit of this method, if it works, is that the *zener clamping method* for the voltage sharing of the series IGBTs, described in section 4.2.8 from page 61, can be used for the break down prevention as well. The implementation of the method is shown on figure 5.17.

It is expected, that the clamping method will eliminate the over voltage from the hard switching, therefore the gate driver needs to receive the error signal when a short circuit is detected, and after that, shut down the IGBT.

To test the method, the short circuit test from the previous section is repeated, but with added protection. The clamping voltage level is set to $V_{clamp} = 800V$. The tests are performed in appendix D.2. The

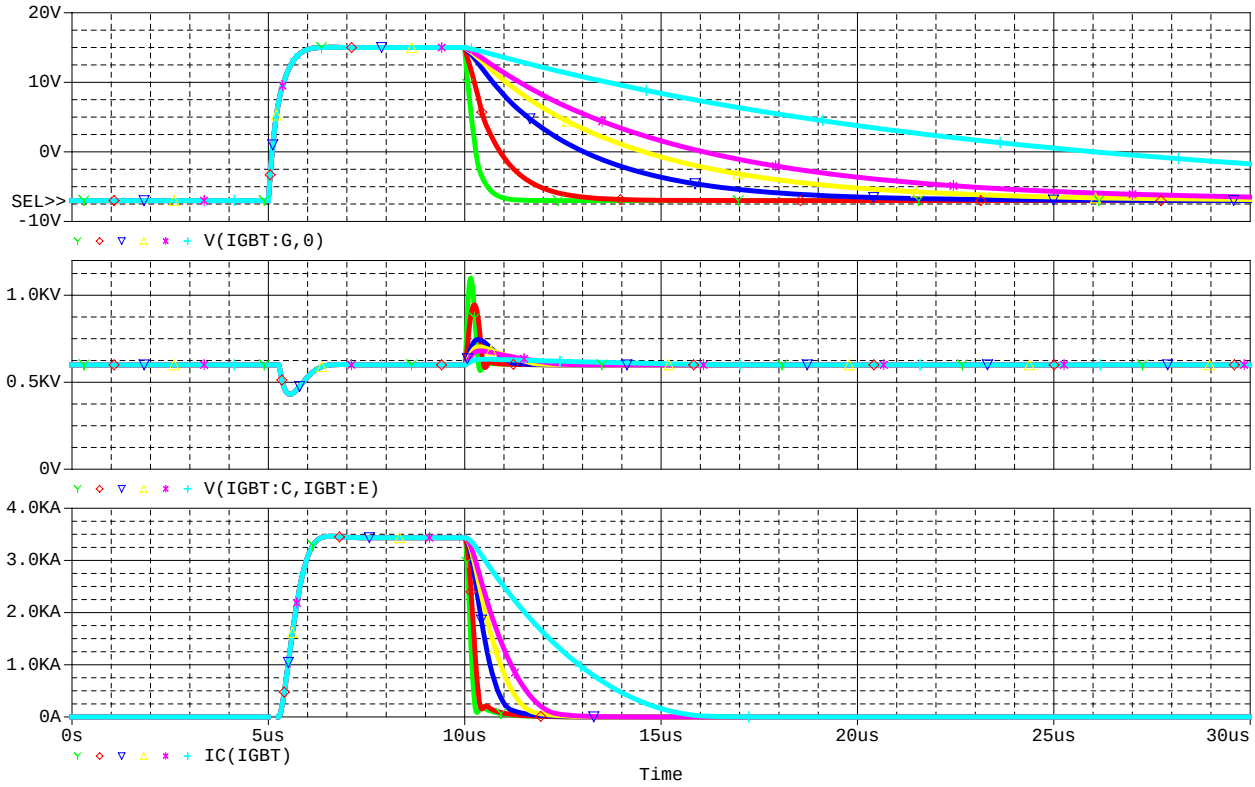


Figure 5.16: *Simulation results of soft shut down protection.* R_{SS}=4.7(Y) ,15($\diamond$), 50(∇), 75(Δ), 100($*$), 263($+$)[Ω] *used for parameter sweep analysis. From the top:* v_{ge}, v_{ce} *and* i_c.

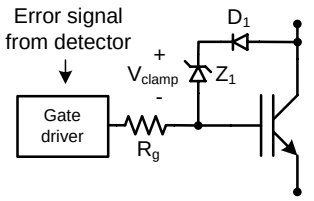


Figure 5.17: *Schematic of break down protection by voltage clamping. The error signal is received from the error detector.*

result of the tests is shown on figure 5.18 and 5.19.

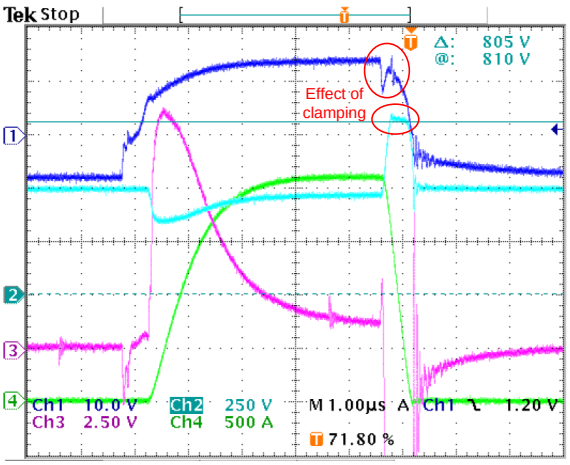


Figure 5.18: *Short circuit test with added clamping protection for $V_{in} = 500V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke} and green = i_c.*

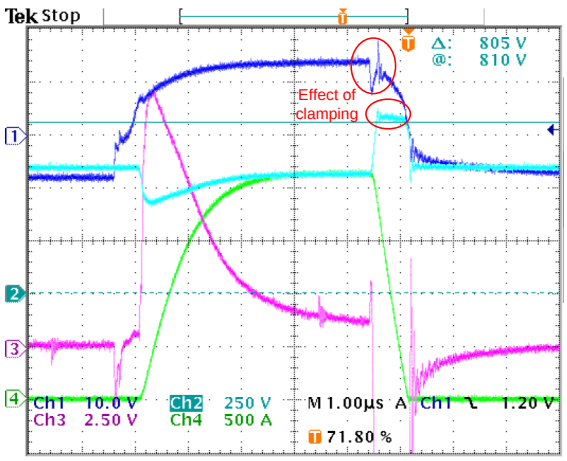


Figure 5.19: *Short circuit test with added clamping protection for $V_{in} = 600V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke} and green = i_c.*

The conclusion of the test is, that the clamping protection works satisfactory by eliminating the damaging over voltage in v_{ce}. By using this method, there is no need to perform a soft shut down of the IGBT, so the turn off time is faster compared to the soft shut down method. The clamping method also has the advantage, that no active shut down hardware is needed in the gate driver, as would be the case for the soft shut down method. The shut down of the IGBT is thereby only performed by the gate driver, which is required to have feature specifically for this purpose.

5.3.3 Evaluation on break down prevention schemes

In this section, two break down prevention schemes were analyzed. The two schemes was *Soft shut down* and *Voltage clamping*. The goal of the prevention schemes was to safely and fast shut down an IGBT under short circuit, avoiding the over voltage in the v_{ce} shown in the previous section. From simulation and test of the two methods, it was concluded that both methods work properly. When compared, the clamping scheme shows some advantages in the form of simplicity. This scheme does not need the active hardware required by the soft shut down method. Also the clamping protection circuit does double duty as snubber, hence minimizing the utilized hardware pr. gate driver.
A subject that has not been mentioned in the break down prevention is the latch-up phenomena. The analyzed fault prevention schemes will not work in a latch up situation. However, the Semikron SKM600GA176D is a trench gate IGBT, and this technology prevents the latch up to some extent [Semikron, -].

5.4 Conclusion

The goal of this chapter was, to identify the fault mechanisms of the IGBT, and analyze methods to detect and prevent short circuits and over voltages. The main fault mechanisms was desaturation, which results in high power dissipation; latch-up which results in loss of control over the IGBT; and over voltage, which causes isolation break down and device destruction.

It was stated, that to protect the IGBT, a fault must be detected and the device shut down in less than $10\mu s$ in worst case. By analyzing two ways of detection, either by desaturation or by emitter / kelvin emitter, and performing short circuit tests at different voltage levels, it was concluded, that a combination of the two detection methods would be the best choice under the circumstances in the tests. The short circuit test's also

showed a clear need for over voltage protection, as a hard switched turn off resulted in large voltage transients.

The v_{eke} detection method is not tested in a slow short circuit situation with significant line impedance. Because the inductance of Z_{eke} is known, the minimum current slope required for a detectable v_{eke} can be determined from knowledge about background noise voltage level. This is not done in this report due to time constrains.

Using the knowledge gained through testing, two fault prevention schemes were proposed. One included a soft shut down sequence of the IGBT, by ramping the gate voltage and preventing hard switching and thereby the over voltage. The other simply clamped the over voltage associated with the hard switching. After simulation and test of the two prevention schemes, it was concluded, that the simple clamping protection, which also does double duty as snubber, could be used with satisfactory results. The soft shut down scheme also proved effective, but required more hardware.

Based in this, the desaturation detection method using hard switch off and the zener clamped over voltage protection is chosen for the realization.

Chapter 6

Problem formulation

In the problem analysis in part I of the report, the following subjects was analyzed:

- The three-level inverter topology.
- Series connection of IGBTs.
- Voltage balancing methods and snubber topologies.
- IGBTs under fault conditions.

In the following, the results and conclusions of the different analysis are summarized.

6.0.0.1 Three-level inverter

The goal of the analysis of the three-level inverter was, to investigate if the topology is well suited for medium voltage applications, and also to make a comparison to the simple and commonly used two-level topology. The conclusion of the analysis was that the three-level inverter is superior to its two-level counterpart in terms of required blocking voltage pr. IGBT device. Also, the THD of the output was half of that from a two-level inverter, because the three-level inverter puts out more voltage levels. The analysis also showed, that disadvantages of the thee-level inverter were issues about neutral point balancing, more devices and unequal loss distribution. The voltage rating advantage of the three-level inverter makes the topology well suited for medium voltage applications.

6.0.0.2 Series connection of IGBTs

The purpose of analyzing series connection of IGBTs was, to obtain medium voltage level capability using standard IGBT's. The analysis showed that connecting two devices in series can affect the voltage sharing of the devices. It was shown, that changes in internal parameters and timing difference in the gate signal produced the unequal voltage sharing, and that the unequal voltage sharing had to be avoided. A very positive result of the analysis was that two standard IGBT's in series has lower losses compared to one double rated device if the frequency reaches above a few hundred Hz. The reason for this result is, that the internal capacitance of the IGBT does not follow the voltage rating of the device linearly. This result means that two IGBT's in series can be operated at a higher switching frequency than one IGBT of higher voltage rating for a given loss. Finally it was concluded, that series connection IGBT's has the same overall probability of failing, as paralleling IGBT's for the same power rating.

6.0.0.3 Voltage balancing methods and snubber topologies

This analysis has it's origin in the chapter about series connection of IGBTs, where it was stated, that an equal voltage sharing between the semiconductors was needed. The voltage balancing is obtained through the utilization of snubbers, and through state of the art analysis on snubber topology, three topologies was selected for further analysis and comparison. These were the *Active gate topology*, the *Passive snubber* and

the *Zener clamped snubber*. These methods were evaluated from their power loss, dynamic performance and ability to be used together with sinusoidal PWM. From simulations, the zener clamped snubber was chosen as the best choice for the project.

6.0.0.4 IGBTs under fault conditions

The analysis of the IGBT module under fault conditions was done, to gain knowledge about the fault mechanisms of the IGBT, and also test fault prevention schemes. The analysis of the fault mechanisms showed, that the large power dissipation associated with desaturation, and the over voltage associated with hard shut down can be fatal to the IGBT. To test how the chosen Semikron IGBT reacted to a short circuit, short circuit test's was performed. From the results of these test's, two fault detection schemes was analyzed; standard *desaturation detection* and *emitter-kelvin emitter voltage detection*. It was concluded that a mix of the two schemes was the optimal solution. Also, two fault prevention schemes was analyzed; $soft\ shutdown$ and *voltage clamping*. It was concluded by simulation and test, that both methods works, but clamping is the simplest one.

From the analysis, the following problem formulation can be stated:

How to design and realize a three-level inverter rated for medium voltage level, based on series connected IGBTs, and protected against fast and slow fault conditions?

6.1 Requirements

The specific requirements for the system are summarized here for convenience.

- DC link voltage $V_{DC} = 2.4kV \pm 10\%$.
- Peak load current $\widehat{i}_{load} = \pm 200A$ but dependent on load.
- Switching frequency $f_{sw} = 5kHz$.
- Modulation frequency $f_{mod} = 50Hz$.
- Protection maximum shut down time $t_{SD,max} \leq 10\mu s$ from fault occurs.
- Allowed over voltage due to hard switching $v_{ce,max} = 700V$.
- Maximum voltage deviation between series IGBTs $\Delta V_{ce,max} = 200V$.
- Third harmonic injection is to be incorporated in the modulation design.

6.2 Problem Boundaries

Due to time constrains, a set of boundaries for the project are listed below.

- All issues about neutral point balancing are omitted.
- Only two inverter phase legs are designed.

Part II:
System Design

Chapter 7

Implementation Model

This chapter describes the implementation model realized for the project. In order to apply with the specifications, and a due to time limitations, it has been chosen to only realize two legs of the inverter. The realized setup schematic is shown on figure 7.1.

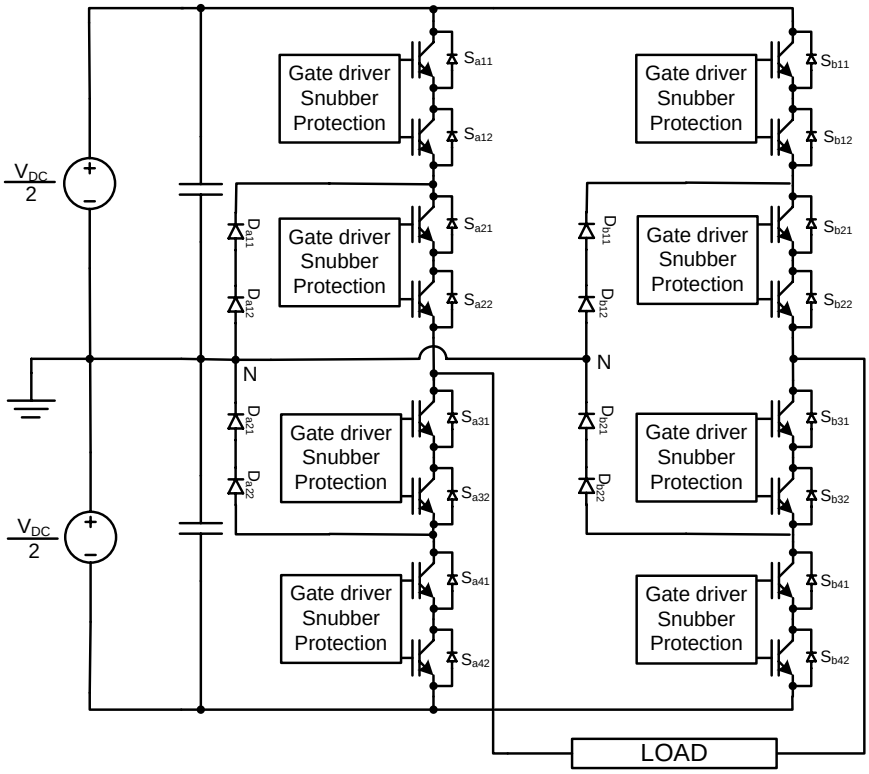


Figure 7.1: *Realized three-level inverter setup.*

Apart from the 16 Semikron SKM600GA176 IGBTs, the setup consists of:

- Medium voltage DC power supply
- DC link capacitors
- High power load
- DSP board

- Gate drivers
- Snubbers for IGBTs and diodes
- Fault detection and protection

For the neutral point diodes, the reverse diode in the Semikron IGBT is used [1], meaning that the total number of IGBTs is 24. In the following sections, each of the bullet points from above will be dimensioned and realized.

7.1 Medium voltage DC power supply

To power the inverter setup, a medium voltage DC supply is needed. Such equipment is not available at the Institute of Energy Technology, so it needs to be designed and build. The demands for the supply are as follows:

- Variable output voltage. This is important to initially test the inverter at low voltages.
- Capable of producing a DC link voltage of $V_{DC} = 2.4kV$.
- Capable of sourcing the current needed for the power dissipation for the load and the inverter. This demand can first be verified in the final test.

It is chosen to realize the power supply by the setup shown in figure 7.2.

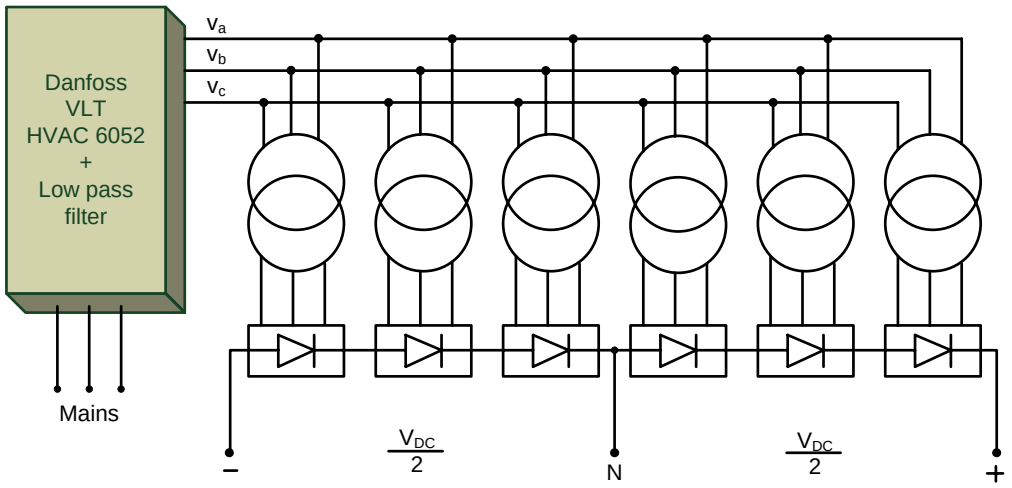


Figure 7.2: *Medium voltage DC supply schematic.*

The details about the design, realization and test of the DC supply can be seen in appendix D.3 on page 180. Also in this appendix, photos of the realized DC supply are found.

The relationship between the adjustable phase to phase output voltage V_{ab} of the VLT and V_{DC} is as follows:

$$V_{DC} = 6 \cdot 1.35 \cdot V_{ab} = \frac{81}{10} \cdot V_{ab} \quad [V] \tag{7.1}$$

For the medium voltage level of $V_{DC} = 2.4kV$, the output voltage for the VLT must be:

$$V_{ab} = \frac{2.4kV \cdot 10}{81} = 296V \tag{7.2}$$

The test performed in appendix D.3 verifies equation (7.2).

[1] This is obtained by short circuiting the gate emitter, hence the IGBT is always off.

7.2 High power Load

The reason not to choose a resistive load is, that the physical size of this load, and the power dissipation, makes it very hard to realize. The power dissipation of a resistive load can be calculated as:

$$P_{res} = V_{out} \cdot I_{out} = \widehat{v}_{out} \cdot \sqrt{D} \cdot \widehat{i}_{out} \cdot \sqrt{D} = \widehat{i}_{out} \cdot \widehat{i}_{out} \cdot D \tag{7.3}$$

because both voltage and current wave forms are square. As an example, a duty cycle D of 50% results in the power dissipation of a resistor connected phase to phase to become:

$$P_{res} = 2.4kV \cdot 200A \cdot 0.5 = 240kW \tag{7.4}$$

This will dissipate a large amount of heat, and also this power need to be supplied into the inverter, setting large requirements on cables and the power source itself.

Instead, the load can be chosen inductive. This in practice means, that the reactive power stored in the inverter will be shifted back and forward between the load inductor and the neutral point capacitors. The only active power needed for this setup is the conduction losses, and hence the amount of power needed from the power supply is much less than in the resistive case. This means, that the three-level inverter can be tested at rated voltage and current values. The apparent power S can is given by:

$$S = P + jQ = I_{load}^2 \cdot R + jI_{load}^2 \cdot X, \quad X = L \cdot 2\pi \cdot f \quad [VA] \tag{7.5}$$

So by having a large reactance X and a small resistance R, the inverter setup of figure 7.1 stores more energy than it dissipates. The load current i_{load} will take the form of the integrated voltage waveform. This can be seen by rearranging the inductor terminal law:

$$v_{out} = \frac{di_{load}}{dt} \cdot L \quad \Rightarrow \quad i_{load} = \frac{1}{L} \cdot \int v_{out}\, dt \quad [A] \tag{7.6}$$

This shows, that if the voltage consists of sinusoidal PWM, the current will be sinusoidal, but shifted 90°. The inductance depends on the switching frequency for a given current and voltage:

$$X = \frac{v_{out}}{i_{load}} \quad \Rightarrow \quad L = \frac{v_{out}}{i_{load} \cdot 2 \cdot \pi \cdot f_{mod}} \quad [H] \tag{7.7}$$

In the project, it is chosen to have a $f_{mod} = 50Hz$, because this corresponds to the danish grid frequency.

The phase to phase voltage v_{ab} by sinusoidal modulation becomes:

$$v_{ab,1} = v_{an,1} - v_{bn,1} \tag{7.8}$$

where $v_{an,1}$ and $v_{bn,1}$ is found from equation (2.37) on page 12, which stated that:

$$v_{aN,1} = Ma \cdot \frac{V_{DC}}{2} \cdot sin(\theta) \tag{7.9}$$

From this, the following equation can be stated:

$$v_{ab,1} = v_{an,1} - v_{bn,1} = Ma \cdot \frac{V_{DC}}{2} \cdot sin(\theta) - Ma \cdot \frac{V_{DC}}{2} \cdot sin\left(\theta + \frac{2\pi}{3}\right) \tag{7.10}$$

$$v_{ab,1} = Ma \cdot \frac{V_{DC}}{2} \cdot \sqrt{3} \cdot sin\left(\theta + \frac{\pi}{6}\right) \tag{7.11}$$

Since the inductor is connected phase to phase according to figure 7.1 on page 82, equation (7.7) can be re-written to:

$$L = \frac{v_{ab,1}}{i_{load} \cdot 2 \cdot \pi \cdot f_{mod}} = \frac{Ma \cdot \frac{V_{DC}}{2} \cdot \sqrt{3} \cdot sin\left(\theta + \frac{\pi}{6}\right)}{i_{load} \cdot 2 \cdot \pi \cdot f_{mod}} \quad [H] \tag{7.12}$$

Which gives an inductance of $L = 28.5mH$ at $Ma = 1.16$ and $\frac{V_{DC}}{2} = 1.2kV$ for the desired output current and DC link voltage values. Pure inductors do not exist, and therefore the series resistance of the windings must be taken into account in the design of the inductor.

7.2.1 Load inductor realization

The inductor must be realize it by applying a core, ore else the number of windings, and hence the wire consumption becomes excessive. Also, the windings have to be able to coop with the current. The RMS value of the maximum load current is $I_{load} = 141A$, and a general rule is, that the current density of the windings does not surpass $5A/mm^2$. This rule originates in motor design, and the reason for the $5A/mm^2$ is due to the heat dissipation issues regarding the isolation of the wires. The cross sectional area of the wire needs to be $A_{wire} = \frac{141A}{5A/mm^2} \geq 28.2mm^2$. Another aspect of the wire is the skin effect and the resulting skin depth δ, which is a measure for the utilization of the wire, and describes the dept where 63% of the current is flowing in the wire. δ is given as:

$$\delta = \sqrt{\frac{\rho}{\pi \cdot \mu \cdot f_{mod}}} \quad [m] \tag{7.13}$$

where ρ is the resistivity of the material. Using the resistivity of copper; $\rho_{Cu}@100°C$ and knowing that $\mu = \mu_0$ for Cu, equation (7.14) can be simplified to [Robert W. Erickson, 2001]:

$$\delta = \frac{75}{\sqrt{f_{mod}}} = \frac{75}{\sqrt{50}} = 10.6mm \tag{7.14}$$

So at $50Hz$, the wire will have a good utilization up to a radius of $10.6mm$ which result in a wire area of $705mm^2$, and this is way more than needed, so the wire utilization at $50Hz$ is not compromised by the skin effect.

The realized load inductor L_{load} consist of six iron core inductors from APC[2] in series, and each of these inductors consist of two sets of windings. Each of these sets consists of a high current and a low current winding. This setup is shown on figure 7.3. The reason for using this setup is, that the core inductors are available at the Institute of Energy Technology at AAU.

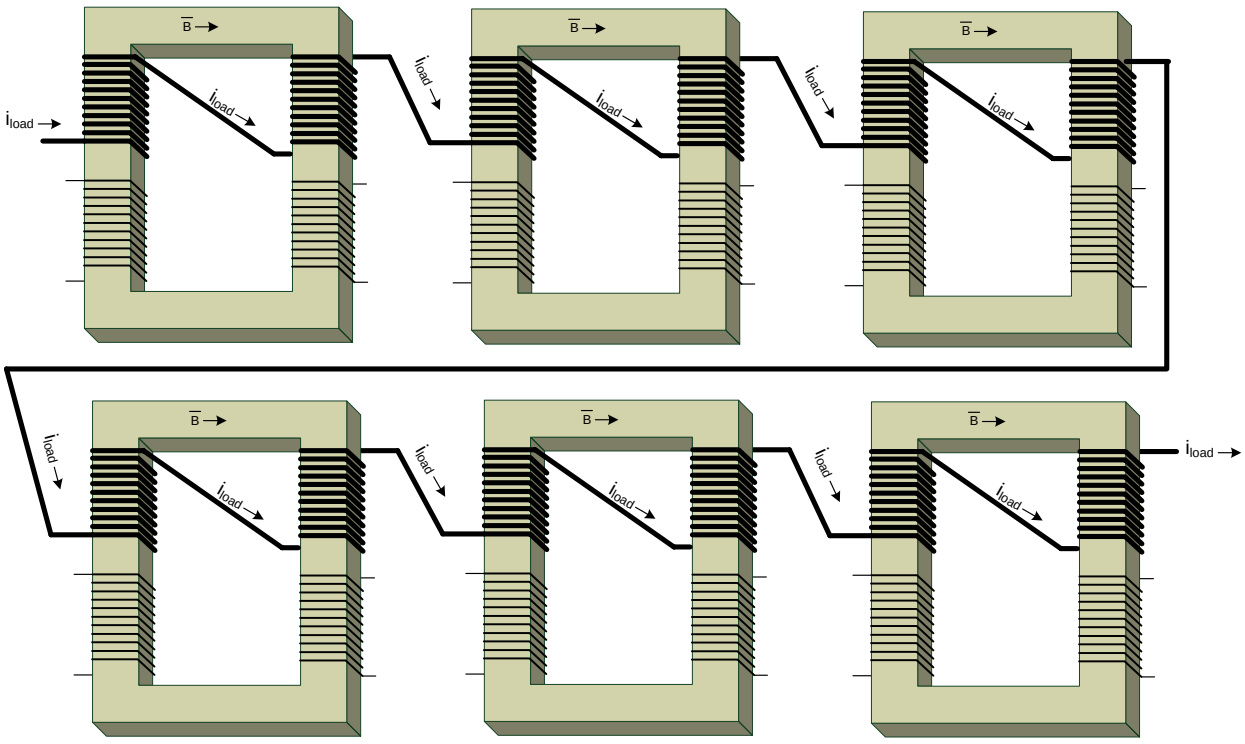


Figure 7.3: *Realized load inductor layout.*

[2]American Power Converter Corp.

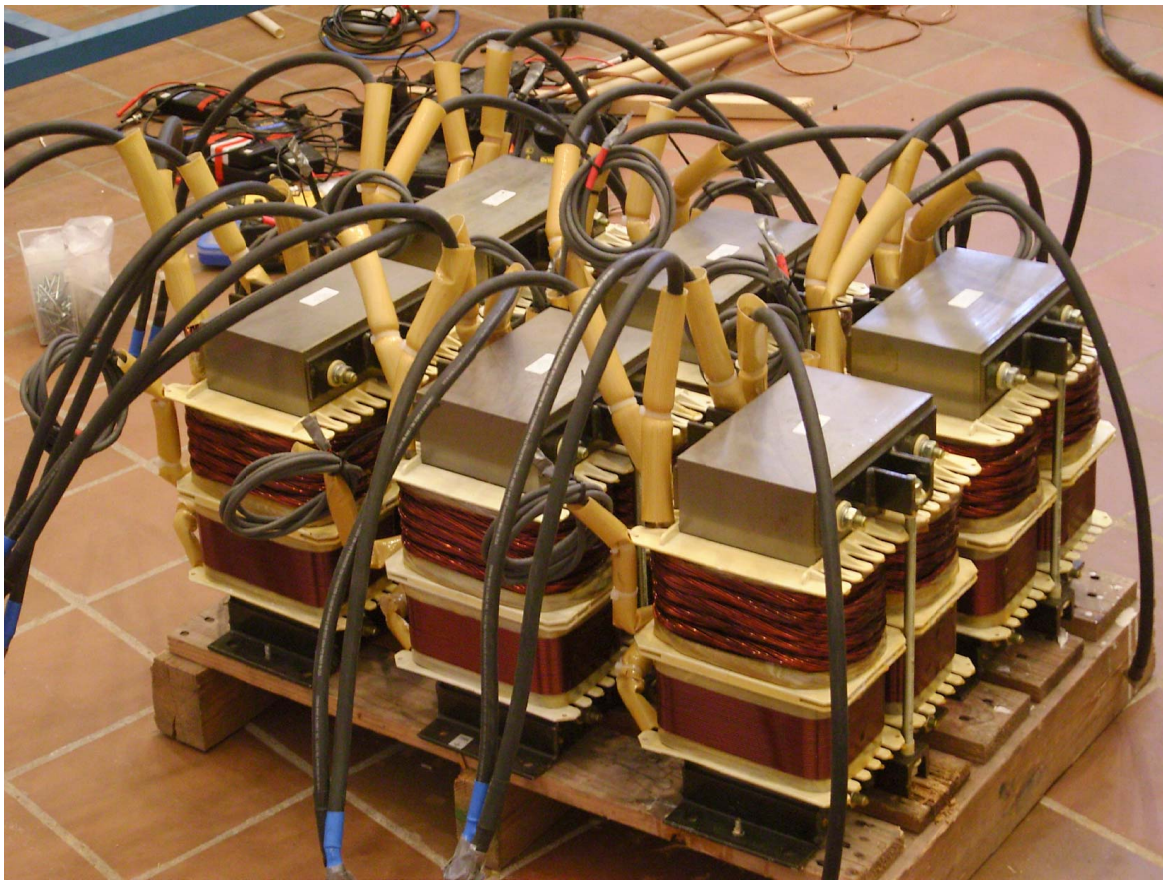


Figure 7.4: *Realized load inductor.*

To realize the load inductance, all the low current windings are disconnected, and the high current windings are series connected, meaning two sets of windings in series pr. core. This means that the inductance is quadrupled by adding twice the windings to the same core, as can be seen from the following equation:

$$L = \frac{n^2}{\Re} \quad [H] \tag{7.15}$$

The realized inductor setup is shown on figure 7.4.

The load inductor is tested in appendix D.4 on page 186. With all six inductors, the inductance is measured to:

$$L = 103mH \tag{7.16}$$

And the total DC resistance is:

$$R_{DC} = 87.6m\Omega \tag{7.17}$$

This is much more than needed, but the inductance can be variated in steps, by disconnecting some of the inductors, to reach the wanted current level. This is an advantage, because the inverter setup can be tested initially at lower current.

An important aspect of using cores in the inductors is saturation. Saturation occurs when no more energy can be stored in the magnetic field of the inductor. Saturation causes the current to rise, and hard saturation is comparable with a short circuit. To calculate the maximum allowed current, the following equation can be used:

$$N \cdot I_{sat} = \phi \cdot \Re \quad \Rightarrow \quad I_{sat} = \frac{\phi \cdot \Re}{N} = \frac{B_{sat} \cdot A_{core} \cdot \Re}{N} \quad [A] \tag{7.18}$$

From the APC data sheet of the inductor, the following data is obtained:

- The core area $A_{core} = 0.00931m^2$.
- The core mean length $l_{core} = 0.844m$.
- Air gap length $l_{gap} = 0.6mm$
- N = 30.

B_{sat} for sheet iron is approximately $1.3T$ [Metals, 2006] and the permeability is $\mu_{iron} = 5000$. The reluctance of the core can be calculated as:

$$\Re = \Re_{core} + \Re_{gap} = \frac{l_{core}}{\mu_{iron} \cdot \mu_0 \cdot A_{core}} + \frac{l_{gap}}{\mu_0 \cdot A_{gap} \cdot 1.2} = 14.4k + 42.7k = 56.6k \quad \left[\frac{A \cdot turns}{Weber}\right] \tag{7.19}$$

The 1.2 factor is used to compensate for the fringing in the air gap.

So the saturation limit I_{sat} for the used cores is:

$$I_{sat} = \frac{1.3T \cdot 0.00931m^2 \cdot 56.6k\frac{A \cdot turns}{Weber}}{30} = 22.8A \tag{7.20}$$

This result means that the cores used are not sufficient. On figure 7.5 and 7.6, the saturation becomes clear, and this verifies equiation (7.20).

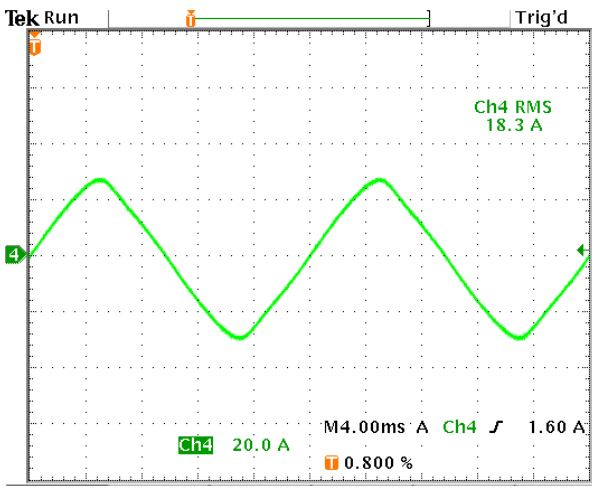


Figure 7.5: *Measured current for one inductor. Notice, that the waveform becomes quasi triangular because it is near saturation.*

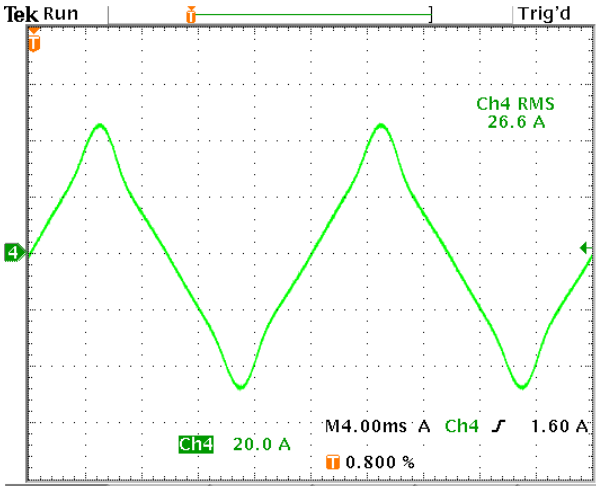


Figure 7.6: *Measured current for one inductor. Notice the saturation at the top of the sinusoidal curve, causing the current to rise.*

To compensate for the small cores, the demands for the project have to be revised. The demand of the load current of $\widehat{i}_{load} = \pm 200A$ can not be obtained by means of the used inductors. However, the six cores can be modified to include a larger air gap. This will, according to equation (7.20) increase the saturation current. However, this will also decrease the inductance according to equation (7.15). The reason for having a large inductance in the first place was, to be able to modulate a $50Hz$ sinusoidal current. By increasing the modulation frequency, the impedance can be raised while the inductance stays constant. This means, that by raising both the modulation frequency, and adding a larger air gab, the load inductor can be redesigned to handle a larger current without going into saturation. The inductance as function of the air gap length can be found by:

$$L(l_{gap}) = \frac{N^2}{\Re_{core} + \Re_{gap}} = \frac{N^2}{\Re_{core} + \frac{l_{gap}}{\mu_0 \cdot A_{core} \cdot 1.2}} \quad [H] \tag{7.21}$$

A plot of this function is shown on figure 7.7. From equation (7.21) the impedance as function of l_{gab} can be found as $R_{DC} + jX(l_{gab}) = R_{DC} + jL(l_{gap}) \cdot 2\pi \cdot f_{mod}$, where $R_{DC} = 87.6m\Omega$. The length of the impedance $|Z|$ is plotted for four different modulation frequencies on figure 7.8. The reason for choosing the maximum modulation frequency to $f_{mod} = 200$ is to avoid base band distortion [Ned Mohan, 2003] at $f_{sw} = 5kHz$.

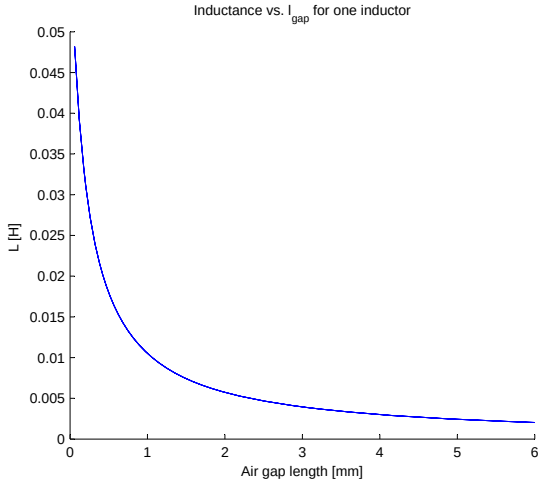


Figure 7.7: *Inductance for one inductor as function of l_{gap}.*

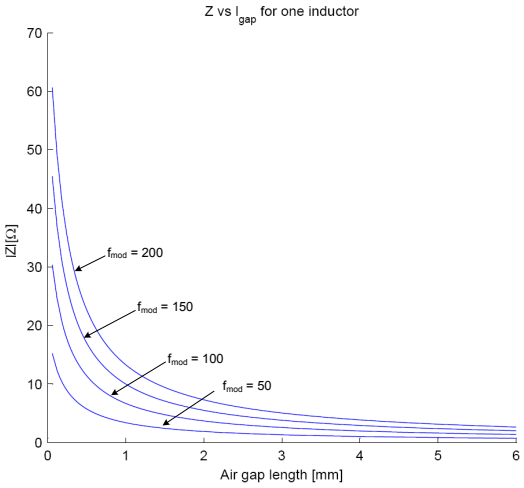


Figure 7.8: *Impedance $|Z|$ for one inductor as function of l_{gap} plotted for $f_{mod} = 50, 100, 150, 200Hz$. The largest frequency gives the largest impedance.*

From figure 7.8, it can be seen, that for $f_{mod} = 200Hz$, the air gap can be much longer for the same impedance than at $50Hz$. Knowing the dependency of l_{gap} on Z, the saturation current I_{sat}, which is frequency independent, then the load current i_{load} given by:

$$i_{load} = \frac{v_{ab,1}}{6 \cdot |Z_{load}|} = \frac{v_{ab,1}}{\sqrt{(2 \cdot \pi \cdot f_{mod} \cdot L(l_{gap})^2 + R_{DC}^2) \cdot 6}} \quad [A] \tag{7.22}$$

can be plotted as function of l_{gap} for the four different frequencies. Z_{load} is $6 \cdot Z$ because all six inductors are used in series in the realized load, and $v_{ab} = 2.4kV$ due to $Ma = 1.16$. i_{load} and I_{sat} are plotted on figure 7.9.

The results from figure 7.9 shows, that by increasing f_{mod} to $200Hz$, the load current stays below the saturation limit. Also, the impedance can be changed by adjusting the air gab length, meaning that the load current of $\widehat{i}_{load} = 200A$ can still be archived. However, based on initial test's of the setup, the demands for the current is changed to $\widehat{i}_{load} = \pm 100A$. This is due to excessive power dissipation of the DC link capacitors designed in section 7.3.

By increasing l_{gap} from $0.6mm$ to $3.8mm$ in all the inductors, a load current of $\widehat{i}_{load} = \pm 100A$ is obtained according to figure 7.9. At this air gap length, the inductance is calculated from equation (7.21) to $L_{load} = 6 \cdot 3.22mH = 19.3mH$. After adding air gab length to all six cores, the inductance is measured in the same way as previous in the section, using the same equipment and setup as in appendix D.4. The test results are shown in table 7.1, and the DC resistance from the previous measurement is used again.

The average value of $|Z|$ is $|Z|_{avg} = 7.3\Omega$, and hence:

$$L = \frac{\sqrt{|Z|_{avg}^2 - R_{DC}^2}}{2 \cdot \pi \cdot 50Hz} \quad [H] \tag{7.23}$$

$$L = \frac{\sqrt{7.3^2 - 0.086^2}}{2 \cdot \pi \cdot 50Hz} = 23mH \tag{7.24}$$

This means, that the air gab is a little shorter than expected, but the redesigned core is accepted and used.

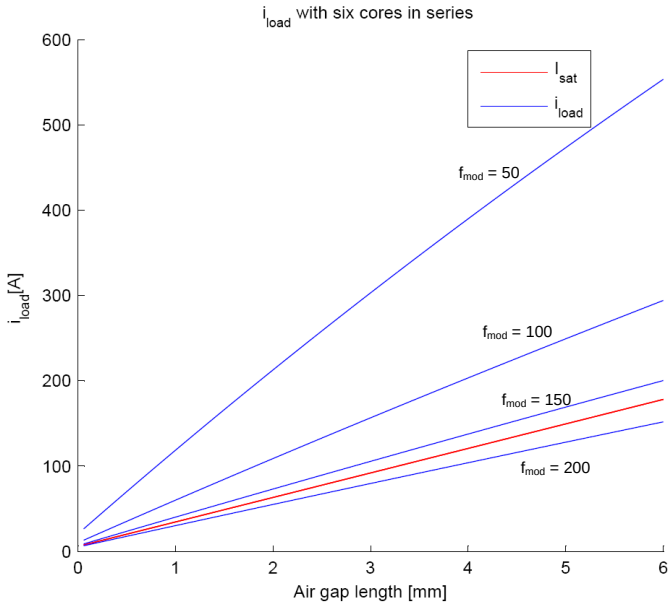


Figure 7.9: *i_{load} and I_{sat} plotted as function of l_{gap} for $f_{mod} = 50, 100, 150, 200Hz$ and $v_{ab} = 2.4kV$.*

V $[V]$	**I** $[A]$	$\|\mathbf{Z}\|$ $[\Omega]$
43.9	6.08	7.22
52.4	7.19	7.28
58.5	8.0	7.31
68.6	9.24	7.42

Table 7.1: *Impedance measurements at $f = 50Hz$ on revised cores.*

7.2.2 Conclusion on inductive load

In this section, the load for the inverter setup has been analyzed. It was chosen to use an inductive load, because the inverter would store energy rather than dissipate it. The load was realized using six large APC iron core inductors. The total inductance was measured to $L_{load} = 0.1H$. After testing, it was concluded that the iron cores would saturate at $\widehat{i}_{load} = \pm 22.8A$ which was only a fraction the specified load current. By increasing the modulation frequency to $f_{mod} = 200Hz$, and add length to the air gap of the cores, it was possible to rate the setup for a load current of $\widehat{i}_{load} = \pm 200A$. However, this load current will cause large power dissipation in the DC link capacitors, and therefore the load current is lowered to $\widehat{i}_{load} = \pm 100A$. So for the rest of the report:

- $f_{mod} = 200Hz$
- $\widehat{i}_{load} = \pm 100A$

7.3 DC link capacitors

In this section, the DC link capacitors, also mentioned as neutral point capacitors, are dimensioned. The reason for using the DC link capacitors is to dampen the voltage ripple in the DC link. The capacitors are placed according to figure 7.1. The demands for the capacitors are:

- To keep the ripple in the DC link at maximum 10% of the DC link voltage.
- Voltage rating of $2.4kV$.

The voltage ripple in the DC link is determined by the load current. If a large current is drawn from the DC link, the rate of change (the ripple) in the capacitor voltage becomes large. This can be seen from the capacitor terminal law:

$$i = \frac{dv}{dt} \cdot C \quad [A] \tag{7.25}$$

So for a large C value, the rate of change for a given current is small. In the case of the two-legged inverter layout, the current drawn from one of the neutral point capacitors is unsymmetrical. This is because the phase angle is 120°, and to have a symmetrically load current, all three phases are needed. So to gain knowledge about the voltage ripple, an OrCad simulation is set up. To make the simulation fit the actual setup, two three phase AC voltage generators and two three-phase rectifiers are used as voltage source. To have a worst case scenario, maximum load current is applied. The goal of the simulation is, to find a value for the capacitor, that keeps the ripple of the DC link within $240V$. The simulation schematic and results can be viewed in appendix D.5 on page 188. The simulation is set up, using capacitor values available at IET. The result of the simulation is, that a capacitor of $C = 825\mu F$ is well suited for the inverter setup.

7.3.1 Realization of DC link capacitors

From appendix D.5, the capacitor value was chosen to $C = 825\mu F$ based on simulation results and available capacitors at the Institute of Energy Technology rated for the medium voltage level. The capacitor is realized by four Siemens $3300\mu F/450V$ B43458-A5448-M electrolyte capacitors in series, giving each neutral point capacitor a voltage rating of $1.8kV$. The data sheet for the chosen capacitor states the equivalent series resistance (R_{ESR}) to $65m\Omega@20°C, 100Hz$. The series resistance is important for calculating the power dissipation of the capacitor banks. The R_{ESR} is frequency dependent as shown on figure 7.11, and because the current in the capacitors follow the switching frequency of $f_{sw} = 5kHz$ the R_{ESR} should, according to the manufacturer, be reduced to 60% resulting in:

$$R_{ESR} = 0.065 \cdot 0.6 = 39m\Omega. \tag{7.26}$$

The tolerance of the used capacitors are ±20%, and because they are series connected, $30.3k\Omega/5\%$ parallel voltage sharing resistors (value from datasheet) R_{vsr} are incorporated to ensure voltage sharing. The equivalent diagram of the capacitors is shown on figure 7.10.

The power dissipation of the capacitor bank is, as mentioned, caused by R_{ESR}, and given by:

$$P_C = I_C^2 \cdot R_{ESR} \quad [W] \tag{7.27}$$

Using the OrCad simulation from appendix D.5, and adding the $R_{ESR} = 4 \cdot 0.039\Omega = 0.156\Omega$, the average power dissipation can be found. The simulation result is shown on figure 7.12.

From figure 7.12, the average power dissipation is read to $P_C = 256W$, meaning that the total power dissipation of both the capacitor banks is expected to be $P_{C,tot} = 512W$.

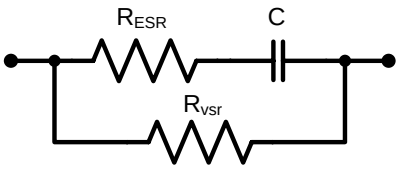


Figure 7.10: *Capacitor circuit model.*

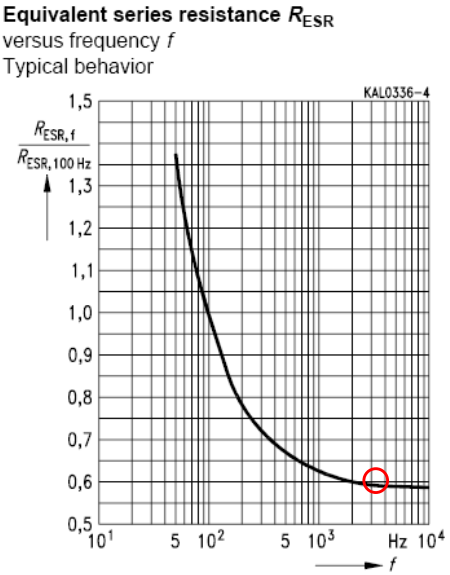


Figure 7.11: *R_{ESR} versus frequency from capacitor data sheet [Siemens, -]. Red circle shows relative R_{ESR} at $f = 5kHz$.*

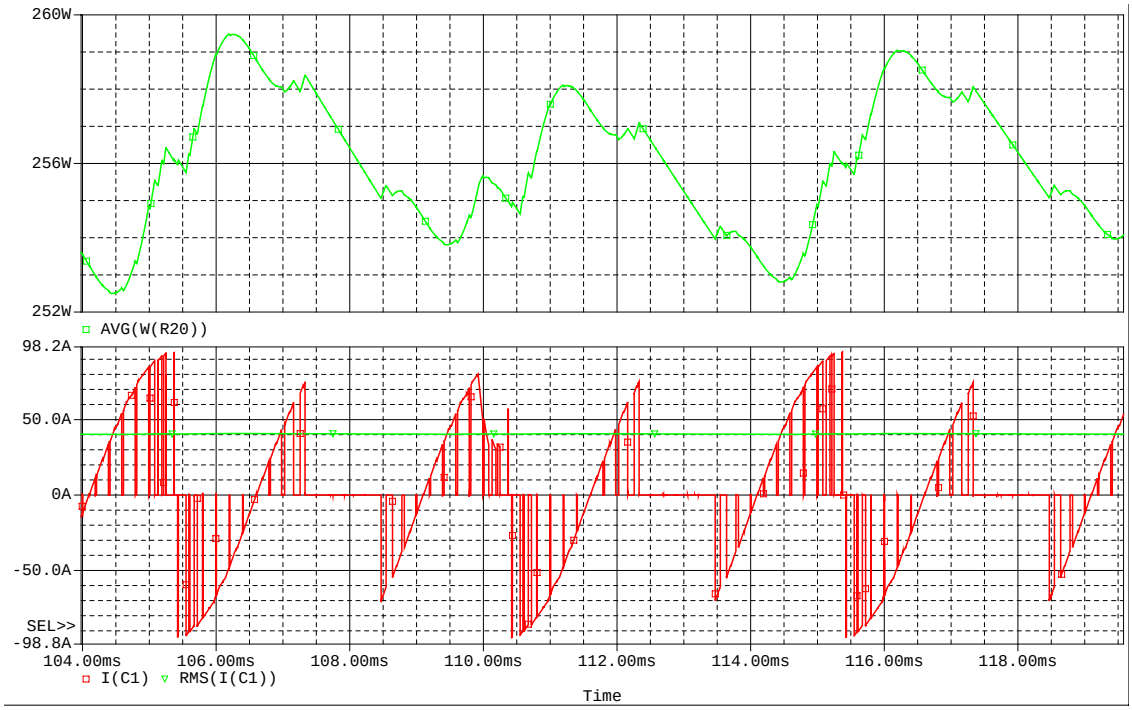


Figure 7.12: *Simulation results for power dissipation caused by the R_{ESR} of 0.156Ω . The top graph show the average power dissipation, and the bottom graph shows the capacitor current (red), and the RMS capacitor current (green).*

7.4 DSP setup

To make the eight sets of IGBTs able to switch, the gate driver circuits must be applied with appropriate gate signals.

A versatile tool for this is a digital signal processor (DSP). This can generate the required gate signals from code, that is easily modified and operated along important functions, as analog current and voltage feedback through ADCs for security. For this reason a DSP is chosen to generate gate signals in this project. The requirements for the DSP are the following:

- Eight logic outputs for the PWM signals to the two phase legs. Each output must be configured with optical transmitters.
- Four logic outputs for measurement of time duration of code execution.
- Four logic inputs to control the functionality of the DSP.
- Five analog to digital converters (ADCs) to set modulation indexes, phase angle and maximum load current reference and one for load current feedback.
- Three counters; Two for carrier based modulation and one to execute an interrupt routine (IRQ).
- $f_{mod,1} = 200Hz$ and $f_{mod,3} = 600Hz$
- $f_{sw} = 5kHz$.
- Dead time of $t_{dead} = 2\mu s$.

For this a Texas Instruments TMSF2812 fixed point DSP is chosen. This is used with three additional extension boards, that supply the eight required optical outputs and up to 16 analog inputs. Four of the analog inputs are designed with build in voltage offset, so that AC quantities can be measured directly. The used DSP setup is shown in figure 7.13.

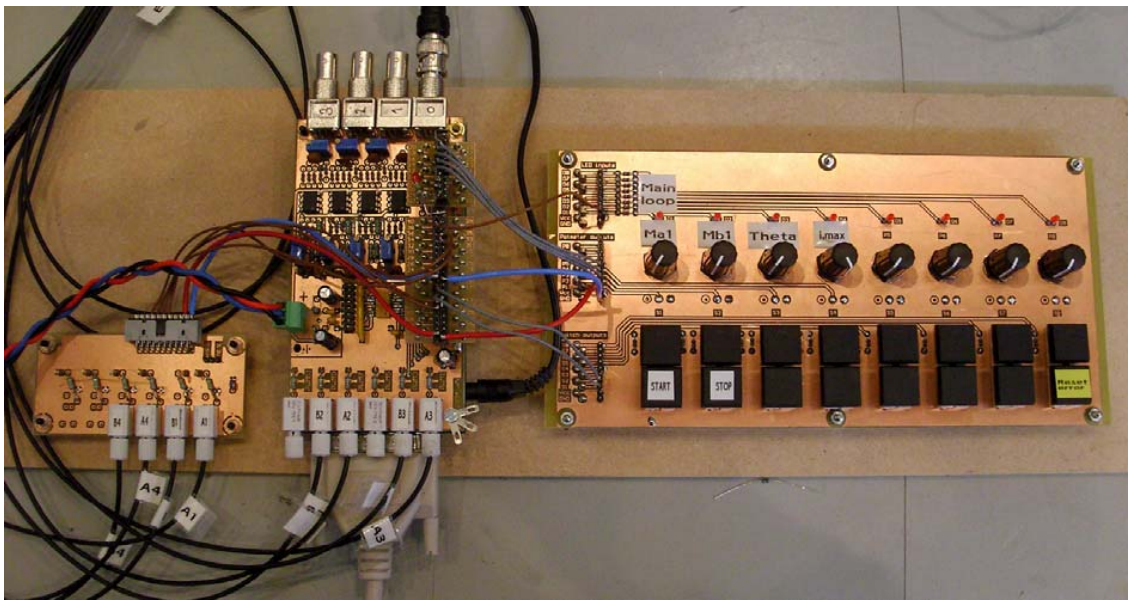


Figure 7.13: *Picture of DSP board, extension I/O board and extra optical transmitters.*

This specific 2812 DSP has an advantage of being able to generate PWM signals based on compare and period values defined in a set of registers. Beside of a single read operation into the counter register, all PWM activity is performed in specially designated hardware, so that the period and pulse width of the

PWM signals will never be affected by additional heavy code executing in the DSP main loop. The period always maintains the value defined in the period register. Also generation of a user defined dead time band is obtained by applying a value to a dedicated hardware register.

7.4.1 DSP code

The generated code for the project is written in `C` and compiled using `Code Composer Studio v. 3.3` (CCS). The developed `C` code can be found on the CD-ROM. The flow chart of the code is shown in figure 7.14.

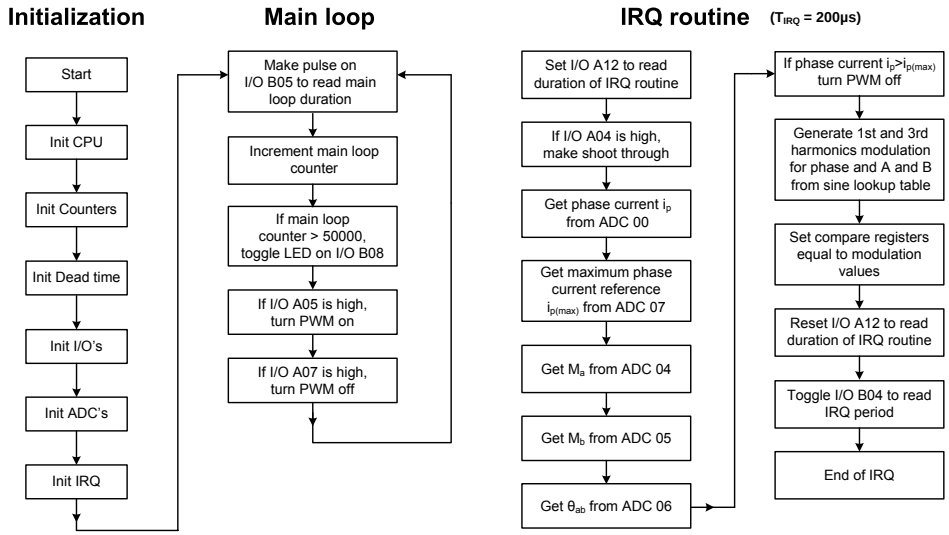


Figure 7.14: *Flow chart of the DSP code.*

The code is designed to give control of the individual inverter phase legs. The modulation indexes for phase A and B, Ma and Mb, and the phase angle between the phases θ_{ab} can be adjusted individually by potentiometers connected to the ADC's. As figure 7.14 shows, four of the eight ADC's in the interrupt routine are used for this purpose. The fifth ADC is used to input a reference value for the maximum allowed load current $i_{p,max}$. If the reference is exceeded, the PWM is turned off for safety, and after this the PWM must be turned on manually.

The code executes in two sections:

1. A main loop, that inputs the logic level of two inputs to turn the PWM on or off, and counts a main loop counter, that toggles an LED to show, that the main loop is executing.

2. An IRQ routine, that inputs the analog values from all ADC's and generates the PWM pattern. The IRQ period is chosen to $T_{IRQ} = T_s = 200\mu s$, because this is the same as the switching period.

   The IRQ routine also samples the load current to detect any slow faults as the ones described in figure 5.2 on page 67. The fast faults can not be guaranteed to be detected, because current rise is much faster than the sample period of $200\mu s$. The detection of fast faults is described in section 7.7.1.

   To be able to determine the proper timing of the IRQ period and the IRQ duration not exceeding the period, two logic outputs are toggled for every period and can be measured by oscilloscope. The measurements are shown in section 7.4.3.

7.4.2 Implementation of PWM

The theory behind the sinusoidal PWM for a three level inverter is described in section 2.3.1.1 on page 2.3.1.1, and here the PWM output is generated by comparing a two triangular carriers and a sinusoidal modulation wave. One carrier for the positive and one for the negative half period of the modulation wave.

The triangular waves are implemented in two hardware counters in the DSP, but the counter registers can not take negative values as required by the lower triangle, because they are unsigned 16 bit registers. Therefore some modifications to the carriers and modulation wave must be done prior to the code realization.

One solution is shown in figure 7.15, where the negative half of the sinusoidal wave is mirrored across the time axis, and along with that the lower triangular wave only takes positive values. Notice, that the lower triangular waves is shifted half a period, because of the sine wave is mirrored compared to figure 2.7 on page 12.

The sinusoidal values are obtained from a 1024 steps sine lookup table read in to the DSP memory and then multiplied by the modulation indexes and then read in to the four timer compare registers. The registers are `EVA CMPR1` and `EVB CMPR4` for phase A, and `EVA CMPR2` and `EVB CMPR5` for phase B. The PWM outputs are set high, when the compare register value is larger than the triangle. `EVA CMPR3` and `EVB CMPR6` are used, if the third phase leg is implemented.

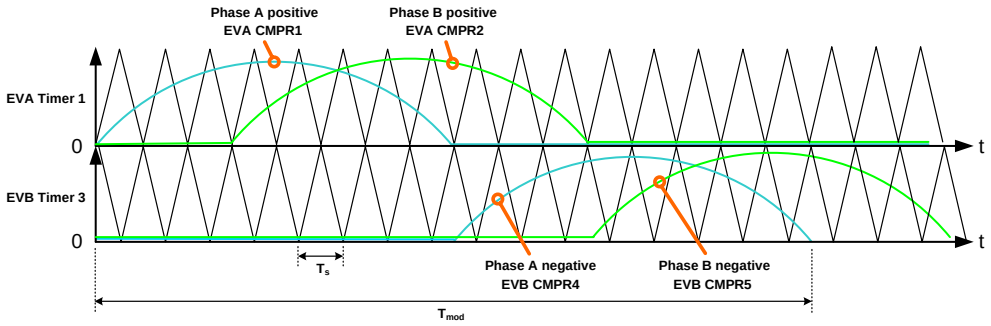


Figure 7.15: *Modified PWM scheme for the three level inverter with only positive wave form values. Blue: Phase A and green: Phase B. Notice, that the third harmonic waveform is not included in the figure.*

7.4.3 Test of DSP

In this section, the DSP is verified by measurement of the eight PWM outputs A_1 to A_4 and B_1 to B_4, the dead time generation and the IRQ period and duration. The results are shown in figure 7.16 to 7.19.

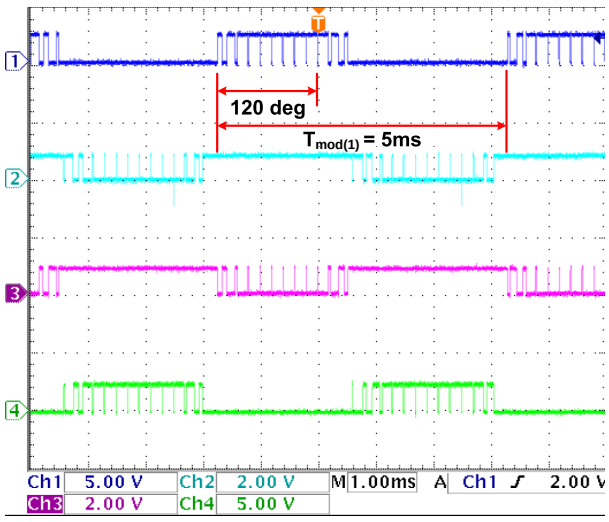


Figure 7.16: *Measured PWM signals for phase A. From the top: A_1 to A_4.*

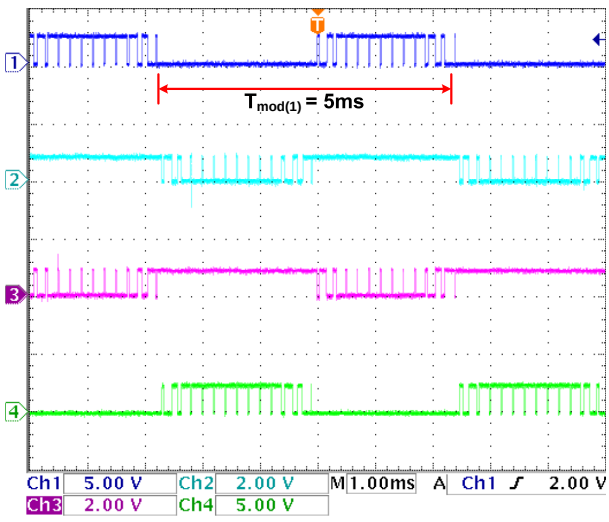


Figure 7.17: *Measured PWM signals for phase B. From the top: B_1 to B_4.*

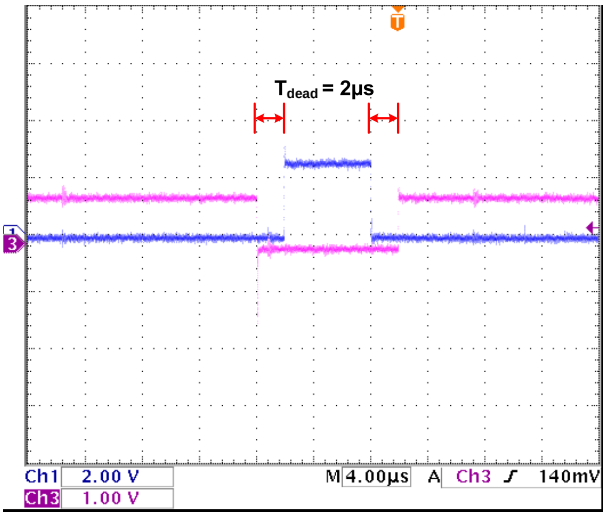


Figure 7.18: *Measured dead time $t_{dead} = 2\mu s$ on DSP output. Blue: switch A1, purple: switch A3. The voltage levels and offset is shifted slightly for clarity.*

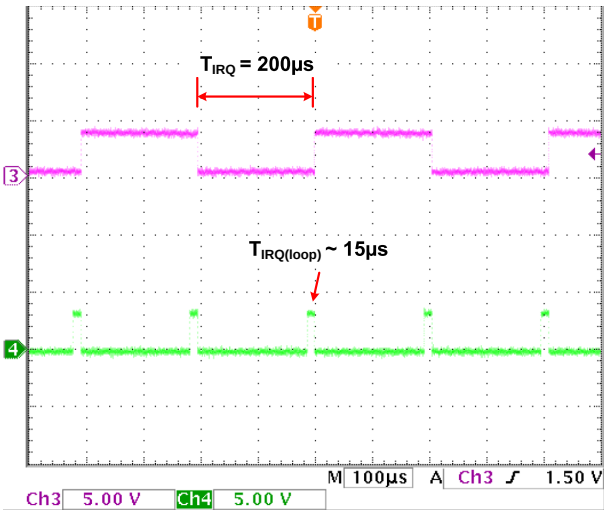


Figure 7.19: *Measured IRQ parameters. Purple: IRQ period and green: IRQ execution time.*

7.4.3.1 Conclusion

Figures 7.16 and 7.17 shows the PWM signals for phase A and B, with $Ma = 1.16$ and $Mb = \frac{Ma}{6}$. As seen, A_1 and A_3 are complementary and the same for A_2 and A_4, and the phase B PWM signals. The fundamental period is $T_{mod(1)} = 5ms$ corresponding to $f_{mod(1)} = 200Hz$, and the phase shift for phase A equals 120° compared to phase B. Because the measurements are comparable with the simulated waveforms in figure 8.3 on page 114, the measurements are accepted.

Figure 7.18 shows the dead time $t_{dead} = 2\mu s$, and this is as required according to section A.5, and therefore the measurements are accepted.

Figure 7.19 shows, that the IRQ period is $T_{IRQ} = 200\mu s$. This is the maximum allowed period of time, because the IRQ loop updates the compare registers, that are used to set the duty cycle for the next switching period. The duty cycle must be updated at least once during one switching period to ensure the correct modulation waveform. The IRQ execution time $T_{IRQ,loop}$ is measured to $\approx 15\mu s$, which is acceptable, because the IRQ routine then only uses $\approx 7.5\%$ of the total IRQ period, and no IRQ overflow appears.

7.5 Gate drive circuits

Each of the IGBTs seen in figure 7.1 need to have a drive circuit to convert the optical signals from the DSP to electrical signals with appropriate voltage levels and current source and sink capabilities. Here a specially designed gate driver, the Semikron Skyper 32 is supplied by Siemens. Details about the driver and the external circuitry required are explained in this chapter, followed by measurement results.

7.5.1 The gate driver

The Skyper 32 gate driver is utilizing the following features:

- Two identical isolated gate drivers in the same housing for two-level applications.
- Galvanically isolated power supply between signal side and driver side.
- Two separate outputs for on and off gate signal for each driver - different gate resistance for different on and off time constants.
- Supply under voltage protection. Triggers, when supply voltage $V_S < 13V$.
- Short circuit protection by v_{ce} desaturation monitoring.
- Error latch / error output.
- Isolation capability from input to output $v_{isol,io} = 4kV_{ac}$ (for $t = 2s$).
- Isolation capability from output 1 to output 2 $v_{isol,12} = 1.5kV_{ac}$ (for $t = 2s$).
- Supply voltage $V_S = 15V$, no load current $i_{min} = 80mA$ and full load current $i_{max} = 450mA$.

The schematic of the driver interior is shown in figure 7.20. This is divided into a primary side and a secondary side, that are galvanically isolated. The isolation border is obtained by two signal transformers and one power transformer.

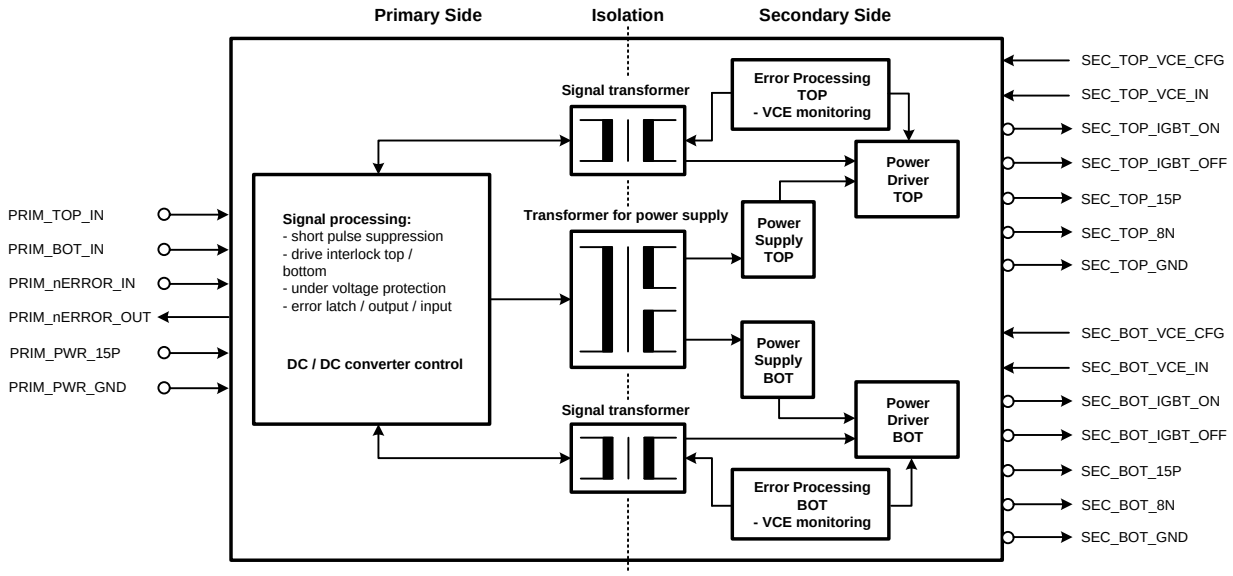


Figure 7.20: *Schematic of the Semikron Skyper 32 gate driver [Semikron, 2007a].*

On the primary side, a signal processing circuit is utilized to shape and filter the signal input pulses from `PRIM_TOP_IN` and `PRIM_BOT_IN` correctly, before transmitting to the secondary side. Switching pulses

shorter than $625ns$ are suppressed and not transmitted to the IGBT to prevent noise in the gate emitter voltages.

Because the driver can operate two switches in a bridge configuration, a dead time between the signals is applied by the driver. The dead time is fixed to $3\mu s$ and can not be changed. This means, that if the the two switches are operated together as one series connected switch, as in this project, two separate drivers must be used. This is because the driver puts out a constant low signal at both outputs permanently, if identical control signals are applied to the inputs [3].

The supply voltage V_s monitor and error monitor is also placed on the primary side. The error monitor enables the `PRIM_nERROR_OUT` output, if the supply voltage drops below $13V$ or if the `PRIM_nERROR_IN` error input is enabled, or if the voltage across one of the two switches differs from the expected value. This happens for instance, if one or both switches short circuit and enter desaturation. The dynamic behavior of the monitor is determined by the resistor and capacitance R_{ce} and C_{ce} on the secondary side.

The secondary side consists of the power driver, that sources the current for the IGBT gate. The driver has two outputs, one for the on state and one for the off state, so that different gate resistance and hence different charge and discharge time constants can be applied. Along with the power driver, an Error Processing unit is used to monitor v_{ce}. The output signal from this unit is fed back through the isolating signal transformer to the error monitor on the primary side, and if an error appears, a signal is sent to the Signal Processor to turn off both switches for safety. Here it must be mentioned, that any turn off transition, also in case of desaturation, is performed hard switched. This means, that no additional turn off gate resistance is applied automatically to obtain soft shut down[4], as described on page 70.

The power driver can source a maximum average current of $i_{out,avg} = \pm 50mA$. This current is a limiting factor for the upper switching frequency for a given required gate charge. The data sheet for the power driver gives the following relationship for the average gate current, gate charge and switching frequency shown in figure 7.21.

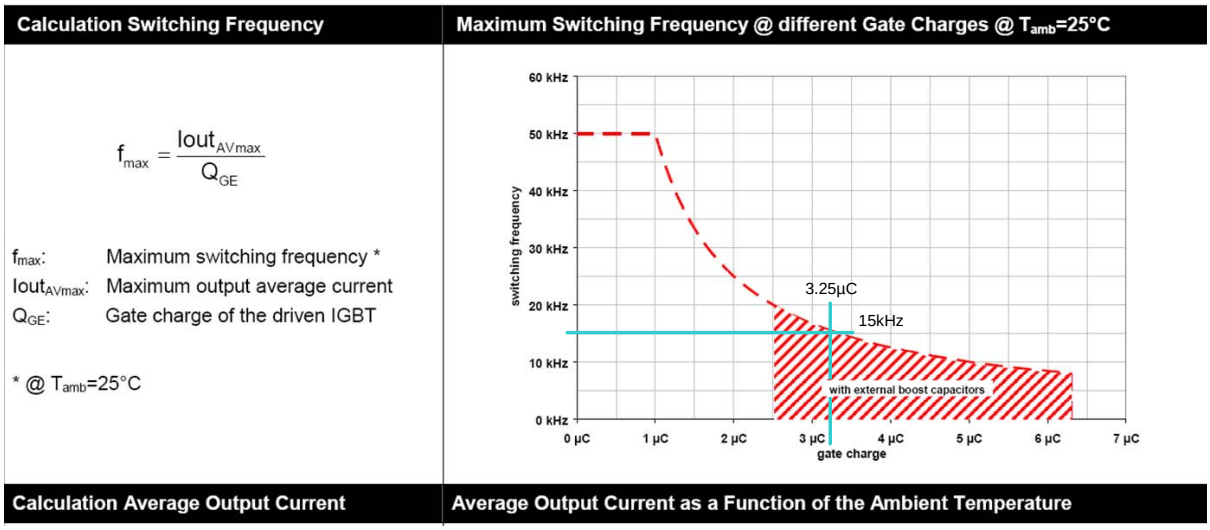


Figure 7.21: *Maximum rating for output charge per pulse [Semikron, 2007a].*

In the figure the average current is given by

$$I_{out,avg} = f_{sw} \cdot Q_{ge} \quad [A] \tag{7.28}$$

As the figure shows, the maximum obtainable switching frequency is very dependent on the gate charge required to turn the given IGBT on. The data sheet value for the Semikron IGBTs nominal gate charge

[3] The dead time can be changed in the Semikron Skyper 32 Pro edition [Semikron, 2007b]
[4] This feature is possible in the Skyper 32 Pro edition [Semikron, 2007b].

is $C_{ge} \approx 3.25\mu C$ for a gate voltage transition from $v_{ge,off} = -7V$ to $v_{ge,on} = 15V$. Comparing this to the information in figure 7.21, the gate driver is capable of switching the IGBTs up to approximately $f_{sw} = 15kHz$ with use of external boost capacitors in the secondary power supply. These are connected between `15P`, `8N` and `GND`. Recommended values according to Semikron [Semikron, 2007a] are given by the expressions

$$C_{boost(15P)}[\mu F] = Q_{ce}[\mu C] \cdot \frac{1}{V} - 2.2\mu F \tag{7.29}$$

$$C_{boost(8N)}[\mu F] = Q_{ce}[\mu C] \cdot \frac{2}{V} - 4.7\mu F \tag{7.30}$$

By inserting $Q_{ce} = 3.25\mu C$, the minimum required capacitances for the boost capacitors become

$$C_{boost(15P)} = 3.25\mu C \cdot \frac{1}{V} - 2.2\mu F = 1.05\mu F \tag{7.31}$$

$$C_{boost(8N)} = 3.25\mu C \cdot \frac{2}{V} - 4.7\mu F = 1.8\mu F \tag{7.32}$$

The on and off state voltages of $v_{ge,on} = 15V$ and $v_{ge,off} = -7V$ are fixed quantities, that can not be changed.

Desaturation detection

The desaturation detection theory is described in detail in section 5.2.2 on page 70. The detection in the driver is obtained by comparing the actual v_{ce} voltage with a reference voltage $v_{CE,ref}$ determined by the first order RC network C_{CE} and R_{CE}. If v_{ce} becomes larger than the reference within a defined blanking time t_{bl}, no action is taken. But after the blanking time has passed, the situation is interpreted as desaturation, and a turn off is performed, and the output pin `PRIM_nERROR_OUT` is set.

Figure 7.22 shows three different fault situations, where desaturation appears and is detected.

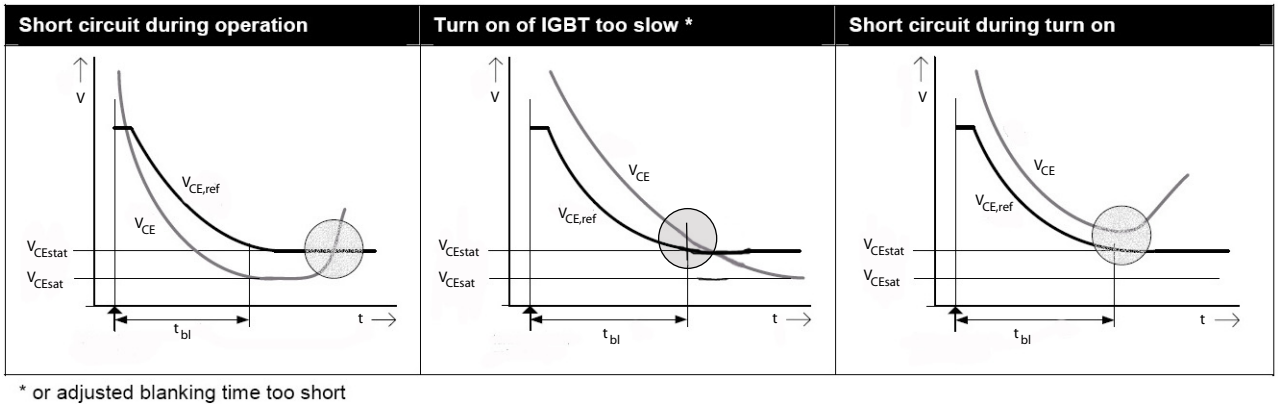


Figure 7.22: *Desaturation in three different short circuit situations [Semikron, 2007a].*

The magnitudes of C_{CE} and R_{CE} are determined by the acceptable dynamic and steady state behavior of the IGBT, that means the maximum acceptable v_{ce} in normal operation, and the acceptable time, for which the IGBT dynamic behavior is ignored. This is called the blanking time t_{bl}.

The data sheet of the gate driver [Semikron, 2007a] gives the following equations for determination of C_{CE} and R_{CE} without further explanation:

$$R_{CE} = -17k\Omega \cdot ln\left(1 - \frac{V_{CE,stat} + R_{VCE} \cdot \frac{V}{k\Omega}}{8.5V}\right) \quad [\Omega] \tag{7.33}$$

$$C_{CE} = \frac{t_{bl}[\mu s] - 2.5\mu s - 0.11\frac{\mu s}{\Omega} \cdot R_{CE}}{0.00323\frac{\mu s}{pF}} \quad [pF] \tag{7.34}$$

Here R_{VCE} is the series resistance of the v_{ce} feedback path, and this is $R_{VCE} = 1k\Omega$. C_{CE} and R_{CE} are now determined from the IGBT characteristics from the data sheet [Semikron, 2006]. The IGBT turn on time in normal operation is $t_{on} \approx 400ns@R_{ge} = 4.7\Omega$, and the on state voltage drop $v_{ce,on}@(T_j = 125°,\ I_c = 400A) = 2.9V$. Also it can be seen from equation (7.33), that the maximum possible choice for $v_{CE,stat}$ is approximately $V_{CE,stat} \approx 7.5V$, because the expression is not valid for negative numbers inside the brackets.

The blanking time t_{bl} is chosen to $t_{bl} = 1\mu s$ to ensure, that the IGBT is turned fully on, before the desaturation detection is enabled, and the threshold for the on state voltage drop is chosen to $V_{CE,stat(max)} = 7V$ to ensure sufficient headroom from the normal on state voltage $V_{CE,stat} = 2.9V$. From this C_{CE} and R_{CE} become:

$$R_{CE} = -17k\Omega \cdot ln\left(1 - \frac{7V + 1k\Omega \cdot \frac{V}{k\Omega}}{8.5V}\right) = 48k\Omega \tag{7.35}$$

$$C_{CE} = \frac{4 - 2.5\mu s - 0.11\frac{\mu s}{\Omega} \cdot 1k\Omega}{0.00323\frac{\mu s}{pF}} = 308pF \tag{7.36}$$

These are shown in the gate driver schematic in figure 7.23.

7.5.2 The gate driver external circuitry

The Semikron gate driver needs additional hardware to interface with two optical inputs and one output and to be protected by variations on the DC power supply to function properly. The schematic of the complete used gate driver system is shown in figure 7.23.

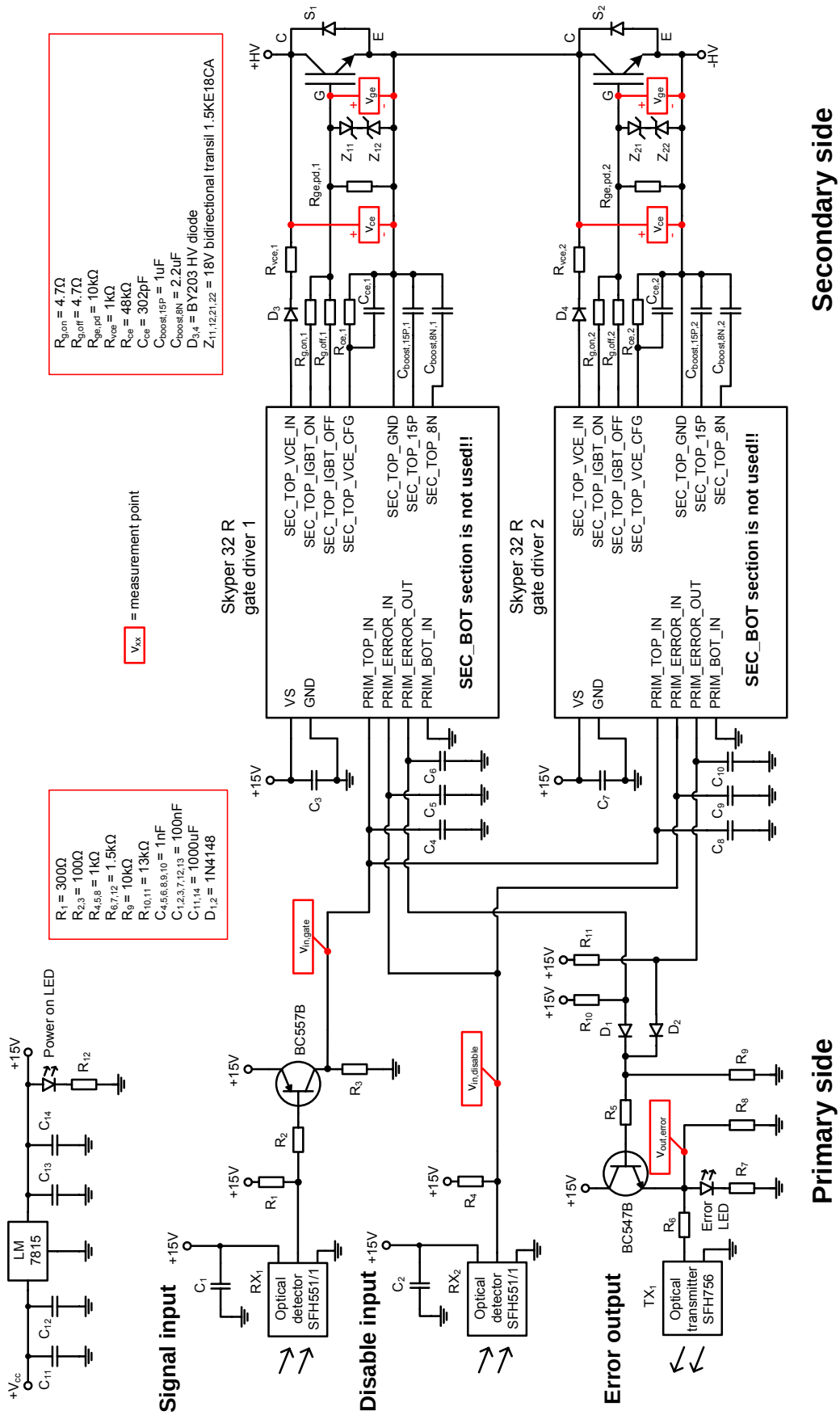


Figure 7.23: *Schematic of the complete gate driver circuit.*

On the primary side, an LM7815 linear regulator is ensuring a constant supply voltage of $+15V$, from an input voltage in the range of $V_{cc} = [+17V; +35V]$.

The two SFH551/1 RX_1 and RX_2 are optical receivers for the gate and the disable signal. Because the receivers are active low and the gate signal input is active high, the signal from RX_1 is inverted by R_1, R_2, R_3 and the BC557B transistor.

The output of RX_2 is connected directly to the `PRIM_nERROR_IN` pin, because this one is active low as well.

The error output SFH756 TX_1 is driven by the transistor BC547B, and D_1, D_2, R_9, R_{10} and R_{11} form a discrete OR gate, because both gate drivers must be able to activate the error output.

On the secondary side, the gate resistors are chosen to be $R_{g,on} = 4.7\Omega$ and $R_{g,off} = 4.7\Omega$ according to appendix A.2. The error monitor feedback network consist of the components R_{ce} and C_{ce}. Important components close to the IGBT are the two $18V$ anti parallel transil diodes across the gate emitter terminals. With these the gate can not be exposed to voltages outside the range of $[-20V; 20V]$, which are critical according to the data sheet. The reason for using transils in stead of regular zener diodes is, that the used transils are designed to dissipate up to $1.5kW$ power for a short while, and this makes them robust as voltage clamps.

A picture of the realized gate driver board is shown in figure 7.24.

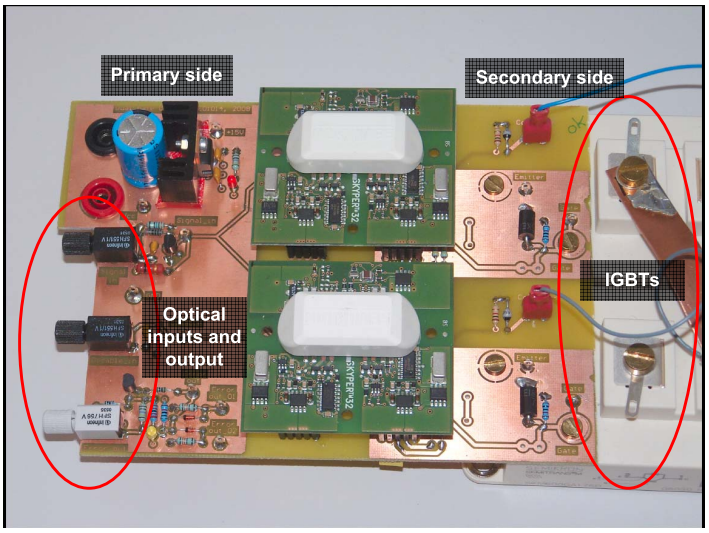


Figure 7.24: *Photography of the gate driver board mounted on two IGBTs.*

7.5.3 Measurement of gate driver signals

Here the signals related to the gate drivers and their interaction are measured to verify the operation of the driver boards and to obtain numeric values for the signal propagation delays. These signals are

- The gate output signal on the DSP $v_{out,DSP}$.
- The gate emitter voltage v_{ge}.
- The collector emitter voltage v_{ce} .
- The gate driver disable input $v_{in,disable}$.
- The gate driver error output $v_{out,error}$.

The measurement points are shown in the gate driver schematic in figure 7.23.

7.5.3.1 Measurement of gate signals

Here the gate signal seen on the DSP board $v_{out,DSP}$, the corresponding gate signal on the the gate driver board $v_{in,gate}$ and the gate emitter voltage v_{ge} are measured. This is done to verify, that the $3\mu s$ dead time generation in the DSP is sufficient to avoid shoot through in the phase legs. The results for the turn on and turn off transients are shown in figures 7.25 and 7.26.

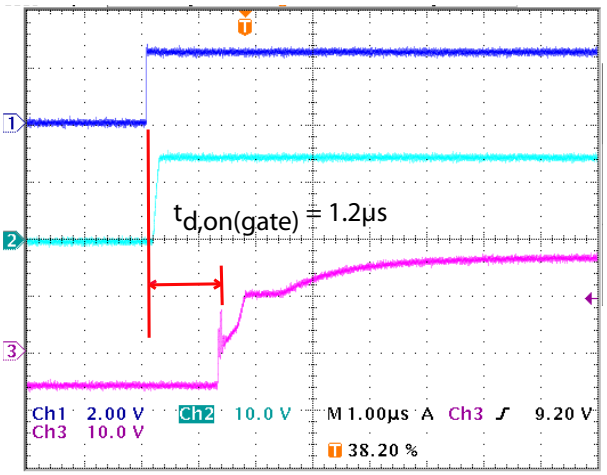


Figure 7.25: *Measured gate driver signals in turn on transition. Blue: $v_{out,DSP}$, magenta: $v_{in,gate}$ and purple: v_{ge}.*

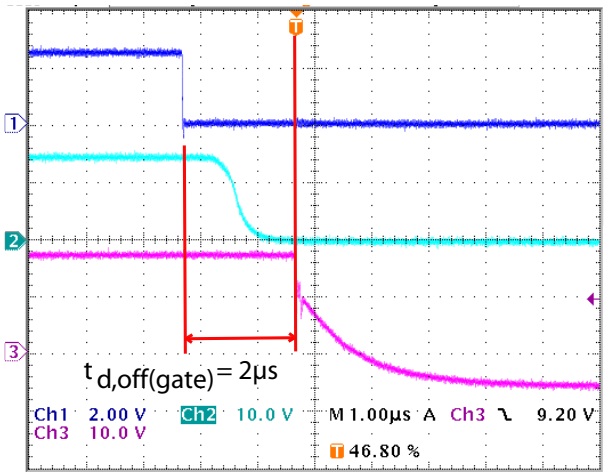


Figure 7.26: *Measured gate driver signals in turn off transition. Blue: $v_{out,DSP}$, magenta: $v_{in,gate}$ and purple: v_{ge}.*

Figure 7.25 shows, that the total turn on delay from the terminals on the DSP $v_{out,DSP}$ to the the actual rise of the gate emitter voltage v_{ge} is $t_{d,on(gate)} = 1.2\mu s$. This includes the rise time of the of the optical transmitter and receiver and the propagation delay in the gate driver circuit.

Figure 7.26 shows, that the total turn off delay from the terminals on the DSP $v_{out,DSP}$ to the the actual fall of the gate emitter voltage v_{ge} is $t_{d,off(gate)} = 2\mu s$.

The conclusion of these measurements are, that the dead time $t_{dead,DSP} = 2\mu s$ chosen for the DSP in section A.3 is sufficient, because the effective dead time will be reduced by $\approx 800ns$ only. This can be shown by equation (7.37).

$$t_{dead,total} = t_{dead,DSP} - t_{d,off(gate)} + t_{d,on(gate)} = 2\mu s - 2\mu s + 1.2\mu s = 1.2\mu s \quad (7.37)$$

The minimum dead time required is $\approx 480ns$, and therefore the measurements are accepted.

7.5.3.2 Measurement of desaturation detection

Here the desaturation detection circuitry is tested and measured to verify proper operation, when a desaturation situation occurs. This is important to verify, because the desaturation detection is used to protect the inverter in case of fast faults, as described in section 5.2.2.

The measured signals are the gate signal on the DSP board $v_{out,DSP}$, the gate emitter voltage v_{ge}, collector emitter voltage v_{ce} and the error output signal $v_{out,error}$. It must be mentioned, that the desaturation situation with high v_{ce} is generated with a pulse generator connected to the collector voltage feed back terminal in stead of generating a real short circuit. Therefore v_{ce} stays high without any inductive turn off over voltage, after v_{ge} goes in to off state, but this considered sufficient to verify the operation. The results as overview and zoom in are shown in figures 7.27 and 7.28.

Figure 7.28 shows the zoomed desaturation, and it can be seen, that the delay between the IGBT entering desaturation and the gate emitter voltage v_{ge} going low is $\approx 8\mu s$. This is a worst case value. The value has

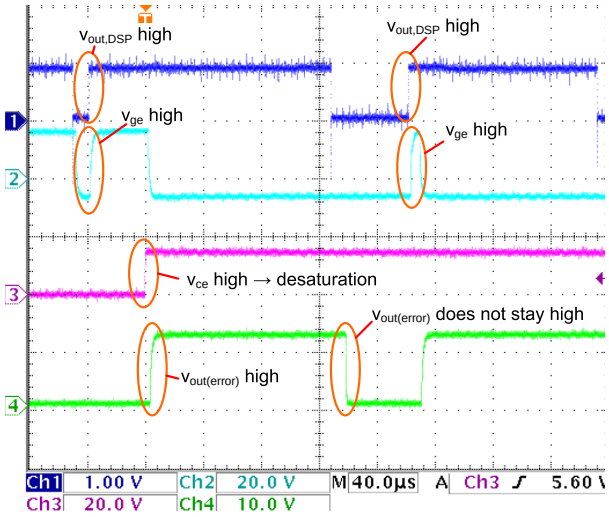


Figure 7.27: *Measured gate driver signals in desaturation situation. Blue: $v_{out,DSP}$, magenta: v_{ge}, purple: v_{ce} and green: $v_{out,error}$.*

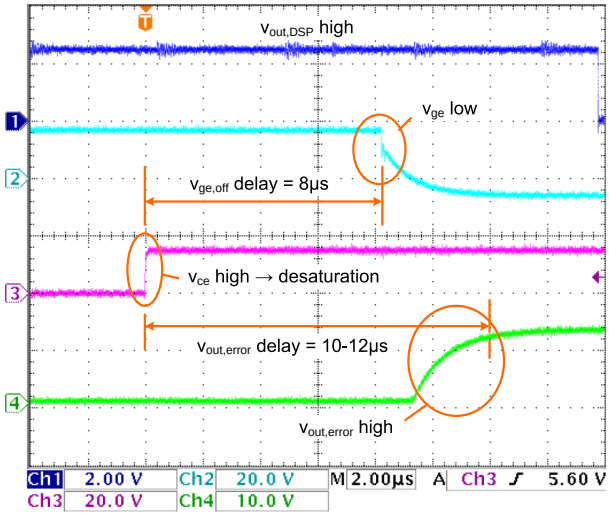


Figure 7.28: *Zoom of gate driver signals in desaturation situation. Blue: $v_{out,DSP}$, magenta: v_{ge}, purple: v_{ce} and green: $v_{out,error}$.*

been measured many times for all 16 gate drivers, and the lowest obtained value is $2\mu s$. The delay is generated internally in the gate driver, and can not be changed by the user.

It must be noted, the the requirement for the desaturation detection is, that it must turn the IGBT off within $10\mu s$, under the conditions described in section 5.2, because of excessive dissipation. The delays measured are within the requirement, but close to the limit, which means, that only one desaturation sequence can be tolerated, to prevent temperature destruction. This is explained in more detail below.

An important detail is, that $v_{out,error}$ is only high as long as the DSP gate signal stays high, which means, it is not latched. As soon as the gate signal goes low again, $v_{out,error}$ also goes low after $\approx 10\mu s$, and in practice this means, that the switches are able to enter desaturation for every turn on transition in case of a fault, until the inverter is fully turned off. The consequence of not latching the turn off of the inverter, when the first desaturation is detected is, that the IGBTs may break down because of over temperature, even though the desaturation detection performs acceptably.

The figure also shows, that the delay between desaturation detection and the error output going high is $10 - 12\mu s$.

7.5.3.3 Measurement of disable input

Here the interaction between the disable input, the error output and the turn off of v_{ge} is tested and measured to verify proper operation and to obtain numeric values for the propagation delays. The disable input is used to turn of the gate driver to make it ignore any wave form in the gate input signals.

The measured signals are the disable input $v_{in,disable}$, the error output $v_{out,error}$ and the gate emitter voltage v_{ge}, and the results as overview and zoom in are shown in figure 7.29 and 7.30.

Figure 7.30 shows the zoomed in situation, where the active low disable input becomes active. The propagation delay between the disable signal $v_{in,disable}$ and the gate emitter voltage v_{ge} going low is $\approx 500ns$. And the delay between $v_{in,disable}$ and the error output $v_{out,error}$ going high is $6\mu s$.

7.5.4 Conclusion

The measurements performed in this section on the gate driver boards show the following aspects:

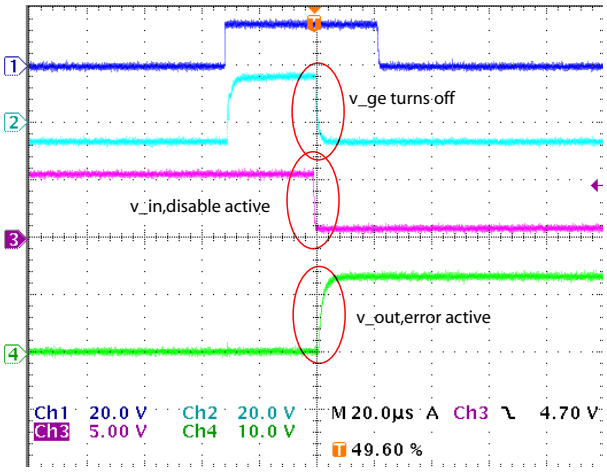


Figure 7.29: *Measured gate driver signals with disable input active. Blue: $v_{out,DSP}$, magenta: v_{ge}, purple: $v_{in,disable}$ and green: $v_{out,error}$.*

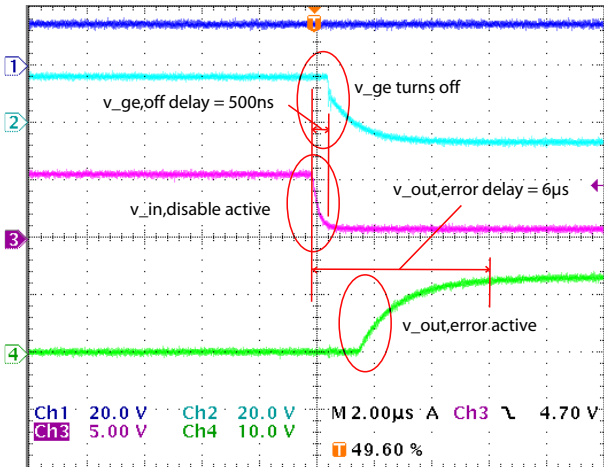


Figure 7.30: *Zoom of gate driver signals with disable input active. Blue: $v_{out,DSP}$, magenta: v_{ge}, purple: $v_{in,disable}$ and green: $v_{out,error}$.*

- The propagation delays seen from the gate signal on the DSP to the gate emitter voltage on the IGBT side of the driver is $1.2\mu s$ and $2.2\mu s$. These values are small, and do not conflict with the $2\mu s$ dead time generation in the DSP, because this values already is including safety margin.
- The delays associated with the desaturation detection is $8\mu s$ worst case for the v_{ge} turn off from detected desaturation and $12\mu s$ worst case for the error output signal $v_{out,error}$. The v_{ge} turn off delay is close to the maximum allowed turn off time of $10\mu s$, that is stated according to the IGBT data sheet. But still the delay is within the limit and is therefore accepted.
- The delay from active disable input signal $v_{in,disable}$ to v_{ge} turning off is $500ns$, and $6\mu s$ for the error output signal $v_{out,error}$. That means, that the disable delay is much smaller than the desaturation shut down delay. These are fixed quantities, that can not be changed by the user, even though is would be desirable to minimize the time delay for the desaturation detection, because this is fixed close to the limit.

The delay times measured here are important, because these have significant influence for the desaturation protection scheme described in section 7.7.1.

7.6 Voltage balancing

The realization of the balancing of the IGBT and diode voltages consist of the following parts:

- Passive snubbers for neutral point diodes .
- Over voltage clamping using zener diodes.

The theory and the simulations for both snubber types are described in section 4.1.1 and 4.2.8.

7.6.1 Passive snubbers for neutral point diodes

Here the passive snubbers are designed based design guide proposed in section 4.1.1, and the used components values are recalculated for the actual maximum load current of $i_{load,max} = \pm 100A$. The minimum required capacitance becomes

$$C_{s,min} = \frac{I_{load} \cdot t_{rv}}{\Delta v_D} = \frac{100A \cdot 16.3ns}{200V} = 8.15nF \tag{7.38}$$

Here a $10nF$ /$2.5kV$ polypropylen capacitor is used. The maximum series resistance R_s is calculated as

$$R_{s,max} = \frac{T_{on,min}}{5 \cdot C_{s,min}} = \frac{2\mu s}{5 \cdot 8.15nF} = 49.1\Omega \tag{7.39}$$

Here a 16.5Ω resistor is used. The use of a smaller resistance than the maximum of 49.1Ω makes the capacitor discharge faster than the required $t_{max} = 2\mu s$, which is acceptable. The power dissipation in the passive snubbers is associated with the energy stored in the capacitors, and this is dissipated into R_s in every turn on. From this the power dissipation capability of the resistors R_s becomes

$$P_{loss,R_s} = f_{sw} \cdot \frac{1}{2} \cdot C_s \cdot V_{Cs}^2 = 5kHz \cdot 10nF \cdot 600V^2 = 9W \tag{7.40}$$

The static balancing resistance $R_s = 200k\Omega$ found in the simulations are also used here, because the calculations are based on the Semikron IGBT. The power dissipation capability of R_s becomes

$$P_{loss,R_p} = R_s \cdot (5 \cdot i_{c,off})^2 = 200k\Omega \cdot (5 \cdot 600\mu A)^2 = 1.8W \tag{7.41}$$

This is a worst case value which only appears, when $Ma = 0$. In this case the inverter stays in zero state, and exposes the parallel resistors of switch S_{x1} and S_{x4} to $600V$ permanently. During operation the dissipation will be less depending on the duty cycle.

The diode D used is a high voltage ultra fast $STTH310/S$ / $1kV$. The component values are summarized in table 7.2.

7.6.2 Zener clamped snubber

The zener clamped snubbers are realized by three transil diodes in series Z_1, Z_2 and D_1 and one parallel resistor R_p. Here the breakdown voltage is chosen to $V_{B,Z} = 700V$ according to the simulation in section 4.2.8, and this gives a maximum allowed DC link voltage of $V_{DC} \approx 2.8kV$ before the transils start to clamp the DC link. With this choice, the safety head room for the DC link voltage in normal operation is $400V$. The reason for using transils diodes in stead of ordinary small signal zener diodes is the transils capability of dissipating high power for short times during the clamping. Normal zeners will be destroyed by high currents.

Transils with a break down voltage of $700V$ are not available for the project, and in stead two transils with break down voltages of $300V$ and $400V$ are connected in series to obtain the required break down. The chosen devices are a $1.5KE300VA$ and $1.5KE400VA$, and these have a peak pulse power capability of

$1.5kW$ $(10/1000\mu s)$. The desired operation of series connecting transils is verified experimentally in appendix D.2.2 with two $400V$ transils in series.

The diode $D1$ i s used to avoid a constant gate current in on state, and here a $300V$ transil of the same type as for Z_1 and Z_2 is used. This transil is operated only in the forward region, this means used as a normal diode only. The parallel resistor for static sharing is also here chosen to $R_p = 200k\Omega$ according to equation (4.18) and dimensioned with respect to power dissipation according to equation (7.41). The components are summarized in table 7.2.

Component	Value / type
Passive snubber	
D_s	$STTH310/S$ / $1kV$ ultra fast
R_s	16.5Ω / $10W$
C_s	$10nF$ / $2.5kV$
R_p	$200k\Omega$ / $4W$
Zener clamped snubber	
Z_{11}	$1.5KE300VA$ / $300V$ transil diode
Z_{12}	$1.5KE400VA$ / $400V$ transil diode
D_1	$1.5KE300VA$ / $300V$ transil diode
R_p	$200k\Omega$ / $4W$

Table 7.2: *Summary of component values for passive snubbers and zener clamped snubbers.*

Both the passive snubber and the zener clamped snubber are now added to the simulation schematic shown on page 8.1, and the simulation results are shown in figures 8.5 and 8.4. The measured results of voltage sharing at $V_{DC} = 2.4kV$ are shown in figures 9.30 to 9.52.

7.7 Fault protection

The realization of the fault protection of the inverter consists of the two following parts:

- Slow fault detection with analog load current feedback to the DSP.
- Fast fault detection with local monitoring for desaturation. This is operated independently of the DSP.

7.7.1 Fast fault protection

The first part of the the load current protection is the fast fault detection scheme. This scheme is based on the desaturation detection method described in section 5.2.2, and in the realized system, the detection is chosen to be performed by the gate drivers as shown in the measurements in figure 7.28 on page 103.

As mentioned, the fast faults must be detected and handled within $10\mu s$ in worst case, because the power dissipation in the IGBTs become excessive, if desaturation appears. The fault could be handled by passing an error signal to the DSP to turn off all gate drivers in case of a fault. But to avoid the time delay related to executing a turn off routine, the fast fault detection and protection scheme is chosen to operate independently of the DSP in separate hardware, here called an optical hub.

In stead the protection scheme is chosen to be based on discrete logic gates, because the propagation delays in these are very low. The proposed block diagram of the system is shown in figure 7.31. Here the detection is performed by the gate drivers.

The protection scheme is based on the optical `Error Out` from every driver board, that goes high, when ever desaturation is detected. All the `Error Out` signals are gathered by optical receivers and `OR'ed` together by `OR` gates. But as described in figure 7.28, `Error Out` does not stay high after the detection. In fact it goes low again, when the gate signal from the DSP goes low, and this may lead to device break down, because the power dissipation will become excessive after several desaturation sequences. Therefore the `Error Out` must be latched externally after the first detection, and this is the first part of

the protection scheme. The latching is obtained by an R/S latch, that must be reset manually by applying an external reset signal.

The second part of the protection ensures, that every gate driver is given a disable signal in case of at least one gate driver detecting a desaturation. This is obtained by distributing the latched `Disable Out` signal to every driver board, even if initially only one driver is detecting a desaturation. This is done to ensure maximum immunity to the fault.

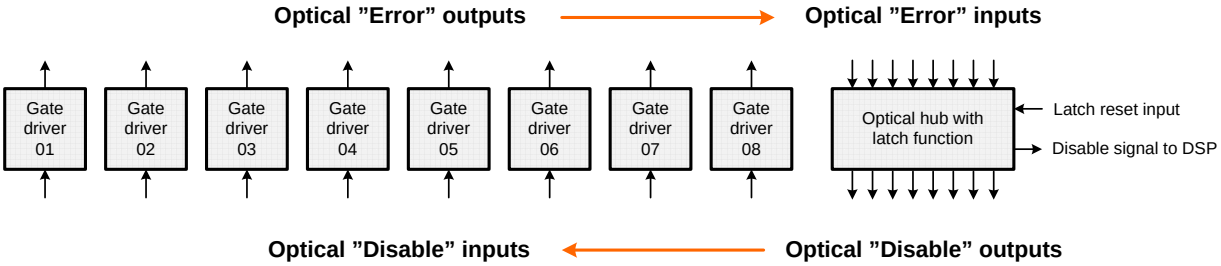


Figure 7.31: *Block diagram of the optical hub used for fast fault protection. The detection of the fast fault is performed by the gate drivers.*

The schematic of the optical hub is shown in figure 7.32. On the left side the optical receivers $SFH551/1V$ are. These are active low, and therefore the outputs are connected to the two 4069 logic inverters named $U1$ and $U2$ to convert the signals to active high. All of these signals are gathered into two 4078 eight input `NOR` gates named $U3$ and $U4$, that are finally inverted before entering the `SET` input of the QUAD `R/S` latch 4078. Here only one out of the four available latches are used. The latch reset is obtained by a separate optical receiver connected to the `RESET` input through an inverter gate.

When one or more error inputs become high, a high value is latched, and the $2N3904$ NPN transistor $Q1$ sources current for the nine optical transmitters $SFH756V$ and a LED.

7.7.1.1 Measurement of propagation delay

The measured propagation delay through the optical hub including the optical receiver and transmitter is shown in figure 7.33. Here a desaturation is emulated by applying a high voltage to the collector feedback pin, and monitoring $v_{out,error}$ and $v_{in,disable}$. The propagation delay is measured as the duration from $v_{out,error}$ going high to the returning signal from the hub activates $v_{in,disable}$. This is measured to $t_{d,hub} \approx 200ns$.

The total expected delay $t_{d,off,total}$ from one gate driver transmitting a high $v_{out,error}$ to the other drivers turning off becomes

$$t_{d,off,total} = t_{d,hub} + t_{d,ge,off} = 200ns + 500ns = 700ns \tag{7.42}$$

$t_{d,ge,off} = 500ns$ is found in figure 7.30 on page 104. Because of the disable delay, the gate drivers are expected to turn off at different times. And even though the delay is small, it is long enough to unbalance the off state collector emitter voltages of the IGBTs, as shown in the simulation figures 3.12 and 3.13 on page 25. Especially if only one gate driver is detecting a desaturation, the corresponding IGBT is expected to see a high v_{ce} only limited by the over voltage protection.

The test results of the fast fault protection is shown in the short circuit test in figures 9.55 to 9.66.

7.7.2 Slow fault protection

The second part of the load current protection is the slow fault detection scheme. As described in figure 5.2 on page 67, the slow faults are characterized by slow current rise compared to a short circuit situation. Typically a slow fault is to be detected, when the inverter is operated in over current mode. Because the current rise is slow, the detection scheme can be satisfied with load current feedback to the DSP, that is sampled within every switching period. It must be repeated here, that the over current situation do not lead

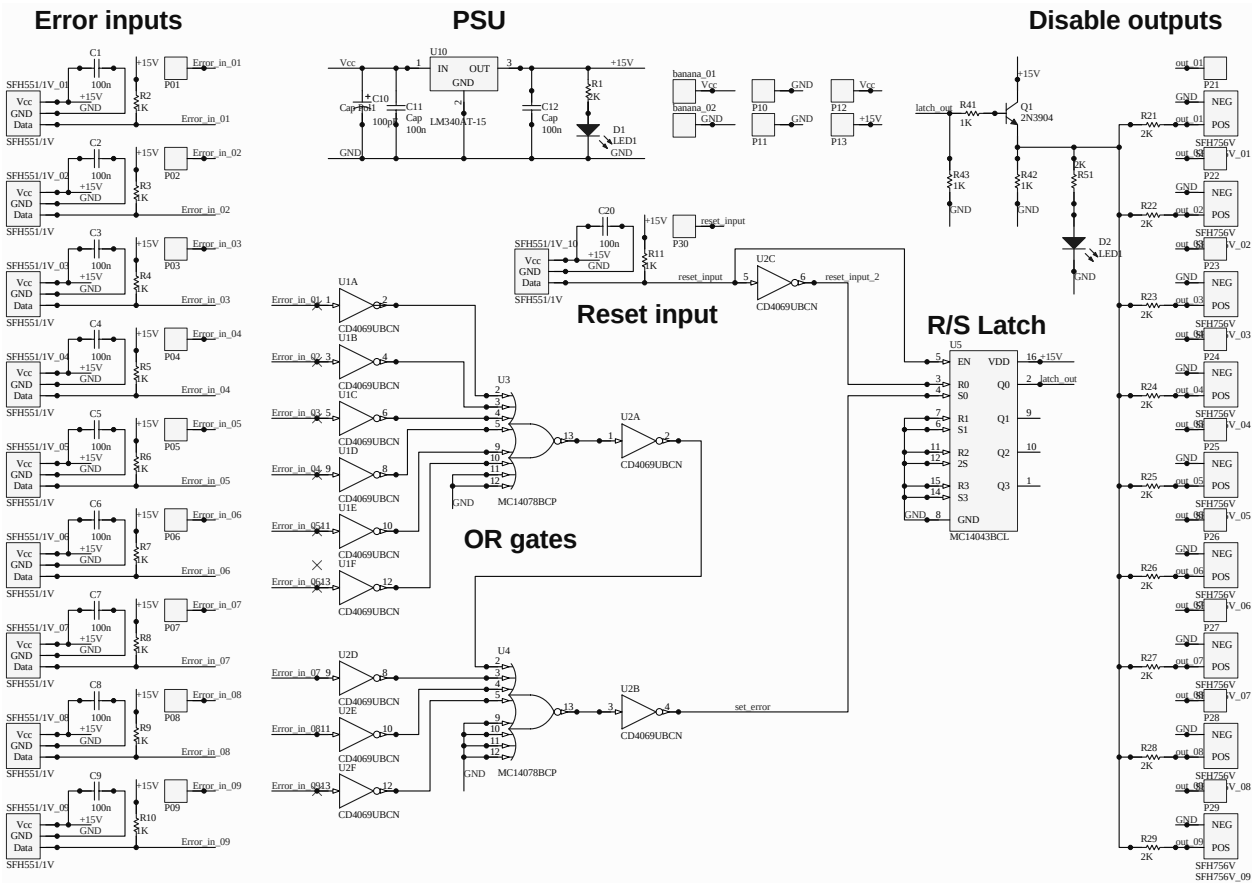


Figure 7.32: *Schematic of the optical hub used for fast fault protection.*

to the same power dissipation as the desaturation, because the on state voltage drop is small. Therefore it is not critical to detect the over current very quickly, as is the $10\mu s$ requirement for a fast fault.

For the load current feedback a LEM current transducer is used, because this is able to measure both AC, DC and pulse currents, and therefore any eventual DC offset in the load current will be detected as well. This is not possible with for example a Rogowski Coil, that is only capable of measuring the change in current, because the measurement is based on changes in flux density around the conductor. Below a given cut off frequency, the induced voltage becomes undetectable.

The decision rule for the for the over current protection to trigger is the following:

$$\text{if} \quad -i_{load,max} \;\geq\; i_{load} \;\geq\; i_{load,max} \quad \text{then disable all PWM outputs} \tag{7.43}$$

The over current protection is implemented in the DSP code, and here the load current is sampled once in the end of every switching period. The reference $i_{load,max}$ is chosen to be an adjustable parameter, that can be set by a analog voltage to an ADC. In this way, the reference and the level of security can be chosen prior to the individual tests.

A detailed description of the measurement results is not given in the report. The current feed back has been tested by setting the reference to $50A$, $100A$ and $150A$, and in each case the protection has shown acceptable behavior by disabling all PWM outputs on the inverter, when the load current has exceeded the reference.

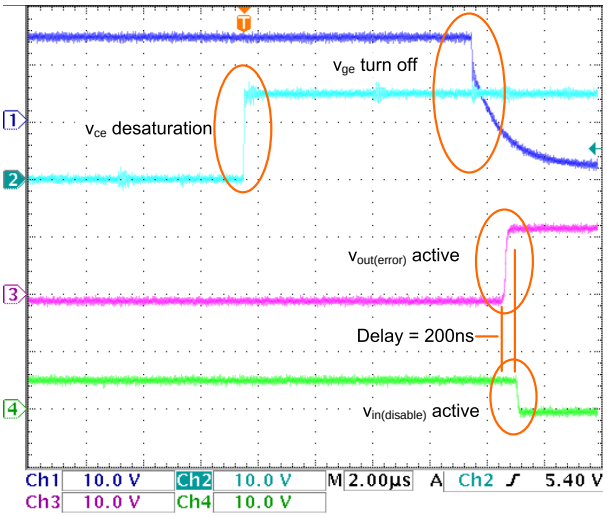


Figure 7.33: *Measured propagation delay $t_{d,hub}$ through the optical hub. Blue: v_{ge}, magenta: v_{ce}, purple: $v_{out,error}$ and green: $v_{in,disable}$.*

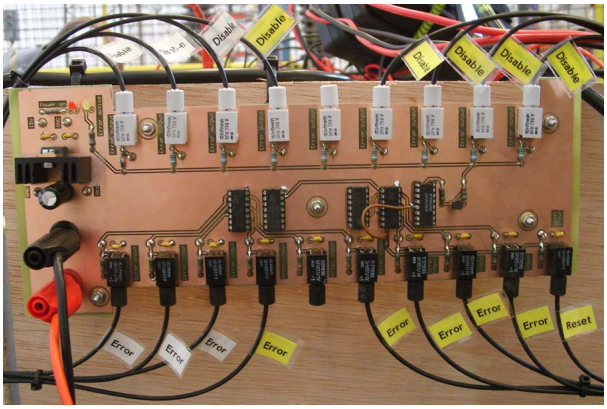


Figure 7.34: *Photography of optical hub.*

Chapter 8

Simulation and realization

In the previous chapters, the individual parts of the inverter are designed, simulated, realized, tested and accepted. These parts include the following:

- Load inductor.
- Neutral point capacitors.
- Medium voltage power supply with six transformers, Danfoss VLT and six three phase rectifiers.
- Gate drivers for the IGBTs.
- DSP to control the gate drivers.
- Protection circuit.

In this chapter, the full thee-level inverter is simulated and realized.

8.1 Simulation

In this section, the full system is simulated in one common simulation file using OrCad. This is done to have a basis for comparison, when the full system is tested in the following section. The required waveforms from the simulations are:

- The output voltages v_{ab}, v_{aN} and v_{bN}.
- The load current i_{load}.
- The voltage $v_{s,nn}$ of the individual IGBTs.
- The voltage $v_{s,n}$ across each switch consisting of two series IGBTs.
- The voltage sharing of the diodes $v_{D,nn}$.
- The voltage $v_{d,n}$ across the diode pair.

The full simulation schematic is shown on figure 8.1, and the results are shown on figure 8.2 to 8.5.

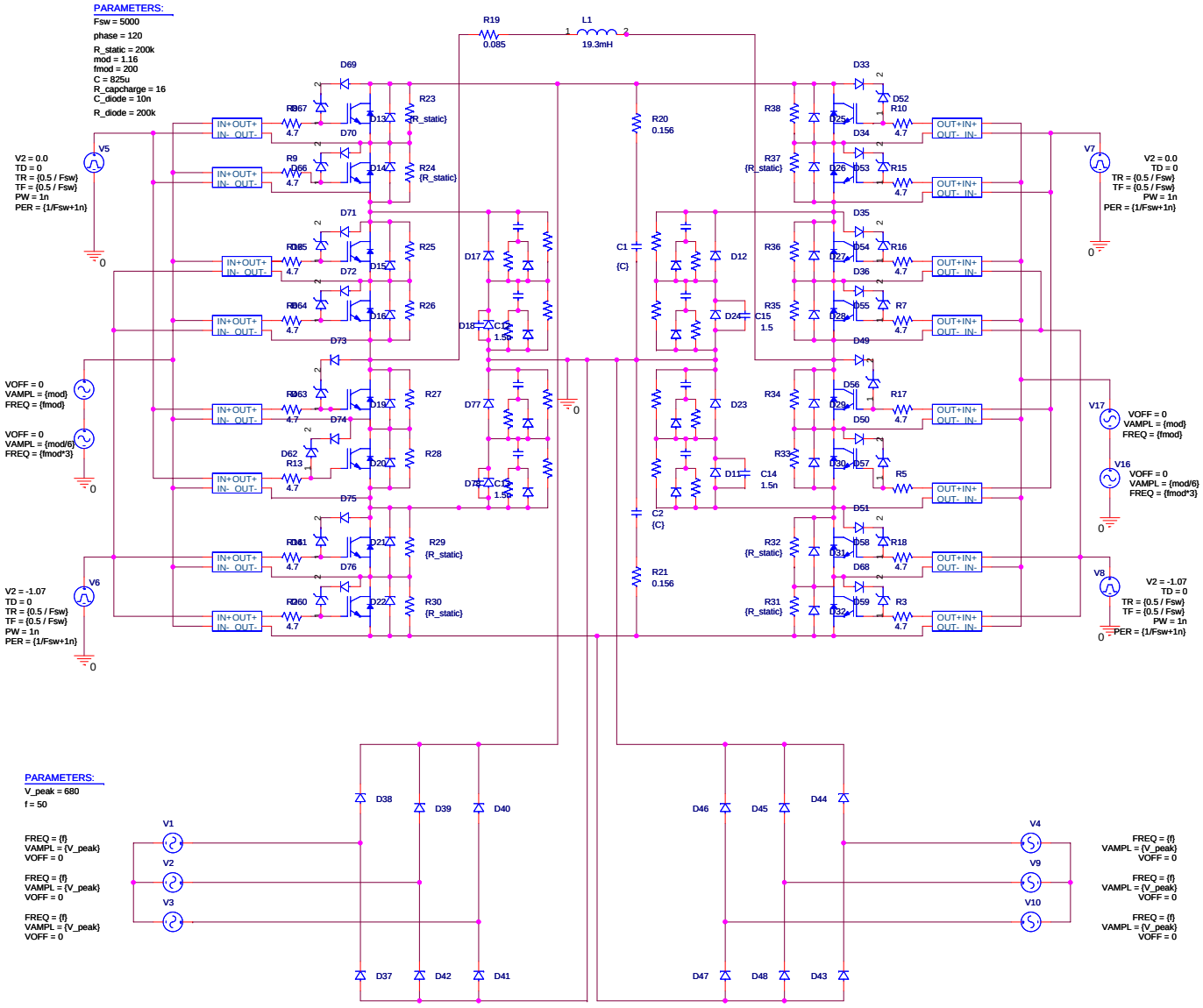


Figure 8.1: *OrCad simulation of three-level inverter. Voltage imbalance for IGBTs obtained by adding a delay to one of the IGBT's in each pair like in section 4.2.9. Parameter deviation for diodes is implemetned by parallel capacitors like in section 4.2.2. The reason for the extra diode across each IGBT is, that the anti parallel diode is not included in the Pspice model of the IGBT.*

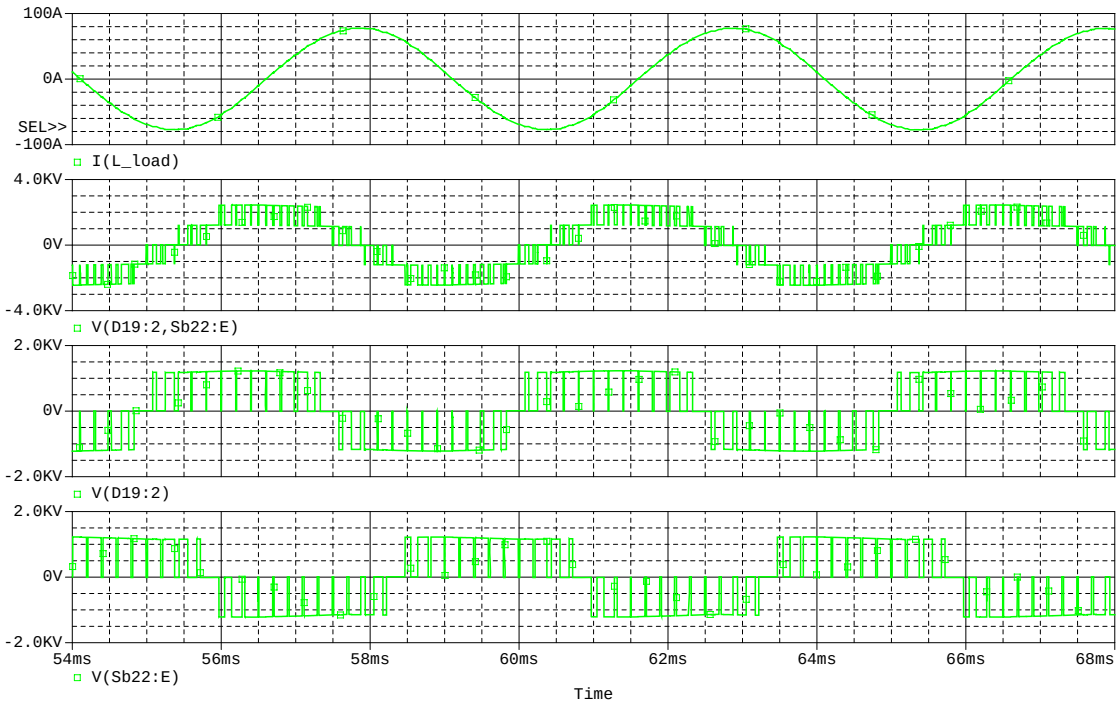


Figure 8.2: *Simulated output waveforms. From the top: (1) Load current i_{load}; (2) phase to phase voltage v_{ab}; (3) phase a to neutral point voltage v_{aN}; and bottom (4) phase b to neutral point voltage v_{bN}.*

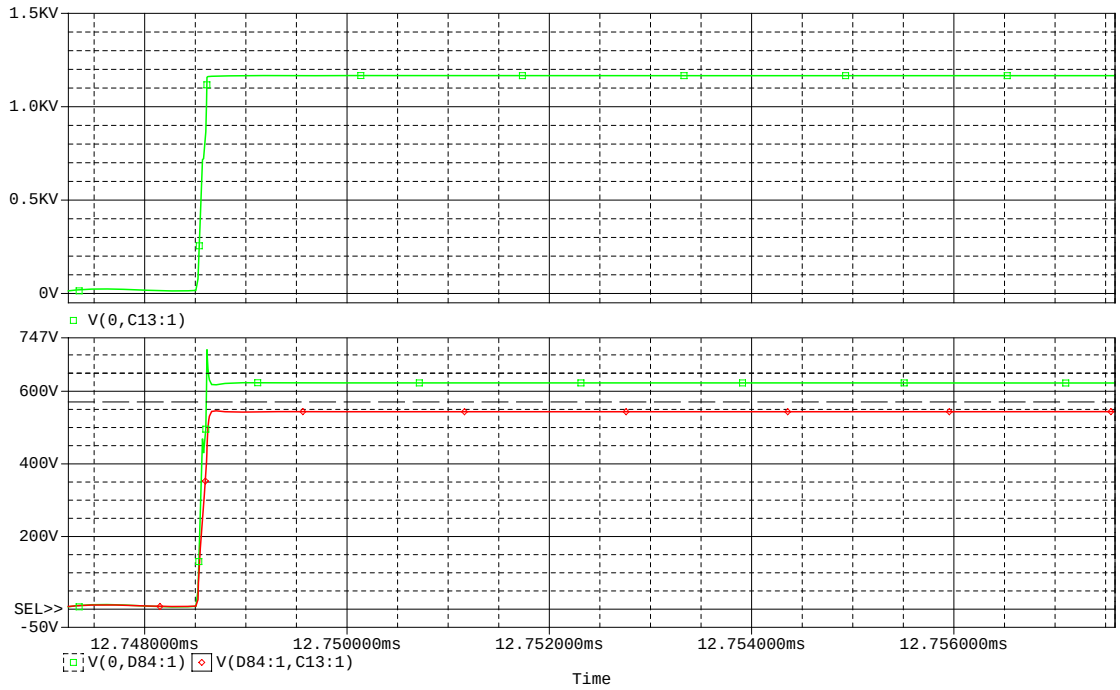


Figure 8.5: *Voltage sharing for two diodes, together with the voltage across a diode pair. Top: Resulting waveform for diode $D_{a31} + D_{a32}$. Bottom; D_{a31} (green), and D_{a32} (red) with an added parallel capacitor of $1.5nF$.*

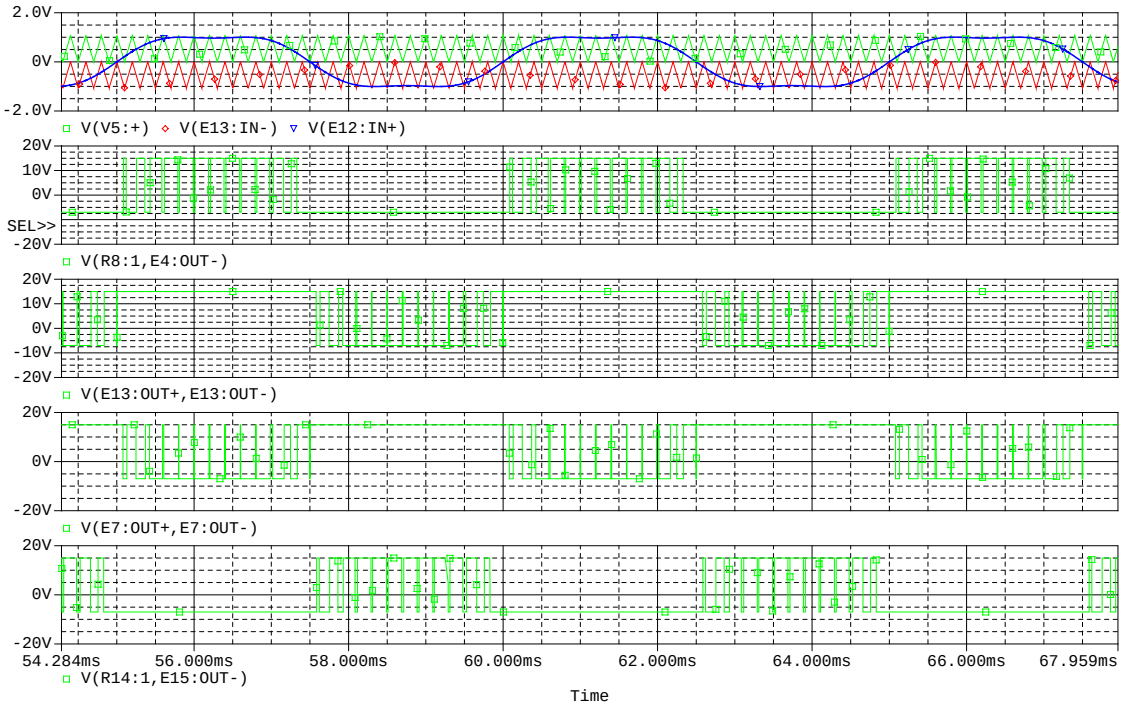


Figure 8.3: *Gate signals for phase a. From the top: (1) Modulation signals green=upper triangle, red lower triangle and blue modulation with third harmonic injection. (2) v_{ge} for S_{a11},S_{a12}. (3) v_{ge} for S_{a21},S_{a22} . (4) v_{ge} for S_{a31},S_{a32} and bottom (5) v_{ge} for S_{a41},S_{a42}.*

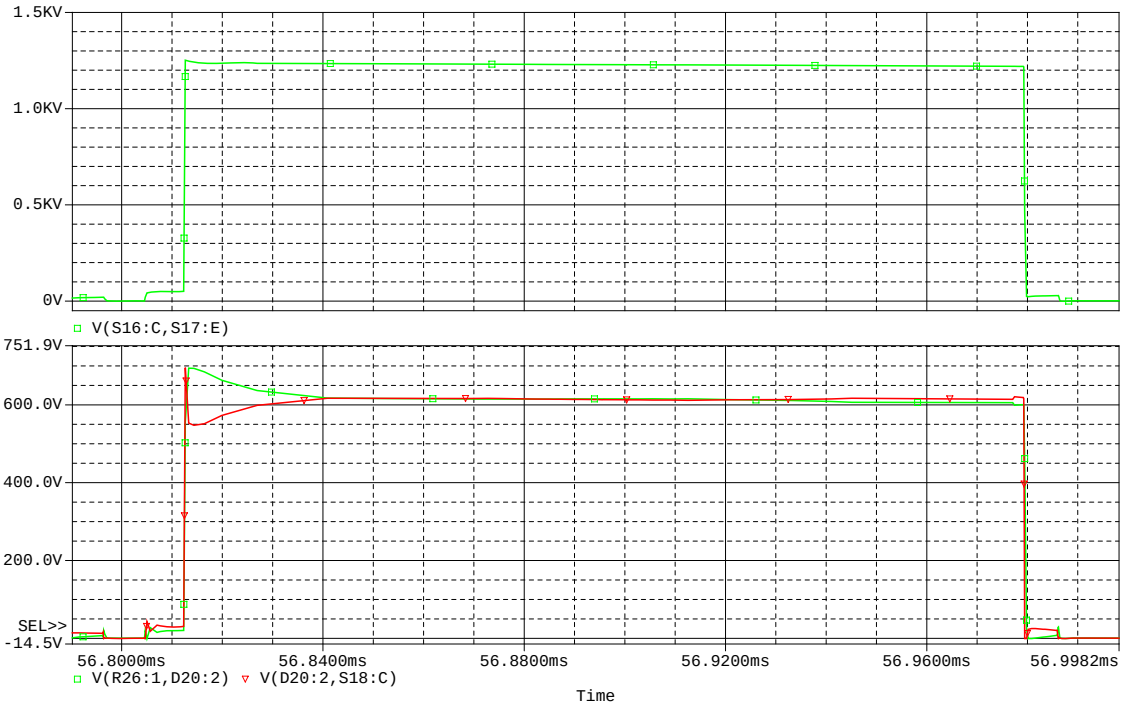


Figure 8.4: *Voltage sharing for two IGBTs, together with the voltage across a switch pair. Top: Resulting waveform for switch $S_{a31} + S_{a32}$. Bottom: S_{a31} (green), and S_{a32} with an added gate signal delay of 170ns.*

8.1.1 Conclusion on simulations

The results of the simulations on figure 8.2 shows, that the three-level performance is obtained. This can be seen by the five level v_{ab} and the three levels of v_{aN} and v_{bN}. Also, the sinusoidal current i_{load} is shifted 90° compared to the output voltage v_{ab} as expected, due to the inductive load. The implementation of modulation strategy, analyzed in section 2.3, is shown on figure 8.3. It shows, that the gate signals have the expected distribution. The simulation of the IGBT voltage sharing on figure 8.4, shows that the zener clamped snubber only allows a deviation of $\Delta V_{ce,max} = 200V$, and that the static voltage sharing resistance ensures static balance. Finally, the simulation of the passive diode snubber, shown on figure 8.5, shows that the voltage deviation is well within the accepted $\Delta V_{ce,max} = 200V$.

The next step is to build and test the inverter. The realization of the full thee-level inverter system is shown in the following section.

8.2 Realization

In this section, photographies are presented of the realized inverter and peripheral equipment. The wiring between the switches is given special attention to minimize the stray inductance. The wiring is chosen to be flat aluminium bars according to the mathematical background for minimum stray inductance described in appendix C on page 167.

A step by step assembly of the inverter system is shown on the figures 8.6 to 8.12.

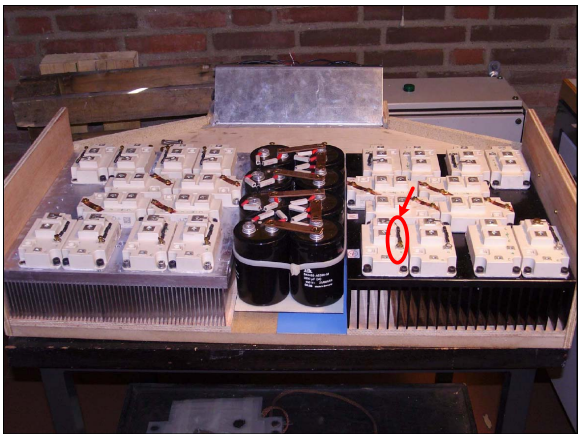


Figure 8.6: *Bottom layer: Layout of the IGBTs, the heat sinks and the neutral point capacitor bank. The zener clamped snubber / protection can be seen next to each IGBT terminal.*

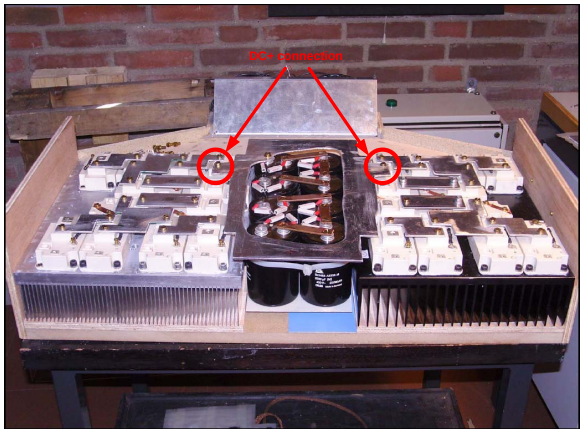


Figure 8.7: *Layer one: Realized connections between switches and the positive supply plate DC+.*

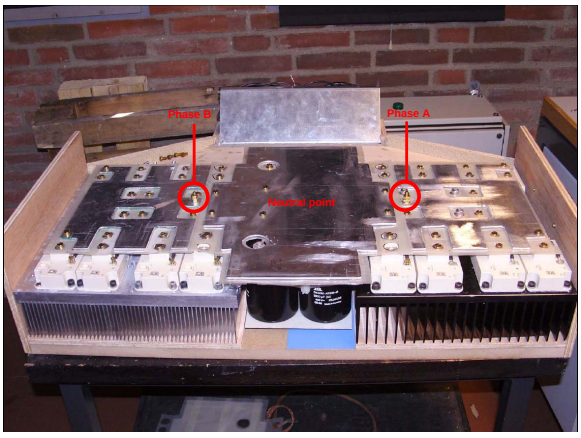


Figure 8.8: *Layer two: The two phase outputs and the neutral point N.*

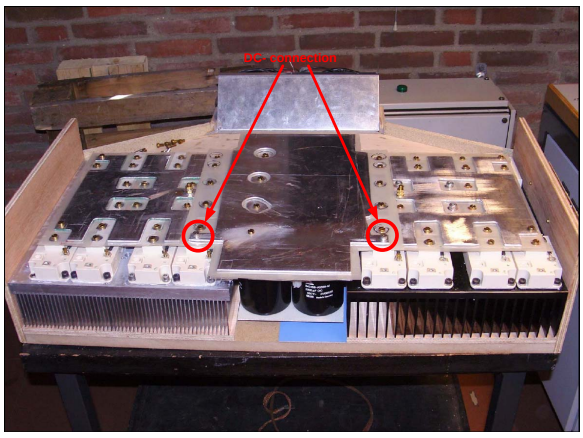


Figure 8.9: *Layer three: Negative supply plate DC−.*

Figure 8.10: *Layer four: Gate drivers and supply/safety terminals for grounding capacitors.*

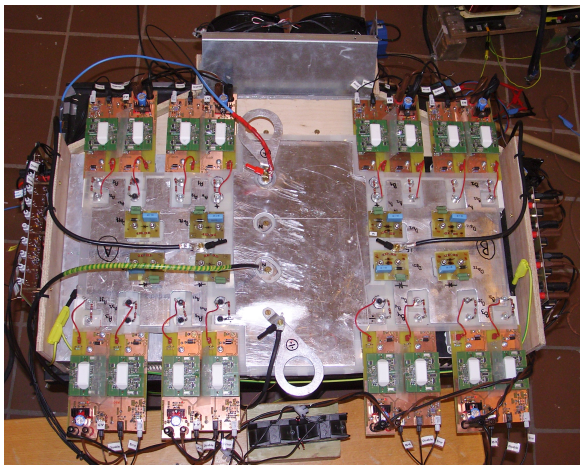


Figure 8.11: *Layer five: Static voltage sharing resistors, fiber optical connections, diode snubbers and optical hub.*

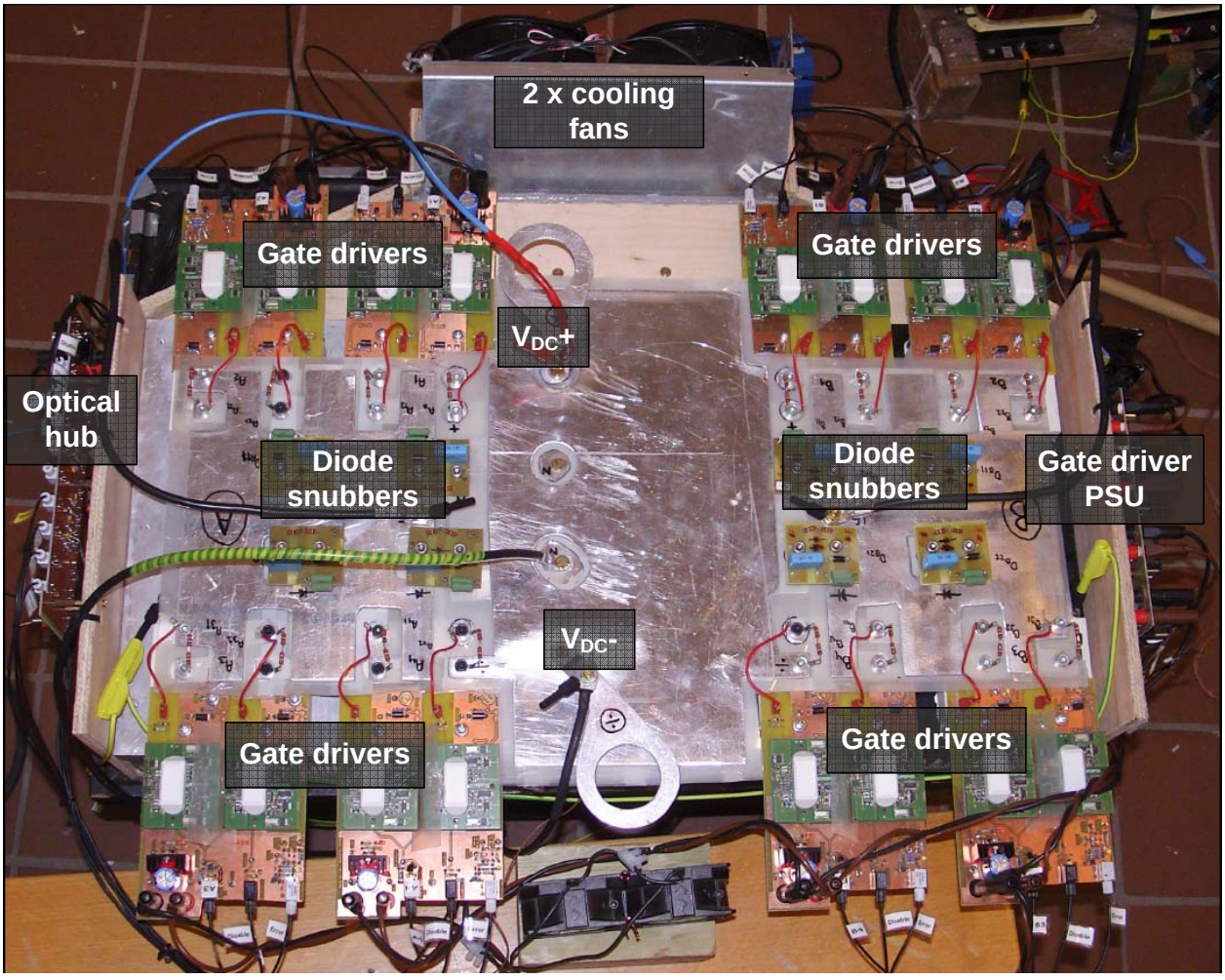


Figure 8.12: *Final layout of the two-phased three-level inverter.*

As shown on the photographies, the connections are made as wide as possible, and also, the current conducting layers are placed on top of each other. The isolation used is Mylax plastic which has a dielectric strength of $120kV/mm$. The diode snubbers of figure 8.11 are bolted directly into the thread of the IGBT terminals to minimize the inductance. The heat sinks below the IGBTs are grounded, to ensure that the potential is not floating. The grounding is obtained by connecting to the floor [1] in the HV laboratory at the Institute of Energy Technology.

Two large electrical fans are mounted onto the heat sinks, to provide extra cooling, and compensate for the heat sink lamellas pointing downwards.

[1] The floor in the laboratory is grounded as one large low impedance metal plate.

Chapter 9

Test

In this chapter, the test of the full system is performed. In the previous chapters, the individual parts of the inverter are designed, simulated, realized, tested and accepted. These parts include the following:

- Load inductor.
- Neutral point capacitors.
- Medium voltage DC power supply.
- Gate drivers for the IGBTs and isolated power supply for each gate driver.
- DSP to control the gate drivers.

The test setup used is presented on figure 9.1.
The used equipment is listed in table 9.1.

Equipment	AAU number	Used for
4 x Tektronix scopes	62796, 62794, 60349, 38387	Data importing
2 x High voltage probe $2kV$	No number	Output voltage
4 x High voltage diff. probes	No number	Switch voltage / output voltage
Rogoflex current transducer	No number	Load current feedback to DSP
Differential voltage probes	56075, 56077, 56078	Switch voltages
Differential voltage probes	38393, 38396, 38398	Switch voltages
2 x Delta SM300 DC power supply	62767, 62765	Initial- and short circuit test
Danfoss $55kVA$ HVAC 6052	No number	Variable main supply
6 x $10kVA$ AXA transformers	38621,38619,38620, 38623,38617, No number	Generation of medium voltage level.
6 x Semikron SKD 30/16 three-phase diode bridge rectifiers	No number	Rectification of the transformer voltage
$32A$ low pass filter	No number	Filters the output to prevent harmonics

Table 9.1: *Equipment used for full system test.*

The tests performed on the system are done at different voltage and current levels, and organized as follows:

- **Initial test at $V_{DC} = 600V$ with added load resistors**. This test is to verify the functionality of the inverter. High power 1kW resistors are connected in series with the load inductor to do initial test of the system at low current.
- **Test at $V_{DC} = 1.2kV$** The purpose of this test is, to test the medium voltage DC power supply, and the inductive load.

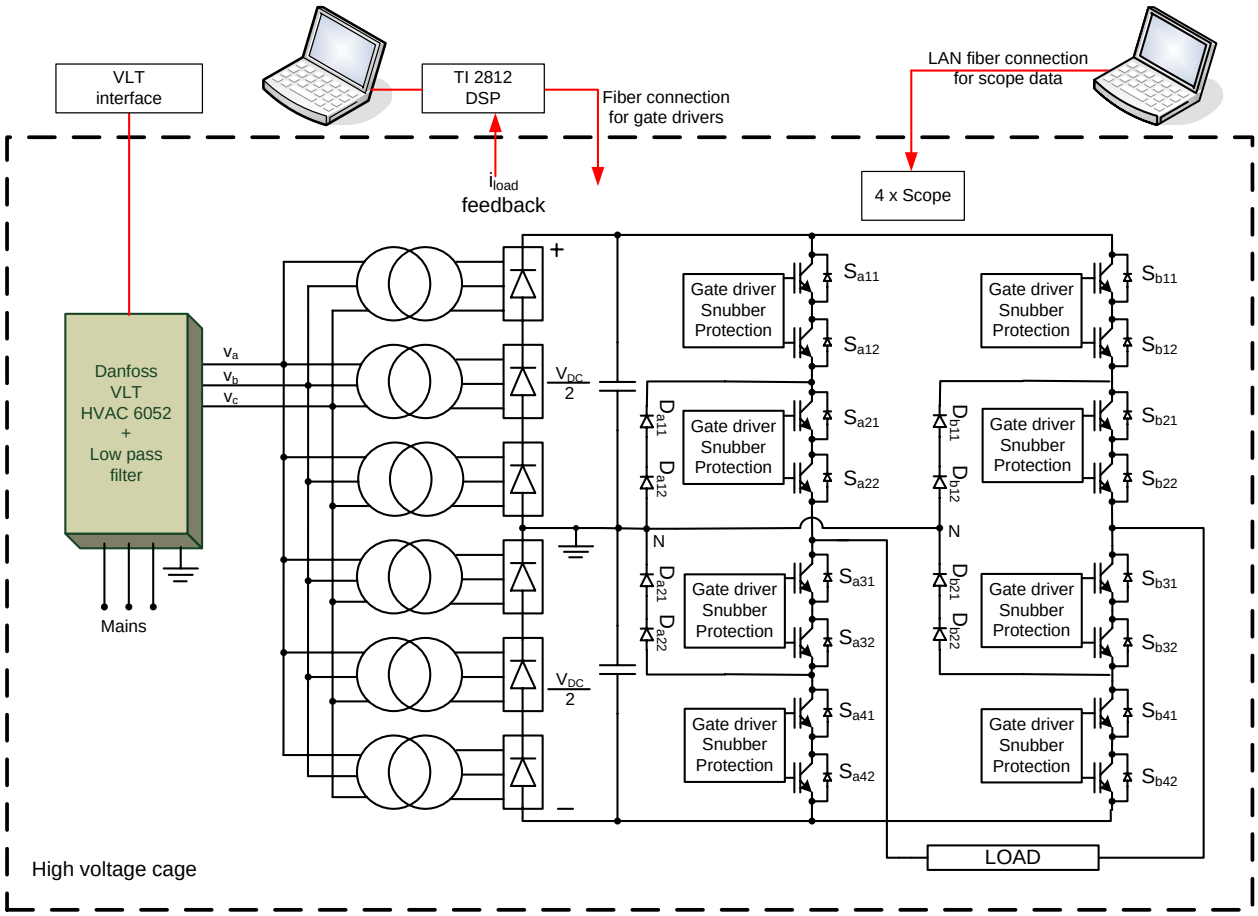


Figure 9.1: *Full test setup.*

- **Final test at $V_{DC} = 2.4kV$ and $\widehat{i}_{load} = \pm 100A$.** The final test is done, to verify the simulation from section 8.1.
- **Short circuit test.** This test is done to verify the protection scheme of the inverter system.

For each test, the following parameters are sought:

- Static and dynamic voltage sharing between the IGBTs and diodes in series.
- Output voltage waveform.
- Output current waveform.
- In the special case of the short circuit test, the sought parameters is explained in section 9.4.

In the following sections, the data from the individual tests are presented.

9.1 Initial test at $V_{DC} = 600V$ with added load resistors

The purpose of this test is, to initially test the functionality of the realized inverter setup. The test is done by means of two delta DC power supplies, and also, an 80Ω power resistor is used in series with the load inductor to limit the load current. The results are shown on figure 9.2 to 9.14.

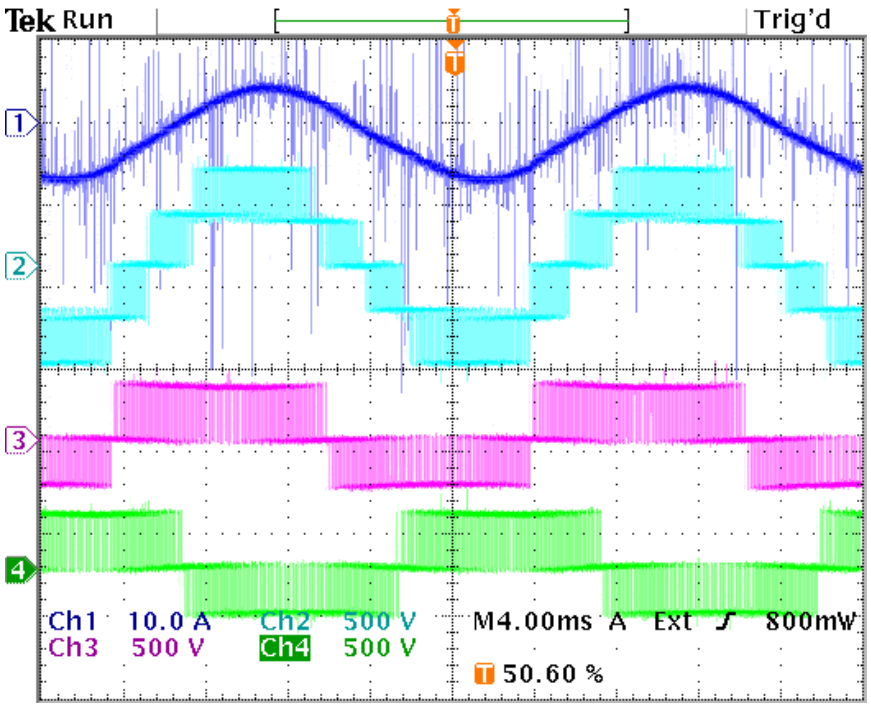


Figure 9.2: *Output waveforms for initial test. Dark blue= i_{load}, light blue = v_{ab}, purple = v_{aN} and green = v_{bN}.*

9.1.1 Results of initial test at $V_{DC} = 600V$ with added resistors

The results of the initial test showed, that the inverter is fully functional, and that the output waveforms is as expected. There is some disturbance in the current. The voltage sharing of the IGBTs is not equal in this test, but this is because the snubber is designed for $V_{DC} = 2.4kV$. The diodes have good voltage sharing, because the passive snubber adapts to the DC link voltage, but the voltage sharing is not the main issue of this test, so no closer inspection is performed until the final test.

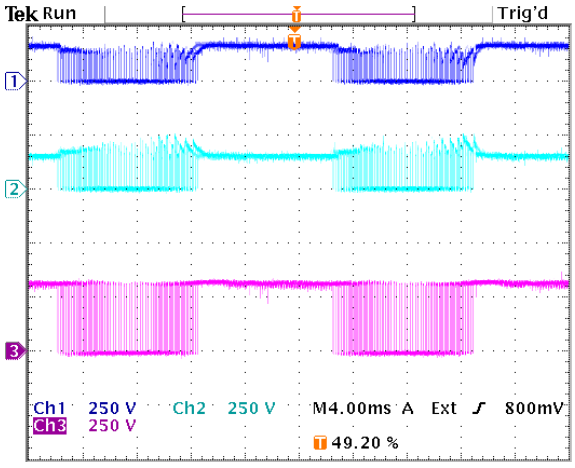


Figure 9.3: *Voltage sharing of switch pair S_{a1}. Dark blue= v_{Sa11}, light blue = v_{Sa12}, purple = v_{Sa1}.*

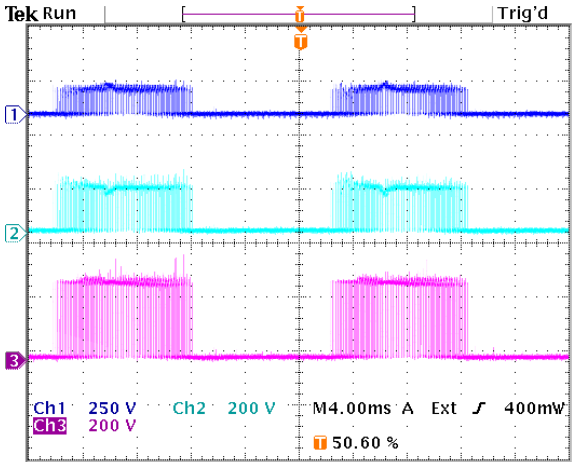


Figure 9.4: *Voltage sharing of switch pair S_{a2}. Dark blue= v_{Sa21}, light blue = v_{Sa22}, purple = v_{Sa2}.*

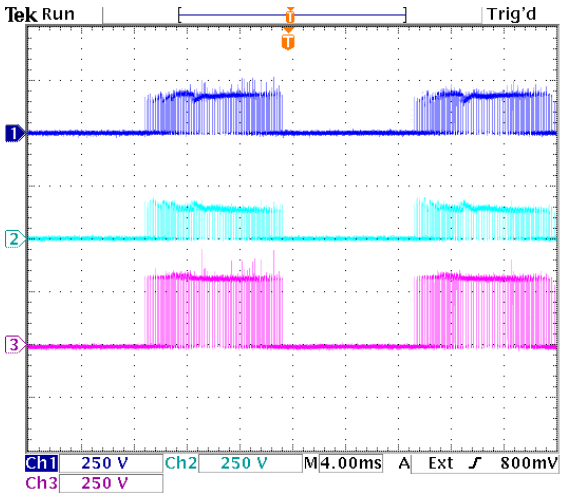


Figure 9.5: *Voltage sharing of switch pair S_{a3}. Dark blue= v_{Sa31}, light blue = v_{Sa32}, purple = v_{Sa3}.*

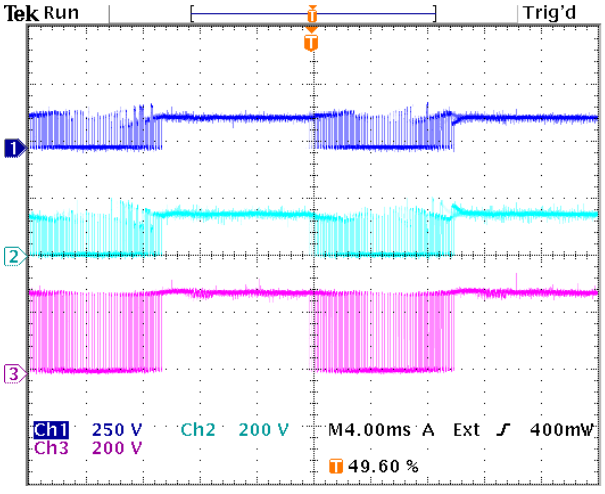


Figure 9.6: *Voltage sharing of switch pair S_{a4}. Dark blue= v_{Sa41}, light blue = v_{Sa42}, purple = v_{Sa4}.*

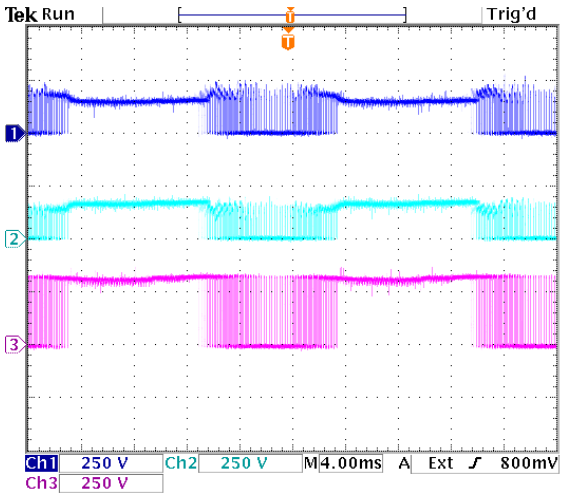


Figure 9.7: *Voltage sharing of switch pair S_{b1}. Dark blue= v_{Sb11}, light blue = v_{Sb12}, purple = v_{Sb1}.*

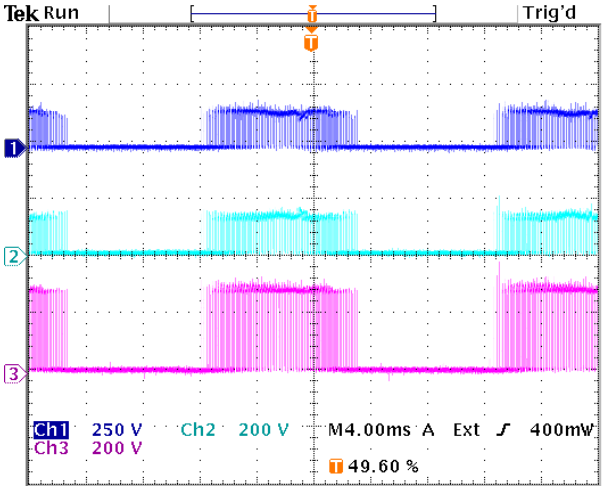


Figure 9.8: *Voltage sharing of switch pair S_{b2}. Dark blue= v_{Sb21}, light blue = v_{Sb22}, purple = v_{Sb2}.*

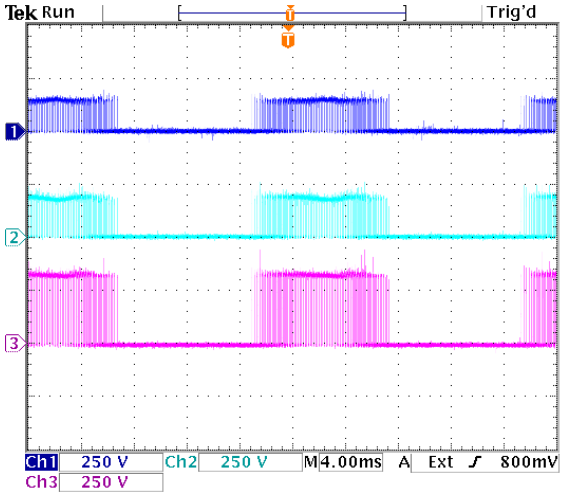


Figure 9.9: *Voltage sharing of switch pair S_{b3}. Dark blue= v_{Sb31}, light blue = v_{Sb32}, purple = v_{Sb3}.*

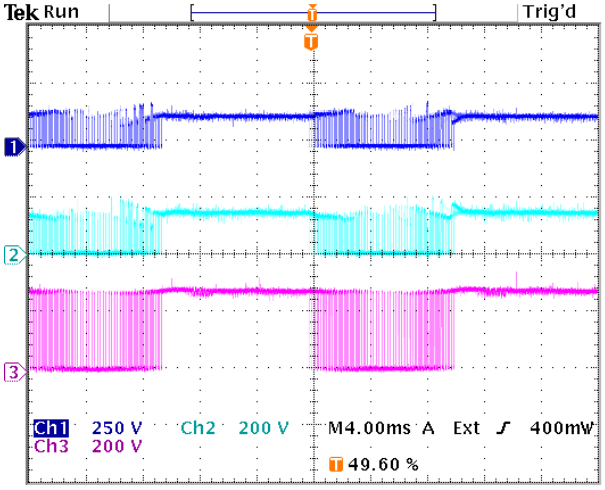


Figure 9.10: *Voltage sharing of switch pair S_{b4}. Dark blue= v_{Sb41}, light blue = v_{Sb42}, purple = v_{Sb4}.*

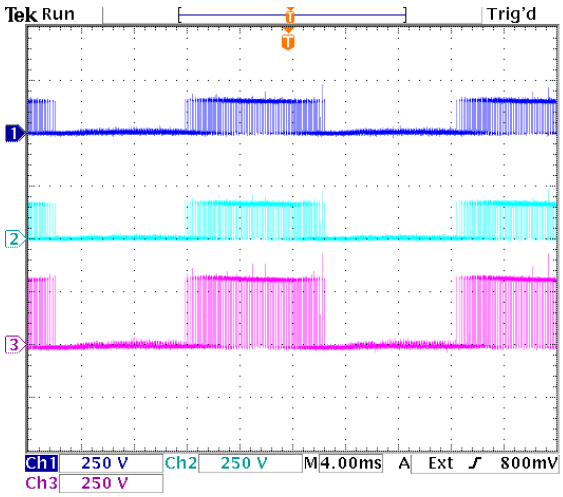


Figure 9.11: *Voltage sharing of diode pair D_{a1}. Dark blue= v_{Da11}, light blue = v_{Da12}, purple = v_{Da1}.*

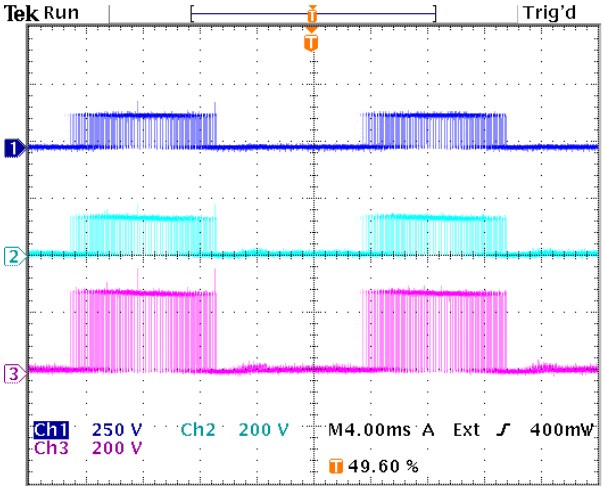


Figure 9.12: *Voltage sharing of diode pair D_{a1}. Dark blue= v_{Da21}, light blue = v_{Da22}, purple = v_{Da2}.*

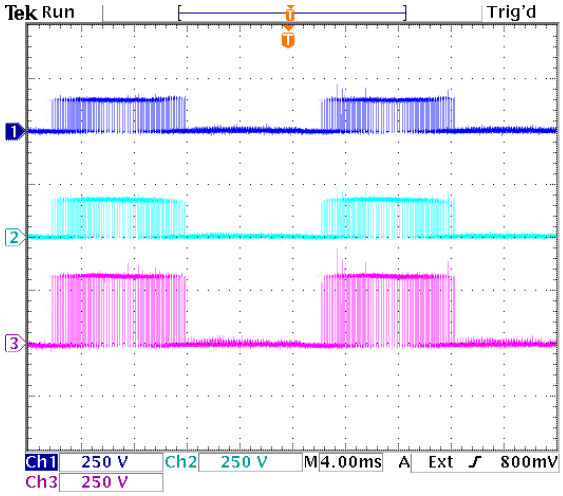


Figure 9.13: *Voltage sharing of diode pair D_{b1}. Dark blue= v_{Db11}, light blue = v_{Db12}, purple = v_{Db1}.*

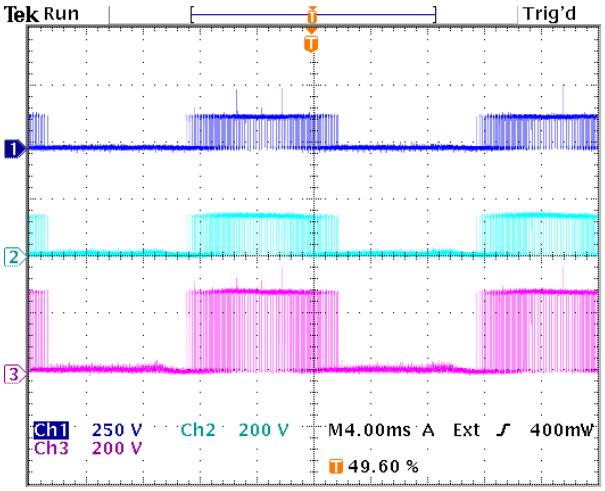


Figure 9.14: *Voltage sharing of diode pair D_{b2}. Dark blue= v_{Db21}, light blue = v_{Db22}, purple = v_{Db2}.*

9.2 Test at $V_{DC} = 1.2kV$ using medium voltage DC supply

The purpose of this test is, to test the functionality of the realized inverter setup, including the effect of the medium voltage PSU. The modulation index Ma is set to 1.16 as in the simulation of the prevuis chapter. The results are shown on figure 9.15 to 9.27.

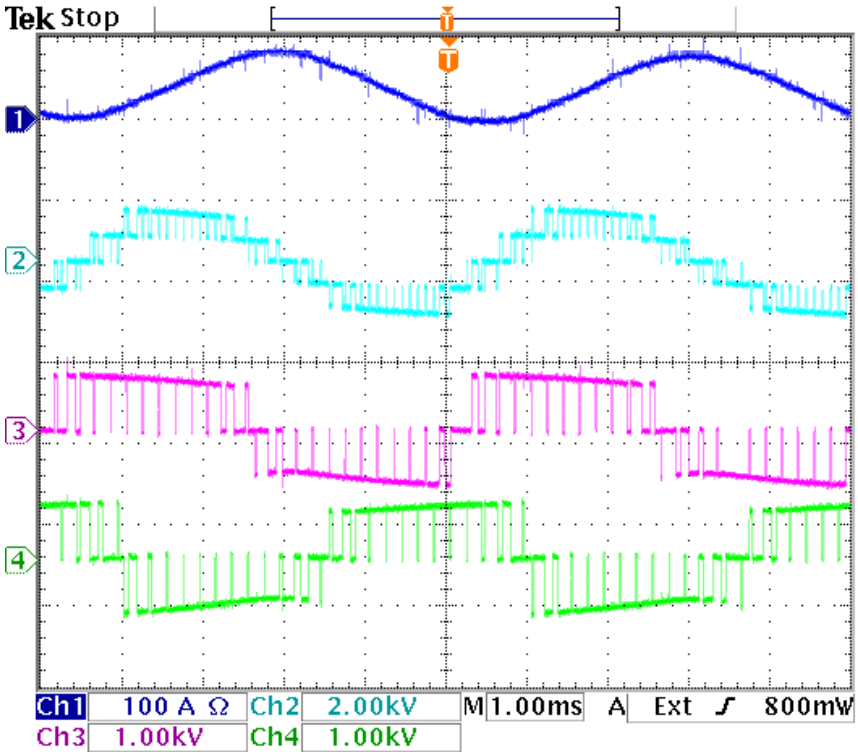


Figure 9.15: *Output waveforms for* $1.2kV$ *test. Dark blue=* i_{load}*, light blue =* v_{ab}*, purple =* v_{aN} *and green =* v_{bN}*. Notice the offset in the current.*

9.2.1 Result of $V_{DC} = 1.2kV$ test

The result of this section shows, that all the switches still works properly. Also the influence of the inductive load can be seen on figure 9.15, where the current is shifted $\approx 90°$ compared to v_{ab}. There is an offset in i_{load}. It can be seen from figure 9.15, that the current has a peak to peak value of $\widehat{i}_{load,pp} \approx 90A$, and this suggest, that the load inductance is approximately the desired value. From the measurements at $V_{DC} = 1.2kV$, the effect of the medium voltage PSU becomes clear. On figure 9.25, the DC link voltage is added to the voltage sharing data, and the effect of the ripple is seen in all the voltages of this test. Like the $V_{DC} = 600V$ test, the voltage sharing is not the issue here, and again, the switches does not share the voltage correct, because the snubbers are fixed to a clamping level of $700V$ pr. switch. The diodes however have an acceptable voltage sharing as shown on figure 9.24 to 9.27. Also the effect of the third harmonic can be seen on figure 9.15, where the peak to peak value of the current can be calculated from equation (7.22) on page 88 to:

$$i_{load,pp} = \frac{v_{ab,1}}{6 \cdot |Z_{load}|} = \frac{v_{ab,1}}{\sqrt{(2 \cdot \pi \cdot f_{mod} \cdot L(l_{gap})^2 + R_{DC}^2) \cdot 6}} \quad [A] \tag{9.1}$$

$$i_{load,pp} = \frac{1.2kV \cdot \sqrt{3} \cdot 1.16}{\sqrt{(2 \cdot \pi \cdot 200Hz \cdot 0.023H)^2 + 0.086^2}} = 83.4A \tag{9.2}$$

This calculated result fit the measured data of figure 9.15, and hence, the third harmonic injection works as expected.

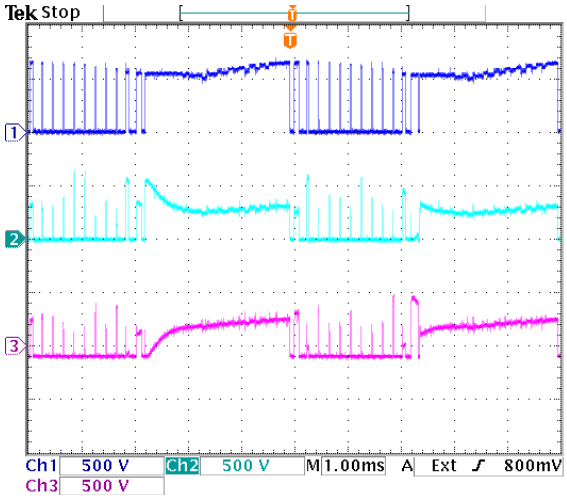


Figure 9.16: *Voltage sharing of switch pair S_{a1}. Dark blue= v_{Sa1}, light blue = v_{Sa11}, purple = v_{Sa12}.*

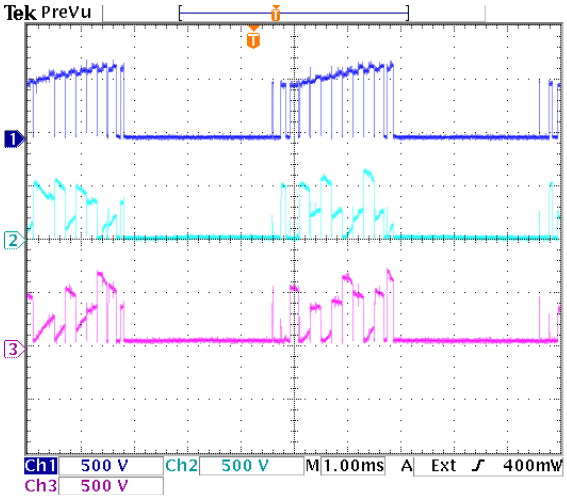


Figure 9.17: *Voltage sharing of switch pair S_{a2}. Dark blue= v_{Sa2}, light blue = v_{Sa12}, purple = v_{Sa22}.*

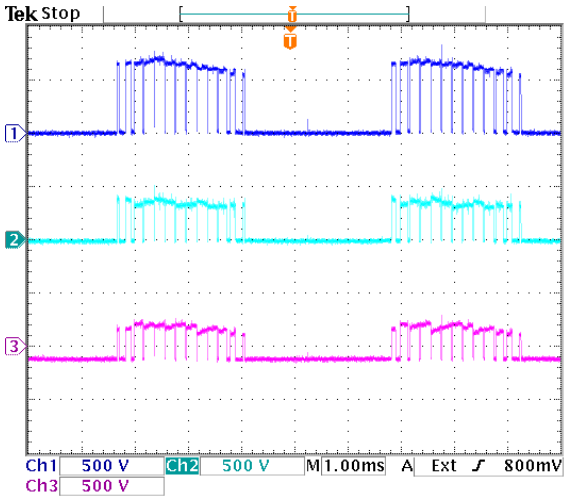


Figure 9.18: *Voltage sharing of switch pair S_{a3}. Dark blue= v_{Sa3}, light blue = v_{Sa31}, purple = v_{Sa32}.*

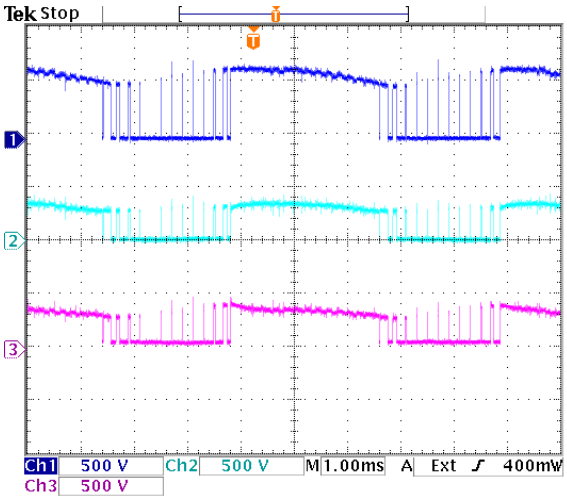


Figure 9.19: *Voltage sharing of switch pair S_{a4}. Dark blue= v_{Sa4}, light blue = v_{Sa41}, purple = v_{Sa42}.*

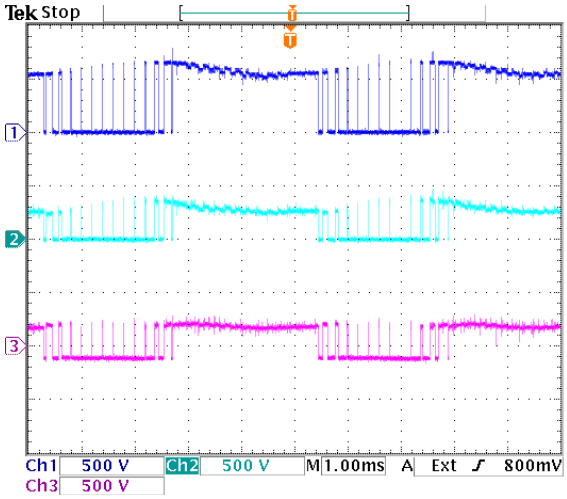


Figure 9.20: *Voltage sharing of switch pair S_{b1}. Dark blue= v_{Sb1}, light blue = v_{Sb11}, purple = v_{Sb12}.*

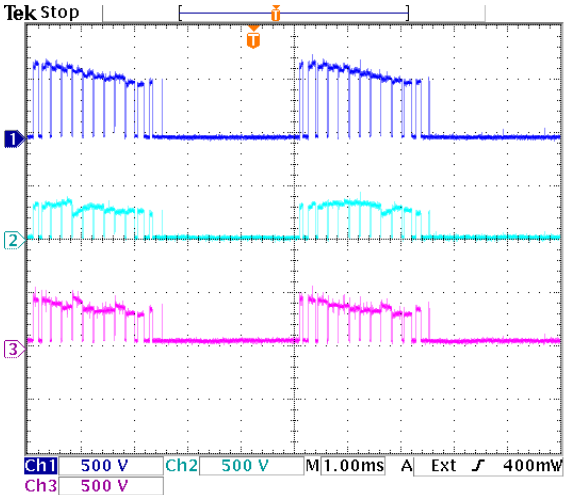


Figure 9.21: *Voltage sharing of switch pair S_{b2}. Dark blue= v_{Sb2}, light blue = v_{Sb21}, purple = v_{Sb22}.*

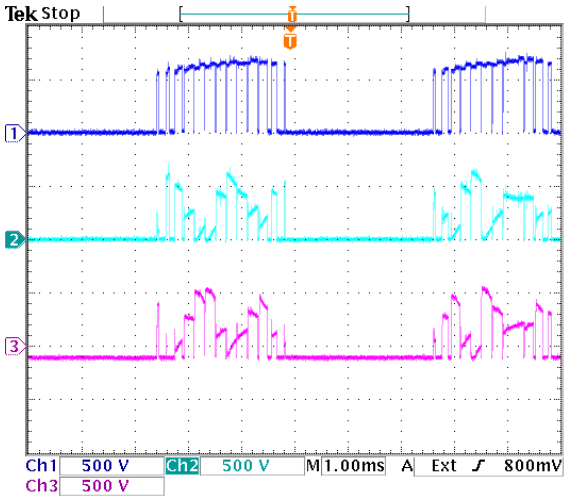


Figure 9.22: *Voltage sharing of switch pair S_{b3}. Dark blue= v_{Sb3}, light blue = v_{Sb31}, purple = v_{Sb32}.*

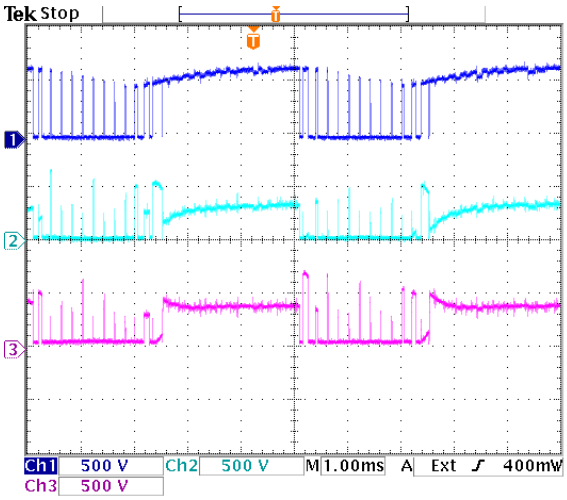


Figure 9.23: *Voltage sharing of switch pair S_{b4}. Dark blue= v_{Sb4}, light blue = v_{Sb41}, purple = v_{Sb42}.*

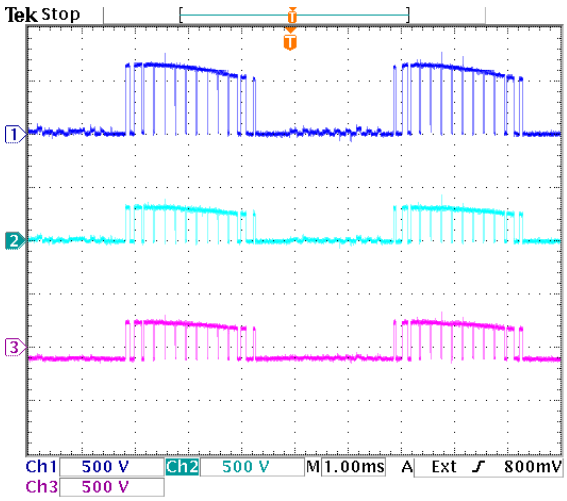


Figure 9.24: *Voltage sharing of diode pair D_{a1}. Dark blue= v_{Da1}, light blue = v_{Da11}, purple = v_{Da12}.*

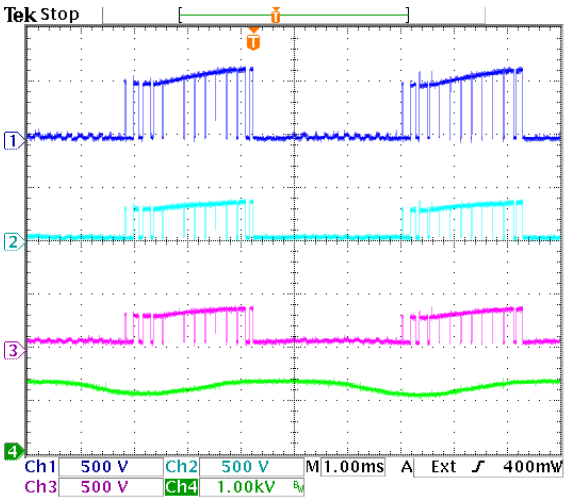


Figure 9.25: *Voltage sharing of diode pair D_{a2}. Dark blue= v_{Da2}, light blue = v_{Da21}, purple = v_{Da22}, green = DC link voltage.*

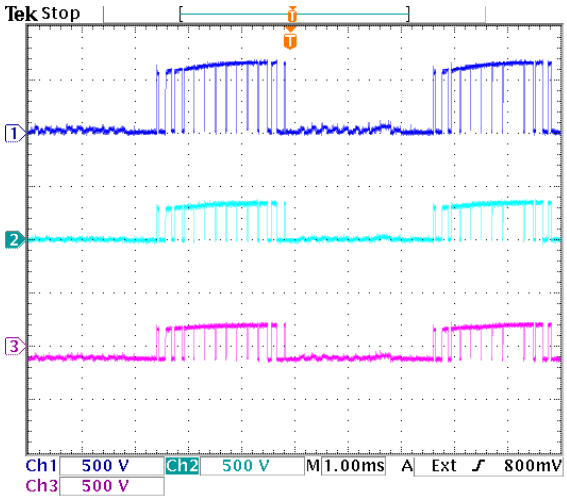


Figure 9.26: *Voltage sharing of diode pair D_{b1}. Dark blue= v_{Db1}, light blue = v_{Db11}, purple = v_{Db12}.*

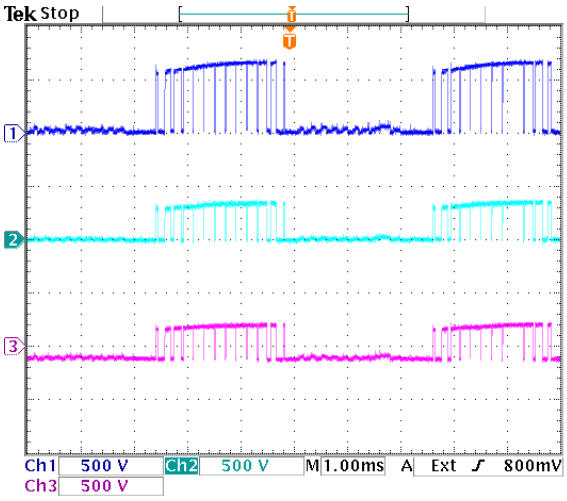


Figure 9.27: *Voltage sharing of diode pair D_{b2}. Dark blue= v_{Db2}, light blue = v_{Db21}, purple = v_{Db22}.*

9.3 Final test at $V_{DC} = 2.4kV$ and $\hat{i}_{load} = \pm 100A$

The purpose of this test is, to verify the data from the simulation of the previous chapter. The goal is, to obtain detailed data regarding the voltage sharing and dynamic performance of the switches. It is expected, that the voltage deviation of the individual switches never surpass $\Delta V_{ce,max} = 200V$. The overall voltage sharing of each switch or diode pair is shown next to a zoom in of the off transition. This is done to be able to comment of both dynamic and static performance of the inverter. The results are shown from figure 9.28 to 9.53.

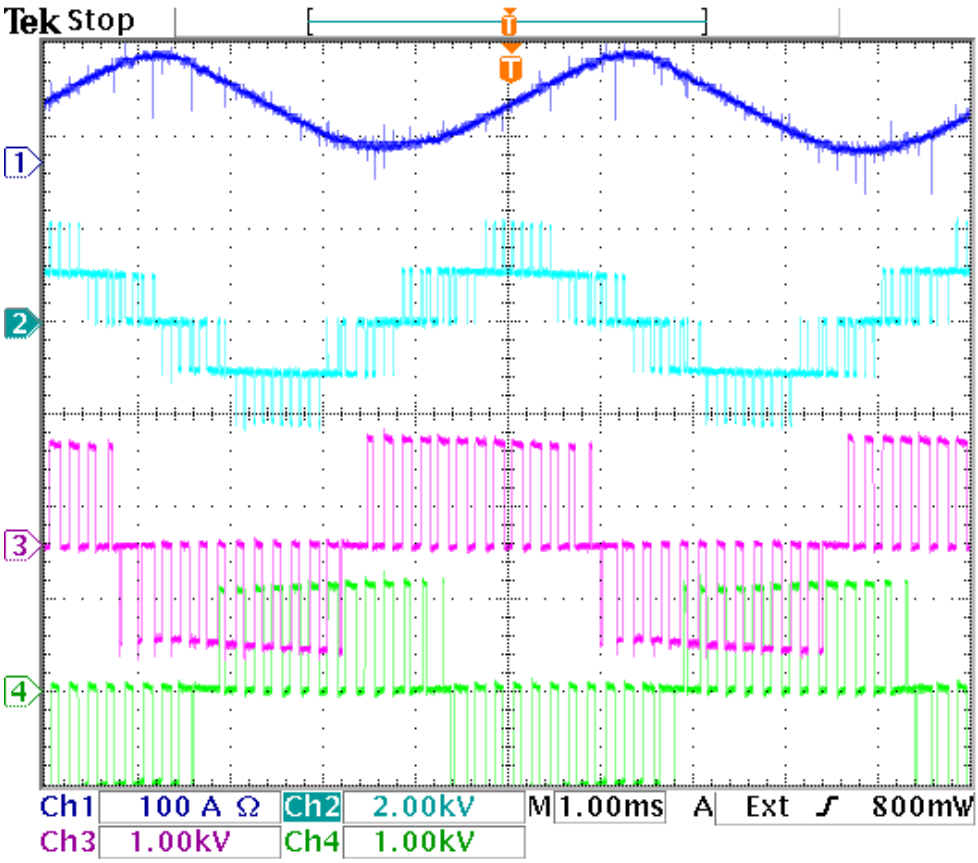


Figure 9.28: *Output waveforms for final test. Dark blue= i_{load}, light blue = v_{ab}, purple = v_{aN} and green = v_{bN}.*

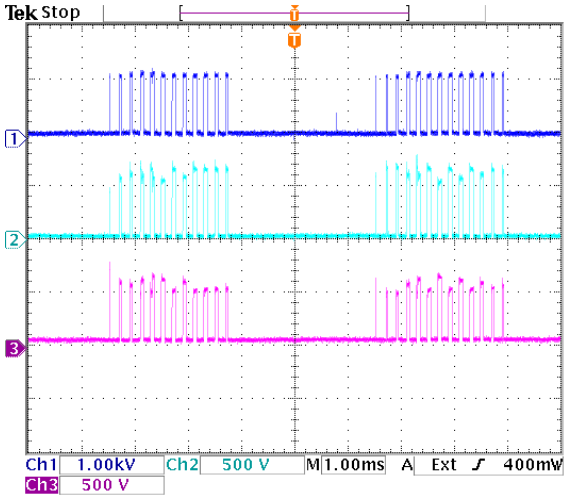


Figure 9.29: *Voltage sharing of switch pair S_{a1}. Dark blue= v_{Sa1}, light blue = v_{Sa11}, purple = v_{Sa12}.*

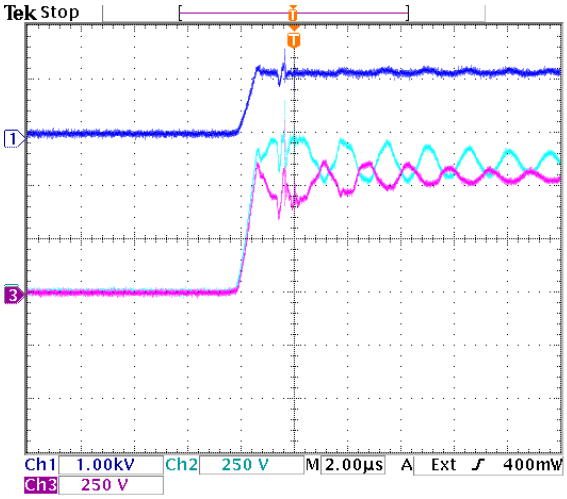


Figure 9.30: *Zoom of turn off transition of switch pair S_{a1}. Dark blue= v_{Sa1}, light blue = v_{Sa11}, purple = v_{Sa12}.*

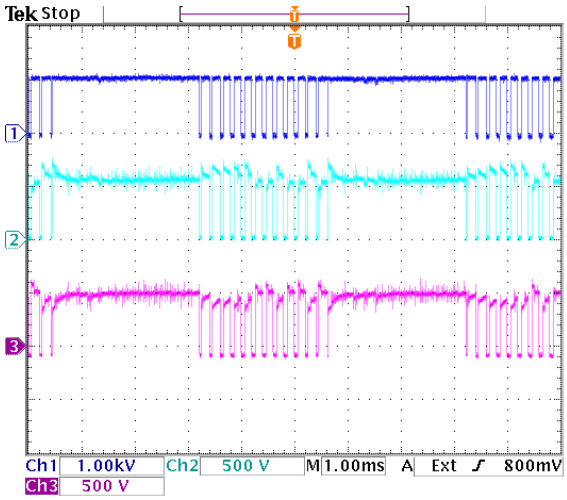


Figure 9.31: *Voltage sharing of switch pair S_{a2}. Dark blue= v_{Sa2}, light blue = v_{Sa21}, purple = v_{Sa22}.*

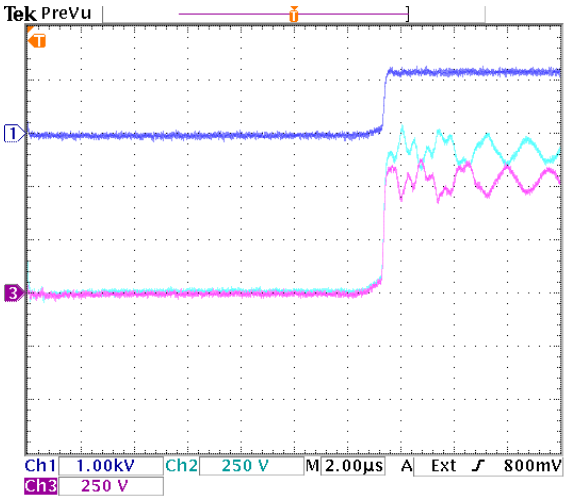


Figure 9.32: *Zoom of turn off transition of switch pair S_{a2}. Dark blue= v_{Sa2}, light blue = v_{Sa21}, purple = v_{Sa22}.*

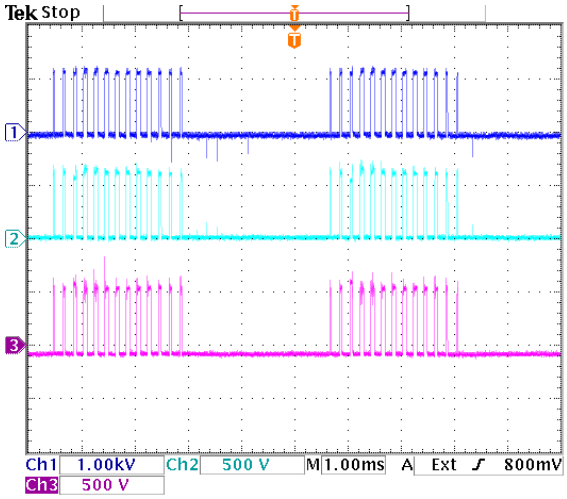


Figure 9.33: *Voltage sharing of switch pair S_{b3}. Dark blue= v_{Sa3}, light blue = v_{Sa31}, purple = v_{Sa32}.*

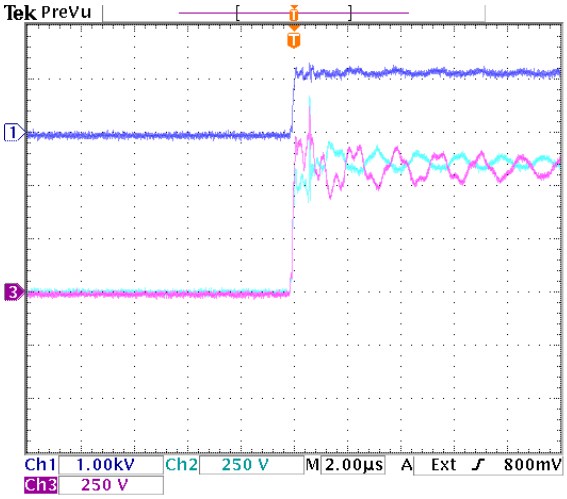


Figure 9.34: *Zoom of turn off transition of switch pair S_{a3}. Dark blue= v_{Sa3}, light blue = v_{Sa31}, purple = v_{Sa32}.*

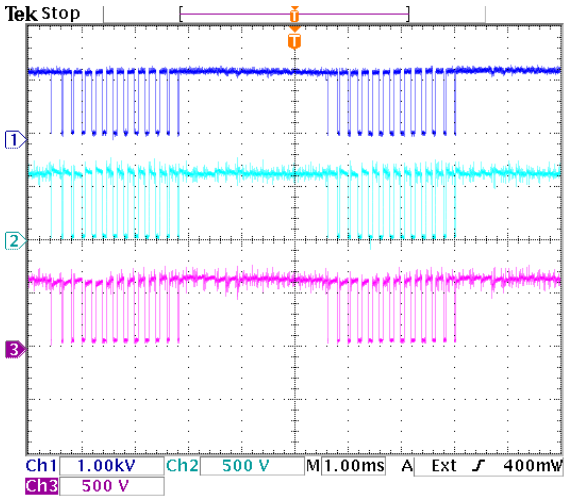


Figure 9.35: *Voltage sharing of switch pair S_{a4}. Dark blue= v_{Sa4}, light blue = v_{Sa41}, purple = v_{Sa42}.*

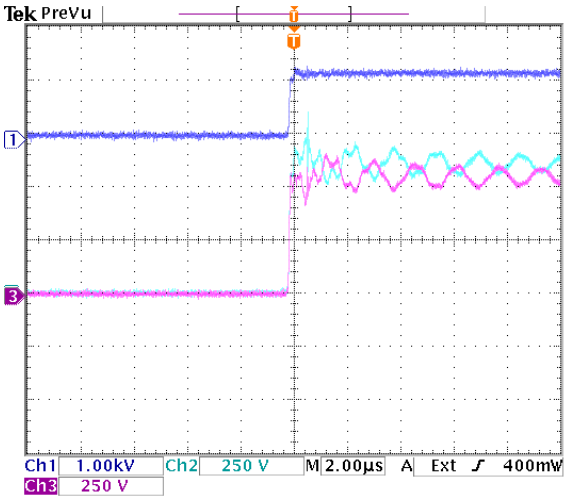


Figure 9.36: *Zoom of turn off transition of switch pair S_{a4}. Dark blue= v_{Sa4}, light blue = v_{Sa41}, purple = v_{Sa42}.*

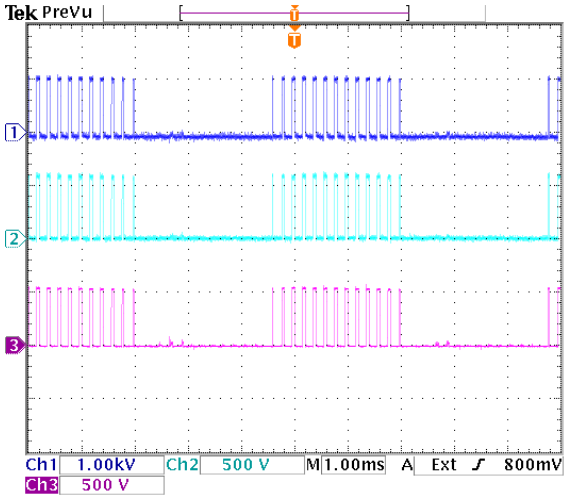


Figure 9.37: *Voltage sharing of diode pair D_{a1}. Dark blue= v_{Da1}, light blue = v_{Da11}, purple = v_{Da12}.*

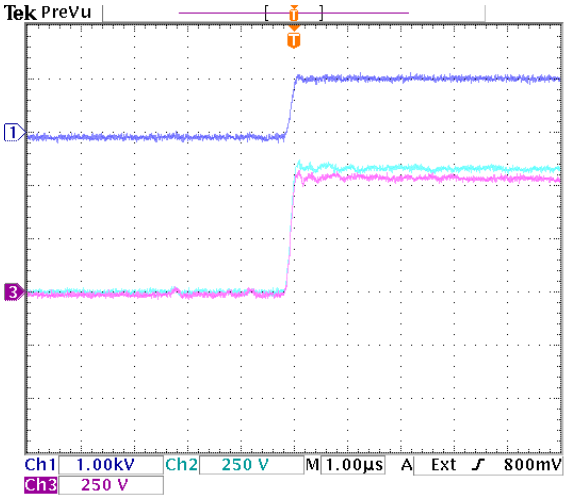


Figure 9.38: *Zoom of turn off transition of the diode pair D_{a1}. Dark blue= v_{Da1}, light blue = v_{Da11}, purple = v_{Da12}.*

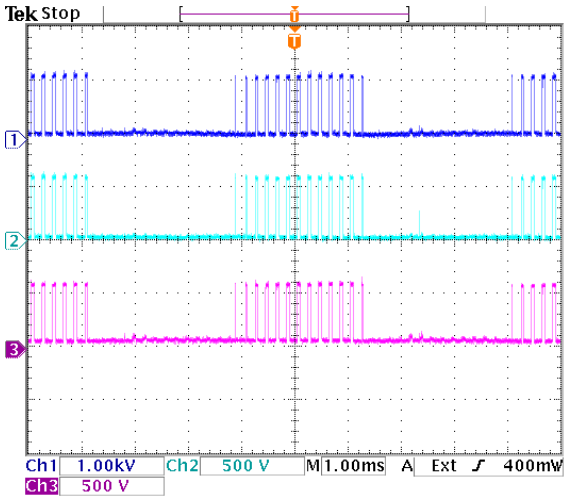


Figure 9.39: *Voltage sharing of diode pair D_{a2}. Dark blue= v_{Da2}, light blue = v_{Da21}, purple = v_{Da22}.*

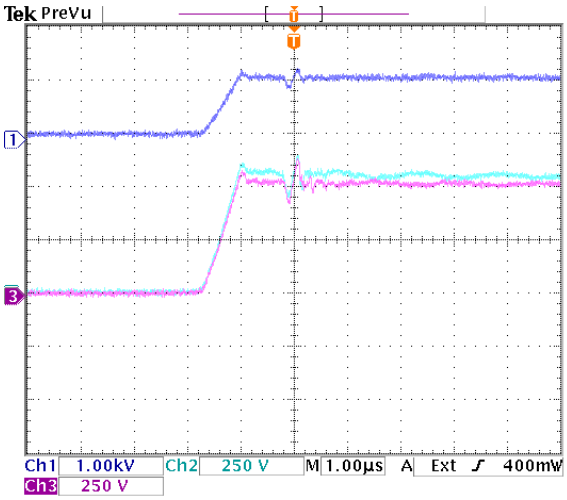


Figure 9.40: *Zoom of turn off transition of diode pair D_{a2}. Dark blue= v_{Da2}, light blue = v_{Da21}, purple = v_{Da22}.*

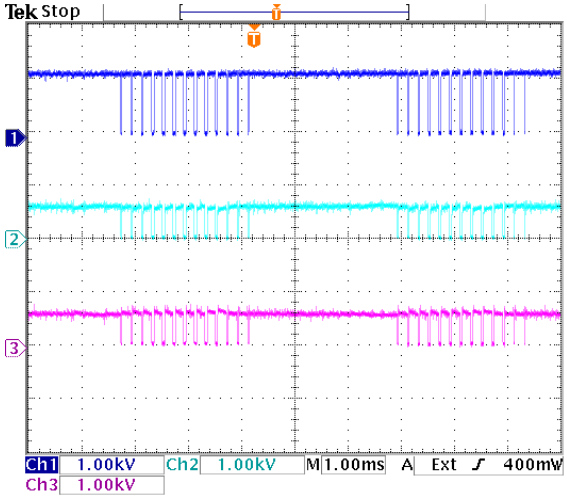


Figure 9.41: *Voltage sharing of switch pair S_{b1}. Dark blue= v_{Sb1}, light blue = v_{Sb11}, purple = v_{Sb12}.*

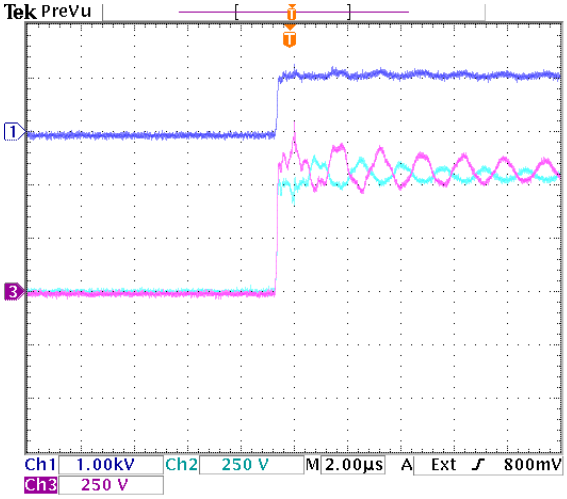


Figure 9.42: *Zoom of turn off transition of switch pair S_{a2}. Dark blue= v_{Sb1}, light blue = v_{Sb11}, purple = v_{Sb12}.*

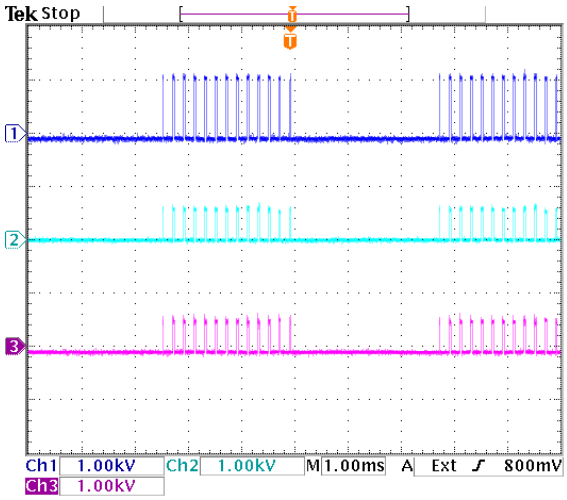


Figure 9.43: *Voltage sharing of switch pair S_{b2}. Dark blue= v_{Sb2}, light blue = v_{Sb21}, purple = v_{Sb22}.*

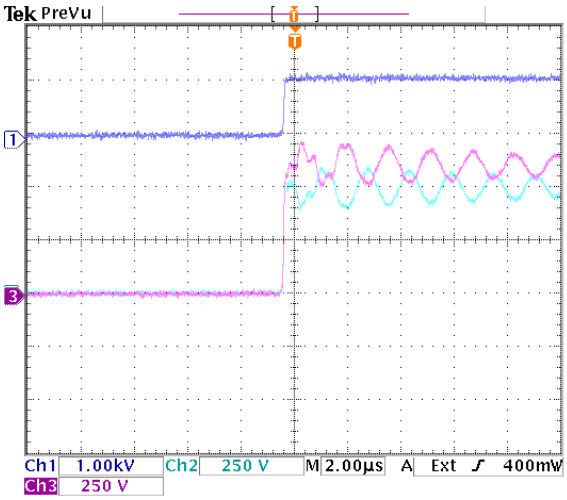


Figure 9.44: *Zoom of turn off transition of switch pair S_{a2}. Dark blue= v_{Sb2}, light blue = v_{Sb21}, purple = v_{Sb22}.*

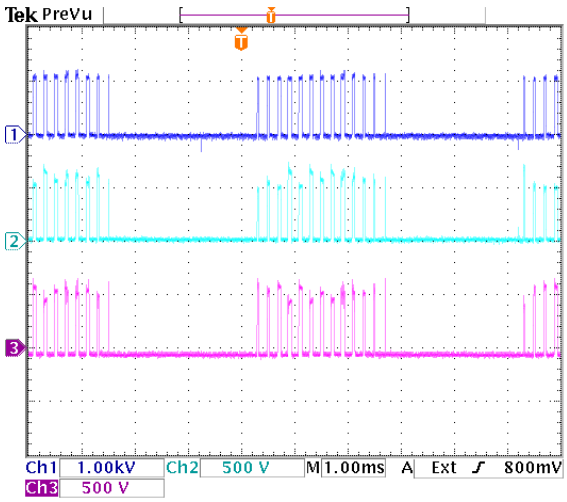


Figure 9.45: *Voltage sharing of switch pair S_{b3}. Dark blue= v_{Sb3}, light blue = v_{Sb31}, purple = v_{Sb32}.*

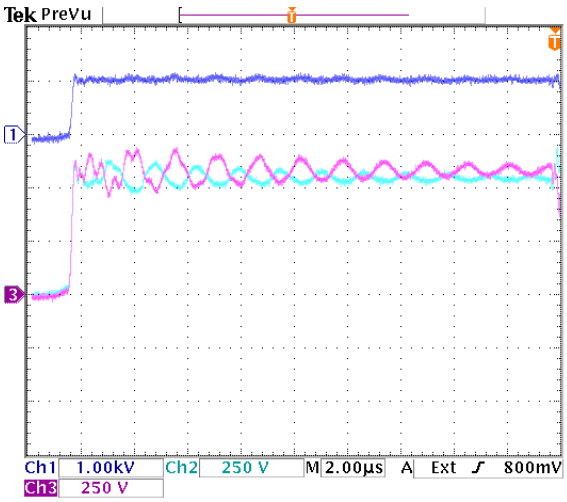


Figure 9.46: *Zoom of turn off transition of switch pair S_{b3}. Dark blue= v_{Sb3}, light blue = v_{Sb31}, purple = v_{Sb32}.*

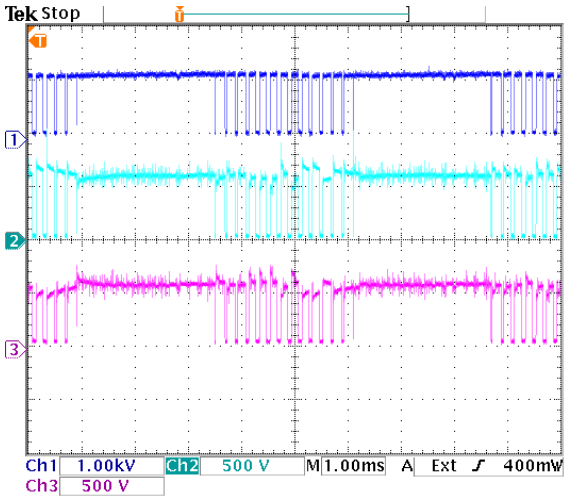


Figure 9.47: *Voltage sharing of switch pair S_{b4}. Dark blue= v_{Sb4}, light blue = v_{Sb41}, purple = v_{Sb42}.*

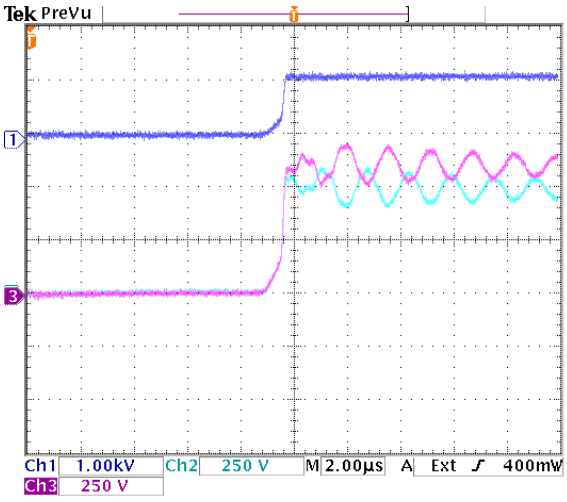


Figure 9.48: *Zoom of turn off transition of switch pair S_{a4}. Dark blue= v_{Sb4}, light blue = v_{Sb41}, purple = v_{Sb42}.*

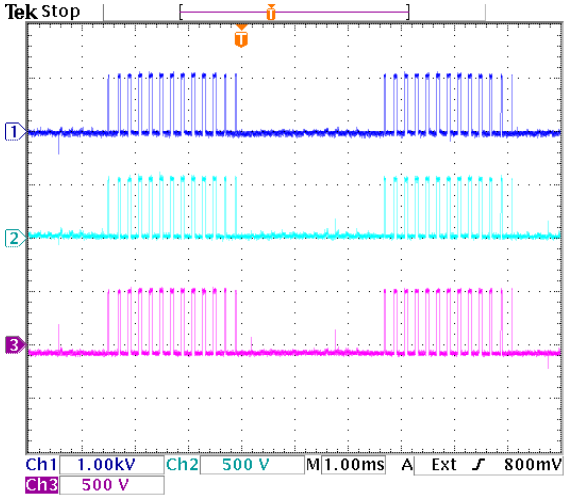


Figure 9.49: *Voltage sharing of diode pair D_{b1}. Dark blue= v_{Db1}, light blue = v_{Db11}, purple = v_{Db12}.*

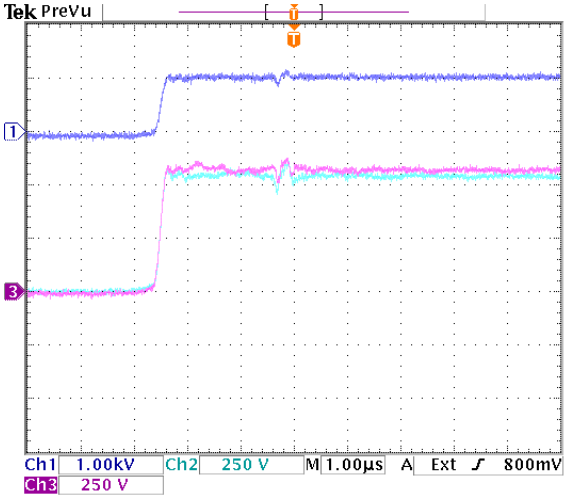


Figure 9.50: *Zoom of turn off transition of diode pair D_{b1}. Dark blue= v_{Db1}, light blue = v_{Db11}, purple = v_{Db12}.*

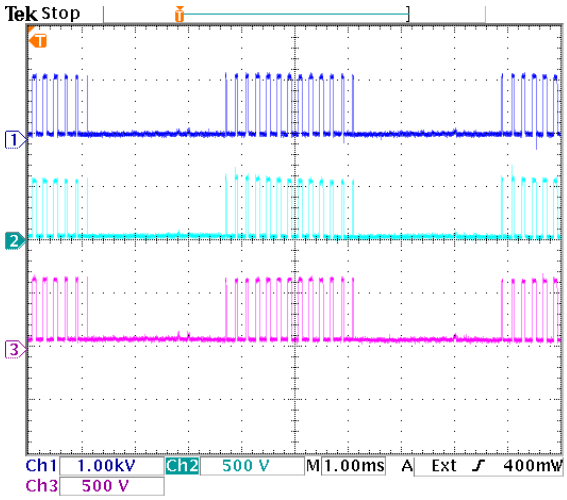


Figure 9.51: *Voltage sharing of diode pair D_{b2}. Dark blue= v_{Db2}, light blue = v_{Db21}, purple = v_{Db22}.*

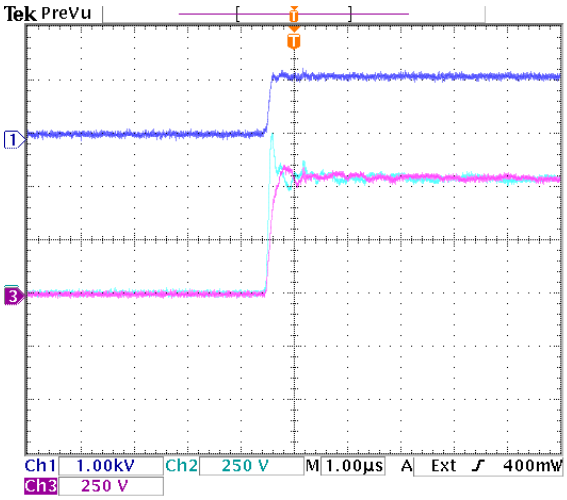


Figure 9.52: *Zoom of turn off transition of diode pair D_{b2}. Dark blue= v_{Db2}, light blue = v_{Db21}, purple = v_{Db22}.*

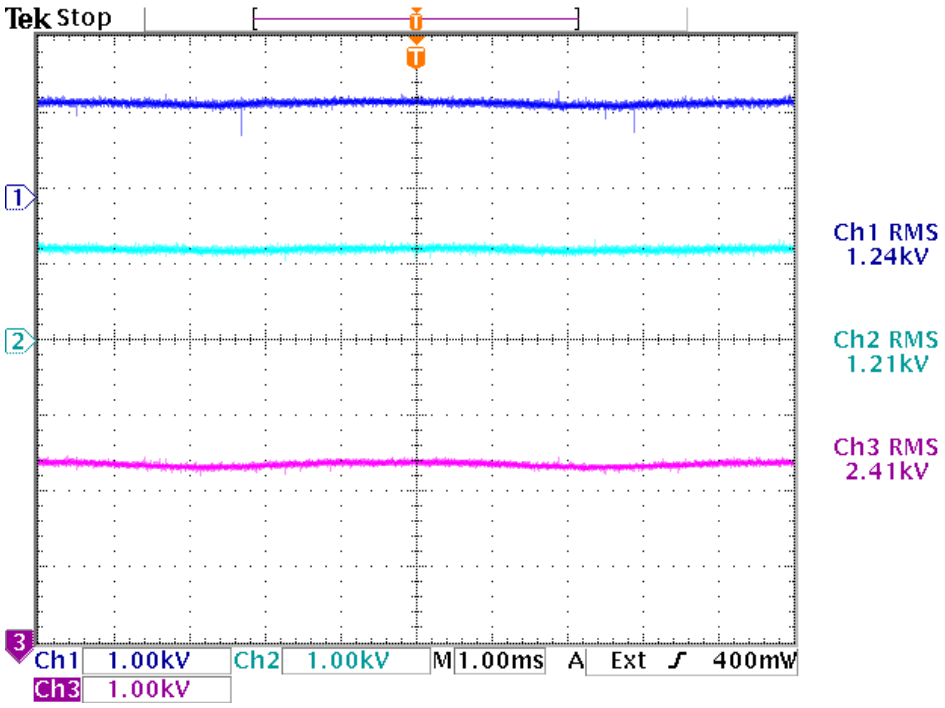


Figure 9.53: *DC link voltage. Dark blue= upper* $\frac{V_{DC}}{2}$*, light blue = lower* $\frac{V_{DC}}{2}$*, purple =* V_{DC}*.*

9.3.1 Conclusion of final test at $V_{DC} = 2.4kV$ and $\widehat{i}_{load} = \pm 100A$

The output waveforms of figure 9.28 showed, that like the $V_{DC} = 1.2kV$ test, the load current has a $\approx 70A$ DC offset. This current offset prevents the current from reaching the simulated $\widehat{i}_{load} = \pm 100A$, because the DC offset causes saturation in the load inductors. The offset is most likely caused by timing deviations, or an unbalanced neutral point, resulting in the output voltage having a DC offset. This offset in the voltage combined with the fact that the resistivity of the load, busbar and wires are in the $100m\Omega$ area means:

$$V_{DC,offset} = I_{DC,offset} \cdot R_{DC} = 70A \cdot 0.1\Omega = 7V \tag{9.3}$$

So just $7V$ of DC offset in the voltage out of the $2.4kV$ can cause the $70A$ DC current offset. Due to time constrains of the project, the reason for the offset is not investigated further.
Figure 9.28 also shows, that the three-level performance is obtained in the voltage waveforms. Also, the effect of the DC link voltage ripple can be seen in the voltage, but due to the fact, that the load current is not pushed to the maximum value, the simulations of the ripple voltage from section 7.3 can not be verified. The DC link voltage is shown on figure 9.53.
In regards to the voltage sharing of the individual switches, the static voltage sharing is acceptable.
Regarding the dynamic performance of the snubber, some unexpected results are obtained. Overall, the performance of the snubber is as expected, meaning that it clamps the voltage at the specified $V_{ce} = 700V$. But it can be seen in almost all the zoom figures of the switches, that the first transition is not clamped. Taking the time division into account, it can also be noted that the overshoot happens around $500 - 800ns$ into the off transition. This could imply, that the overshoot is due to the collector current in the IGBT module turning off. Remembering that the voltage rises before the current falls in the IGBT, and the off time of the used IGBT is $\approx 480ns$ according to appendix A.3 page 161, the overshoot can be induced voltage between the measurement terminals, even though the measure probes are placed as close to the terminals of the device as possible.

The diodes static voltage sharing results are very satisfactory, and the dynamic voltage sharing of figure 9.38, 9.40 and 9.50 is also way within the accepted limits. The dynamic sharing of diode pair D_{b2} on figure

9.52 shows a $150V$ overshoot for v_{Db21}. This has been further investigated by measuring the components, and the measurement shows, that the capacitor of diode snubber D_{b22} is approximately 2% larger that the other capacitors. This means, that the snubber of D_{b21} will charge faster.

There is a difference in diode voltage slope of figure 9.38 and 9.40. This is not an error, but a result of the data being sampled at difference instances in time. In figure 9.38, the instantaneous value of the current is larger than in figure 9.40, hence charging the capacitor of the snubber faster.

9.4 Short circuit test

In this section, the inverter is short circuited to verify the functionality of the protection scheme. The demands for the protection of the inverter are:

- IGBTs have to be shut down within $10\mu s$ after desaturation is entered.
- The over voltage associated with the hard switched shut down, performed by the gate drivers, has to be clamped at $v_{ce,max} = 700V$.
- The error must be latched, such that the protection and the system has to be manually reset after an error.
- In the case of a slow fault, the DSP has to shut down the inverter.

To create the short circuit, the inverter is short circuited phase to phase by a short wire. A gate pulse of $t = 100\mu s$ is then applied to the appropriate switches th create the shot through. Figure 9.54 shows, how the short circuit test is set up. To test the protection circuits of all IGBTs, two tests are performed.

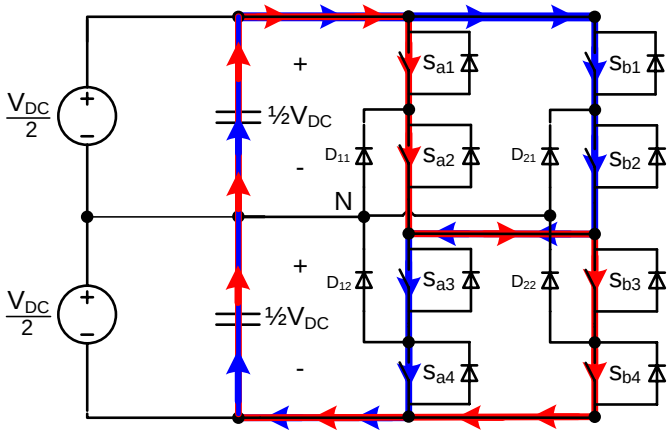


Figure 9.54: *Schematic of short circuit test. The red line is the current path for test 1, and the blue line is the current path for test 2.*

The DC link voltage is kept to $V_{DC} = 600V$ for safety, and the two Delta power supplies from the initial test is used as voltage sources.

On figure 9.54 it can be seen, that during test 1, the switch pairs S_{a1}, S_{a2}, S_{b3} and S_{b4} are turned on by the applied gate pulse. In test 2, the switches are mirrored, such that the short circuit path is though S_{b1}, S_{b2}, S_{a3} and S_{a4}. The reason for this is, that the layout does not allow for current measurements in one leg.

On the figures 9.55 to 9.66, the short circuit current, the v_{ce} and v_{ge} of the individual IGBTs can be seen. It must be mentioned, that the scopes used for test is synchronized by triggering on the same gate signal. This signal is therefore shown in the top of every figure. The gate signal of the IGBT's is measured to verify, that all IGBT's turns off, and stay turned off, when an error occurs. This is to verify the latching action of the optical hub.

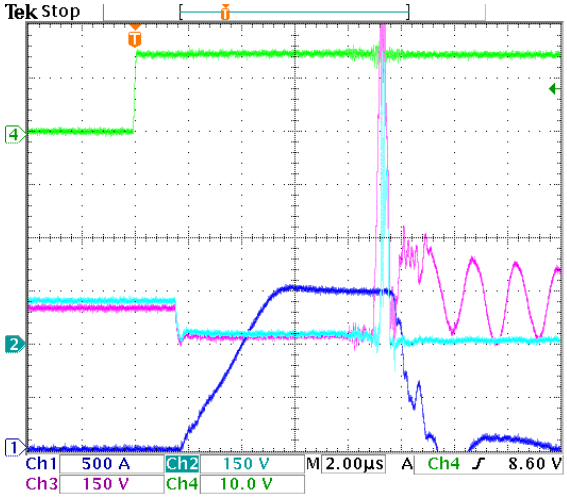


Figure 9.55: *Short circuit test 1. Dark blue= i_{load}, light blue = $v_{ce,Sa11}$, purple = $v_{ce,Sa12}$, green = gate trigger signal.*

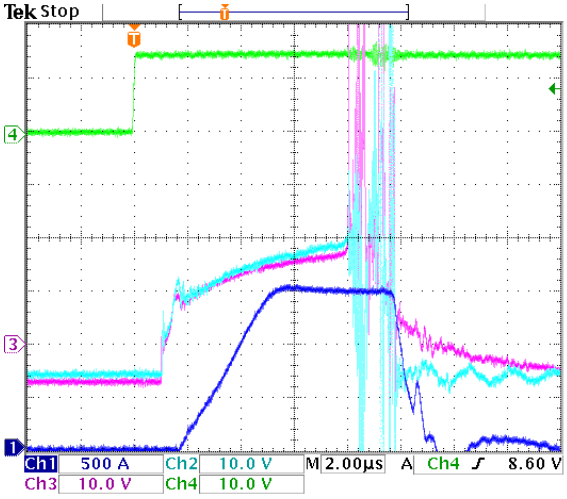


Figure 9.56: *Gate signals of short circuit test 1. Dark blue= i_{load}, light blue = $v_{ge,Sa11}$, purple = $v_{ge,Sa12}$, green = gate trigger signal.*

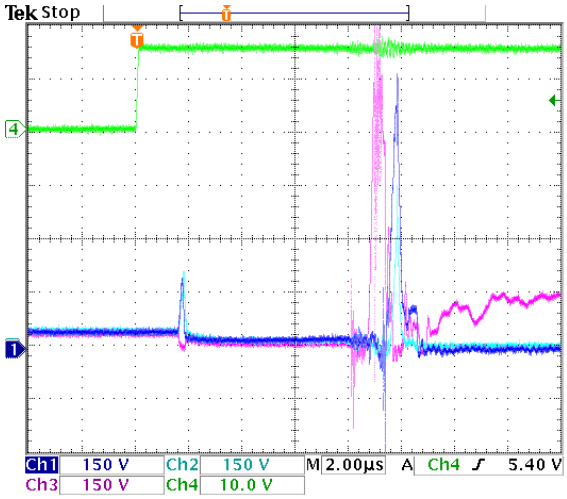


Figure 9.57: *Short circuit test 1. Dark blue= $v_{ce,Sa21}$, light blue = $v_{ce,Sa22}$, purple = $v_{ce,Sb31}$, green = gate trigger signal.*

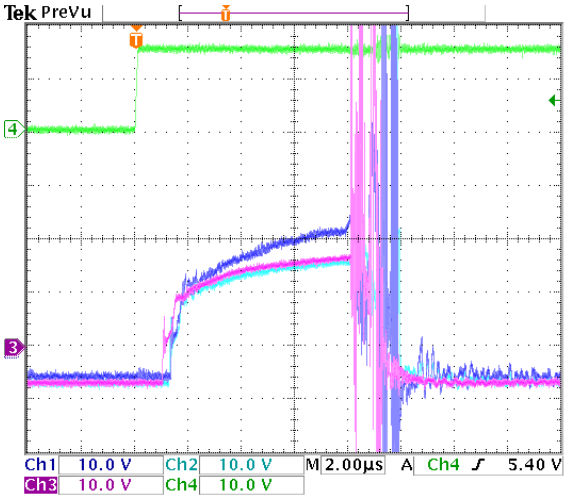


Figure 9.58: *Gate signals of short circuit test 1. Dark blue= $v_{ge,Sa21}$, light blue = $v_{ge,Sa22}$, purple = $v_{ge,Sb31}$, green = gate trigger signal.*

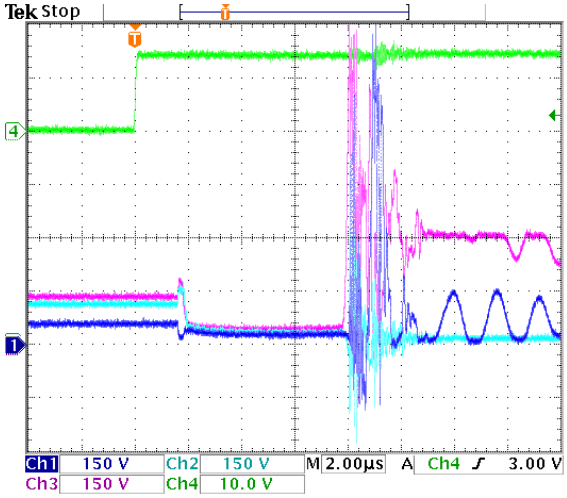


Figure 9.59: *Short circuit test 1. Dark blue= $v_{ce,Sb32}$, light blue = $v_{ce,Sb31}$, purple = $v_{ce,Sb32}$, green = gate trigger signal.*

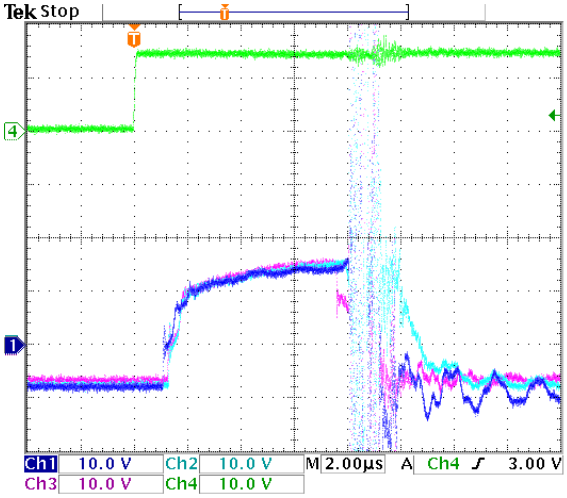


Figure 9.60: *Gate signals of short circuit test 1. Dark blue= $v_{ge,Sb32}$, light blue = $v_{ge,Sb41}$, purple = $v_{ge,Sb42}$, green = gate trigger signal.*

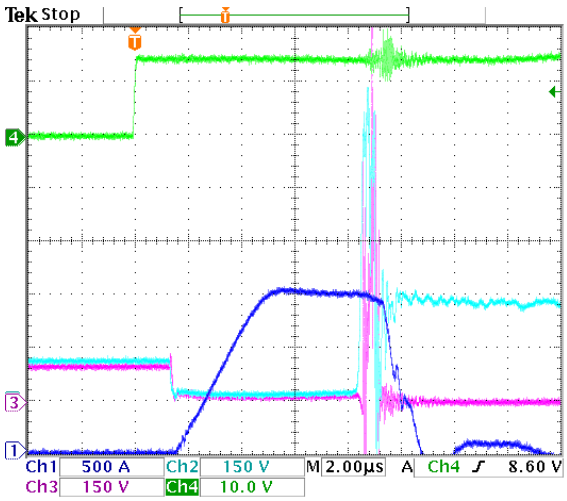


Figure 9.61: *Short circuit test 2. Dark blue = i_{load}, light blue = $v_{ce,Sb11}$, purple = $v_{ce,Sb12}$, green = gate trigger signal.*

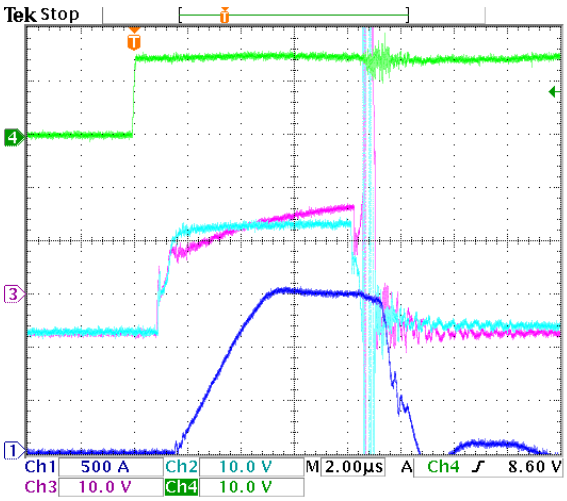


Figure 9.62: *Gate signals of short circuit test 2. Dark blue = i_{load}, light blue = $v_{ge,Sb11}$, purple = $v_{ge,Sb12}$, green = gate trigger signal.*

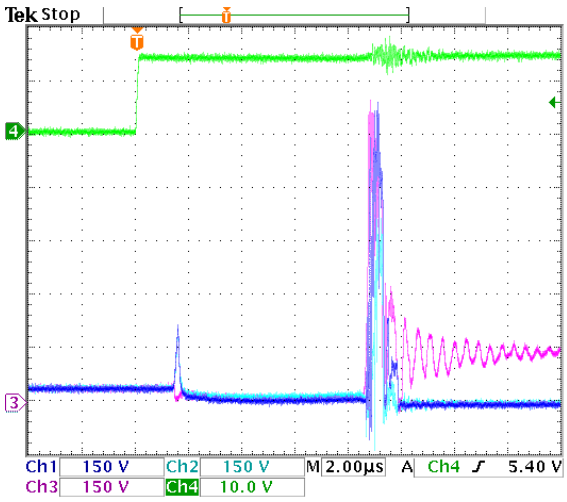


Figure 9.63: *Short circuit test 2. Dark blue= $v_{ce,Sb21}$, light blue = $v_{ce,Sb22}$, purple = $v_{ce,Sa31}$, green = gate trigger signal.*

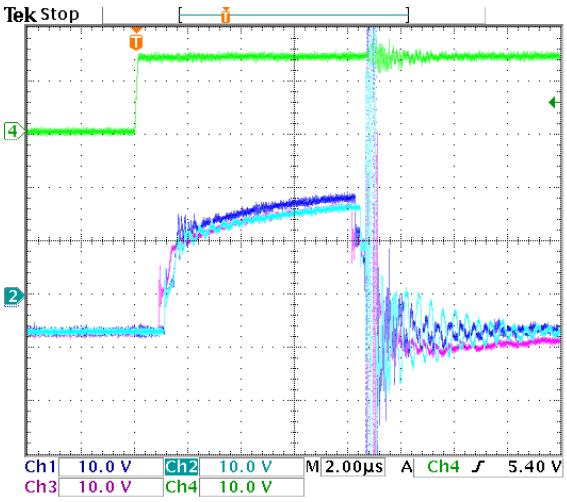


Figure 9.64: *Gate signals of short circuit test 2. Dark blue= $v_{ge,Sb21}$, light blue = $v_{ge,Sb22}$, purple = $v_{ge,Sa31}$, green = gate trigger signal.*

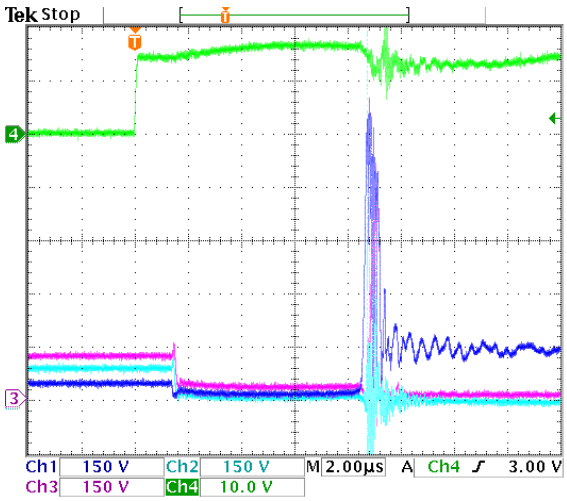


Figure 9.65: *Short circuit test 2. Dark blue= $v_{ce,Sa32}$, light blue = $v_{ce,Sa41}$, purple = $v_{ce,Sa42}$, green = gate trigger signal.*

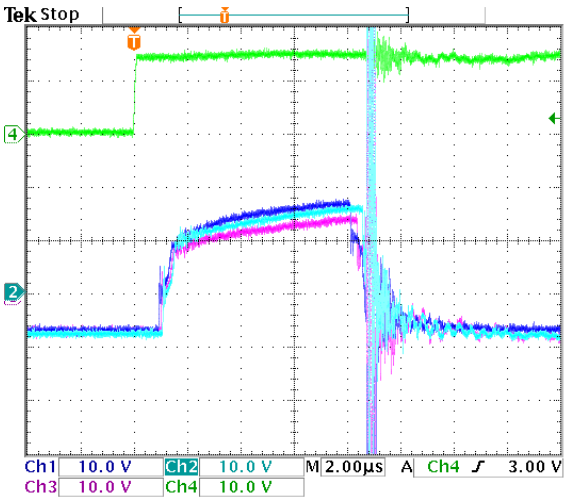


Figure 9.66: *Gate signals of short circuit test 2. Dark blue= $v_{ge,Sa32}$, light blue = $v_{ge,Sa41}$, purple = $v_{ge,Sa42}$, green = gate trigger signal.*

9.4.1 Conclusion on short circuit test

A detail, that can be noticed from figure 9.55 to 9.65 is, that the IGBTs in the off state (before the short circuit) has unequal voltage sharing. This is due to the fact, that the diode snubbers include a $200k\Omega$ static voltage sharing resistor, and hence the IGBTs S_{a21}, S_{a22}, S_{a31}, S_{a32}, S_{b21}, S_{b22}, S_{b31} and S_{b32} has only half the static resistance due to the fact, that the diode snubber is placed in parallel with these IGBTs. This changes the resistive voltage division, and is supported by the results.

The voltage sharing after the system has been shut down is unequal, but it will converge towards the steady state values. However there is no demand for this, because the system has to be manual reset after a fault.

A very important aspect of the short circuit test is the over voltages associated with the hard shut down. In almost every case on figure 9.55 to 9.64, the v_{ce} has a voltage spike that reaches above the clamping level of $700V$. This can be due to induced noise in the probes, but if this is not the case, then the clamping protection does not fulfil the requirements, even though the method has been tested in section 5.3 on page 73 and concluded functional. Steps have been taken to minimize measurement noise, such as twisting the wires on the differential probes, and keeping them separated from the busbar.

The gate signals prove, that either the optical hub turns off all the IGBTs after one of the gate drivers report an error, or the desaturation protection of the Skyper gate driver shut down the driver. This is supported by figure 9.59 and 9.60, where $v_{ge,Sb42}$ purple triggers because of the corresponding $v_{ce,Sb42}$ going into desaturation as the first IGBT of test 1. After switch S_{b42} shuts down, all the other affected IGBT's shuts down within $3\mu s$, the last of test 1 being switch S_{Sb41} on figure 9.60. It must be mentioned, that the Skyper gate driver interprets v_{ge} above $7.5V$ in the on state as desaturation, and therefore it is difficult to determine when the desaturation actually occurs. This is because both the current and voltage do not become as high as in section 5.3, due to the fact, that the resistance of the short circuit path is larger because of the high number of devices.

9.5 Conclusion on tests

In this chapter, the realized two phase three-level inverter, all the peripheral equipment and the protection scheme was tested. The result of the test was as follows:

The initial test at $V_{DC} = 600V$ proved, that all the switches worked, and that the inverter is capable of three-level performance and sinusoidal PWM modulation. This test verified the functionality of; the gate drivers, the IGBTs, the DSP interface and the code written for the modulation strategy.

The test at $V_{DC} = 1.2kV$ proved the functionality of the medium voltage PSU, and the effect of the third harmonic injection. This test also showed, that there is a DC offset in the current.

The final test of the system at $V_{DC} = 2.4kV$ proved, that the static voltage sharing was acceptable, and the overall dynamic voltage sharing was as expected from the simulation in the previous chapter. But there were voltage spikes above the clamping level. It was concluded, that these could be due to induced voltage in the probes. The performance of the diode snubbers was very satisfactory, except for one snubber where parameter deviances affected the dynamic performance. Like in the $1.2kV$ test, there was an offset in the current. This offset was properly caused by an unbalanced neutral point, or timing issues in the DSP. Because of the offset, the modulation index Ma could not be increased to 1.16, and therefore the goal of $\widehat{i}_{load} = \pm 100A$ could not be reached due to saturation issues of the load inductor cores. The time constrains for the project did not allow further analysis of this problem, but the offset of the current could be controlled by applying feedback control or adding an offset to the reference waveform.

The short circuit test showed, that the time demands of $10\mu s$ inverter shut down time after desaturation is upheld. The over voltage clamping protection however did not perform as expected, allowing v_{ce} voltage

spikes at $900V$. This is still within the ratings of the IGBTs, but above the specified values of $v_{ce,max} = 700V$, and therefore the crucial over voltage protection can not be concluded functional. Even though the voltage spikes can be due to measurement noise, these voltage spikes were also present in the final system test, although not to the same degree as in the short circuit test.

Chapter 10

Conclusion

The goal of the master thesis was, to analyze medium voltage inverters suited for wind turbine applications. The medium voltage level of the inverter should be obtained by means of series connecting standard IGBTs. In part I of the report, analysis of the three-level inverter topology, series connection of IGBTs, voltage balancing methods suited for series connection of IGBTs, and IGBTs under fault conditions was performed. The conclusions of these analysis were;

- The three-level inverter topology is well suited for medium voltage applications, it has lover THD than the two-level inverter, but is also more complex.
- The voltage imbalance in v_{ce} of two series connected devises was caused by parameter deviations and/or delays in the gate signals. The balancing of the IGBTs in series can be improved by adding snubbers. The best suited snubber for this project, of the analyzed snubbers, was the Zener clamped snubber.
- Series connection of two IGBTs will have lower switching losses compared to one IGBT with the double voltage rating. This means that two series IGBTs can be switched faster than one large IGBT, and have a lower total loss when the switching frequency reaches a level around 400Hz dependent of the type of IGBT.
- The analysis of the IGBT module under fault condition concluded, that the large power dissipation associated with desaturation, and the over voltage associated with hard shut down can be fatal to the IGBTs. The fault prevention scheme chosen for the project was desaturation detection and voltage clamping.

Based on these conclusions of the analysis part of the report, a two phase three-level inverter setup was designed, realized and tested. The inverter was rated for medium voltage ($V_{DC} = 2.4kV$) level, and based on series connected IGBTs. A fault protection scheme was design and implemented. This was based on desaturation detection and clamping of over voltage. The peripheral equipment needed for testing of the inverter was also designed realized and tested. This equipment included a medium voltage DC supply, a load inductor of $23mH$, gate drivers for the IGBTs, snubbers, optical hub for shut down and C-code and optical interface to a TI2812 DSP.
After realization of the inverter setup, the inverter system was tested against the requirements set in the problem formulation. These requirements were:

- DC link voltage $V_{DC} = 2.4kV \pm 10\%$.
- Peak load current $\widehat{i}_{load} = \pm 200A$ but dependent on load.
- Switching frequency $f_{sw} = 5kHz$.
- Modulation frequency $f_{mod} = 50Hz$.
- Maximum voltage deviation between series IGBTs $\Delta V_{ce,max} = 200V$.

- Protection maximum shut down time $t_{SD,max} \leq 10\mu s$ from fault occurs.
- Allowed over voltage due to hard switching $V_{ce,max} = 700V$.

The DC link voltage of $V_{DC} = 2.4kV \pm 10\%$ was reached, and the inverter performed as expectet in the test.
The peak load current of $\widehat{i}_{load} = \pm 200A$ was revised to $\widehat{i}_{load} = \pm 100A$ due to the capacitors. In the final test, a DC offset in the current caused the load inductor to saturate, when the current reached $\widehat{i}_{load,pp} = 100A$, and hence this demand is not fulfilled.
The test showed, that there was no problem associated with the switching frequency of $f_{sw} = 5kHz$, so this demand is satisfied.
The modulation frequency of $f_{mod} = 50Hz$ was revised to $f_{mod} = 200Hz$ to increase the impedance of the load. This was revised due to saturation issues.
In the final test, the static and dynamic performance of the switches verified the demand of $\Delta v_{ce,max} = 200V$. However there were voltage spikes that reached above $700V$, but these could be due to noise.
In regards to the protection scheme, the short circuit test showed, that the protection maximum shut down time $t_{SD,max} \leq 10\mu s$ was upheld. However, the allowed over voltage reached above the clamping level of $v_{ce} = 700V$, so the over voltage protection is not acceptable according to the test.

The conclusion of the project is, that medium voltage level can be obtained by series connection of standard IGBT modules, this is in theory also associated with lower switching losses, and hence the switching frequency can be increased compared to a single IGBT. Also, the three-level inverter is well suited for medium voltage applications, due to its voltage sharing nature. The zener clamped snubber is a simple and reliable snubber topology, but using it as over voltage protection in short circuit situations has limitations.

Chapter 11

Perspective

During this Master Thesis, we have been very fortunate by cooperating with Siemens Wind Power. We have had the chance to discuss our solutions and ideas, and also the limiting factors of implementing medium voltage technology in real wind turbine applications. What we have experienced is, that implementing medium voltage inverters and generators may not be the largest challenge, but the safety rules in regards to service of the wind turbines and space requirements of the three-level topology in an already crowded nacelle, is the real challenges that has to be solved, in order to push a shift in technology.
Regarding the series connection of IGBTs, the results, and especially the fact that series IGBTs can be switched faster than one lager device, makes this approach toward medium voltage performance interesting. This is because switching an inverter faster lowers the requirements for the output filter, and also base band noise is reduced.

Further Development

The main part of the work effort of this project was spent on designing, debugging and testing hardware. This has resulted in a working two-phase three-level inverter. The next logical step is, to duplicate one of the legs, and build the full three-phase setup. This setup can now be used for testing of modulation strategies suited for the three-level inverter. Also experimental data at high power levels can be obtained, like the ones in this report, meaning that the real life effect of modulation strategies, such as THD, over voltage, common mode voltage and power dissipation and loss optimization can be investigated at medium voltage level.

Regarding the snubbers chosen for further analysis in this project, it seams like the passive snubber could be interesting to apply to the IGBTs. This is based on its almost flawless performance, and its independence of the DC link voltage. However care must be taken regarding power dissipation and conflicts with dead time.

The performance of the clamping protection was not as expected, when it went from stand alone test to the realized total setup. The "ringing" behavior of the snubber have been observed before, when the clamp by accident was placed between the collector and emitter. This could imply that the gate protection, which is a bipolar transil diode, clamps the collector emitter unintended. Why this did not happen in the stand alone test needs further investigating. Also, a short circuit test at $V_{DC} = 2.4kV$ could be performed to see if the voltage level reach above the rated value.

Chapter 12

Nomenclature List

Parameter:	**Variable:**	**Value:**
DC link voltage	V_{DC}	$0 - 2.4kV$
Load current	$\widehat{i}_{load}$	$\pm 0 - 100A$
Load resistance	R_{load}	$-$
Load inductance	L_{load}	$-$
Load impedance	Z_{load}	$-$
Phase to phase voltage	v_{ab}	$0 - 2.4kV$
Phase to neutral voltage	v_{aN}	$-$
Star point to neutral point voltage	v_{sN}	$-$
Phase to star point voltage	v_{as}	$-$
Modulation index for fundamental	Ma_1	$0 - 1.16$
Modulation index for third harmonic	Ma_3	$0 - \frac{1}{6}$
Modulation sine wave	v_{sin}	$0 - 1$
Upper carrier wave signal	$v_{tri,upper}$	$0 - 1$
Lower carrier wave signal	$v_{tri,lower}$	$0 - 1$
Modulation frequency	f_{mod}	$200Hz$
Switching frequency	f_{sw}	$5kHz$
Switching period	T_{sw}	$200\mu s$
IGBT on state voltage drop	$v_{ce,on}$	$-$
IGBT off state voltage	$v_{ce,off}$	$-$
IGBT collector current	i_c	$-$
IGBT leakage current	$i_{c,off}$	$-$
IGBT gate emitter voltage	v_{ge}	$-$
IGBT gate emitter threshold voltage	$v_{ge,th}$	$-$
IGBT collector gate voltage	v_{cg}	$-$
IGBT gate emitter capacitance	C_{ge}	$-$
IGBT collector emitter capacitance	C_{ce}	$-$
IGBT collector gate capacitance	C_{cg}	$-$
IGBT gate resistance	R_g	$-$
DSP dead time	t_{dead}	$2\mu s$

Table 12.1: *Nomenclature list.*

Chapter 13

Contents of CD-ROM

- **Articles:**
  - This folder contains all articles used as references in the bibliography.
- **Data sheets:**
  - This folder contains all data sheets related to the software and hardware used in the laboratory.
- **Pictures:**
  - This folder contains additional pictures of the laboratory test setup.
- **Report source files:**
  - This folder contains all source files in the Latex project file structure.
- **Simulation files:**
  - This folder contains all files used for Matlab and OrCad simulations .
- **Software:**
  - This folder contains some additional free ware used for the project.
- **PCB files:**
  - This folder contains printable PCB layouts for the snubbers, gate drivers and DSP extension board.
- **DSP:**
  - This folder contains the *C* code for the DSP.

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Part III:
Appendix

Appendix A

IGBT characteristics

The IGBTs are devices, that have combined characteristics of a BJT and a MOSFET. The BJT has low conduction losses in the on state, specially for devices with larger blocking voltages compared to MOSFET's, but they have longer switching times and are current controlled. The voltage controlled MOSFET can switch faster than the BJT, but they have higher conduction losses. The combination of these two semiconductors is the IGBT, which have the best features of each one.

A.1 Equivalent circuit model

As mentioned, the IGBT is a combination of the BJT and the MOSFET. It is not easy to model exactly, but some approximation can be made. Figure A.1 shows one equivalent circuit, among several, for the IGBT.

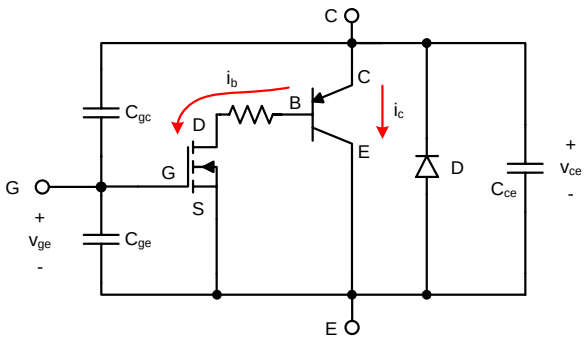

Figure A.1: *Equivalent circuit for the IGBT.*

The combination of the BJT and the MOSFET here is clear. In the on state with high gate voltage, the MOSFET will conduct the base current from collector to base, and the BJT will be in the on state. The C_{ge} is the gate capacitance, that is charged during turn on and vice versa. Because of this capacitance, the gate emitter voltage can not change from zero to the final gate voltage in zero time. C_{gc} is the capacitance between gate and collector, and this is strongly dependent of the gate collector voltage v_{gc} because of the internal structure of the IGBT. The capacitance C_{ce} is the capacitance between the power terminals of the IGBT. This is also dependent on the voltage v_{ce}.

The diode D is a freewheeling diode, which is typically an integrated part of the silicon of the IGBT. This is added to achieve an alternative current path, to prevent destruction of the device, when applying inductive loads. All of the internal capacitances mentioned, characterize the IGBT ans have great influence on the switching characteristics of the IGBT. These are described in more detail in section A.1.2.

A.1.1 Current voltage characteristics

The i/v characteristics of an n-channel IGBT, which is commonly used, are shown in figure A.2 and A.3, which show similarities to a BJT except, that the controlling parameter is a voltage, the gate emitter voltage, instead of a current.

The transfer curve i_c/v_{ge} from figure A.2 is identical to that of a power MOSFET. Above $v_{ge,th}$ the curve is linear, becoming non linear, when the value is close to $v_{ge,th}$. If v_{ge} is smaller than the threshold voltage, then the IGBT is turned off.

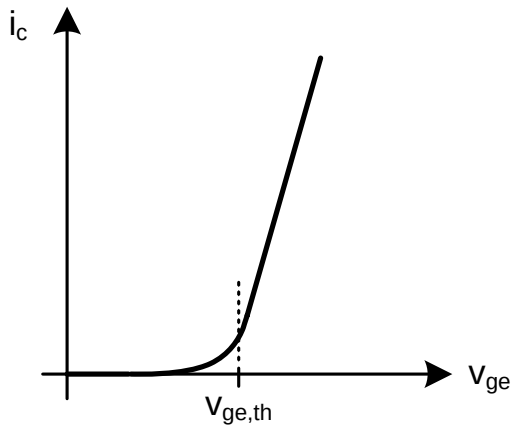

Figure A.2: *Transfer characteristic for an n-channel IGBT.*

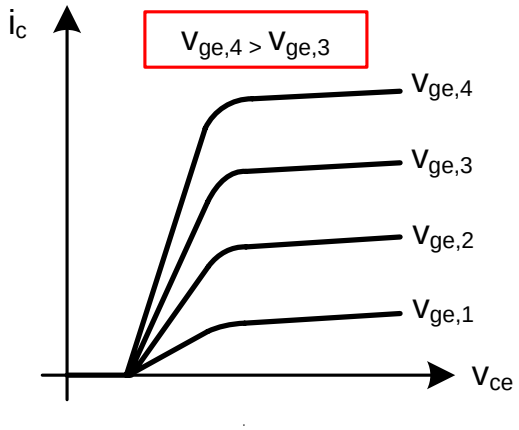

Figure A.3: *Output characteristics for the n-channel IGBT.*

Figure A.3 shows, how the maximum value of i_c depends on the gate emitter voltage. For small gate emitter voltage, the current will be equally low. The figure also shows, that the on state collector to emitter voltage v_{ce} depends on the current for a constant v_{ge}.

A.1.2 Switching waveforms

The switching waveforms for the turn on and turn off transients are shown in figure A.4. As shown, both transients do not happen instantaneously, but are delayed depending on the quantities of the internal capacitances. In the turn on, the current rises before the voltage across the IGBT drops, and opposite for the turn off.

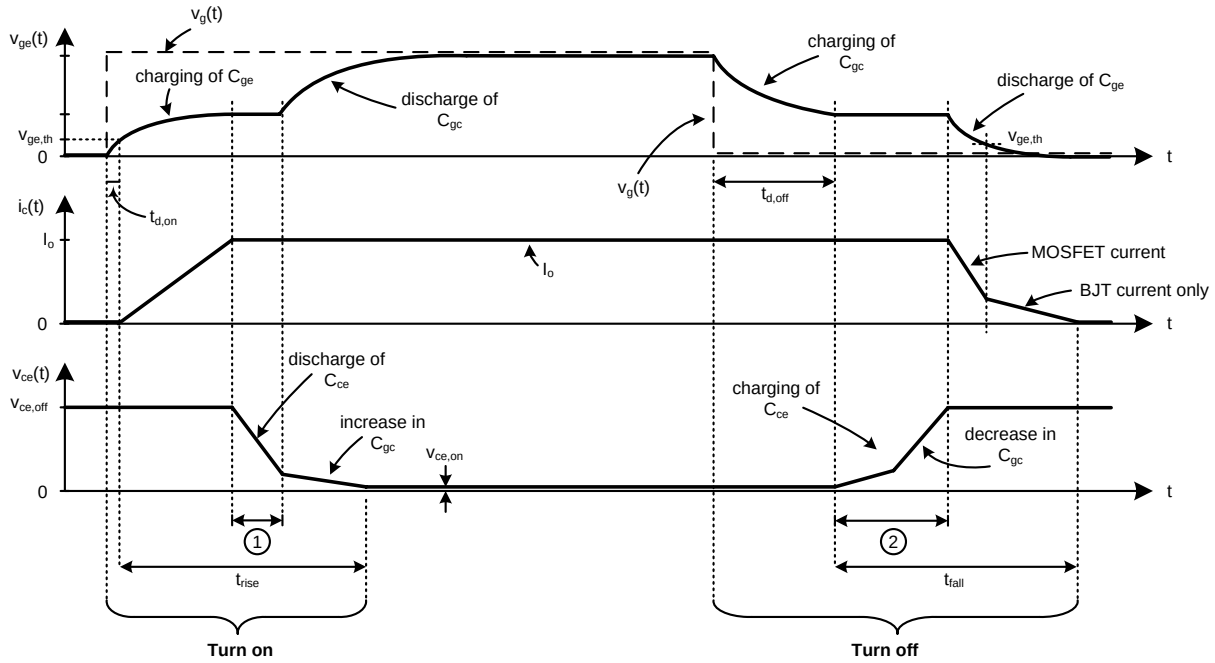

Figure A.4: *Turn on and off waveforms for the IGBT.*

Turn on

In the turn on, the gate signal $v_g(t)$ goes high as a step, charging the gate capacitance. After reaching the threshold level $v_{ge,th}$, the current i_c starts to flow through the IGBT. When this reaches the maximum level, the collector emitter voltage v_{ce} starts to drop in two steps with different slopes. In the first step (marked with a (1)), the voltage decreases linearly, but it must be noted, that the gate voltage v_{ge} stays constant, without being at its maximum, during this step. This is explained by examining the transfer curve for the IGBT seen in figure A.5. This shows, that for constant current and changing collector emitter voltage, the gate emitter voltage must remain constant.

In the second step, the slope of the voltage drop decreases. This is due to the fact, that the capacitance C_{gc} is dependent on the voltage across the IGBT. The capacitance increases, when v_{ce} decreases, leading to longer discharge.

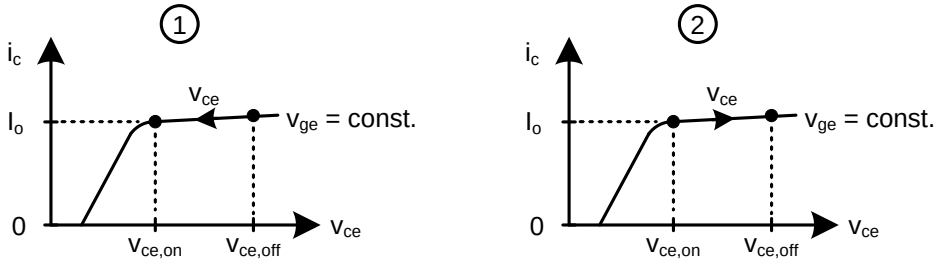

Figure A.5: *Transfer curve for the IGBT.* ***(1)*** *in the turn on.* ***(2)*** *in the turn off.*

Turn off

In the off transition, the gate signal $v_g(t)$ goes low as a step. The gate capacitance C_{ge} is discharged to some level, and C_{gc} starts to charge. At one instant, v_{ce} starts to rise, and the gate voltage stays constant during the rise. This is explained by the transfer curve in the same manner as for the turn on, as shown in figure

A.5 (2). Here again, the rising voltage does not have constant slope due to the voltage dependency of the gate collector capacitance.

When the voltage v_{ce} has reached its maximum value, the current starts to drop. This also happens in two steps. The first step is the time required for the gate drive circuit to discharge the IGBT gate to emitter capacitance to the threshold value, which causes the effective MOSFET in the IGBT to turn off. This time can be minimized by use of a high current gate drive circuit, which discharges the gate capacitance quickly. However, switching off the effective MOSFET does not completely interrupt the current i_c, because the current continues to flow through the effective BJT for a short while, called tail current. This happens in step two, and after this, the device is turned off.

A.1.3 Losses in IGBT

All switching devices dissipate power losses during the operation. The power dissipation happens due to four different factors:

- **Turn on losses** P_{rise}
- **Turn off losses** P_{fall}
- **Conduction losses** P_{on}
- **Reverse recovery losses** P_{rr}

In general, the energy dissipated in the IGBT can be obtained according to equation (A.1).

$$E = \int_0^t v_{ce}(t) \cdot i_c(t) \cdot dt \quad [J] \tag{A.1}$$

where t is the duration of operation. It is clear that, when both voltage and current get significant, the energy dissipation increases. This usually happens during the switching of the devices.

As figure A.4 shows, the voltage and current do not change at the same time in the transitions, and this leads to energy dissipation in the devices. The power losses related to the switching are linearly dependent to the switching frequency $f_{sw} = \frac{1}{T_{sw}}$, both for the turn on and turn off transients. The turn on power losses P_{rise} take place during t_{rise} and the average turn on power during one switching period is given by equation (A.2)

$$P_{rise} = f_{sw} \cdot \int_0^{t_{rise}} v_{ce}(t) \cdot i_c(t) \cdot dt \quad [W] \tag{A.2}$$

where the frequency f_{sw} accounts for the number of switching transitions each second.

In the same manner, the average turn off power losses take place during t_{fall} and are given by equation (A.3)

$$P_{fall} = f_{sw} \cdot \int_0^{t_{fall}} v_{ce}(t) \cdot i_c(t) \cdot dt \quad [W] \tag{A.3}$$

The instantaneous on state conduction losses $P_{on}(t)$ are dependent on the on state voltage drop $v_{ce,on}$ and the current, and is shown in equation (A.4).

$$P_{on}(t) = v_{ce,on}(t) \cdot i_c(t) \quad [W] \tag{A.4}$$

From this the average power P_{on} during one switching period becomes

$$P_{on} = f_{sw} \cdot \int_0^{t_{on}} v_{ce,on}(t) \cdot i_c(t) \cdot dt \quad [W] \tag{A.5}$$

It must be noticed, that the on state voltage drop is not constant, but dependent on the collector current i_c as shown in figure A.2.

The reverse recovery losses for the IGBT is related to the reverse diode path in the device. These losses are given by equation (A.6).

$$E_{rr} = v_{ce} \cdot Q_{rr} \quad [J] \quad \Leftrightarrow \quad P_{rr} = f_{sw} \cdot v_{ce} \cdot Q_{rr} \quad [W] \tag{A.6}$$

where E_{rr} is the energy required to push the charge Q_{rr} across the electrical potential v_{ce}. f_{sw} is the switching frequency, v_{ce} is the voltage across the IGBT, that is conducting the diode reverse recovery current i_D, and Q_{rr} is the amount of charge moving during the recovery period. The recovery charge is normally dependent on the $\frac{di}{dt}$ in the turn off transient, which depends on the gate resistance used for the IGBTs and the leakage inductance of the connections between devices, controlling the current slope. The reverse recovery current behavior is shown in figure A.6.

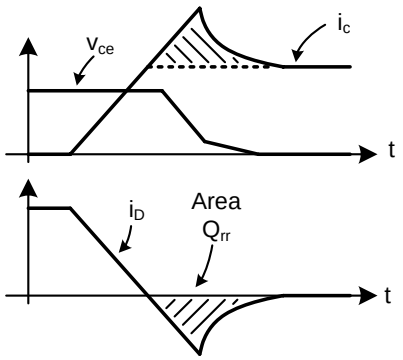

Figure A.6: *Reverse recovery current through a diode and switch.*

The total amount of power loss P_{tot} in a device, is given by equation (A.7).

$$P_{tot} = P_{rise} + P_{fall} + P_{on} + P_{rr} \quad [W] \tag{A.7}$$

It is often convenient to minimize the power losses in any device because of the requirement of additional cooling and heat sinks. Among the four parameters in equation (A.7), the on state power losses P_{on} are hard to manipulate, because the on state voltage drop can not be modified in any manner, without lowering the current through the given device.

But for the three other losses, an optimum design may exist with respect to minimizing the losses. This optimum depends on the rise and fall times and the reverse recovery charge Q_{rr} for the reverse diode path in the devices, and these can be controlled by adjusting for instance the gate resistance.

A.2 Choice of gate resistance

In this section, the characteristics of the SKM 600GA176D IGBTs used for the project are examined to determine an appropriate value for the gate resistances R_g. As described above, an optimum resistance may exist with respect to minimizing the losses, and this is in fact the main goal for the choice of resistance in this case.

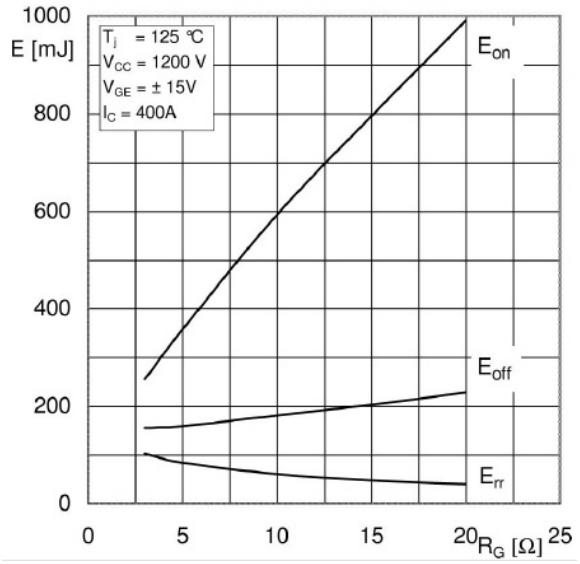

Figure A.7: *Turn on and off energy as function of gate resistance for the SKM600GA176D [Semikron, 2006].*

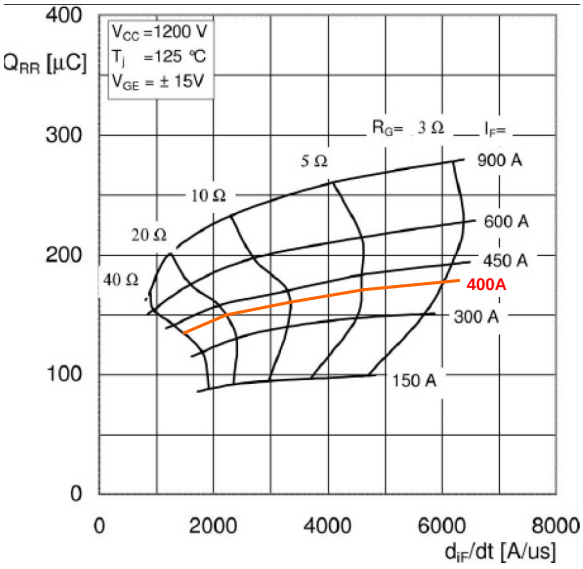

Figure A.8: *Reverse recovery charge for the reverse diode as function of forward current and gate resistance for the SKM600GA176D [Semikron, 2006].*

From the IGBT's data sheet, the turn on and off energy consumption and reverse recovery charge for different gate resistance values are given as shown in figure A.7 and A.8.

The actual peak current is chosen in the introduction on page 4 to only $\widehat{i}_c = \pm 200A$ and the maximum voltage is chosen to $v_{ce} \approx 700V$ because of the zener clamped snubbers. But the data in figure A.7 are given at $I_c = 400A$ and off state voltage $V_{ce,off} = 1.2kV$, so the information in figure A.7 can not be used directly for an estimate of the optimal gate resistance. No additional loss data is available for the $100A/700V$ conditions, and therefore the data from the data sheet is used, even though the estimate may not become accurate.

It must be mentioned, that in the data in figure A.7, the reverse recovery energy is included in the turn on energy, and it must be subtracted to obtain the turn on energy only.

Figure A.8 shows, that the reverse recovery charge for a forward diode current of $I_F = 400A$ stays with in the range of $Q_{rr} = [140; 175\mu C]$ depending on the gate resistance.

Figure A.9 shows an estimate of the sum of turn on, turn off and the reverse recovery loss energy for one single on and off transition, estimated for $I_c = 400A$ and $v_{ce,off} = 1.2kV$. It is assumed here, that one single diode reverse recovery appears for one IGBT turn on transition, even though this may not always be true.

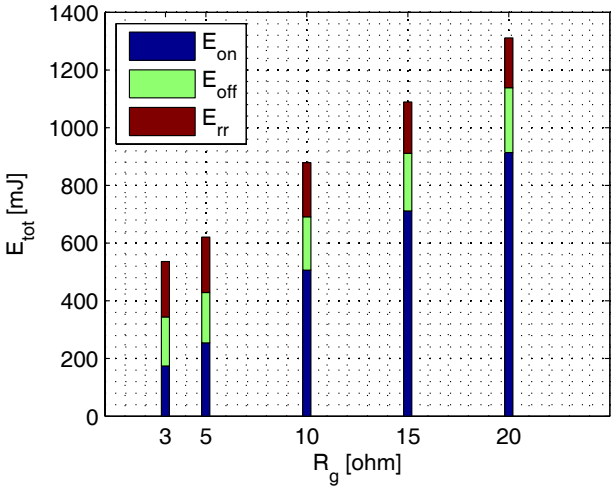

Figure A.9: *Estimate of sum of turn on, turn off and reverse recovery loss energy for one single transition estimated for* $I_c = 400A$ *and* $V_{ce,off} = 1.2kV$.

The energies noted here are valid for one transition only, and to obtain the power loss over time, the switching frequency or period must be included according to equations (A.3) to (A.6).

Figure A.9 shows, that the turn on loss energy E_{on} is largest at $R_g = 20\Omega$, because this leads to longer discharge of the gate capacitance. The turn off loss energy E_{off} also increases for larger R_g, but the change is only a fraction compared to the turn on energy.

The reverse recovery energy E_{rr} is almost constant for any choice of gate resistance. At $R_g = 3\Omega$ it is $E_{rr,3\Omega} \approx 190mJ$ and slightly less at $R_g = 20\Omega$. The change is insignificant compared to the change in turn on and off loss energy mentioned above, and may be ignored.

From these results, the gate resistance may be chosen from a loss point of view. By choosing a large value of resistance, the switching losses increase, even though the reverse recovery energy decreases. By choosing a small value, the losses decrease, but it must be kept in mind, that fast switching also may induce high potentials across wires depending on the quantity of stray inductance. At this time, the stray inductance of the realized inverter is unknown, and must be measured properly in advance to estimate any induced voltages. So therefore the choice of gate resistance is based on minimizing the losses only without focus on any induced voltages. From this the choice is

$$R_g = 3\Omega \tag{A.8}$$

The on state losses are not treated here, because these in general are not dependent on the gate resistance and the rise and fall times of the devices.

A.3 Choice of dead time

The dead time t_{dead} is an important parameter to include in the control of the switching. The fact, that the devices do not switch momentarily, may lead to a short duration short circuit for a set of complementary coupled devices, because one device turns off slower, than the other turns on.

The dead time can be chosen freely, as long as the minimum value is determined with respect to the device rise and fall times. But it must usually be chosen much smaller than the switching period - otherwise it will become significant in the input / output voltage relationship.

In this case, the dead time is chosen with respect to the turn off and on times related to the choice of gate resistance in section A.2. For $R_g = 3\Omega$, the device rise, fall and on and off delay times are shown in figure A.10.

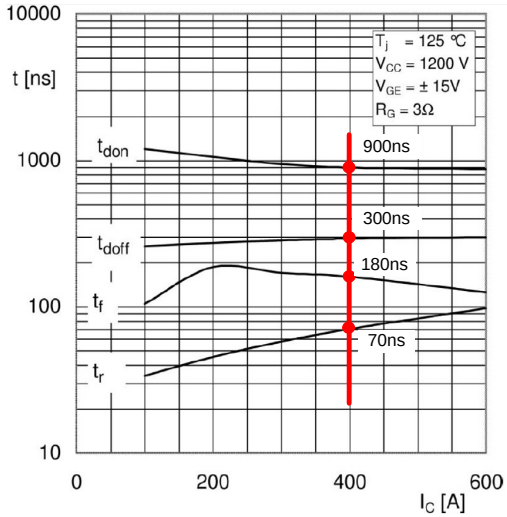

Figure A.10: *Rise and fall times as function of collector current I_c for the SKM600GA176D with $R_g = 3\Omega$ and $v_{ce} = 1.2kV$ [Semikron, 2006].*

The relevant time values at $I_c = 400A$ are summarized in table A.1.

Variable	**Value** $[ns]$
$t_{d(on)}$	900
t_{rise}	70
$t_{d(off)}$	300
t_{fall}	180

Table A.1: *Rise, fall and delay times for the SKM600GA176D at $I_c = 400A$, $V_{ce,off} = 1.2kV$ and $R_g = 3\Omega$ [Semikron, 2006].*

To determine an appropriate dead time, one device must be turned off completely, before the complementary one can be turned on. This means, that the dead time must be chosen equal to or larger than the total turn off time t_{off} for the conducting device.

$$t_{off} \quad = \quad t_{d,off} + t_{fall} = 300ns + 180ns \quad = \quad 480ns \tag{A.9}$$

From this, the dead time is chosen together with additional safety margin to:

$$t_{dead} \geq t_{off} \quad \Rightarrow \quad t_{dead} = 2\mu s \tag{A.10}$$

The safety margin is added, because the on and off times may vary with temperature and aging.

A.4 Choice of switching frequency

The switching frequency f_{sw} is chosen within the frequency range, for which the used integrated gate drive Semikron Skyper 32 can source the gate charge. This is described in detail in section 7.5 on page 96. Here

it is stated from the data sheet, that the maximum obtainable switching frequency with a gate charge of $C_g = 3.25\mu C$[1] is $f_s \approx 15kHz$.

An appropriate switching frequency can be chosen within the range, where the chosen dead time $t_{dead} = 2\mu s$ does not become significant compared to the switching period. For the frequency range $f_{sw} = [0; 15kHz]$, the switching period T_{sw} stays within the range $T_{sw} = [\infty; 66.6\mu s]$. From this, the switching period is initially chosen to

$$T_{sw} = 200\mu s \quad \Leftrightarrow \quad f_{sw} = 5kHz \tag{A.11}$$

because this dead time here only covers $\approx 1\%$ of the switching period, and can be considered insignificant.

A.5 Conclusion

In this section the chosen Semikron IGBT's characteristics are examined closer to obtain data regarding to switching losses and turn on and off times. From these values the gate resistance is chosen from a switching loss minimization point of view. The conduction losses are not estimated here.

From the gate resistance, the dead band time and finally the switching frequency is chosen. The values are summarized in table A.2.

Variable	**Value**
R_g	3Ω
t_{dead}	$2\mu s$
f_{sw}	$5kHz$

Table A.2: *Chosen gate resistance, dead time and switching frequency.*

It must be mentioned here, that the gate emitter voltage supplied by the Skyper 32 gate driver is $v_{ge} = +15/-7V$, where the same data from the IGBT date sheets are given at $v_{ge} = \pm 15V$. This will naturally give some degree of deviation in the amounts of loss energy, that are used as background for the choices in this section.

Finally it must be mentioned, that this appendix has been conducted relatively late during the project work, and at the time of writing, the gate resistances have been chosen and used initially to $R_g = 4.7\Omega$, because this value was used for the IGBTs in the 9th semester project [Mads P. Vaerens, 2007], which has worked as an initiator for this Master Thesis. The consequence of a slightly larger gate resistance for the realized system is, that the turn off and on times increase slightly, which may become critical with respect to the dead time. But as mentioned, the $2\mu s$ dead time chosen has included $1.5\mu s$ of safety margin, and therefore the initially used 4.7Ω gate resistors are accepted and kept throughout the thesis.

[1] This is the gate charge required by the SKM600GA176D

Appendix B

Short circuit types

The current magnitude i and rate of change $\frac{di}{dt}$ of a short circuit current depends on the short circuit impedance Z_{sc} and the DC link voltage V_{DC}. In this section, different short circuits situations in the three level inverter are described to expose the influence of a short circuit appearing in the vicinity of the inverter or separated by significant impedance.

This is important, because different short circuit detection techniques depend on significant $\frac{di}{dt}$ and/or significant i to operate properly. In general, the short circuits can be divided into fast faults and slow faults, depending on the short circuit impedance.

B.1 Influence of short circuit impedance

The influence of wire impedance, which for grid lines is mainly inductive, can be explained by observing, how many switching periods it takes for the inverter, before the IGBT current exceeds the rated value or even enter desaturation. For a very small inductance, $\frac{di}{dt}$ is very large, and desaturation can occur almost immediately as shown on figure B.1.

In the case of large inductance and smaller $\frac{di}{dt}$, the current peaks after a sequence of switching periods as shown on figure B.2. If the short circuit impedance is high, the switches may not even enter desaturation at all, but rather conduct the current waveform controlled by the switching scheme, with a peak value much higher than the rated value.

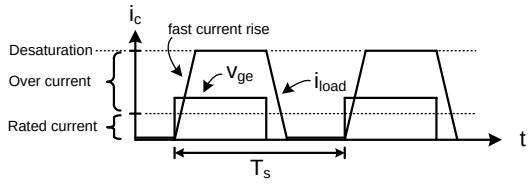

Figure B.1: *Desaturation by fast fault with small inductance. Desaturation occurs immediately after short circuit.*

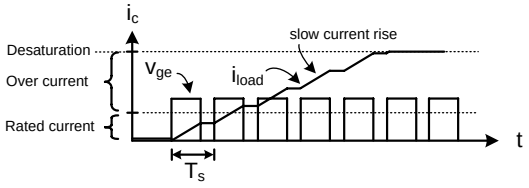

Figure B.2: *Desaturation by slow fault with large inductance. Desaturation occurs after a sequence of switching periods.*

In the following section, the current paths for fast and slow faults in the three level inverter are described along with with typical causes for the faults.

B.2 Fast faults

- **Fast faults - occur very close to the inverter - Z_{sc} small**
  - **Cause**

* Failure in dead time generation
* Failure in gate drivers
* Failure in DSP
* Short circuit in the DC link bus bar.

– **Effect**

* Characterized by very fast current rise
* IGBTs enter desaturation within the switching period of the fault.

For the fast faults, the impedance is given by $Z_{sc,fast}$ as

$$Z_{sc,fast} = Z_{busbar} + n \cdot Z_{IGBT} \quad [\Omega] \tag{B.1}$$

where n is the number of IGBTs in the short circuit path, and Z_{busbar} is the impedance of the DC link bus bar and the connection between the IGBTs. Figures B.3 to B.5 show three different fast fault situations in the three level inverter.

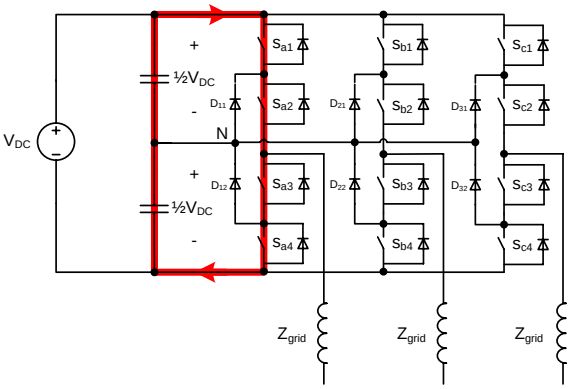

Figure B.3: *Fast fault with shoot through in one phase leg. Characterized by very fast current rise.*

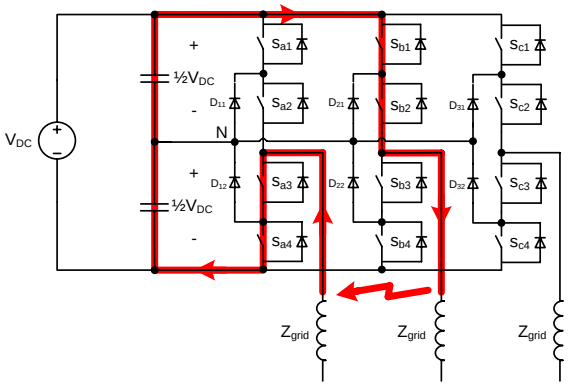

Figure B.4: *Fast fault with phase to phase short circuit. Characterized by very fast current rise.*

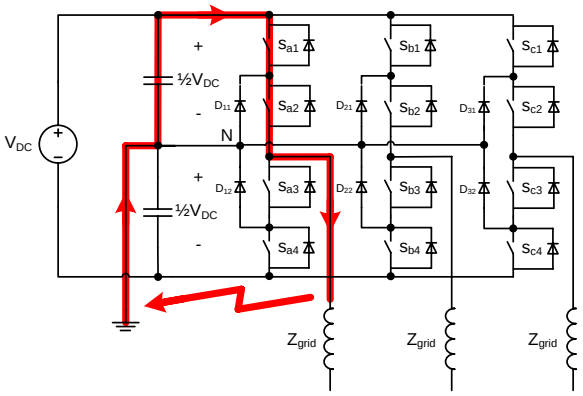

Figure B.5: *Fast fault with phase to ground short circuit. Characterized by fast current rise, but only involving half of the DC link voltage.*

Figure B.3 shows the current path for a shoot through fault, where all four switches in one phase are turned on at the same time. The switches are exposed to full DC link voltage, and only the impedance of the

DC link bus bar and the IGBT is present. This fault leads to the fastest $\frac{di}{dt}$ of the short circuits types described.

Figure B.4 shows the current path for a phase to phase fault right at the output terminals of the inverter. Also here the switches are exposed to the full DC link voltage. The impedance of the current path is only marginally larger than the one for the shoot through fault, and is also characterized by very large $\frac{di}{dt}$.

Figure B.5 shows a phase to ground short circuit close to the inverter. This fault only involves half of the DC link voltage, because ground is connected to the neutral point. If it is assumed, that the ground impedance is zero, then the short circuit impedance becomes half of the phase to phase short circuit of figure B.4, because only half the amount of IGBTs and half the electrical length of the bus bar is involved. This means, that ideally a phase to ground short circuit will lead to the same $\frac{di}{dt}$ as the phase to phase short circuit.

B.3 Slow faults

- **Slow faults - occur away from the inverter - Z_{sc} large**
  - **Cause**
    - Failure in the load
    - Machine winding short circuit due to insulation failure
    - Grid short circuit.
  - **Effect**
    - Characterized by slow current rise
    - IGBTs do not generally enter desaturation within the switching period of the fault. This may happen after several periods, depending on the total wire inductance and if the duty cycle is increasing or decreasing.

For the slow faults, the impedance is given by $Z_{sc,slow}$ as

$$Z_{sc,slow} = Z_{busbar} + n \cdot Z_{IGBT} + Z_{grid} \quad \approx \quad Z_{grid} \quad [\Omega] \tag{B.2}$$

because the grid impedance Z_{grid} is dominant. Figures B.6 and B.7 show two different slow fault situations in the three level inverter.

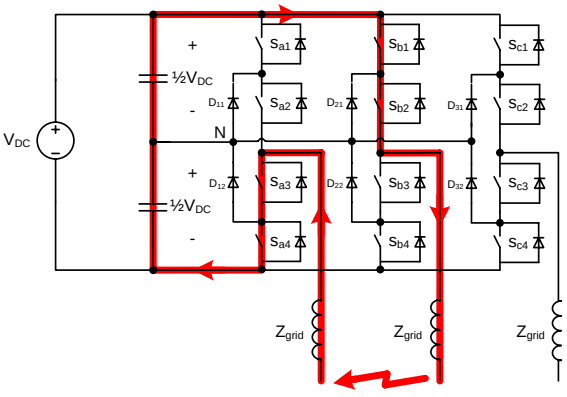

Figure B.6: *Slow fault with phase to phase short circuit.*

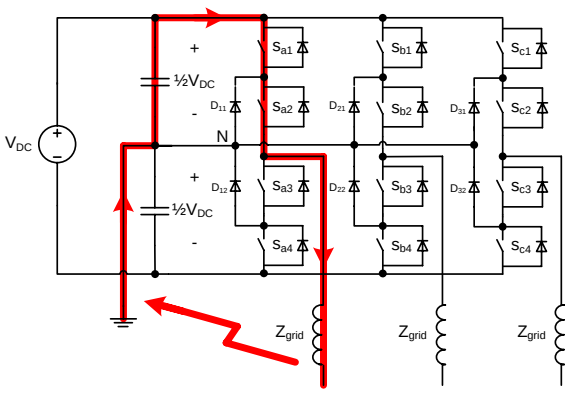

Figure B.7: *Slow fault with phase to ground short circuit.*

Figure B.6 shows a phase to phase fault occurring at a distance from the inverter. Because the wires have significant self inductance, $\frac{di}{dt}$ becomes much slower compared to the fast faults. Figure B.7 shows a slow

phase to ground fault at a distance from the inverter also involving the wire impedance.

As for the fast faults, the phase to phase and the phase to ground faults will lead to the same current rise $\frac{di}{dt}$.

B.4 Conclusion

This appendix gives a short description of fast and slow short circuits. Fast short circuits are characterized by very large $\frac{di}{dt}$, which means, that the conducting switches can enter desaturation within the switching period. In this project the fast fault is characterized by the current increasing from zero current up to the desaturation limit within one switching period.

The slow short circuits are characterized by smaller $\frac{di}{dt}$, and here the load current may not exceed the desaturation limit at all, but rather conduct the current waveform controlled by the switching scheme, with a peak value much higher than the rated value.

More types of short circuits are possible for a three phase inverter, but not examined in detail here. These are the three phases short circuit, the two phases to ground and three phases to ground short circuit [Voerts, December 1963].

Appendix C

Self inductance in conducting wires

All electrical conductors represent a certain amount of self inductance depending on the length and geometry of the conductor. The self inductance is closely related to the flux around the conductor for a given current as given in equation (C.1). In many applications the self inductance does not lead to any difficulties or might even be required, but for applications with high rates of change in current, self inductance can become a problem. This is due to high voltages induced across the conductor by rapidly changing currents as given in equation (C.2).

$$L = \frac{\phi}{i} \quad [H] \tag{C.1}$$

$$v_L = L \cdot \frac{di_L}{dt} \quad [V] \tag{C.2}$$

In this appendix, three different procedures to minimize the inductance are described by the equations for different wire geometries and layout according to [Wisler, December 1996]. In one of the cases, the inductance can theoretically be canceled out completely by choosing an appropriate wire layout and return path for the current.

C.1 One flat wire

For one flat wire without a magnetically coupled return path, the self inductance is dependent of the thickness, the width and the length of the wire - see figure C.1. The self inductance for this wire geometry is given by equation (C.3).

$$L = 2 \cdot 10^{-7} \cdot l \cdot \left(\underbrace{ln\left(\frac{2}{b+c}\right)}_{I} + 0.5 + \underbrace{0.22 \cdot \frac{b+c}{l}}_{II} \right) \quad [H] \tag{C.3}$$

Equation (C.3) consist of two parts - part I is dominating for a sum of small values of b and c and part II is dominating for small values of l. This can also be seen in figure C.2, that shows the inductance for a flat wire of fixed thickness $c = 5mm$ and different lengths l. For every choice of c and l, there exist a minimum inductance at some value of width b, which can be used as a parameter for an optimum design.

In a practical application, the minimum inductances from the figure may be difficult to obtain. For example, a wire of length $50mm$ must be approximately $450mm$ wide to minimize the inductance, and this may not be realistic in most applications. So for the flat single wire geometry, the inductance is practically minimized by using wires, that are as wide and short as possible.

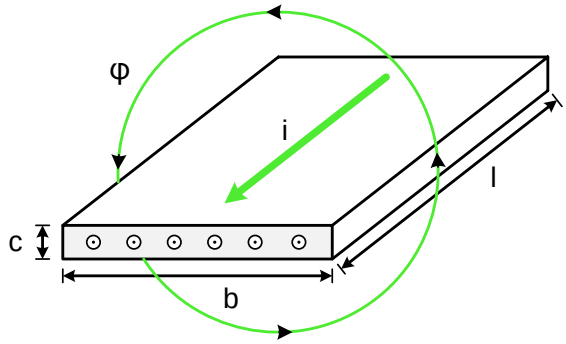

Figure C.1: *Layout of a single flat wire with no current return path.*

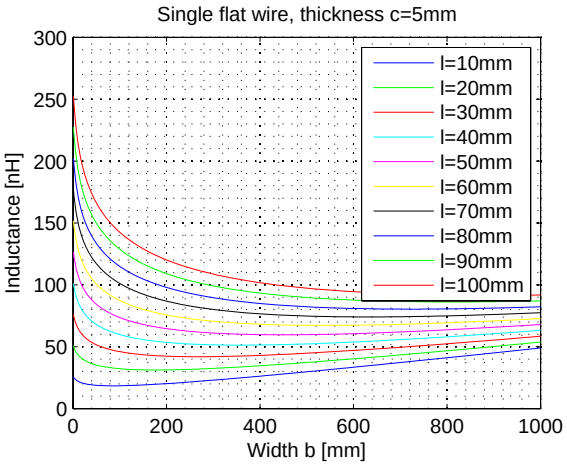

Figure C.2: *Self inductance one flat parallel wire according to equation (C.3).*

C.2 One flat wire with identical return path

For one flat wire with a coupled return path, the self inductance is dependent on the width, length and the distance between the wires. It becomes independent of the thickness of the wire, as long as the wires are oriented exactly parallel - see figure C.3. In the case, where the currents i_1 and i_2 in the upper and lower conductors have the same magnitude but flowing in opposite direction, the self inductance is given by equation (C.4).

$$L = 4 \cdot 10^{-7} \cdot l \cdot ln\left(1 + \pi \cdot \frac{a}{b}\right) \quad [H], \quad b \geq 2 \cdot a \tag{C.4}$$

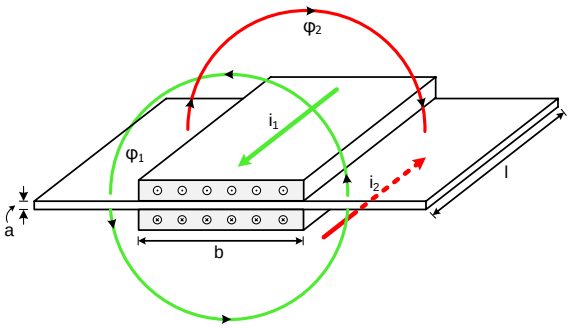

Figure C.3: *One flat wire with identical return path*

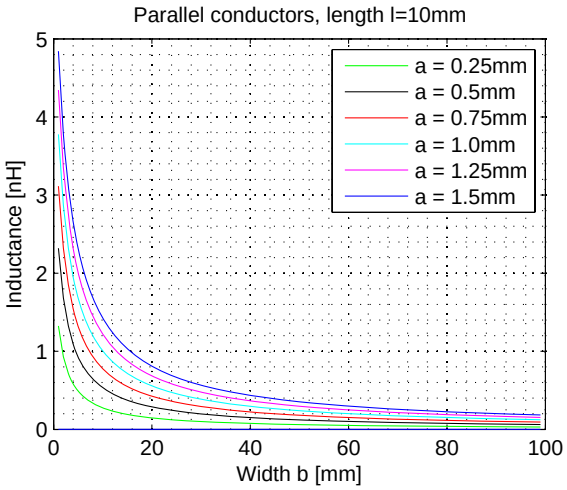

Figure C.4: *Self inductance for two flat parallel wires according to equation (C.4).*

Figure C.4 shows the inductance for a wire of length $l = 10mm$. Here the inductance becomes small, when the width b is large and the distance a between the wires is small. In the ideal case with infinitely small distance a, the inductance reaches zero, which is explained by the flux lines ϕ_1 and ϕ_2 of the two conductors

canceling each other completely because of opposite signs and same magnitude.

In a practical application this means, that to minimize the inductance, the isolation between the wires must be chosen as thin as possible, without exceeding the dielectric strength of the isolation. And the width of the wire must be chosen as large as the application allows.

C.3 One flat wire with non identical return path

For one flat wire with a non identical coupled return path, the self inductance is dependent on the width, length and the distance between the wires. It becomes independent of the thickness of the wire, as long as the wires are oriented exactly parallel as for the case with identical flat wires. The self inductance in this case is given by equation (C.5), under the restriction, that the two widths satisfies $b_2 >> b_1$.

$$L = 2 \cdot 10^{-7} \cdot l \cdot ln\left(1 + 2 \cdot \pi \cdot \frac{a}{b_1}\right) \quad [H], \quad b_1 \geq 4 \cdot a \tag{C.5}$$

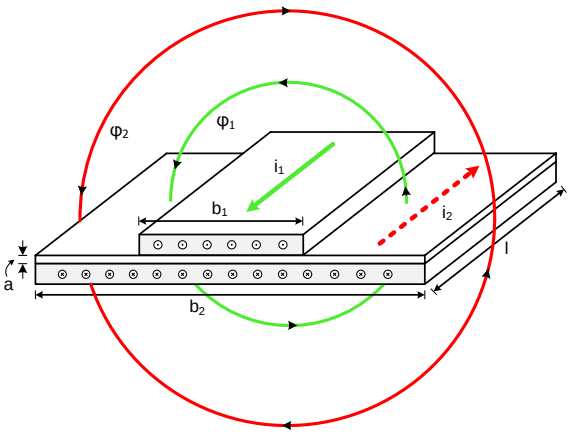

Figure C.5: *One flat wire with non identical return path.*

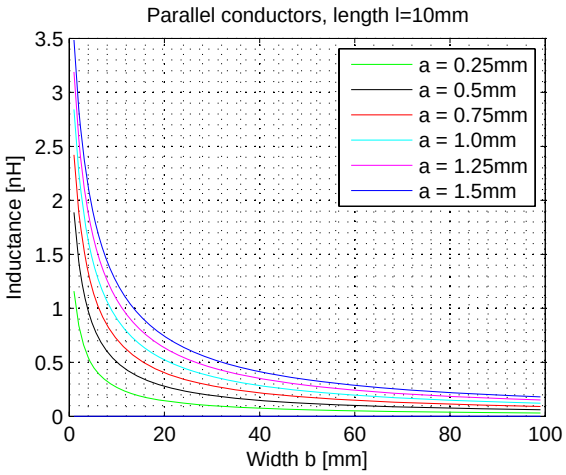

Figure C.6: *Self inductance for two flat parallel non identical wires according to equation (C.5).*

Figure C.5 shows the inductance for a wire of length $l = 10mm$. Here the inductance becomes small, when the width b_1 is large and the distance a between the wires is small. In the ideal case with infinitely small distance a, the inductance reaches zero.

Appendix D

Measurements

D.1 IGBT short circuit characteristics

D.1.1 Purpose

The purpose of this test is to obtain the short circuit characteristics of the Semikron SKM600GA178 IGBT. This is done to gain knowledge about the IGBT, and to obtain data regarding the emitter kelvin-emitter voltage v_{eke} across the impedance Z_{eke} shown on figure D.1. and if it is possible to detect a short circuit before desaturation occurs. This is important, because according to Semikron, desaturation can only be handled in approximately $10\mu s$. Another required parameter is the over voltage in the v_{ce} due to hard switching.

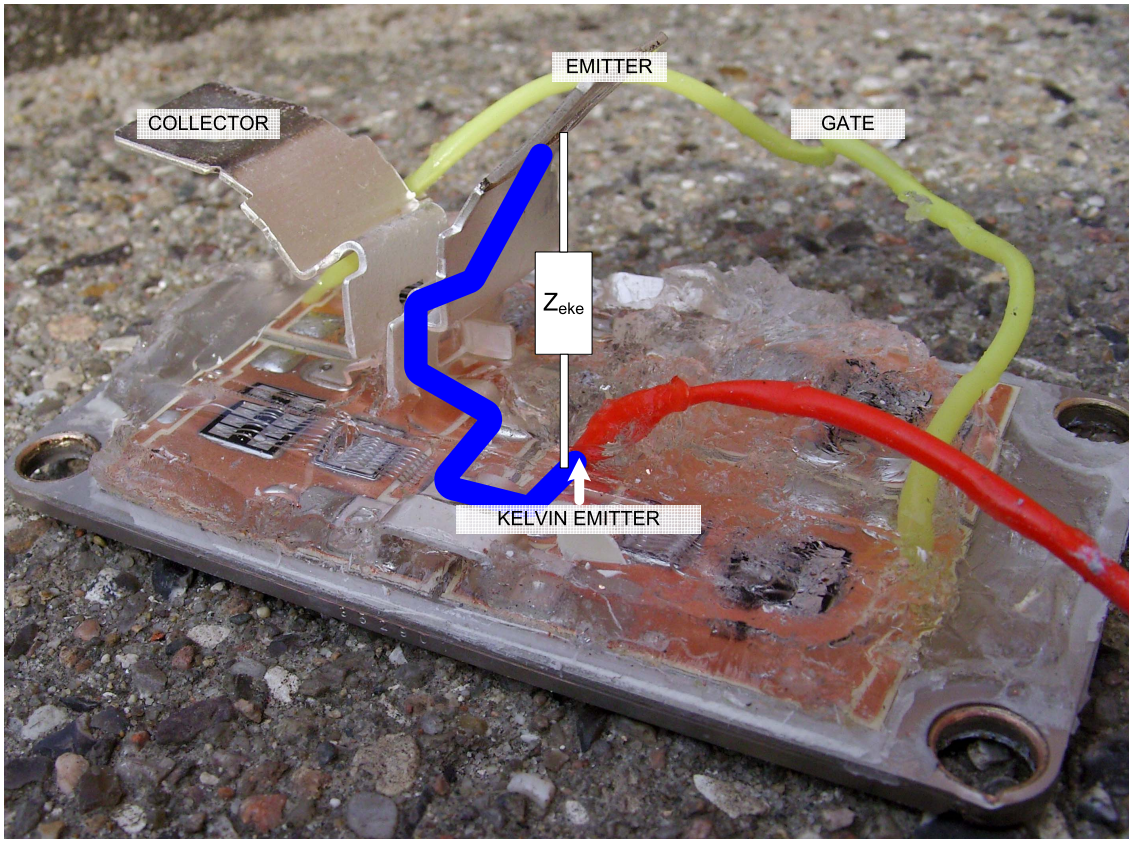

Figure D.1: *Picture of the internal of a Semikron IGBT. Z_{eke} is shown by the blue line.*

D.1.2 Setup

The used equipment is listed in table D.1 and the test setup is shown in figure D.2.

Equipment	AAU number	Used for
Tektronix oscilloscope	3307	Obtaining parameters
HP 937A multimeter	35936	Monitor capacitor voltage
2 x Delta SM 300 s Power supply	62765, 62768	Main supply V_{in}
3 x Differential probes	55719, 56076 , no number	v_{ge}, v_{ce} and v_{eke}
Tabor Electronic series 8201	35553	Pulse generator
$10m\Omega$ shunt	no number	Collector current
$2.3mF$ capacitor bank C	no number	Charge for short circuit
$R_{charge} = 100\Omega$ charge resistor	no number	Limits charging current
$R_{discharge} = 28k\Omega$ discharge resistor	no number	Discharge the capacitor bank.

Table D.1: *Equipment used for short circuit test.*

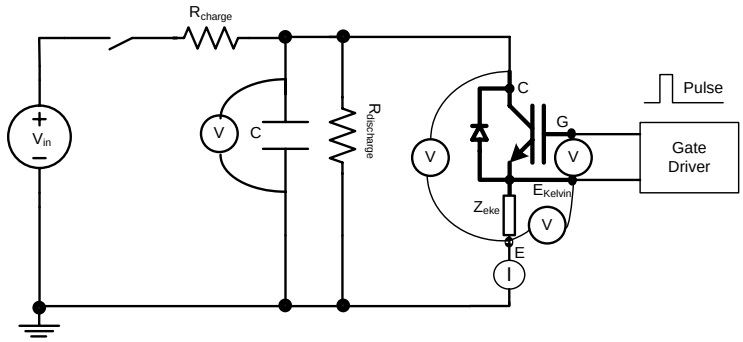

Figure D.2: *Test setup for short circuit test.*

D.1.3 Measurements

The measurements are performed at the following voltage levels: V_{in} = 150V, 200V, 300V, 400V, 500V and 600V. The pulse width of the gate voltage is $5\mu s$.

The reason for this, is to ensure the survival of the IGBT, and still get close to a realistic operating situation at 600 V. The laboratory temperature was $19°C$ at time of test.

D.1.4 Data evaluation

To elaborate on the measurements, two of the figures from above is explained in detail on figure D.9 and D.10.

On figure D.9 it becomes clear, that the desaturation occurs approximately $2\mu s$ after the short circuit starts. However, the v_{eke} can be detected almost at the same instance. It can also be seen, that the impedance from emitter to kelvin emitter is mainly inductive, because v_{eke} becomes constant at a constant rate of change in the current, and approximately zero at a constant current in desaturation. The approximate inductance value can be calculated as:

$$L_{eke} = \frac{v_{eke}}{\frac{di_C}{dt}} = \frac{7.5V}{\frac{2kA}{2\mu s}} = 7.5nH \tag{D.1}$$

The resistive part of the impedance from emitter to kelvin emitter is ignored, but has an approximate value of $R_{eke} = \frac{0.5V}{1.8kA} = 277\mu\Omega$ obtained in the desaturation region of figure D.9. The negative spike in v_{eke} before the positive spike, is due to the line impedance of the kelvin emitter terminal wire. This is backed up by the

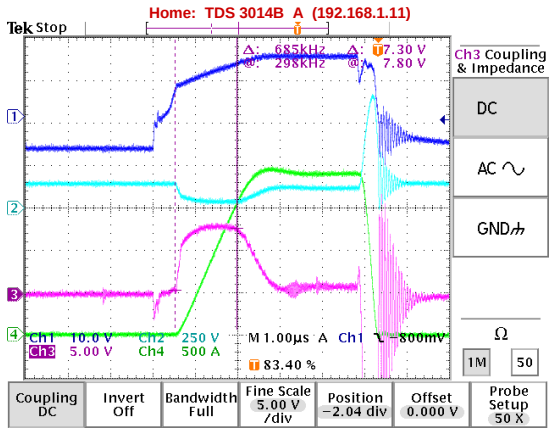

Figure D.3: *Short circuit test for $V_{in} = 150V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_C.*

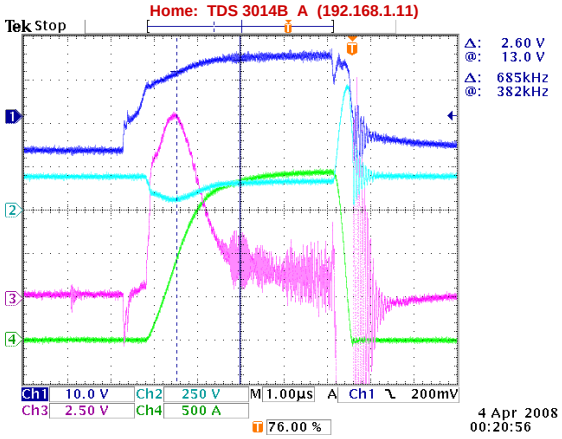

Figure D.4: *Short circuit test for $V_{in} = 200V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_C.*

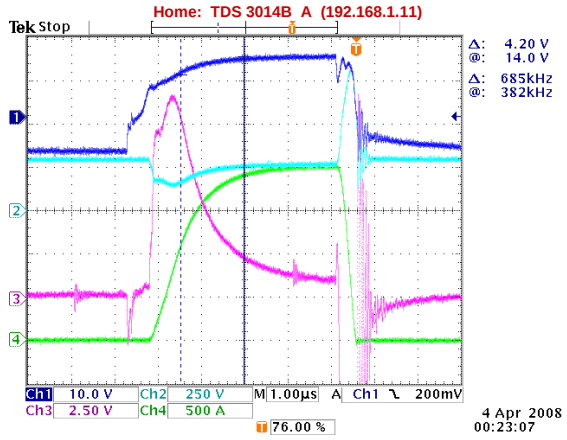

Figure D.5: *Short circuit test for $V_{in} = 300V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_C.*

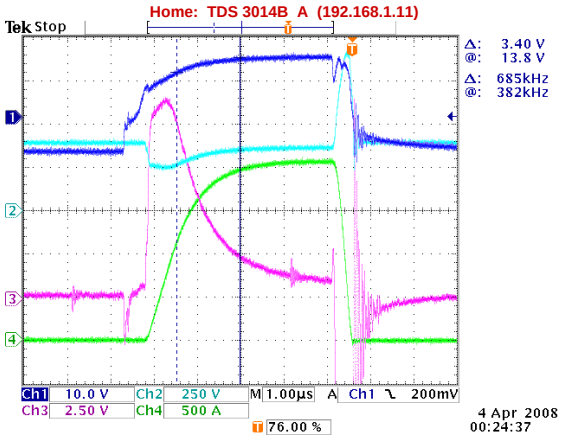

Figure D.6: *Short circuit test for $V_{in} = 400V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_C.*

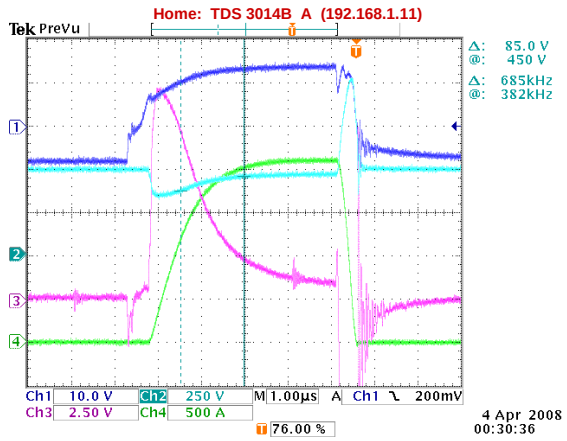

Figure D.7: *Short circuit test for $V_{in} = 500V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_C.*

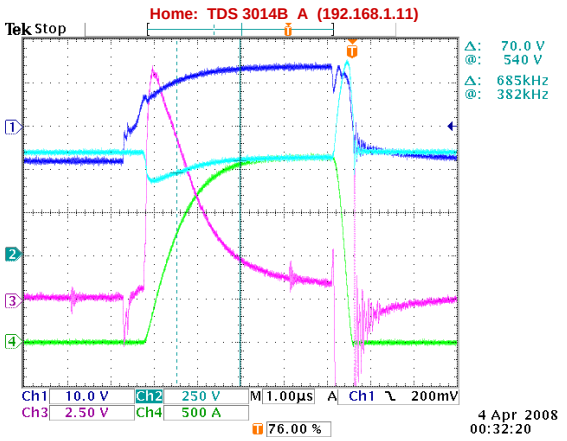

Figure D.8: *Short circuit test for $V_{in} = 600V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_C. Notice that the offset for v_{ce} has changed.*

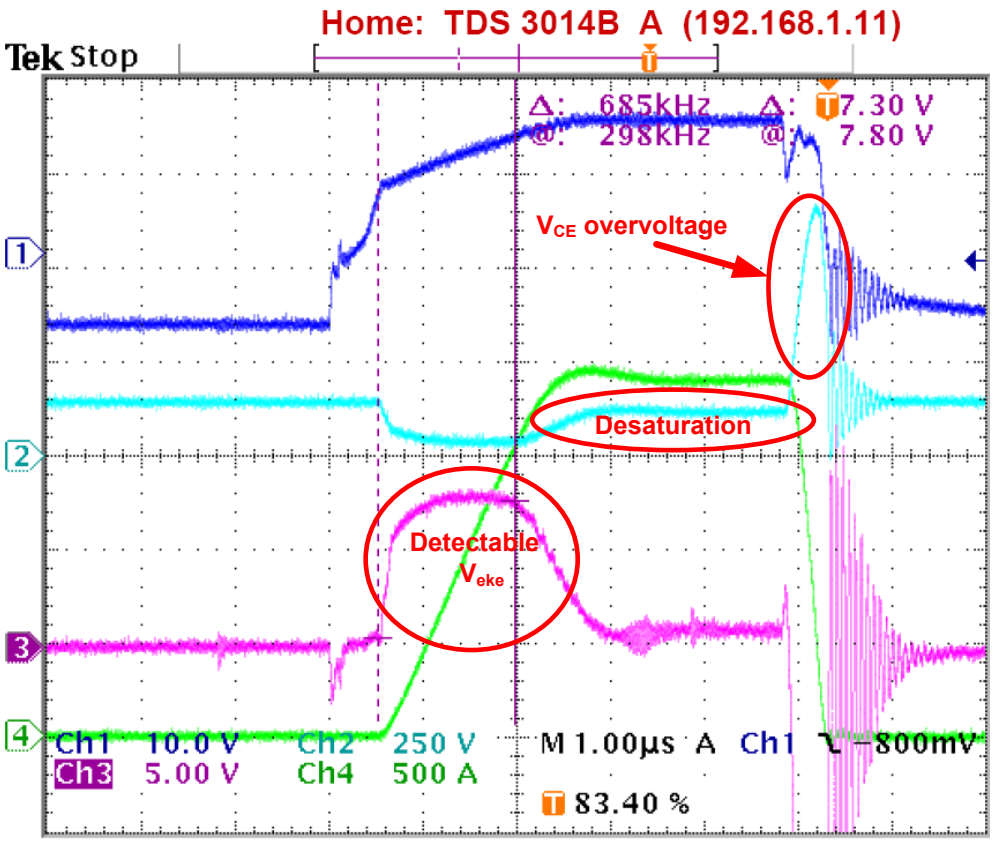

Figure D.9: *Short circuit test for $V_{in} = 150V$. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_C.*

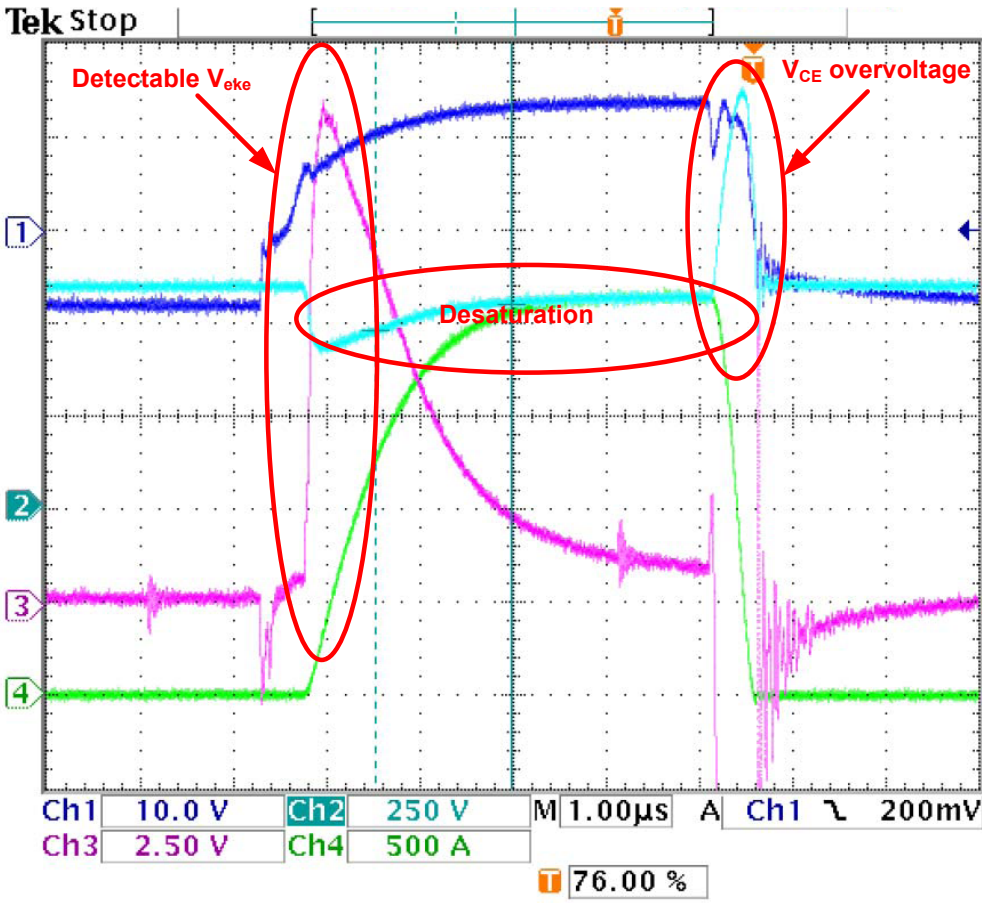

Figure D.10: *Short circuit test for $V_{in} = 600$. Dark blue = v_{ge}, Light blue = v_{ce}, purple = v_{eke}, green = i_C. Notice that the offset for v_{ce} has changed, and that the desaturation occurs immediately.*

fact that the spike occurs at the same time as the gate signal, hence there is a current change in the kelvin emitter wire. On figure D.10 the desaturation occurs from the beginning of the on-state. The short circuit is detectable in both v_{eke} as before, but there is no advantage in detecting it compared to the desaturation. The v_{ce} over voltage has a maximum value of $1.2kV@V_{in} = 600V$ due to the hard switching, and this is within the device rating. However, the over voltage will be dependent of the stray inductance of the actual inverter busbar, and the busbar stray inductance is expected to be larger, so the over voltage has to be addressed as a very critical factor of the protection scheme.

D.1.5 Conclusion

The conclusion of the test is, that a short circuit can be detected by monitoring v_{eke}. Also, the over voltage due to hard switching can cause device destruction and needs to be taken into account in a protection scheme. From the two tests shown in detail on figure D.9 and D.10, an important aspect can be identified;
For the $V_{in} = 150V$ test, v_{ce} reaches zero and then goes into desaturation. This is the equivalent of having a short circuit occur while the IGBT is on. In this case, the v_{eke} will be the fastest way of detecting the error by a margin of approximately $2\mu s$. For the $V_{in} = 600V$ test from figure D.10, the desaturation is detectable almost immediately. This is the equivalent of turning the IGBT on, while a short circuit is present in the inverter.

These results shows, that using both v_{eke} and desaturation detection to detect an error, will increase the reliability of the protection. If the IGBT short circuit while turned on, the v_{eke} will trigger the protection, and if the IGBT turns on into a short circuit, the error is detectable in both v_{eke} and v_{ce} at the same time. Also, choosing two detectors pr. IGBT, will add redundancy to the inverter protection scheme, meaning that a backup system is in place, in case of a defect in the detector. To ensure that a normal switching operation is not detected as a short circuit, an integration of v_{eke} can be incorporated to ensure that only a large current will trigger an error.

D.2 Protection by voltage clamping method test

In this appendix section, the protection by voltage clamping method is tested. This is done to verify if the zener clamped snubber can be used as protection.

D.2.1 Purpose

The purpose of the test is, to repeat the tests from appendix D.1, but with added over voltage protection in the form of two transil diodes, which are more robust version of the zener diode. This is to test, if the over voltage, that was a consequence of the hard switched shut down, can be eliminated. This over voltage was concluded as a major risk for the destruction of the IGBTs in appendix D.1.

D.2.2 Setup

The used equipment is listed in table D.2 and the test setup is shown in figure D.11. The clamping level is set to $V_{clamp} = 800V$, and therefore only the two tests from appendix D.1 at $V_{in} = 500$ and $V_{in} = 600V$ is repeated, because the over voltage in these tests went above the clamping level.

Equipment	AAU number	Used for
Tektronix oscilloscope	3307	Obtaining parameters
HP 937A multimeter	35936	Monitor capacitor voltage
2 x Delta SM 300 s Power supply	62765, 62768	Main supply V_{in}
3 x Differential probes	55719, 56076 , no number	v_{ge}, v_{ce} and v_{eke}
Tabor Electronic series 8201	35553	Pulse generator
$10m\Omega$ Shunt	no number	Collector current
$2.3mF$ capacitor bank C	no number	Charge for short circuit
$R_{charge} = 100\Omega$ charge resistor	no number	Limits charging current
$R_{discharge} = 28k\Omega$ discharge resistor	no number	Discharge the capacitor bank.
2 x Transil diode $1.5ke400A$ / $400V$	no number	Series connected to clamp $v_{ce} = 800V$

Table D.2: *Equipment used for protection by clamping test.*

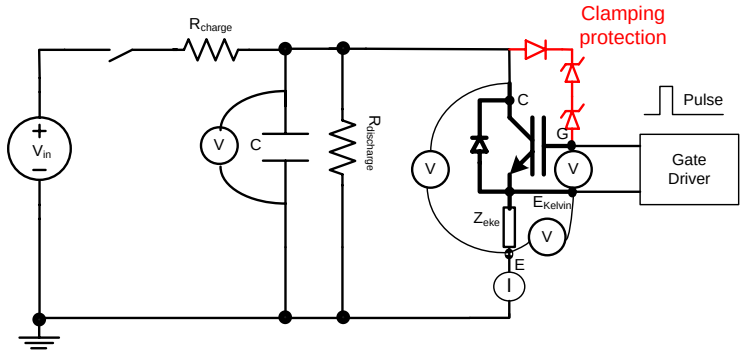

Figure D.11: *Test setup for protection by clamping test.*

D.2.3 Measurements

The measured waveforms is shown on figure D.12 and D.13. The laboratory temperature was $19°C$ at time of test.

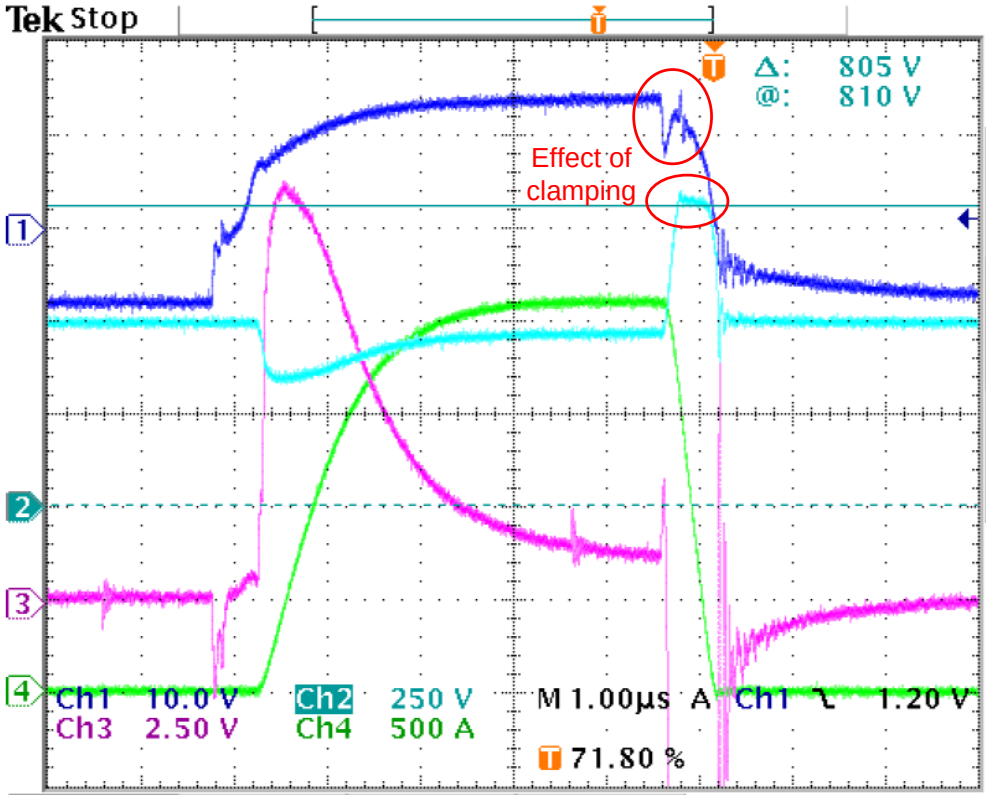

Figure D.12: *Short circuit test for $V_{in} = 500V$ with added clamping protection. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_c.*

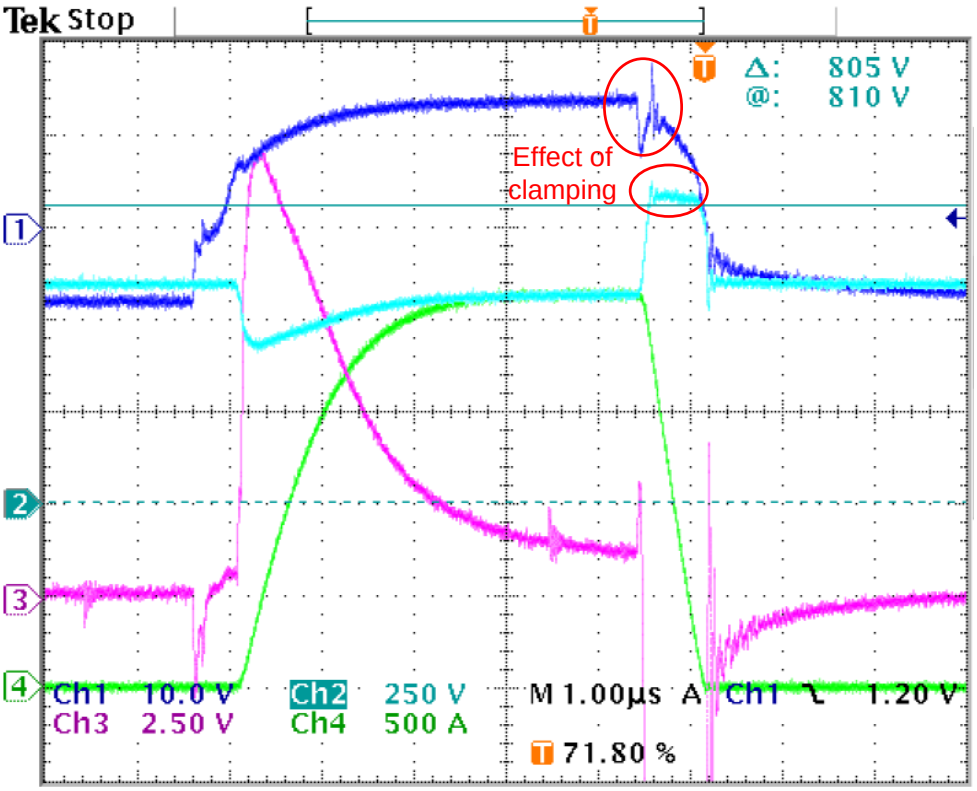

Figure D.13: *Short circuit test for $V_{in} = 600V$ with added clamping protection. Dark blue = v_{ge}, light blue = v_{ce}, purple = v_{eke}, green = i_c.*

D.2.4 Data evaluation

The obtained data from figure D.12 and D.13 shows the effect of the clamping. It is seen, that when the transils clamp the over voltage, the v_{ge} is turned on for a short while. This is because the transils inject current into the gate. The required clamping level of the $v_{clamp} = 800V$ is read to $v_{clamp} = 810V$ on figure D.12, and $v_{clamp} = 825V$ on figure D.13.

D.2.5 Conclusion

The conclusion of the test is, that the voltage clamping protection works satisfactory by eliminating the damaging over voltage in v_{ce}. By using this method, there is no need to perform a soft shut down of the IGBT, so the turn off time is faster compared to the soft shut down method. The clamping method also has the advantage, that no active shut down hardware is needed in the gate driver, as would be the case for the soft shut down method. The shut down of the IGBT is thereby only performed by the gate driver.

D.3 Medium voltage DC supply measurements

The medium voltage DC supply for the inverter is designed and tested in this appendix. The demands for the supply are as follows:

- Variable voltage regulation. This is important to test the inverter at low voltages in the beginning.
- Capable of producing a DC link voltage of $V_{DC} = 2.4kV$.
- Capable of supplying the current needed for the power dissipation for the load and the inverter.

No high voltage DC supply exist at AAU, so one must be build. This is done as shown in figure D.14.

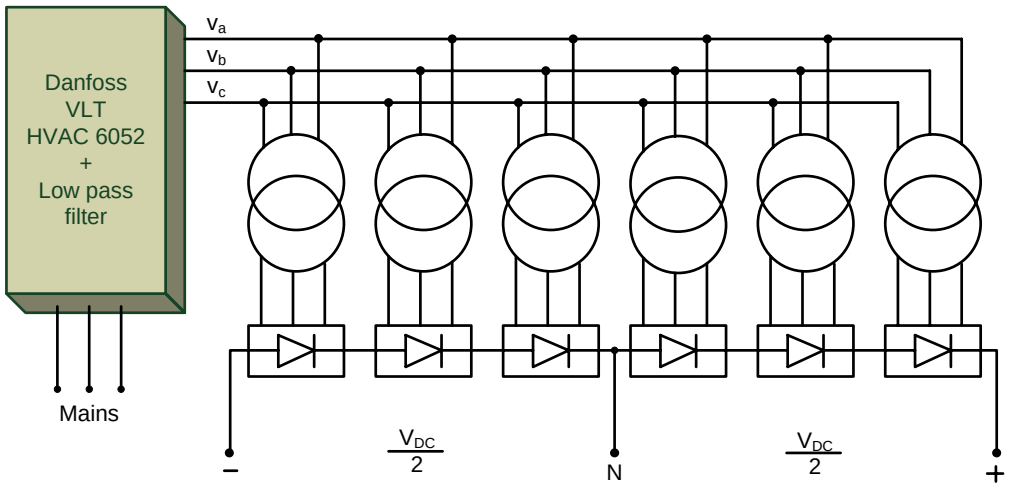

Figure D.14: *Medium voltage DC supply.*

To obtain an analytical expression of the relationship between the phase voltages and the DC component of the rectifier output, when the DC link contains no filter capacitor, the voltage waveforms at the input and the output on the rectifier are examined. These are shown in figure D.15.

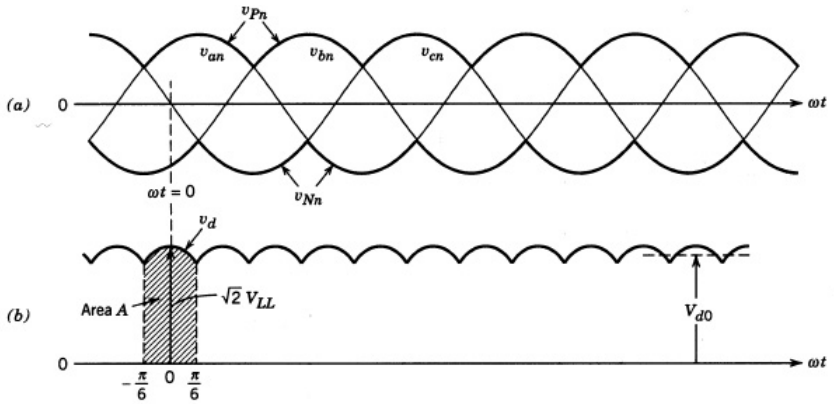

Figure D.15: *Three phase rectifier voltages. [Ned Mohan, 2003]*

The average value of the output voltage V_{DC} from the rectifier is found by considering only a small fraction of one full period. Here only one of the six equal sub periods of duration $\frac{\pi}{3} = 60°$ is sufficient to calculate v_d, which is the instantaneous value of the output voltage.

$$v_d \quad = \quad v_{ab} = \sqrt{2} \cdot V_{LL} \cdot cos(\omega t), \qquad -\frac{\pi}{6} < \omega t < \frac{\pi}{6} \tag{D.2}$$

when the time $t = 0s$ is chosen, where the line to line voltage v_{ab} is at its maximum. V_{LL} is the RMS value of the line to line voltages. Now by integrating over the period $[-\frac{\pi}{6}; \frac{\pi}{6}] = \frac{\pi}{3}$, the volt-second area A becomes

$$A = \int_{-\pi/6}^{\pi/6} \sqrt{2} \cdot V_{LL} \cdot cos(\omega t)\ d(\omega t) = \sqrt{2} \cdot V_{LL} \tag{D.3}$$

By dividing A by the period $\frac{\pi}{3}$, the average value V_{DC} of v_d becomes:

$$V_{DC} = \frac{1}{\pi/3} \int_{-\pi/6}^{\pi/6} \sqrt{2} \cdot V_{LL} \cdot cos(\omega t) = \frac{3}{\pi} \cdot \sqrt{2} \cdot V_{LL} = 1.35 \cdot V_{LL} \tag{D.4}$$

This expression covers one transformer and one rectifier from figure D.14, so the total V_{DC} for the medium voltage DC supply as a function of the line to line voltage is:

$$V_{DC} = 6 \cdot 1.35 \cdot V_{LL} = \frac{81}{10} \cdot V_{LL} \tag{D.5}$$

For the medium voltage level of $V_{DC} = 2.4kV$, the output voltage for the VLT must be:

$$V_{ab} = \frac{2.4kV \cdot 10}{81} = 296V \tag{D.6}$$

This is tested later in this section.

D.3.1 Realization of medium voltage DC supply

The equipment used for the supply on figure D.14 is listet in table D.3.

Equipment	AAU number	Used for
Danfoss $55kVA$ HVAC 6052	No number	Variable main supply
6 x $10kVA$ AXA transformers	38621,38619,38620, 38623,38617, No number	Generation of medium voltage level
6 x Semikron SKD 30/16 three-phase diode bridge rectifiers	No number	Rectification of the transformer voltage
$32A$ low pass filter	No number	Filters the VLT output to prevent harmonics

Table D.3: *Components for medium voltage DC supply.*

Initial test showed a problem with the transformers, which contained a safety relay that could not handle input voltages below $V_{ab} = 200V$, so these had to be bypassed. However, the safety of the setup is not compromised by this, as the Danfoss VLT is galvanically isolated from the user. Furthermore, the setup is placed in a safety cage in the high voltage lab of AAU, so the local emergency stops on the transformers are not usable by the operators of the system anyway. The VLT is fitted with a switch to enable and disable it, and also a potentiometer to control the VLT. This is done based on a Danfoss application note in the manual of the VLT 6052. This interface is also galvanically isolated from the user of the system.
The VLT used in the setup has a disadvantage that is quite limiting for the project. The output voltage can not be adjusted manually while the VLT is running. To accommodate this, a V/F ramp is used to reach a target output voltage and hence the required V_{DC}. The reason for using a ramp is, that the neutral point capacitors will act as a short circuit at start up, and needs to be slowly charged. The power rating of the setup is determined by the filter, because the VLT and transformers have larger power rating than this. The filter has a power rating of $16kVA@V_{ab} = 296V$.

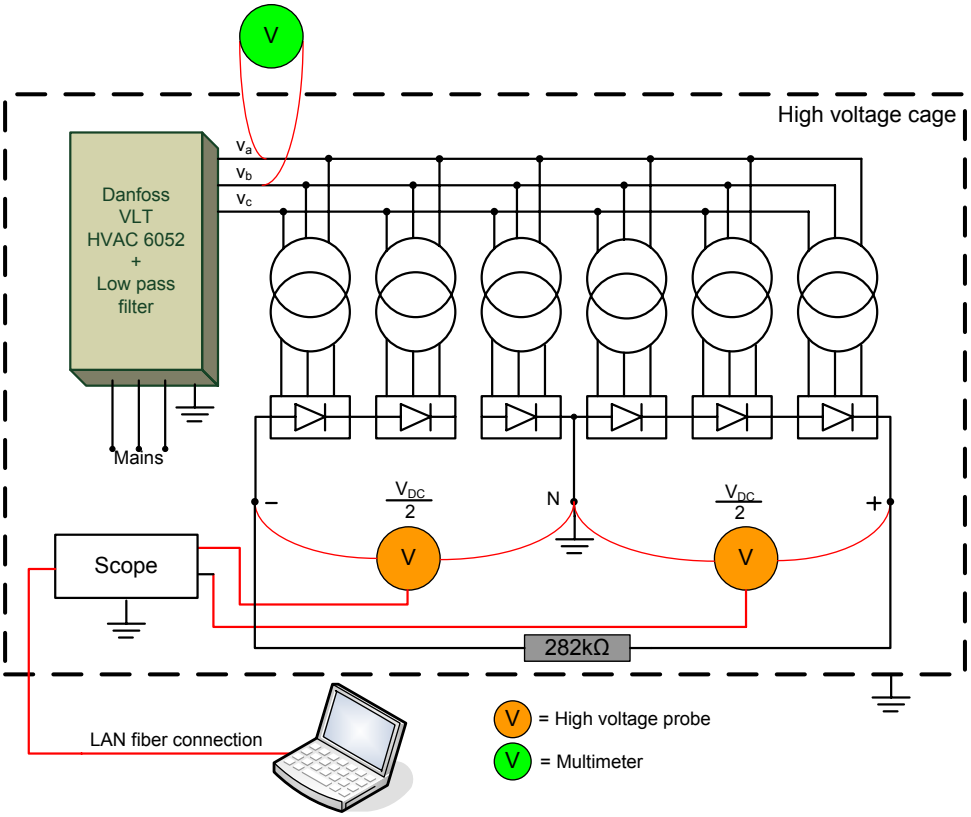

Figure D.16: *Schematic view of medium voltage DC supply test setup.*

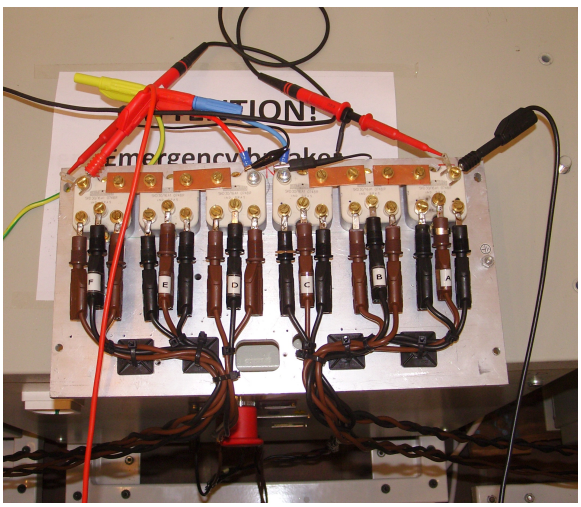

Figure D.17: *Diode bridge rectifier and high voltage propes.*

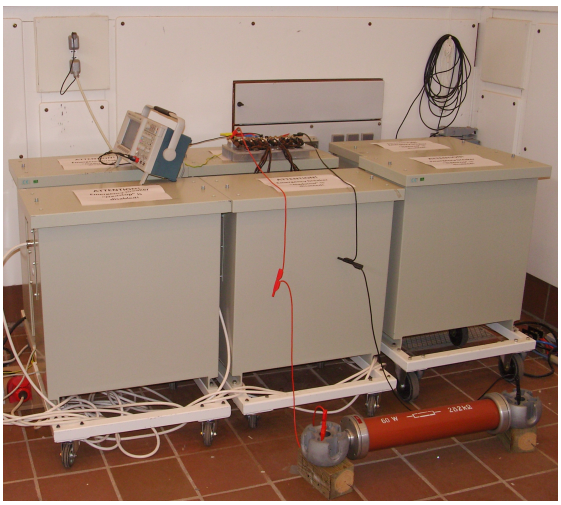

Figure D.18: *The six AXA transformers with the diode bridge from figure D.17 on top. In the bottom, the load resistor is seen.*

Equipment	AAU number	Used for
Tektronix oscilloscope	62796	Measure V_{DC}
2 x High voltage probes $2kV$	No number	Measurement of $\frac{V_{DC}}{2}$
Fluke multimeter	62785	Monitor VLT output voltage v_{ab}

Table D.4: *Equipment used for short circuit test.*

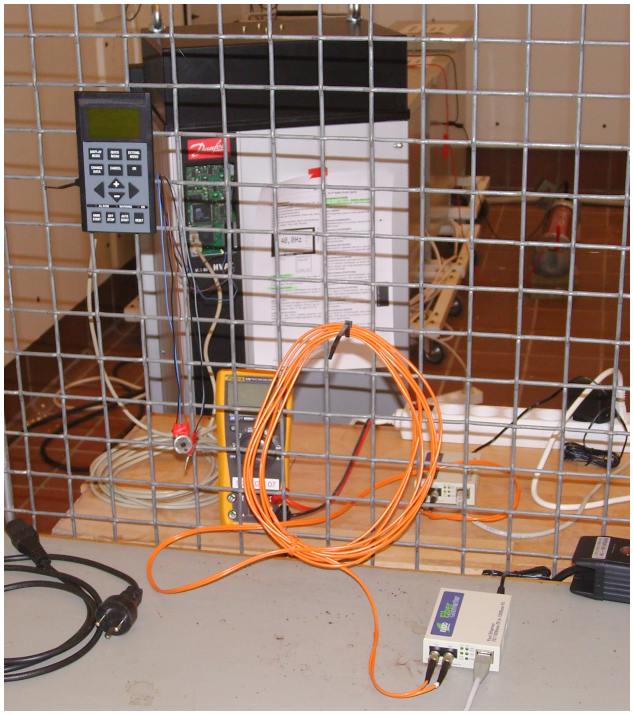

Figure D.19: *The Danfoss HVAC 6052 VLT. Notice the display on the cage and the two fiber converters connected via the orange fiber. This equipment is used to control the VLT and the scopes by LAN interface.*

D.3.2 Test of medium voltage DC supply

The purpose of the test is, to verify equation (D.6), and also obtain knowledge about the output voltage ripple. The used equipment is listed in table D.4, the test setup schematic is shown in figure D.16 and the realized DC supply is shown in figure D.17, D.18 and D.19.

The test results are shown on figure D.20, D.21 and D.22. The laboratory temperature was $18°C$ at time of test.

D.3.3 Data evaluation

From figure D.20, D.21 and D.22, it is shown, that the mean value of the DC link voltage approximately fits equation (D.6). Also, the two DC link voltages is reasonable symmetrically with a maximum difference of $50V$. Considering measurement equipment tolerances this is acceptable. There is a large ripple voltage of approximately $500V_{pp}$ in figure D.22. The measured DC link voltage is plotted as a function of the VLT output voltage on figure D.23, together with calculated values for equation (D.6).

D.3.4 Conclusion

The purpose of this test was to verify equation (D.6). From the scope pictures in the previous subsection, the equation was deemed valid. The secondary objective of the test was, to gain knowledge about the ripple voltage. This was also done by the scope pictures, where the ripple peak to peak voltage was read to $500V$.

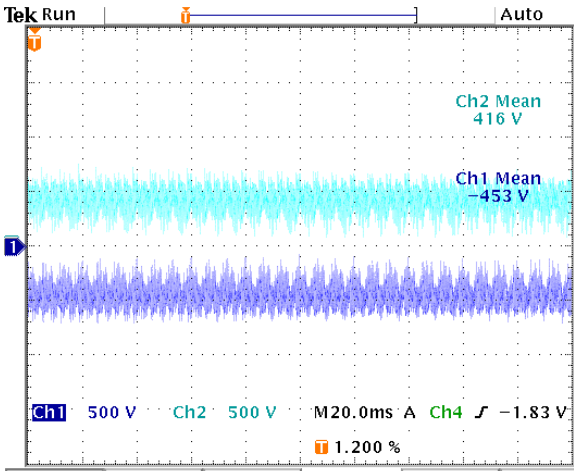

Figure D.20: *DC link voltage for* $V_{ab} = 100V$.

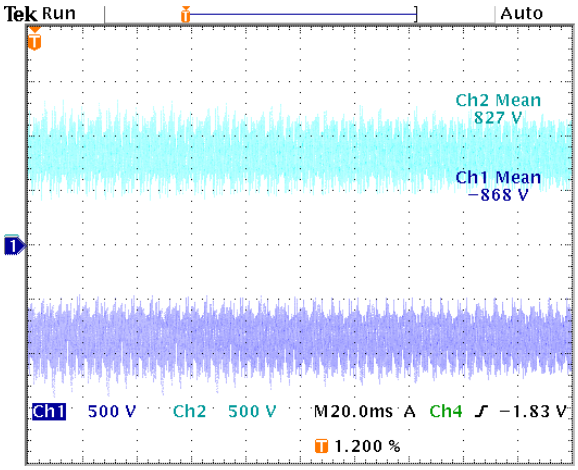

Figure D.21: *DC link voltage for* $V_{ab} = 200V$.

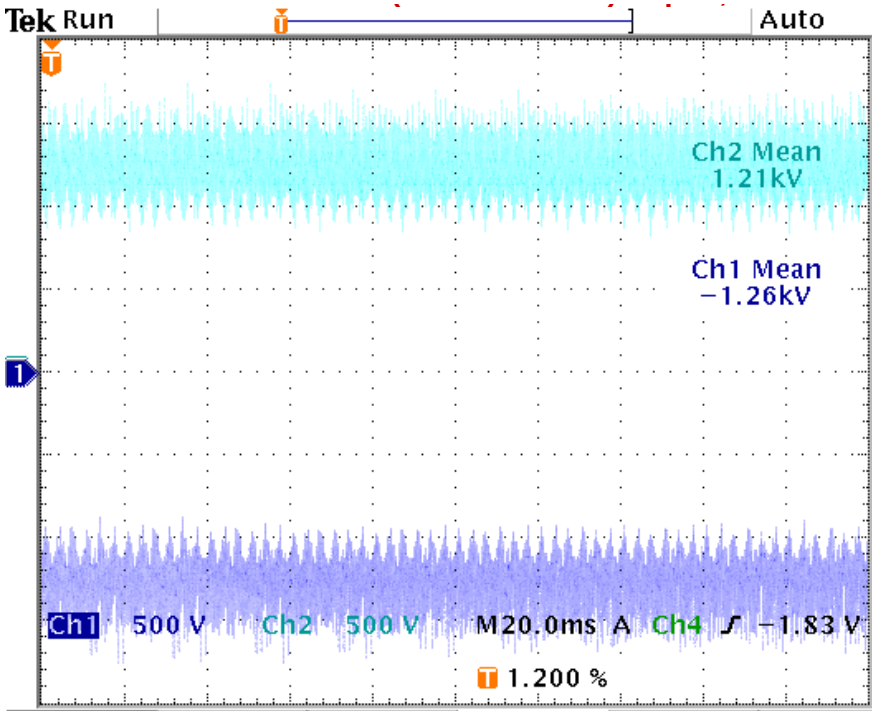

Figure D.22: *DC link voltage for* $V_{ab} = 296V$.

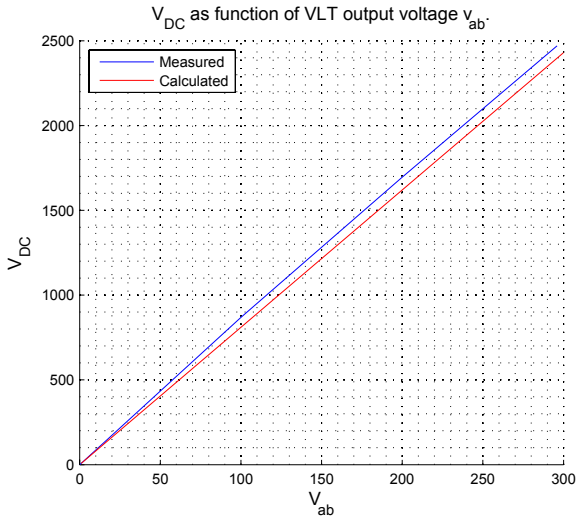

Figure D.23: *DC link voltage as function of the VLT output. Equation (D.6) is plotted for reference (red).*

This is unacceptable, but it must be mentioned that the neutral point capacitors are not included in the setup. By adding these large capacitors, the ripple is expected to be significantly reduced. Also the supply was lightly loaded under the test, so small voltage deviances can be expected, when the three-level inverter is connected. This is however not seen as a problem, since the VLT can generate a $V_{ab} = 400V$ output hence a DC link voltage of $V_{DC} = 3.4kV$.

D.4 Load inductor measurements

In this appendix section, the realized load inductance is measured.

D.4.1 Purpose

The purpose of the test is, to determine the inductance and the DC resistance of the inductor setup.

D.4.2 Test setup

For the inductance measurement, an LCR meter is used to measure the inductance at various frequencies. Also, the DC resistance[1] , and hence the theoretically power dissipation of the inductor is measured by this device. The use equipment are listed in table D.5

Equipment	AAU number	Used for
HP 4248 precision LCR meter	3307	Inductance
Fluke multimeter	70395	DC resistance
Fluke multimeter	62785	DC resistance
INSTEK Power supply	55702	DC resistance
Vario Trafo		Power supply

Table D.5: *Equipment used for inductance measurements.*

The test setup for the DC resistance is shown on figure D.24.

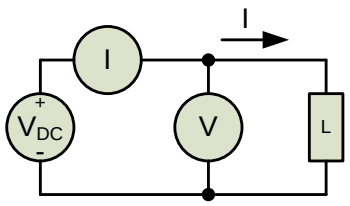

Figure D.24: *Resistance measurement test setup.*

D.4.3 Measurements

The initial measurements with the LCR meter was discarded, because the LCR meter is only capable of sourcing $200mA$, and this gives an unreliable result, because the cores cant be properly magnetized. Instead, the DC resistance setup on figure D.24 is used with an AC voltage source, in the form of a variable transformer, replacing the DC source. From measuring the RMS values of the voltage and current, the impedance of the inductor setup can be found. The measured values for the impedance is listed in table D.6.

[1] due to the large skin depth and the low frequency, $R_{AC} \approx R_{DC}$

V $[V]$	**I** $[A]$	$\lvert Z\rvert$ $[\Omega]$
10	0.49	20
20	0.86	23.5
40	1.53	26.1
80	2.73	29.3
100	3.28	30.4
125	3.98	31.4
150	4.65	32.3
175	5.36	32.6
200	6.06	33.0
230	6.88	33.4
250	7.45	33.5

Table D.6: *Impedance measurements at* $f = 50Hz$.

The measured values for the DC resistance R_{DC} is listed in table D.7.

V $[V]$	**I** $[A]$	$\mathbf{R_{DC}}$ $[\Omega]$
0.02	0.23	0.086
0.044	0.48	0.091
0.081	0.91	0.089
0.146	1.70	0.086
0.168	1.95	0.086

Table D.7: *DC resistance measurements. Average* $R_{DC} = 87.6m\Omega$.

D.4.4 Data evaluation

From table D.7, the reason for not using the LCR meter becomes clear. At low voltages, the variation in impedance is significant, but it stabilizes when the current becomes high. This is because the iron cores needs to be magnetized. It can be seen, that from $125V$ to $250V$ the deviation is smaller than from $10V$ to $20V$. From this, the impedance is obtained from the average value from $125V$ to $250V$ giving $|Z| = 32.6\Omega$. The DC resistance has some slight deviations, but the average value of $R_{DC} = 87.6m\Omega$ is deemed realistic. Knowing $|Z|$ and R_{DC}, the following equation can be used.

$$|Z|^2 = R_{DC}^2 + (j2 \cdot \pi \cdot f_{mod} \cdot L)^2 \quad \Rightarrow \quad L = \frac{\sqrt{|Z|^2 - R_{DC}^2}}{2 \cdot \pi \cdot f_{mod}} \quad [H] \tag{D.7}$$

$$L = \frac{\sqrt{32.6^2 - 0.0876^2}}{2 \cdot \pi \cdot 50} = 103mH \tag{D.8}$$

D.4.5 Conclusion

The conclusion of the test is, that the inductance is $L = 103mH$ and the DC resistance is $R_{DC} = 87.6m\Omega$.

D.5 Simulation of DC link capacitor.

D.5.1 Purpose

The purpose of the simulation is, to gain knowledge about the non symmetrical current drawn from the DC link capacitors, and hence the resulting voltage ripple. From this ripple, an appropriate capacitor can be chosen.

D.5.2 Simulation setup

The simulation schematic can be seen on figure D.25.

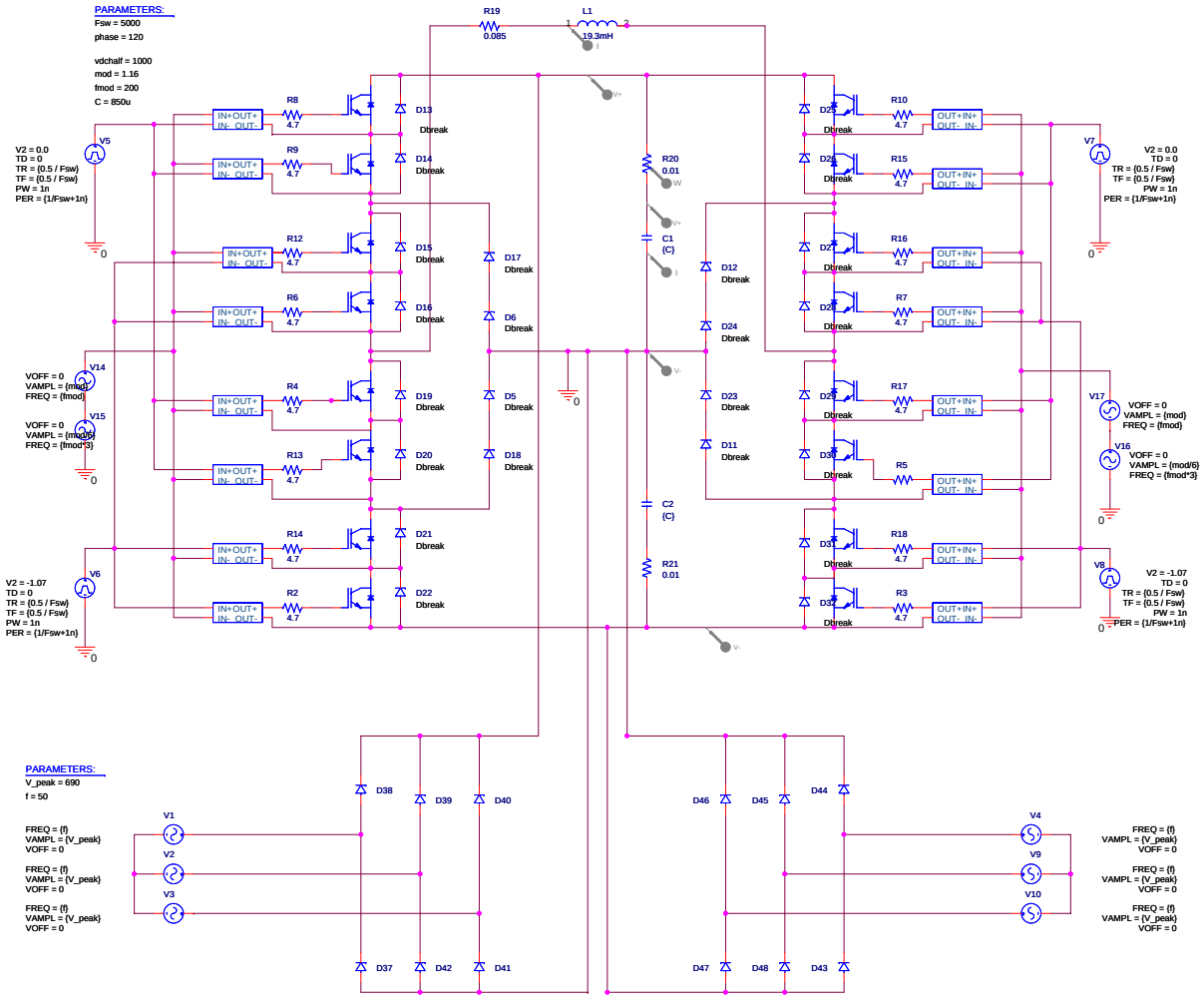

Figure D.25: *OrCad simulation schematic for capacitor simulation.*

The load inductance is set to $L_{load} = 19.7mH$ to simulate maximum current, that has been changed to $\widehat{i}_{load} = \pm 100A@Ma = 1.16$ when third harmonic injection is included. and a series resistance is included in the capacitor to model the R_{ESR}. Due to available capacitors at AAU, which can withstand the DC link voltage of $2.4kV$, the simulation is set up as a parameter sweep with three different capacitor values; 400, 825 and $1100\mu H$.

D.5.3 Simulation results

The initial simulation results are seen on figure D.26.

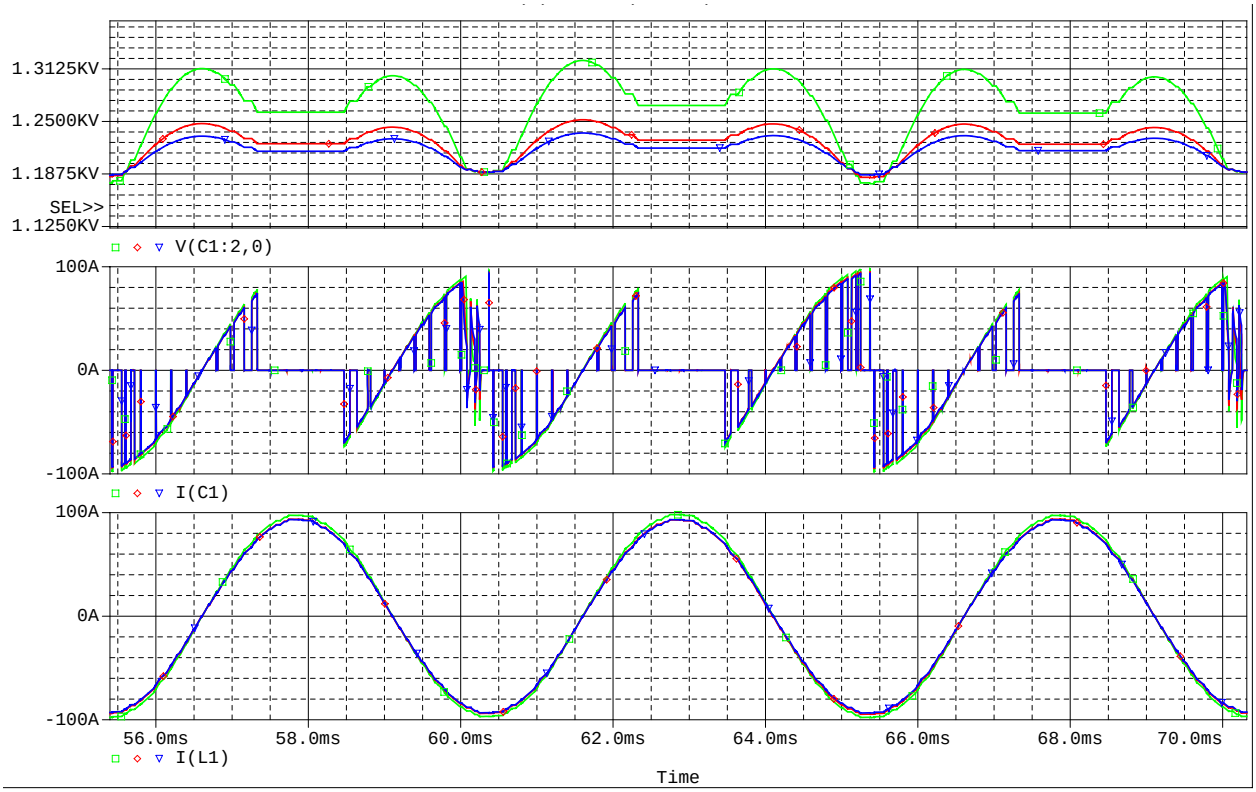

Figure D.26: *Initial simulation results. The colors represents: green = 400μF, red = 825μF and blue = 1100μF. The top graph shows the voltage across the top DC link capacitor, the middle shows the capacitor current and the bottom graph shows the load current.*

From the initial test, the 400μF capacitor is discarded, because it results in a large voltage ripple. On figure D.26, the unsymmetrically load currents effect on the ripple voltage can be seen. In the following simulations, shown on figure D.27, the two remaining capacitor values are closer inspected regarding the current and voltage ripple.

Figure D.27 shows the simulated waveforms for the 825μF and 1100μF capacitor values. On the top graph, the capacitor voltage v_C is shown, together with the average ($\frac{V_{DC}}{2}$) value. It can be seen, that the average DC link voltage varies slightly, approximately $v_{ripple} = 20V$ for the 825μF capacitor and approximately $v_{ripple} = 16V$ for the 1100μF capacitor. The ripple is defined as:

$$v_{ripple} = \widehat{v}_C - \frac{V_{DC}}{2} \quad [V] \tag{D.9}$$

Because the maximum voltage is of interest, due to the snubbers and the overall maximum voltage rating for the used equipment.

The middle and bottom graph of figure D.27 shows the capacitor current, together with the average current waveform. This waveform only deviates a little for the two different capacitor values because it is mainly dependent on the load.

D.5.4 Choice of capacitor value

Both capacitors of 825μF and 1100μF can be used, but remembering that the choice of capacitor values was done from available values, the voltage rating plays an important role. The value of 825μF can be realized by

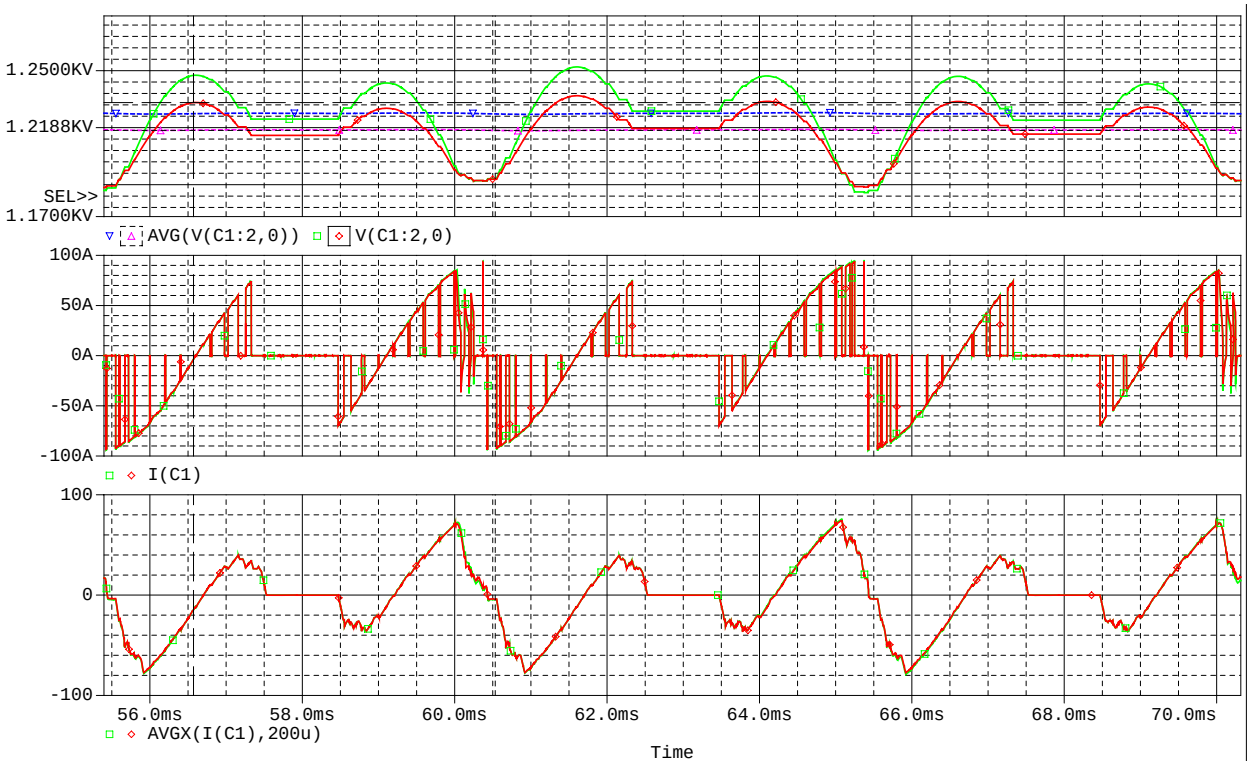

Figure D.27: *Initial simulation results. The colors represents: green/blue = 825μF and red/purple = 1100μF. The top graph shows the voltage across the top DC link capacitor (red/green) together with the DC value of the voltage (blue/purple). The middle graph shows the capacitor current (red/green). The bottom graph shows the average waveform of the capacitor current (blue/purple).*

four $3300\mu F/450V$ capacitors giving each neutral point capacitor a voltage rating of $1.8kV$, and the $1100\mu F$ value can be realized by three $3300\mu F/450V$ reaching a voltage rating of $1350V$. This is rater close to the DC value of $1.2kV$, and therefor the chosen capacitor is the four $3300\mu F/450V$ capacitors in series, yielding: $C = 825\mu F/1.8kV$.